National Semiconductor

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TP5510
Full Duplex Analog Front End (AFE) for Consumer Applications

General Description

The TP5510 consists of a μ-law monolithic AFE device utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial data interface. The device is fabricated using National's advanced double-poly CMOS process (microCMOS).

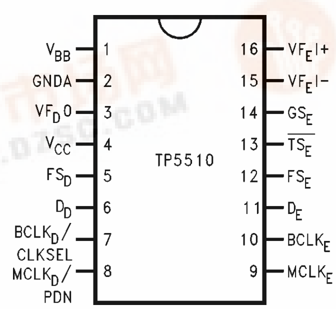
The A/D portion of the device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise, and a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a compressing A/D which samples the filtered signal and converts it to the μ-law digital format. The decode portion of the device consists of an expanding D/A, which reconstructs the analog signal from the compressed μ-law code, a low-pass filter which corrects for the sin x/x response of the D/A output and rejects signals above 3400 Hz, followed by a single-ended power amplifier capable of driving low impedance loads. The device requires a 1.536 MHz, 1.544 MHz or 2.048 MHz master clock, bit clocks which may vary from 64 kHz to 2.048 MHz; and 8 kHz frame sync pulses.

Features

- Complete A/D and D/A with filter system including:
  - Serial Data Interface
  - Encode high-pass and low-pass filter
  - Decode low-pass filter with sin x/x correction
  - Active RC noise filters
  - μ-law compatible A/D and D/A
  - Internal precision voltage reference
  - Internal auto-zero circuitry
- μ-law—TP5510
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes PC card circuit density
- Plastic DIP and SOIC packages
- 8-bit digital I/O
- 13-bit dynamic range
- Use with DSP processor
- Applications: Tapeless Answering Machines, Cordless Phones, Cellular Radio

Connection Diagram

Dual-In-Line Package



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Top View

Order Number TP5510WM
See NS Package Number M16B

Order Number TP5510N
See NS Package Number N16A

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Block Diagram

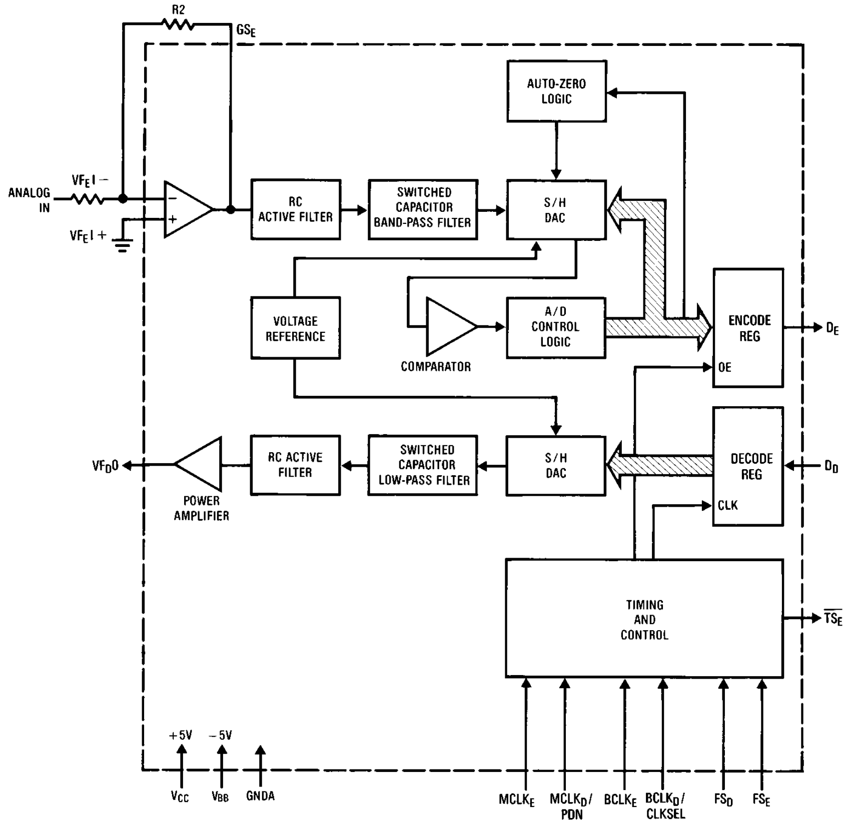

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FIGURE 1

Pin Description

Symbol	Function
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.
GNDA	Analog ground. All signals are referenced to this pin.
VF_DO	Analog output of the receive power amplifier.
V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
FS_D	Decode frame sync pulse which enables $BCLK_R$ to shift data into D_D. FS_D is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
D_D	Decode data input. Data is shifted into D_D following the FS_D leading edge.
$BCLK_D$/CLKSEL	The bit clock which shifts data into D_D after the FS_D leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_D$ is used for both encode and decode directions (see Table 1).

Pin Description (Continued)

Symbol	Function
$MCLK_D$/PDN	Encode master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_E$, but should be synchronous with $MCLK_E$ for best performance. When $MCLK_D$ is connected continuously low, $MCLK_E$ is selected for all internal timing. When $MCLK_D$ is connected continuously high, the device is powered down.
$MCLK_E$	Encode master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_D$. Best performance is realized from synchronous operation.
FS_E	Encode frame sync pulse input which enables $BCLK_E$ to shift out the data on D_E. FS_E is an 8 kHz pulse train, see *Figures 2* and *3* for timing details.
$BCLK_E$	The bit clock which shifts out the data on D_E. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_E$.
D_E	The TRI-STATE® data output which is enabled by FS_E.
$\overline{TS_E}$	Open drain output which pulses low during the A/D time slot.
GS_E	Analog output of the encode input amplifier. Used to externally set gain.
VF_EI^-	Inverting input of the encode input amplifier.
VF_EI^+	Non-inverting input of the encode input amplifier.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the AFE and places it into a power-down state. All non-essential circuits are deactivated and the D_E and VF_DO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_D$/PDN pin *and* FS_E and/or FS_D pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_D$/PDN pin high; the alternative is to hold both FS_E and FS_D inputs continuously low—the device will power-down approximately 2 ms after the last FS_E or FS_D pulse. Power-up will occur on the first FS_E or FS_D pulse. The TRI-STATE data output, D_E, will remain in the high impedance state until the second FS_E pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the encode and decode directions. In this mode, a clock must be applied to $MCLK_E$ and the $MCLK_D$/PDN pin can be used as a power-down control. A low level on $MCLK_D$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_E$ will be selected as the master clock for both the encode and decode circuits. A bit clock must also be applied to $BCLK_E$ and the $BCLK_D$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_D$/CLKSEL pin, $BCLK_E$ will be selected as the bit clock for both the encode and decode directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_D$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_E$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_E$.

Each FS_E pulse begins the encoding cycle and the data from the previous encode cycle is shifted out of the enabled D_E output on the positive edge of $BCLK_E$. After 8-bit clock periods, the TRI-STATE D_E output is returned to a high impedance state. With an FS_D pulse, data is latched via the D_D input on the negative edge of $BCLK_E$ (or $BCLK_D$ if running). FS_E and FS_D must be synchronous with $MCLK_{E/D}$.

TABLE I. Selection of Master Clock Frequencies

$BCLK_D$/CLKSEL	Master Clock Frequency Selected
	TP5510
Clocked	1.536 MHz or 1.544 MHz
0	2.048 MHz
1	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate encode and decode clocks may be applied. $MCLK_E$ and $MCLK_D$ must be 1.536 MHz or 1.544 MHz for the TP5510, and need not be synchronous. For best transmission performance, however, $MCLK_D$ should be synchronous with $MCLK_E$, which is easily achieved by applying only static logic levels to the $MCLK_D$/PDN pin. This will automatically connect $MCLK_E$ to all internal $MCLK_D$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_E starts each A/D conversion cycle and must be synchronous with $MCLK_E$ and $BCLK_E$. FS_D starts each D/A conversion cycle and must be synchronous with $BCLK_D$. $BCLK_D$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_E$ and $BCLK_D$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The AFE can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_E and FS_D, must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS_E high during a falling edge of $BCLK_E$, the next rising edge of $BCLK_E$ enables the D_E TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_E output. With FS_D high during a falling edge of $BCLK_D$ ($BCLK_E$ in synchronous mode), the next falling edge of $BCLK_E$ latches in the sign bit. The following seven falling

Functional Description (Continued)

edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_E and FS_D, must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS_E, the AFE will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_E TRI-STATE output buffer is enabled with the rising edge of FS_E or the rising edge of $BCLK_E$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_E$ rising edges clock out the remaining seven bits. The D_E output is disabled by the falling $BCLK_E$ edge following the eighth rising edge, or by FS_E going low, whichever comes later. A rising edge on the decode frame sync pulse, FS_D, will cause the data at D_D to be latched in on the next eight falling edges of $BCLK_D$ ($BCLK_E$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

ENCODE SECTION

The encode section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the A/D sample-and-hold circuit. The A/D is of compressing type according to μ-law coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (See Table of Transmission Characteristics). The FS_E frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_E at the next FS_E pulse. The total encoding delay will be approximately 165 μs (due to the encode filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

DECODE SECTION

The decode section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The DAC is μ-law and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifier capable of driving a 600Ω load to a level of 7.2 dBm. The decode section is unity-gain. Upon the occurrence of FS_D, the data at the D_D input is clocked in on the falling edge of the next eight $BCLK_D$ ($BCLK_E$) periods. At the end of the DAC time slot, the D/A conversion cycle begins, and 10 μs later the DAC output is updated. The total DAC delay is ~10 μs (DAC update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GNDA 7V

V_{BB} to GNDA −7V

Voltage at any Analog Input or Output $V_{CC}+0.3V$ to $V_{BB}-0.3V$

Voltage at any Digital Input or Output $V_{CC}+0.3V$ to GNDA−0.3V

Operating Temperature Range −25°C to +125°C

Storage Temperature Range −65°C to +150°C

Lead Temperature (Soldering, 10 seconds) 300°C

ESD (Human Body Model) 2000V

Latch-Up Immunity = 100 mA on any Pin

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	D_E, I_L=3.2 mA $\overline{SIG_D}$, I_L=1.0 mA $\overline{TS_E}$, I_L=3.2 mA, Open Drain			**0.4** **0.4** **0.4**	V V V
V_{OH}	Output High Voltage	D_E, I_H=−3.2 mA SIG_D, I_H=−1.0 mA	**2.4** **2.4**			V V
I_{IL}	Input Low Current	GNDA≤V_{IN}≤V_{IL}, All Digital Inputs	**−10**		**10**	µA
I_{IH}	Input High Current	V_{IH}≤V_{IN}≤V_{CC}	**−10**		**10**	µA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_E, GNDA≤V_O≤V_{CC}	**−10**		**10**	µA
ANALOG INTERFACE WITH ENCODE INPUT AMPLIFIER (ALL DEVICES)						
I_IEA	Input Leakage Current	−2.5V≤V≤+2.5V, VF_EI^+ or VF_EI^-	**−200**		**200**	nA
R_IEA	Input Resistance	−2.5V≤V≤+2.5V, VF_EI^+ or VF_EI^-	10			MΩ
R_OEA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LEA	Load Resistance	GS_E	10			kΩ
C_LEA	Load Capacitance	GS_E			50	pF
V_OEA	Output Dynamic Range	GS_E, R_L≥10 kΩ	**−2.8**		**2.8**	V
A_VEA	Voltage Gain	VF_EI^+ to GS_E	**5000**			V/V
F_UEA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}EA$	Offset Voltage		**−20**		**20**	mV
$V_{CM}EA$	Common-Mode Voltage	CMRREA > 60 dB	−2.5		2.5	V
CMRREA	Common-Mode Rejection Ratio	DC Test	60			dB
PSRREA	Power Supply Rejection Ratio	DC Test	60			dB
ANALOG INTERFACE WITH DECODE FILTER (ALL DEVICES)						
R_ODF	Output Resistance	Pin VF_DO		1	3	Ω
R_LDF	Load Resistance	VF_DO=±2.5V	600			Ω
C_LDF	Load Capacitance				500	pF
VOS_DO	Output DC Offset Voltage		−200		200	mV
POWER DISSIPATION (ALL DEVICES)						
$I_{CC}0$	Power-Down Current	No Load (Note)		0.5	**3**	mA
$I_{BB}0$	Power-Down Current	No Load (Note)		0.05	**1**	mA
$I_{CC}1$	Power-Up Active Current	No Load		6.0	**12**	mA
$I_{BB}1$	Power-Up Active Current	No Load		6.0	**12**	mA

Note: $I_{CC}0$ and $I_{BB}0$ are measured after first achieving a power-up state.

Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C. All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V. See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clocks	Depends on the Device Used and the $BCLK_D$/CLKSEL Pin. $MCLK_E$ and $MCLK_D$		1.536 1.544 **2.048**		MHz MHz MHz
t_{DM}	Rise Time of Master Clock	$MCLK_E$ and $MCLK_D$			50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_E$ and $MCLK_D$			50	ns
t_{PB}	Period of Bit Clock		485	**488**	15725	ns
t_{DB}	Rise Time of Bit Clock	$BCLK_E$ and $BCLK_D$			50	ns
t_{FB}	Fall Time of Bit Clock	$BCLK_E$ and $BCLK_D$			50	ns
t_{WMH}	Width of Master Clock High	$MCLK_E$ and $MCLK_D$	**160**			ns
t_{WML}	Width of Master Clock Low	$MCLK_E$ and $MCLK_D$	**160**			ns
t_{SBFM}	Set-Up Time from $BCLK_E$ High to $MCLK_E$ Falling Edge	First Bit Clock after the Leading Edge of FS_E	**100**			ns
t_{SFFM}	Set-Up Time from FS_E High to $MCLK_E$ Falling Edge	Long Frame Only	**100**			ns
t_{WBH}	Width of Bit Clock High	V_{IH} = 2.2V	**160**			ns
t_{WBL}	Width of Bit Clock Low	V_{IL} = 0.6V	**160**			ns
t_{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	**0**			ns
t_{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	**0**			ns
t_{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	**115**			ns
t_{DBD}	Delay Time from $BCLK_E$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	0		140	ns
t_{DBTS}	Delay Time to $\overline{TS_E}$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from $BCLK_E$ Low to Data Output Disabled	C_L = 0 pF to 150 pF	50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_E or $BCLK_E$, Whichever Comes Later	C_L = 0 pF to 150 pF	20		165	ns
t_{SDB}	Set-Up Time from D_D Valid to $BCLK_{D/E}$ Low		**50**			ns
t_{HBD}	Hold Time from $BCLK_{D/E}$ Low to D_D Invalid		**50**			ns
t_{SF}	Set-Up Time from $FS_{E/D}$ to $BCLK_{E/D}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**50**			ns
t_{HF}	Hold Time from $BCLK_{E/D}$ Low to $FS_{E/D}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**100**			ns
t_{HBFl}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_E or FS_D)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	**100**			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	**160**			ns

Timing Diagrams

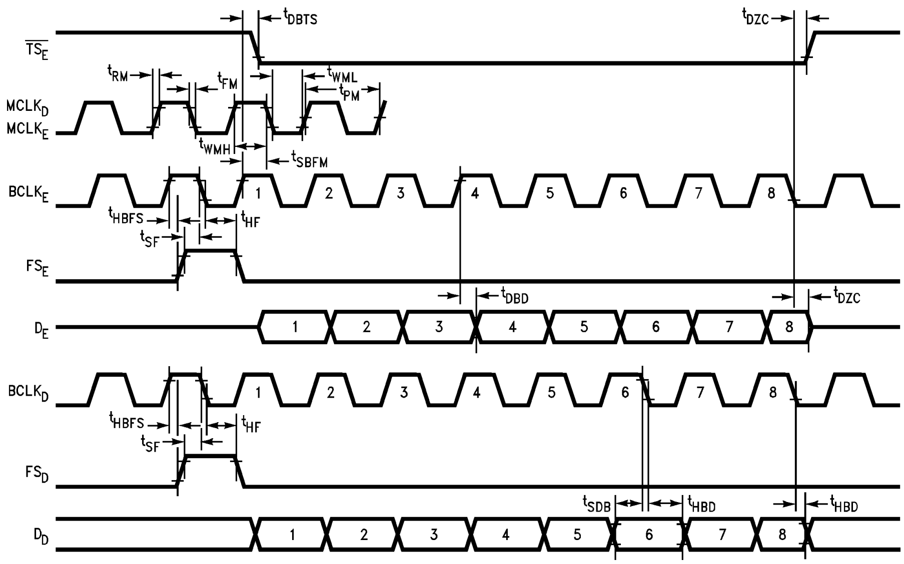

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FIGURE 2. Short Frame Sync Timing

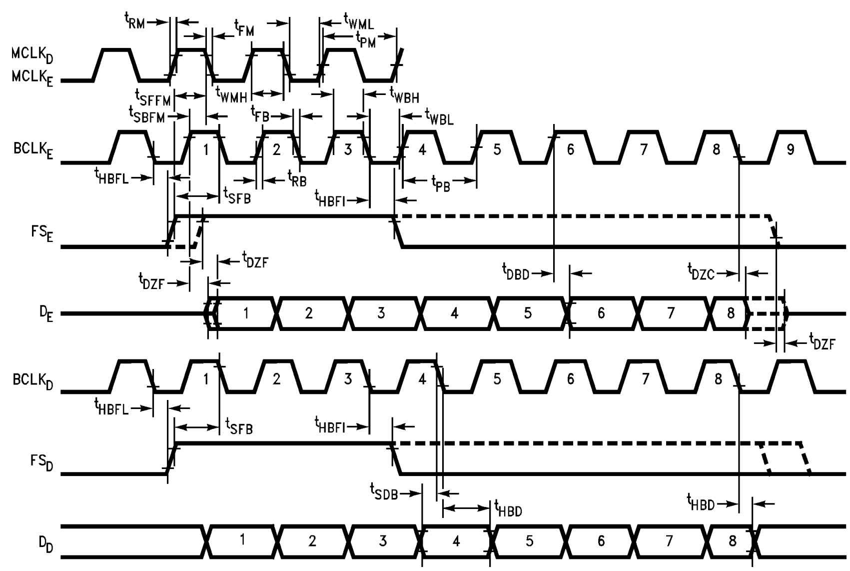

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FIGURE 3. Long Frame Sync Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, encode input amplifier connected for unity gain non-inverting. Typicals specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels (Definition of Nominal Gain)	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0		1.2276		Vrms
t_{MAX}	Max Overload Level	TP5510, (3.17 dBm0)		2.501		V_{PK}
G_{EA}	Encode Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input at GS_E=0 dBm0 at 1020 Hz	**−0.5**		**0.5**	dB
G_{ER}	Encode Gain, Relative to G_{EA}	f=16 Hz f=50 Hz f=60 Hz f=200 Hz f=300 Hz−3000 Hz f=3400 Hz f=4000 Hz f=4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 **−2.0** **−0.5** **−1.5**		−35 −25 **−21** −0.1 **0.15** **0.5** **−10** **−25**	dB dB dB dB dB dB dB dB
G_{EAT}	Absolute Encode Gain Variation with Temperature	Relative to G_{EA}	−0.3		0.3	dB
G_{ERL}	Encode Gain Variations with Level	Sinusoidal Test Method Reference Level=−10 dBm0 VF_EI^+=−40 dBm0 to +3 dBm0 VF_EI^+=−50 dBm0 to −40 dBm0	 **−0.4** **−0.8**		 **0.4** **0.8**	 dB dB
G_{DA}	Decode Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input=Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	**−0.5**		**0.5**	dB
G_{DR}	Decode Gain, Relative to G_{DA}	f=0 Hz to 3000 Hz f=3400 Hz f=4000 Hz	**−0.5** **−1.5**		**0.5** **0.5** **−14**	dB dB dB
G_{DAT}	Absolute Decode Gain Variation with Temperature	Relative to G_{DA}	−0.3		0.3	dB
G_{DAV}	Absolute Decode Gain Variation with Supply Voltage	Relative to G_{DA}	**−0.05**		**0.05**	dB
G_{DRL}	Decode Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded PCM Level =−40 dBm0 to +3 dBm0 =−50 dBm0 to −40 dBm0 =−55 dBm0 to −50 dBm0	 **−0.4** **−0.8** **−2.5**		 **0.4** **0.8** **2.5**	 dB dB dB
V_{DO}	Decode Output Drive Level	R_L=600Ω	−2.5		2.5	V

Transmission Characteristics Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, encode input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
NOISE						
N_{EC}	Encode Noise, C Message Weighted	TP5510 (Note 1)		12	16	dBrnC0
N_{DC}	Decode Noise, C Message Weighted	Digital Code is Alternating Positive and Negative Zero —TP5510		8	11	dBrnC0
N_{DS}	Noise, Single Frequency	f=0 kHz to 100 kHz, Loop Around Measurement, VF_EI^+=0 Vrms			−53	dBm0
$PPSR_E$	Positive Power Supply Rejection, Encode	VF_EI^+ = −50 dBm0 V_{CC}=5.0 V_{DC}+100 mVrms f=0 kHz−50 kHz (Note 2)	**−30**			dBC
$NPSR_E$	Negative Power Supply Rejection, Encode	VF_EI^+ = −50 dBm0 V_{BB}=−5.0 V_{DC}+100 mVrms f=0 kHz−50 kHz (Note 2)	**−30**			dBC
$PPSR_D$	Positive Power Supply Rejection, Decode	PCM Code Equals Positive Zero V_{CC}=5.0 V_{DC}+100 mVrms Measure VF_D0 f=0 Hz−4000 Hz f=4 kHz−50 kHz	**30** **30**			dBC dB
$NPSR_D$	Negative Power Supply Rejection, Decode	PCM Code Equals Positive Zero V_{BB}=−5.0 V_{DC}+100 mVrms Measure VF_D0 f=0 Hz−4000 Hz f=4 kHz−50 kHz	**30** **30**			dBC dB

Transmission Characteristics Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, encode input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz to 3400 Hz Input Digital Code Applied at D_D.			−30	dB
		4600 Hz–7600 Hz			−30	dB
		7600 Hz–8400 Hz			−30	dB
		8400 Hz–100,000 Hz			−30	dB
DISTORTION						
STD_E STD_D	Signal to Total Distortion Encode or Decode Half-Channel	Sinusoidal Test Method (Note 3)				
		Level = 3.0 dBm0	28			dBC
		= 0 dBm0 to −30 dBm0	**30**			dBC
		= −40 dBm0	**25**			dBC
SFD_E	Single Frequency Distortion, Encode				**−41**	dB
SFD_D	Single Frequency Distortion, Decode				**−41**	dB
IMD	Intermodulation Distortion	Loop Around Measurement, $VF_{Encode}+$ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			−35	dB
CROSSTALK						
CT_{E-D}	Encode to Decode Crosstalk, 0 dBm0 Encode Level	f=300 Hz–3400 Hz D_D=Quiet Code		−90	−70	dB
CT_{D-E}	Decode to Encode Crosstalk, 0 dBm0 Decode Level	f=300 Hz–3400 Hz, VF_EI=Multitone (Note 2)		−90	−70	dB

Format at D_E Output

	TP5510 μ-Law
V_{IN} (at GS_E) = +Full-Scale	1 0 0 0 0 0 0 0
V_{IN} (at GS_E) = 0V	{ 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN} (at GS_E) = −Full-Scale	0 0 0 0 0 0 0 0

Applications Information

POWER SUPPLIES

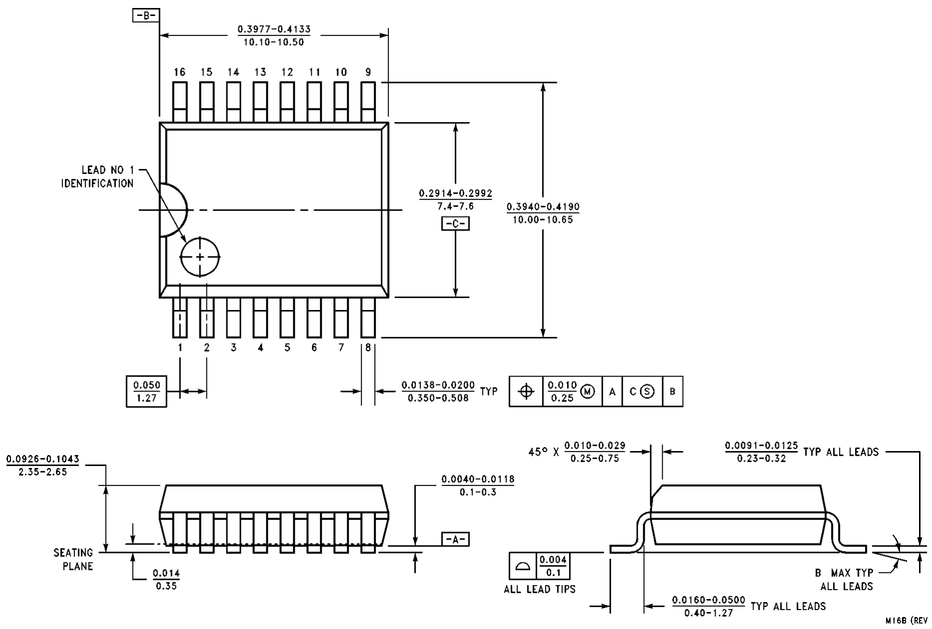
While the pins of the AFE are well protected against electrical misuse, it is recommended but not mandatory that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a ''hot'' socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}, as close to the device as possible.

For best performance, if more than 1 AFE is on a card, the ground point of each AFE on a card should be connected to a common card ground in star formation, rather than via a ground bus.

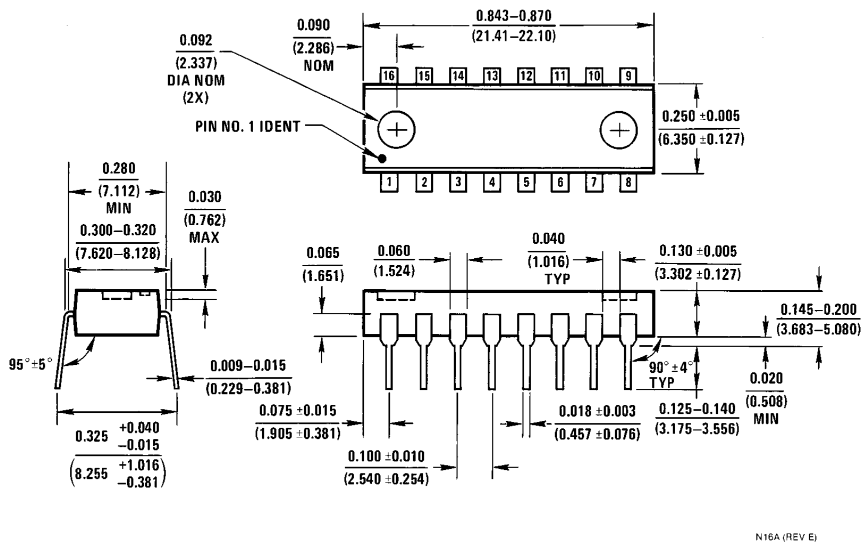
This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Outline Package (WM)
Order Number TP5510WM
NS Package Number M16B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
Order Number TP5510N
NS Package Number N16A

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