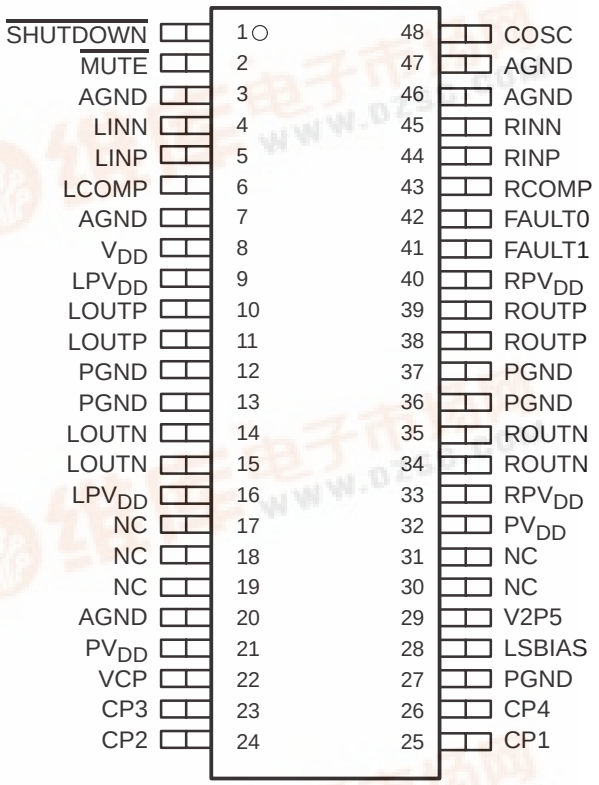
TPA005D02
2-W STEREO CLASS-D AUDIO POWER AMPLIFIER

SLOS227C – AUGUST 1998 – REVISED MARCH 2000

NOT RECOMMENDED FOR NEW DESIGNS

- **Choose TPA2000D2 For Upgrade**
- **Extremely Efficient Class-D Stereo Operation**
- **Drives L and R Channels**
- **2-W BTL Output into 4 Ω**
- **5-W Peak Music Power**
- **Fully Specified for 5-V Operation**
- **Low Quiescent Current**
- **Shutdown Control**
- **Thermally-Enhanced PowerPAD™ Surface-Mount Packaging**
- **Thermal and Under-Voltage Protection**

DCA PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPA005D02 is a monolithic power IC stereo audio amplifier. It operates in extremely efficient Class-D operation, using the high switching speed of power DMOS transistors. These transistors replicate the analog signal through high-frequency switching of the output stage. This allows the TPA005D02 to be configured as a bridge-tied load (BTL) amplifier.

When configured as a BTL amplifier, the TPA005D02 is capable of delivering up to 2 W of continuous average power into a 4-Ω load at 0.5% THD+N from a 5-V power supply in the high fidelity range (20 Hz to 20 kHz).

A BTL configuration eliminates the need for external coupling capacitors on the output. A chip-level shutdown control limits total supply current to 400 µA. This makes the device ideal for battery-powered applications.

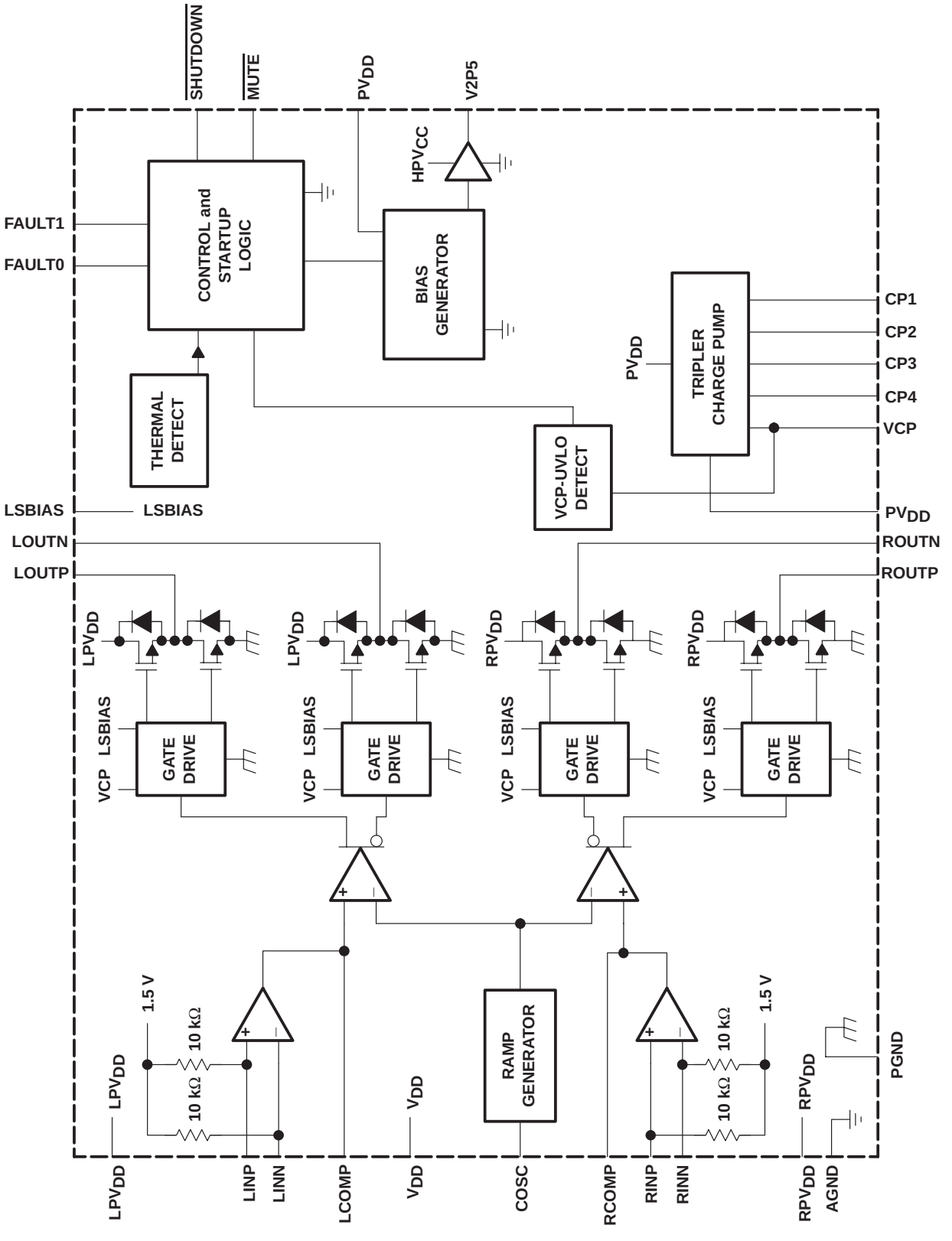
Protection circuitry increases device reliability: thermal and under-voltage shutdown, with two status feedback terminals for use when any error condition is encountered.

The high switching frequency of the TPA005D02 allows the output filter to consist of three small capacitors and two small inductors per channel. The high switching frequency also allows for good THD+N performance.

The TPA005D02 is offered in the thermally enhanced 48-pin PowerPAD TSSOP surface-mount package (designator DCA).

PowerPAD is a trademark of Texas Instruments Incorporated.

TPA005D02
2-W STEREO CLASS-D AUDIO POWER AMPLIFIER



NOTE A: LPV_{DD}, RPV_{DD}, V_{DD}, and PV_{DD} are externally connected. AGND and PGND are externally connected.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AGND	3, 7, 20, 46, 47	Analog ground for analog sections
COSC	48	Capacitor I/O for ramp generator. Adjust the capacitor size to change the switching frequency.
CP1	25	First diode node for charge pump
CP2	24	First inverter switching node for charge pump
CP3	23	Second diode node for charge pump
CP4	26	Second inverter switching node for charge pump
FAULT0	42	Logic level fault0 output signal. Lower order bit of the two fault signals with open drain output.
FAULT1	41	Logic level fault1 output signal. Higher order bit of the two fault signals with open drain output.
LCOMP	6	Compensation capacitor terminal for left-channel Class-D amplifier
LINN	4	Class-D left-channel negative input
LINP	5	Class-D left-channel positive input
LOUTN	14, 15	Class-D amplifier left-channel negative output of H-bridge
LOUTP	10, 11	Class-D amplifier left-channel positive output of H-bridge
LPV_{DD}	9, 16	Class-D amplifier left-channel power supply
LSBIAS	28	Level-shifter power supply, to be tied to VCP
$\overline{\text{MUTE}}$	2	Active-low logic-level mute input signal. When $\overline{\text{MUTE}}$ is held low, the selected amplifier is muted. When $\overline{\text{MUTE}}$ is held high, the device operates normally. When the Class-D amplifier is muted, the low-side output transistors are turned on, shorting the load to ground.
NC	17, 18, 19, 30, 31	No internal connection
PGND	12, 13	Power ground for left-channel H–bridge only
PGND	27	Power ground for charge pump only
PGND	36, 37	Power ground for right-channel H-bridge only
PV_{DD}	21, 32	V_{DD} supply for charge-pump and internal logic circuitry
RCOMP	43	Compensation capacitor terminal for right-channel Class-D amplifier
RINN	45	Class-D right-channel negative input
RINP	44	Class-D right-channel positive input
RPV_{DD}	33, 40	Class-D amplifier right-channel power supply
ROUTN	34, 35	Class-D amplifier right-channel negative output of H-bridge
ROUTP	38, 39	Class-D amplifier right-channel positive output of H-bridge
$\overline{\text{SHUTDOWN}}$	1	Active-low logic-level shutdown input signal. When $\overline{\text{SHUTDOWN}}$ is held low, the device goes into shutdown mode. When $\overline{\text{SHUTDOWN}}$ is held at logic high, the device operates normally.
V2P5	29	2.5-V internal reference bypass
VCP	22	Storage capacitor terminal for charge pump
V_{DD}	8	V_{DD} bias supply for analog circuitry. This terminal needs to be well filtered to prevent degrading the device performance.

Class-D amplifier faults

Table 1. Amplifier Fault Table

FAULT 0†	FAULT 1†	DESCRIPTION
1	1	No fault—The device is operating normally.
1	0	Charge pump under-voltage lock-out (VCP-UV) fault—All low-side transistors are turned on, shorting the load to ground. Once the charge pump voltage is restored, normal operation resumes, but FAULT1 is still active. FAULT1 is cleared by cycling MUTE, SHUTDOWN, or the power supply.
0	0	Thermal fault—All the low-side transistors are turned on, shorting the load to ground. Once the junction temperature drops 20°C, normal operation resumes. But the FAULTx terminals are still set and are cleared by cycling MUTE, SHUTDOWN, or the power supply.

† These logic levels assume a pull up to PV_{DD} from the open-drain outputs.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP† (DCA)
–40°C to 125°C	TPA005D02DCA

† The DCA package is available in left-ended tape and reel. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA005D02DCAR).

absolute maximum ratings over operating free-air temperature range, T_C = 25°C (unless otherwise noted)‡

Supply voltage, V_{DD} (PV_{DD}, LPV_{DD}, RPV_{DD}, V_{DD}) . . . . . 5.5 V
Bias voltage (LSBIAS) . . . . . 12 V to 20 V
Input voltage, V_I (SHUTDOWN, MUTE, MODE) . . . . . –0.3 V to 5.8 V
Output current, I_O (FAULT0, FAULT1), open drain terminated . . . . . 1 mA
Charge pump voltage, V_{CP} . . . . . PV_{DD} + 20 V
Continuous H-bridge output current . . . . . 2 A
Pulsed H-Bridge output current, each output, I_{max} (see Note 1) . . . . . 5 A
Continuous total power dissipation, T_C = 25°C . . . . . 4.5 W§
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating case temperature range, T_C . . . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
§ Thermal shutdown activates when T_J = 125°C.
NOTE 1: Pulse duration = 10 ms, duty cycle ≤ 2%

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$¶ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
DCA	5.6 W	44.8 mW/°C	3.6 W	2.9 W	1.1 W

¶ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, PV_{DD}, LPV_{DD}, RPV_{DD}, V_{DD}	4.5		5.5	V
High-level input voltage, V_{IH}	4.25			V
Low-level input voltage, V_{IL}			0.75	V
Audio inputs, LINN, LINP, RINN, RINP, HPLIN, HPRIN, differential input voltage			1	V_{RMS}
PWM frequency	100		500	kHZ

electrical characteristics, $V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 5$ V, $R_L = 4\ \Omega$, $T_C = 25°C$, See Figure 1 (resistive load) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power supply rejection ratio	$V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD}$ = 4.9 V to 5.1 V		40		dB
I_{DD}	Supply current	No load or output filter		25	40	mA
$I_{DD(MUTE)}$	Supply current, mute mode	$\overline{MUTE}$ = 0 V		10	15	mA
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0 V		400	2000	μA
I_{IH}	High-level input current	V_{IH} = 5.3 V			10	μA
I_{IL}	Low-level input current	V_{IL} = –0.3 V			–10	μA
$r_{DS(on)}$	Total static drain-to-source on-state resistance (low-side plus high-side FETs)	I_D = 0.5 A		620	750	mΩ
$r_{DS(on)}$	Matching		95%	99.5%		

operating characteristics, $V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 5$ V, $R_L = 4\ \Omega$, $T_C = 25°C$, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	RMS output power, THD = 0.5%, per channel			2		W
THD+N	Total harmonic distortion plus noise	P_O = 1 W, f = 1 kHz		0.2%		
	Efficiency	$R_L = 8\ \Omega$		80%		
A_V	Gain			24		dB
	Left/right channel gain matching			95%		
	Noise floor			60		dB
	Dynamic range			70		dB
	Crosstalk	f = 1 kHz		55		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20,000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JP}$	Thermal resistance, junction-to-pad				10	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-pad†			22.3		°C/W

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PARAMETER MEASUREMENT INFORMATION

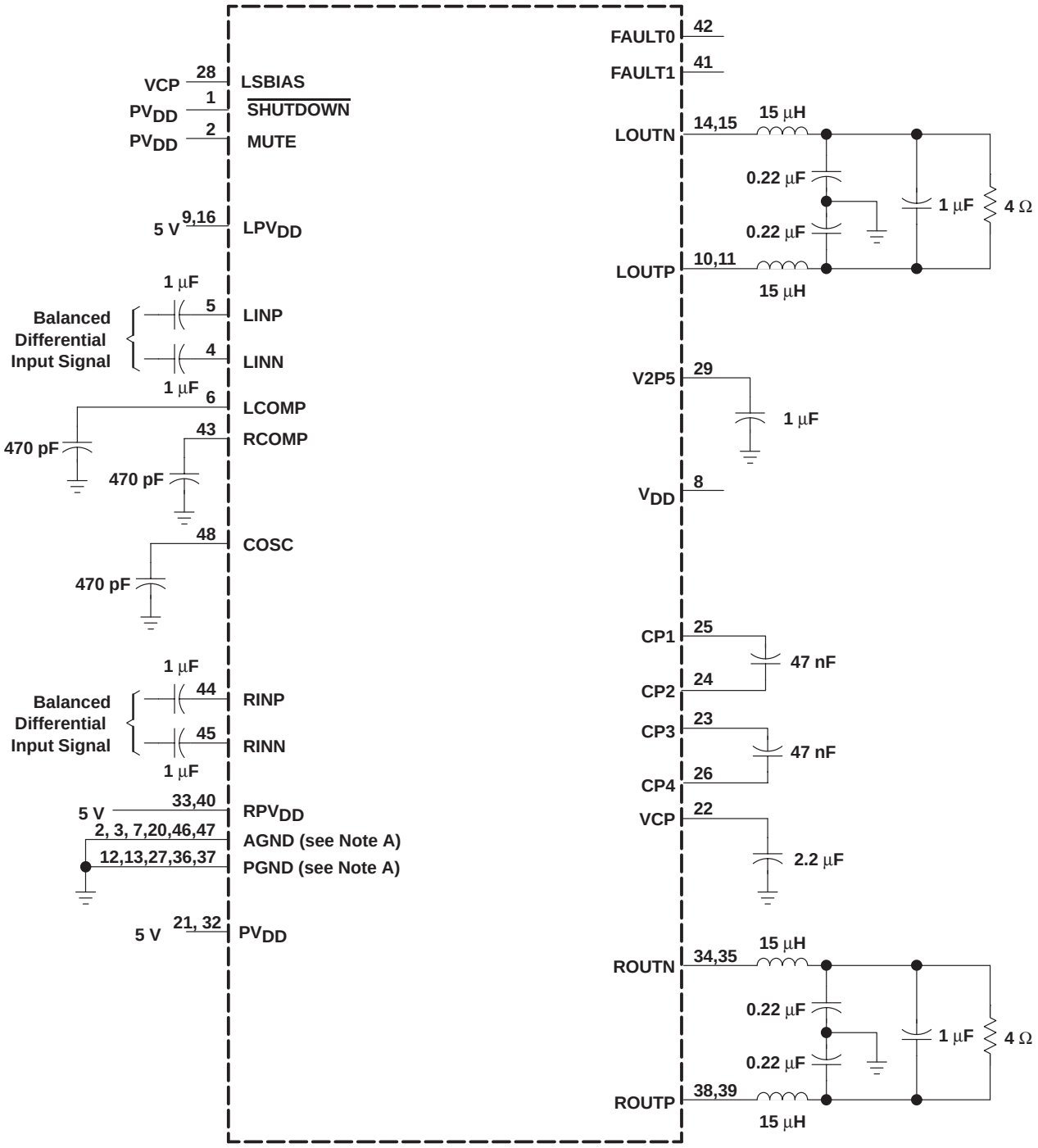


Figure 1. 5-V, 4-Ω Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{DD}	Supply current	vs Switching frequency	2
		vs Free-air temperature	3
THD+N	Total harmonic distortion plus noise	vs Frequency	4, 5
		vs Output power	6, 7
	Voltage amplification and phase shift	vs Frequency	8
	Crosstalk	vs Frequency	9
	Efficiency	vs Output power	10

SUPPLY CURRENT
vs
SWITCHING FREQUENCY

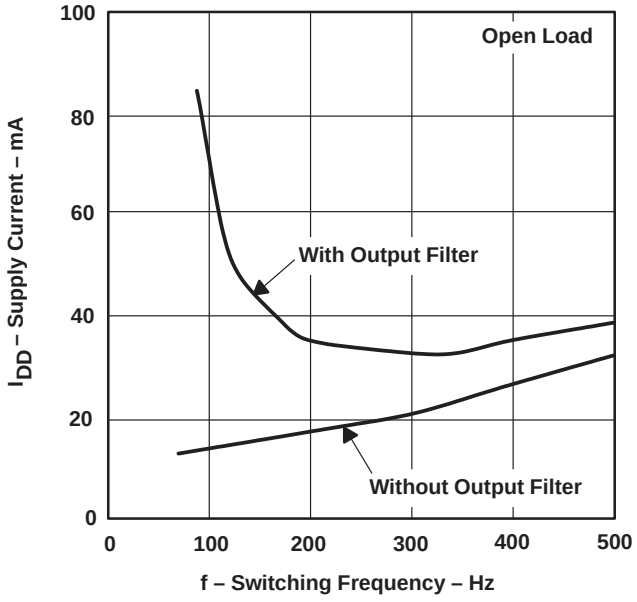


Figure 2

SUPPLY CURRENT
vs
FREE–AIR TEMPERATURE

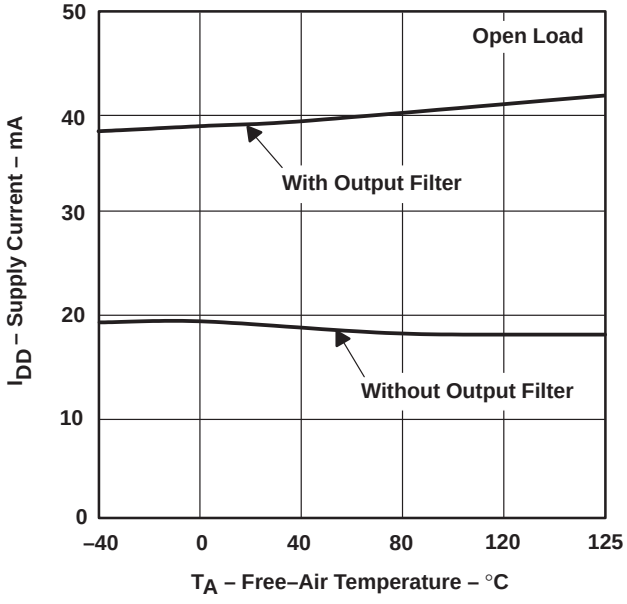


Figure 3

TYPICAL CHARACTERISTICS

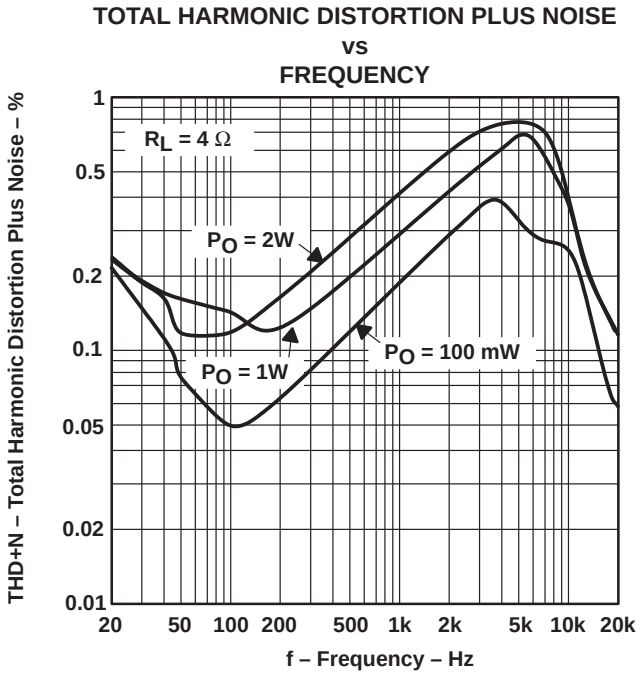


Figure 4

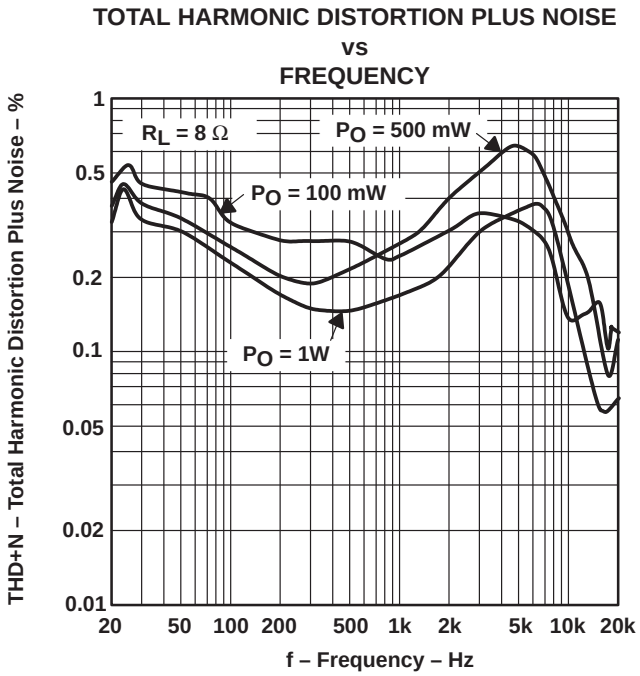


Figure 5

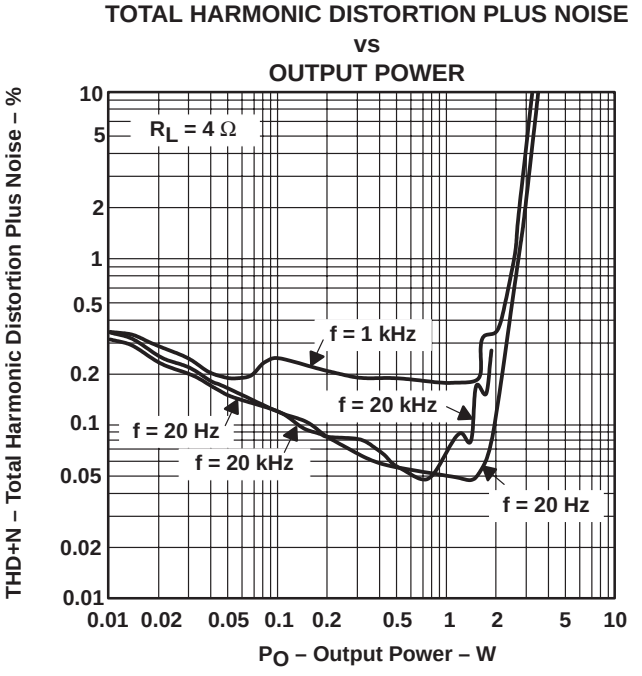


Figure 6

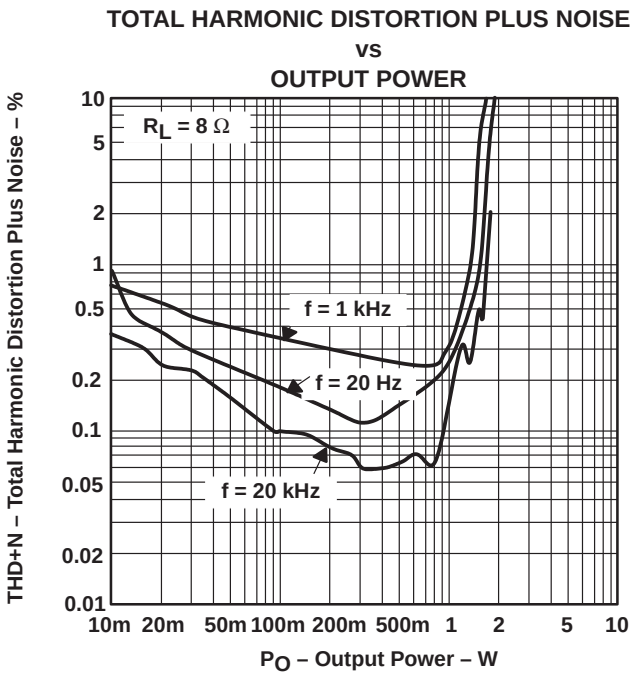


Figure 7

TYPICAL CHARACTERISTICS

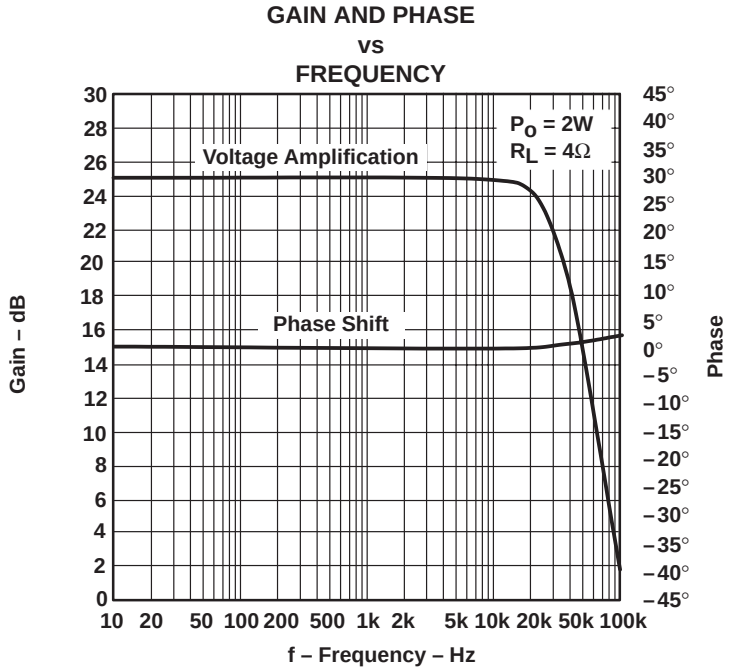


Figure 8

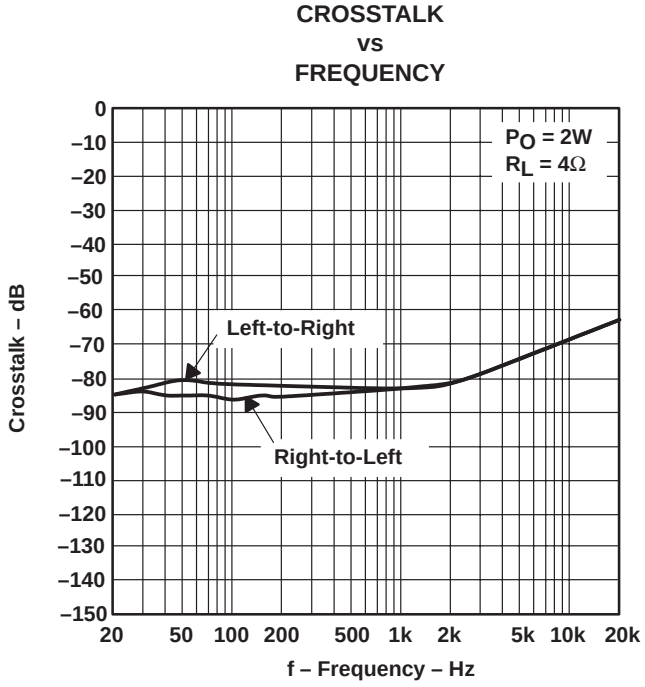


Figure 9

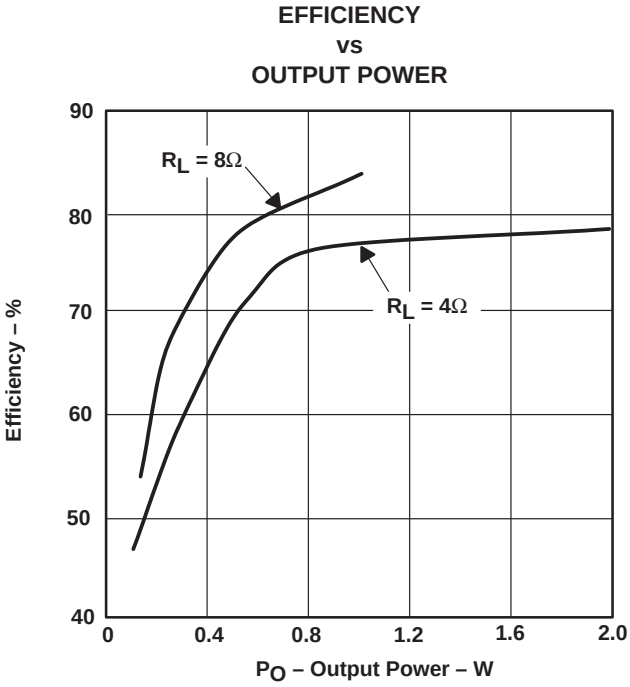


Figure 10

THERMAL INFORMATION

The thermally enhanced DCA package is based on the 56-pin TSSOP, but includes a thermal pad (see Figure 11) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

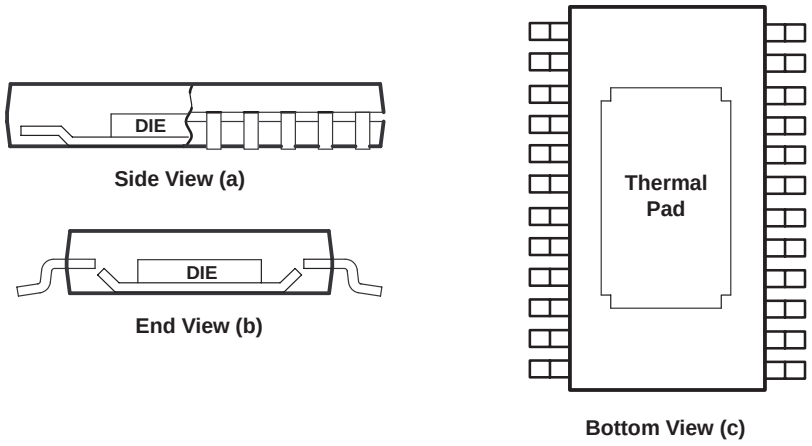
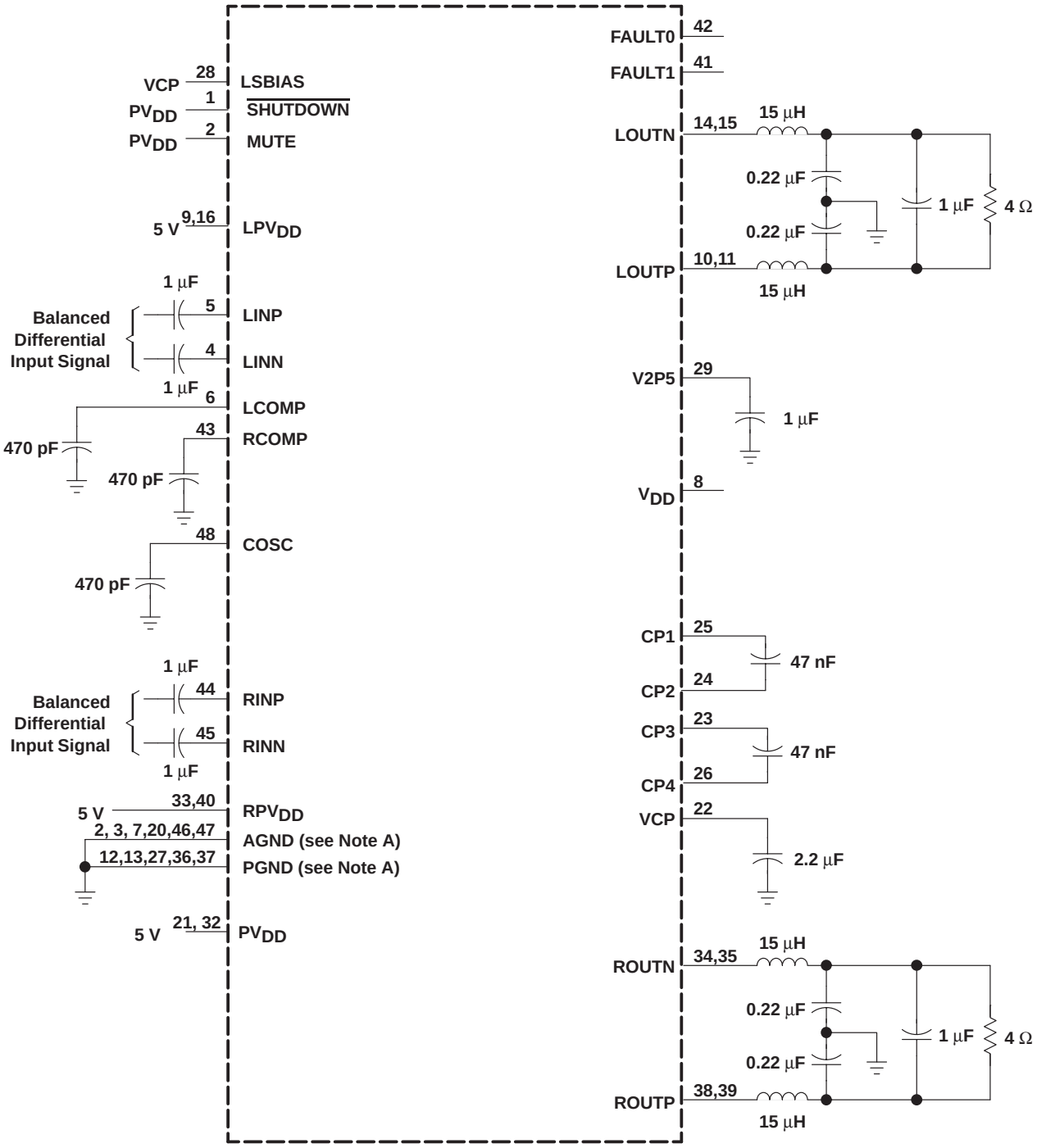


Figure 11. Views of Thermally Enhanced DCA Package

selection of components

Figure 12 is a schematic diagram of a typical notebook computer application circuit.

APPLICATION INFORMATION



NOTE A: A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 12. TPA005D02 Typical Configuration Application Circuit

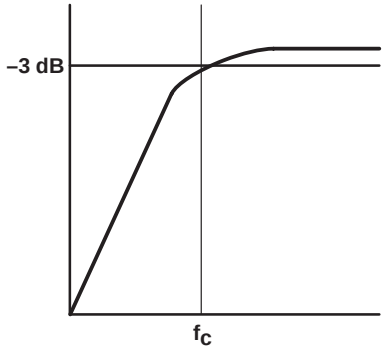
APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_{IN}, the TPA005D002's input resistance forms a high-pass filter with the corner frequency determined in equation 8.

$$f_{c(highpass)} = \frac{1}{2\pi R_{IN} C_I} \quad (8)$$

R_{IN} is nominally 10 kΩ



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_{IN} f_c} \quad (9)$$

In this example, C_I is 0.40 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A low-leakage tantalum or ceramic capacitor is the best choice for the input capacitors. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input as the dc level there is held at 1.5 V, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

differential input

The TPA005D02 has differential inputs to minimize distortion at the input to the IC. Since these inputs nominally sit at 1.5 V, dc-blocking capacitors are required on each of the four input terminals. If the signal source is single-ended, optimal performance is achieved by treating the signal ground as a signal. In other words, reference the signal ground at the signal source, and run a trace to the dc-blocking capacitor which should be located physically close to the TPA005D02. If this is not feasible, it is still necessary to locally ground the unused input terminal through a dc-blocking capacitor.

power supply decoupling, C_S

The TPA005D02 is a high-performance Class-D CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device's various V_{DD} leads works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

The TPA005D02 has several different power supply terminals. This was done to isolate the noise resulting from high-current switching from the sensitive analog circuitry inside the IC.

APPLICATION INFORMATION

mute and shutdown modes

The TPA005D02 employs both a mute and a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 400 μA. Mute mode alone reduces I_{DD} to 10 mA.

Table 2. Shutdown and Mute Mode Functions

INPUTS†				OUTPUT	AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	HP/$\overline{\text{LINE}}$	MUTE IN	$\overline{\text{SHUTDOWN}}$	MUTE OUT	INPUT	OUTPUT
Low	Low	Low	Low	Low	L/R Line	BTL
X	X	—	High	—	X	Mute
X	X	High	—	High	X	Mute
Low	High	Low	Low	Low	L/R HP	BTL
High	Low	Low	Low	Low	L/R Line	SE
High	High	Low	Low	Low	L/R HP	SE

† Inputs should never be left unconnected.
X = do not care

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

output filter components

The output inductors are key elements in the performance of the class D audio amplifier system. It is important that these inductors have a high enough current rating and a relatively constant inductance over frequency and temperature. The current rating should be higher than the expected maximum current to avoid magnetically saturating the inductor. When saturation occurs, the inductor loses its functionality and looks like a short circuit to the PWM signal, which increases the harmonic distortion considerably.

A shielded inductor may be required if the class D amplifier is placed in an EMI sensitive system; however, the switching frequency is low for EMI considerations and should not be an issue in most systems. The DC series resistance of the inductor should be low to minimize losses due to power dissipation in the inductor, which reduces the efficiency of the circuit.

Capacitors are important in attenuating the switching frequency and high frequency noise, and in supplying some of the current to the load. It is best to use capacitors with low equivalent-series-resistance (ESR). A low ESR means that less power is dissipated in the capacitor as it shunts the high-frequency signals. Placing these capacitors in parallel also parallels their ESR, effectively reducing the overall ESR value. The voltage rating is also important, and, as a rule of thumb, should be 2 to 3 times the maximum rms voltage expected to allow for high peak voltages and transient spikes. These output filter capacitors should be stable over temperature since large currents flow through them.

APPLICATION INFORMATION

efficiency of class D vs linear operation

Amplifier efficiency is defined as the ratio of output power delivered to the load to power drawn from the supply. In the efficiency equation below, P_L is power across the load and P_{SUP} is the supply power.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

A high-efficiency amplifier has a number of advantages over one with lower efficiency. One of these advantages is a lower power requirement for a given output, which translates into less waste heat that must be removed from the device, smaller power supply required, and increased battery life.

Audio power amplifier systems have traditionally used linear amplifiers, which are well known for being inefficient. Class D amplifiers were developed as a means to increase the efficiency of audio power amplifier systems.

A linear amplifier is designed to act as a variable resistor network between the power supply and the load. The transistors operate in their linear region and voltage that is dropped across the transistors (in their role as variable resistors) is lost as heat, particularly in the output transistors.

The output transistors of a class D amplifier switch from full OFF to full ON (saturated) and then back again, spending very little time in the linear region in between. As a result, very little power is lost to heat because the transistors are not operated in their linear region. If the transistors have a low ON resistance, little voltage is dropped across them, further reducing losses. The ideal class D amplifier is 100% efficient, which assumes that both the ON resistance ($R_{DS(ON)}$) and the switching times of the output transistors are zero.

the ideal class D amplifier

To illustrate how the output transistors of a class D amplifier operate, a half-bridge application is examined first (Figure 13).

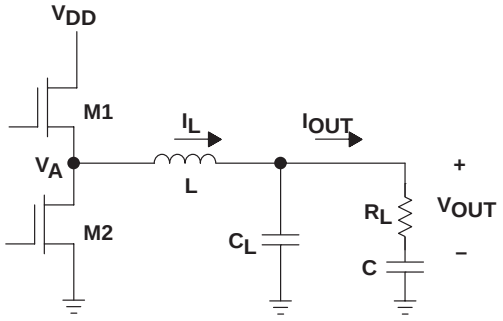


Figure 13. Half-Bridge Class D Output Stage

Figures 14 and 15 show the currents and voltages of the half-bridge circuit. When transistor M1 is on and M2 is off, the inductor current is approximately equal to the supply current. When M2 switches on and M1 switches off, the supply current drops to zero, but the inductor keeps the inductor current from dropping. The additional inductor current is flowing through M2 from ground. This means that V_A (the voltage at the drain of M2, as shown in Figure 13) transitions between the supply voltage and slightly below ground. The inductor and capacitor form a low-pass filter, which makes the output current equal to the average of the inductor current. The low pass filter averages V_A, which makes V_{OUT} equal to the supply voltage multiplied by the duty cycle.

APPLICATION INFORMATION

the ideal class D amplifier (continued)

Control logic is used to adjust the output power, and both transistors are never on at the same time. If the output voltage is rising, M1 is on for a longer period of time than M2.

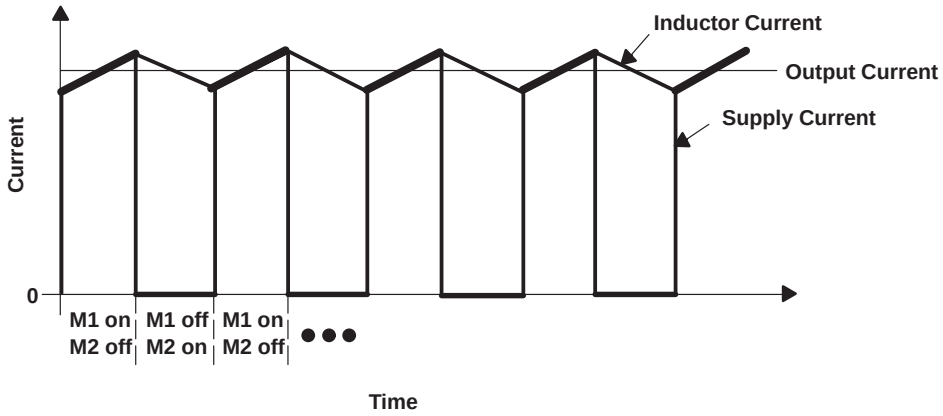


Figure 14. Class D Currents

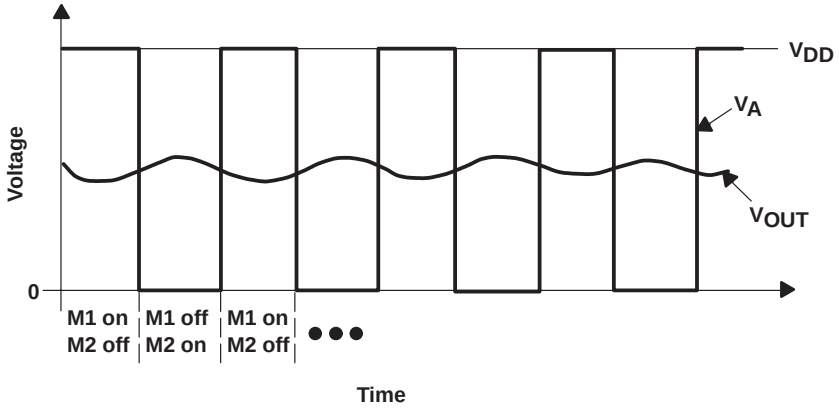


Figure 15. Class D Voltages

APPLICATION INFORMATION

the ideal class D amplifier (continued)

Given these plots, the efficiency of the class D device can be calculated and compared to an ideal linear amplifier device. In the derivation below, a sine wave of peak voltage (V_P) is the output from an ideal class D and linear amplifier and the efficiency is calculated.

CLASS D	LINEAR
$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$	$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$
$\text{Average}\left(I_{DD}\right) = \frac{I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$P_L = \frac{V_{L(rms)}^2}{R_L} = \frac{V_P^2}{2\ R_L}$
$P_L = V_L \times I_L$	$\text{Average}\left(I_{DD}\right) = \frac{2}{\pi} \times \frac{V_P}{R_L}$
$P_{SUP} = V_{DD} \times \text{Average}\left(I_{DD}\right)$	$P_{SUP} = V_{DD} \times \text{Average}\left(I_{DD}\right) = \frac{V_{DD}\ V_P}{R_L} \times \frac{2}{\pi}$
$P_{SUP} = \frac{V_{DD} \times I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$
$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$	$\text{Efficiency} = \eta = V_{DD} \times \frac{\frac{V_P^2}{2R_L}}{\frac{2}{\pi} \times \frac{V_P}{R_L}}$
$\text{Efficiency} = \eta = 1$	$\text{Efficiency} = \eta = \frac{\pi}{4} \times \frac{V_P}{V_{DD}}$

In the ideal efficiency equations, assume that $V_P = V_{DD}$, which is the maximum sine wave magnitude without clipping. Then, the highest efficiency that a linear amplifier can have without clipping is 78.5%. A class D amplifier, however, can ideally have an efficiency of 100% at all power levels.

The derivation above applies to an H-bridge as well as a half-bridge. An H-bridge requires approximately twice the supply current but only requires half the supply voltage to achieve the same output power—factors that cancel in the efficiency calculation. The H-bridge circuit is shown in Figure 16.

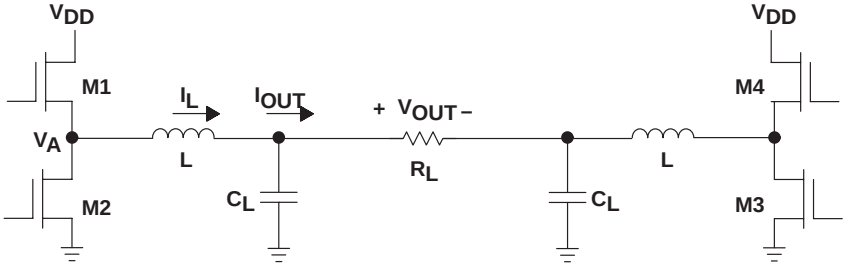


Figure 16. H-Bridge Class D Output Stage

APPLICATION INFORMATION

losses in a real-world class D amplifier

Losses make class D amplifiers nonideal, and reduce the efficiency below 100%. These losses are due to the output transistors having a nonzero $R_{DS(on)}$, and rise and fall times that are greater than zero.

The loss due to a nonzero $R_{DS(on)}$ is called conduction loss, and is the power lost in the output transistors at nonswitching times, when the transistor is ON (saturated). Any $R_{DS(on)}$ above 0 Ω causes conduction loss. Figure 17 shows an H-bridge output circuit simplified for conduction loss analysis and can be used to determine new efficiencies with conduction losses included.

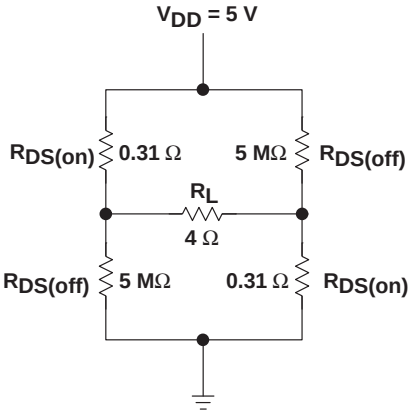


Figure 17. Output Transistor Simplification for Conduction Loss Calculation

The power supplied, P_{SUP}, is determined to be the power output to the load plus the power lost in the transistors, assuming that there are always two transistors on.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

$$\text{Efficiency} = \eta = \frac{I^2R_L}{I^2\ 2R_{DS(on)} + I^2R_L}$$

$$\text{Efficiency} = \eta = \frac{R_L}{2R_{DS(on)} + R_L}$$

$$\text{Efficiency} = \eta = 95\% \left(\text{at all output levels } R_{DS(on)} = 0.1,\ R_L = 4\right)$$

$$\text{Efficiency} = \eta = 87\% \left(\text{at all output levels } R_{DS(on)} = 0.31,\ R_L = 4\right)$$

APPLICATION INFORMATION

losses in a real-world class D amplifier (continued)

Losses due to rise and fall times are called switching losses. A plot of the output, showing switching losses, is shown in Figure 18.

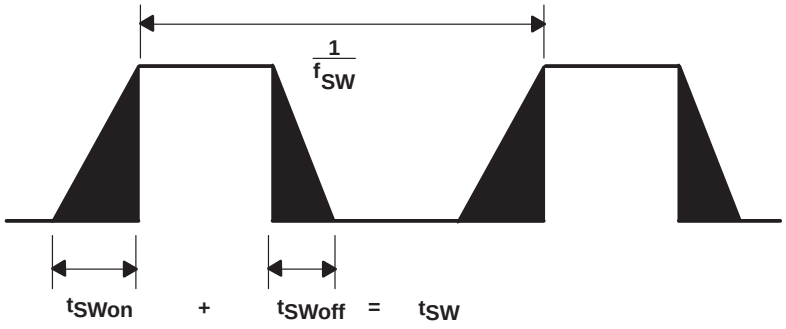


Figure 18. Output Switching Losses

Rise and fall times are greater than zero for several reasons. One is that the output transistors cannot switch instantaneously because (assuming a MOSFET) the channel from drain to source requires a specific period of time to form. Another is that transistor gate-source capacitance and parasitic resistance in traces form RC time constants that also increase rise and fall times.

Switching losses are constant at all output power levels, which means that switching losses can be ignored at high power levels in most cases. At low power levels, however, switching losses must be taken into account when calculating efficiency. Switching losses are dominated by conduction losses at the high output powers, but should be considered at low powers. The switching losses are automatically taken into account if you consider the quiescent current with the output filter and load.

class D effect on power supply

Efficiency calculations are an important factor for proper power supply design in amplifier systems. Table 2 shows Class D efficiency at a range of output power levels (per channel) with a 1-kHz sine wave input. The maximum power supply draw from a stereo 1-W per channel audio system with 8-Ω loads and a 5-V supply is almost 2.7 W. A similar linear amplifier such as the TPA005D02 has a maximum draw of 3.25 W under the same circumstances.

Table 3. Efficiency vs Output Power in 5-V 8-Ω H-Bridge Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.25	63.4	2	0.145
0.5	73	2.83	0.183
0.75	77.1	3.46	0.222
1	79.3	4	0.314
1.25	80.6	4.47†	0.3

† High peak voltages cause the THD to increase

APPLICATION INFORMATION

class D effect on power supply (continued)

There is a minor power supply savings with a class D amplifier versus a linear amplifier when amplifying sine waves. The difference is much larger when the amplifier is used strictly for music. This is because music has much lower RMS output power levels, given the same peak output power (Figure 19); and although linear devices are relatively efficient at high RMS output levels, they are very inefficient at mid-to-low RMS power levels. The standard method of comparing the peak power to RMS power for a given signal is crest factor, whose equation is shown below. The lower RMS power for a set peak power results in a higher crest factor

$$\text{Crest Factor} = 10 \log \frac{P_{PK}}{P_{rms}}$$

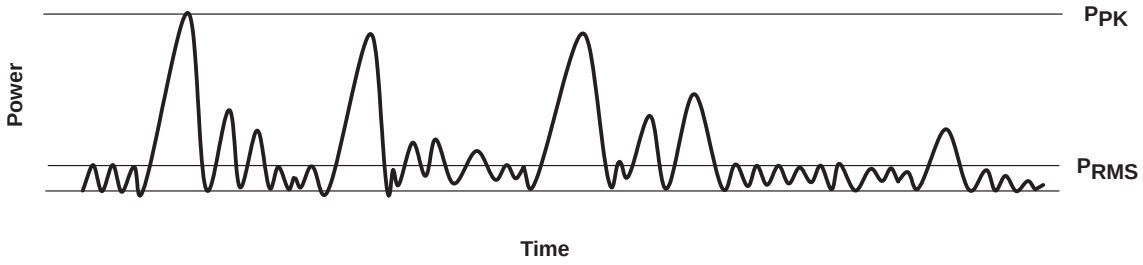


Figure 19. Audio Signal Showing Peak and RMS Power

Figure 20 is a comparison of a 5-V class D amplifier to a similar linear amplifier playing music that has a 13.76-dB crest factor. From the plot, the power supply draw from a stereo amplifier that is playing music with a 13.76 dB crest factor is 1.02 W, while a class D amplifier draws 420 mW under the same conditions. This means that just under 2.5 times the power supply is required for a linear amplifier over a class D amplifier.

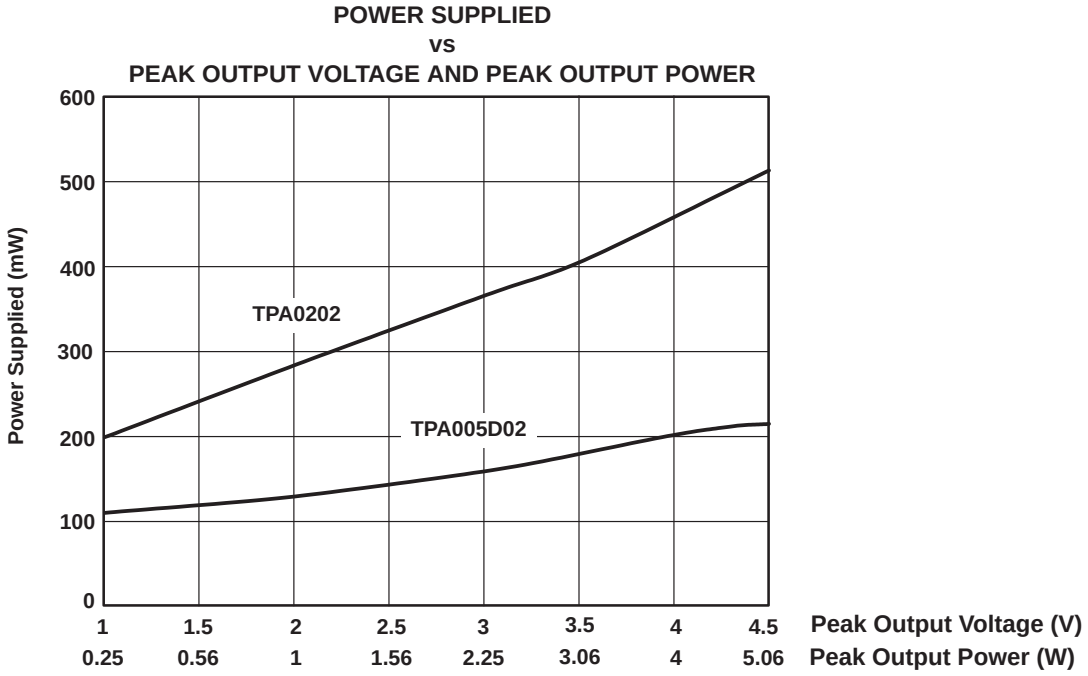


Figure 20. Audio Signal Showing Peak and RMS Power (with Music Applied)

APPLICATION INFORMATION

class D effect on battery life

Battery operations for class D amplifiers versus linear amplifiers have similar power supply savings results. The essential contributing factor to longer battery life is lower RMS supply current. Figure 21 compares the TPA005D02 supply current to the supply current of the TPA0202, a 2-W linear device, while playing music at different peak voltage levels.

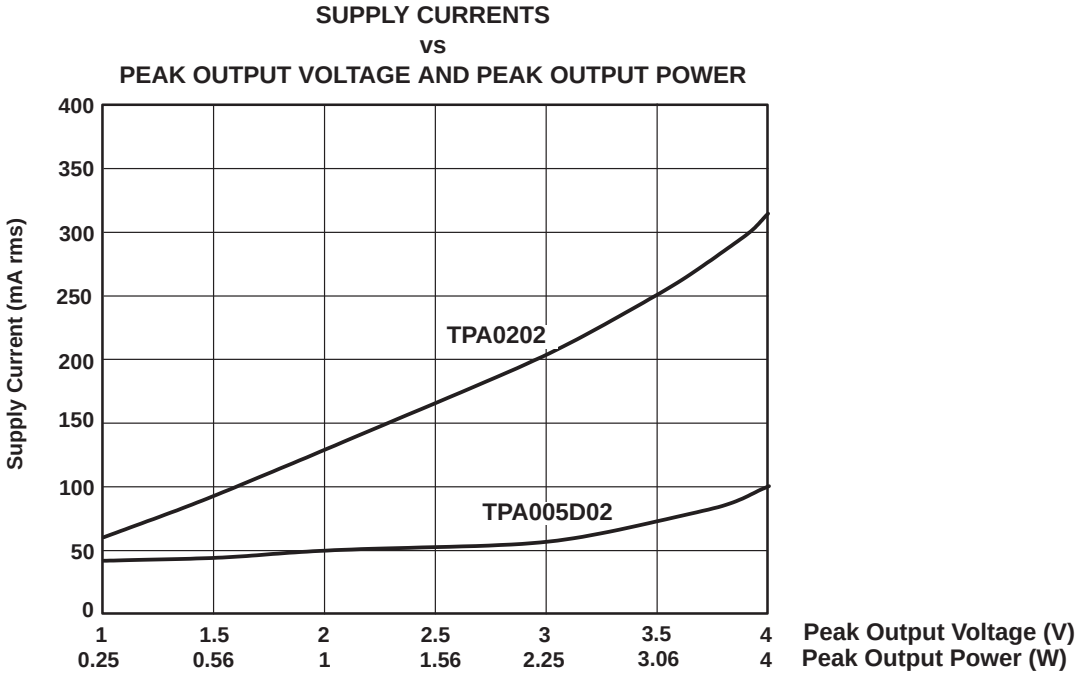


Figure 21. Supply Current vs Peak Output Voltage of TPA005D02 vs TPA0202 With Music Input

This plot shows that a linear amplifier has approximately three times more current draw at normal listening levels than a class D amplifier. Thus, a class D amplifier has approximately three times longer battery life at normal listening levels. If there is other circuitry in the system drawing supply current, that must also be taken into account when estimating battery life savings.

APPLICATION INFORMATION

crest factor and thermal considerations

A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA005D02 data sheet, one can see that when the TPA005D02 is operating from a 5-V supply into a 4-Ω speaker that 4 W peaks are available. Converting Watts to dB:

$$P_{dB} = 10\,\text{Log}\left(\frac{P_W}{P_{ref}}\right) = 10\text{Log}\left(\frac{4}{1}\right) = 6\ \text{dB} \tag{17}$$

Subtracting the crest factor restriction to obtain the average listening level without distortion yields:

6.0 dB − 18 dB = − 12 dB (15 dB crest factor)
6.0 dB − 15 dB = − 9 dB (15 dB crest factor)
6.0 dB − 12 dB = − 6 dB (12 dB crest factor)
6.0 dB − 9 dB = − 3 dB (9 dB crest factor)
6.0 dB − 6 dB = − 0 dB (6 dB crest factor)
6.0 dB − 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \tag{18}$$

= 63 mW (18 dB crest factor)
= 125 mW (15 dB crest factor)
= 250 mW (12 dB crest factor)
= 500 mW (9 dB crest factor)
= 1000 mW (6 dB crest factor)
= 2000 mW (3 dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 4-Ω system, the internal dissipation in the TPA005D02 and maximum ambient temperatures is shown in Table 4.

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 4. TPA005D02 Power Rating, 5-V, 4-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	0.56	125°C
4	1000 mW (6 dB)	0.30	136°C
4	500 mW (9 dB)	0.23	139°C
4	250 mW (12 dB)	0.20	141°C
4	120 mW (15 dB)	0.14	143°C
4	63 mW (18 dB)	0.09	146°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
DCA	5.6 W	44.8 mW/°C	3.5 W	2.9 W

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 CFM data from the dissipation rating table, the derating factor for the DCA package with 6.9 in^2 of copper area on a multilayer PCB is 44.8 mW/°C. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}} \quad (19)$$

$$= \frac{1}{0.0448}$$

$$= 22.3°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA005D02 is 150 °C. The internal dissipation figures are taken from the Efficiency vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \quad (20)$$

$$= 150 - 22.3(0.14 \times 2) = 143°C \text{ (15 dB crest factor)}$$

$$= 150 - 22.3(0.56 \times 2) = 125°C \text{ (3dB crest factor)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with a 15 dB crest factor per channel.

Table 4 shows that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA005D02 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 4 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

THERMAL INFORMATION

The thermally enhanced DCA package is based on the 56-pin TSSOP, but includes a thermal pad (see Figure 59) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface-mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

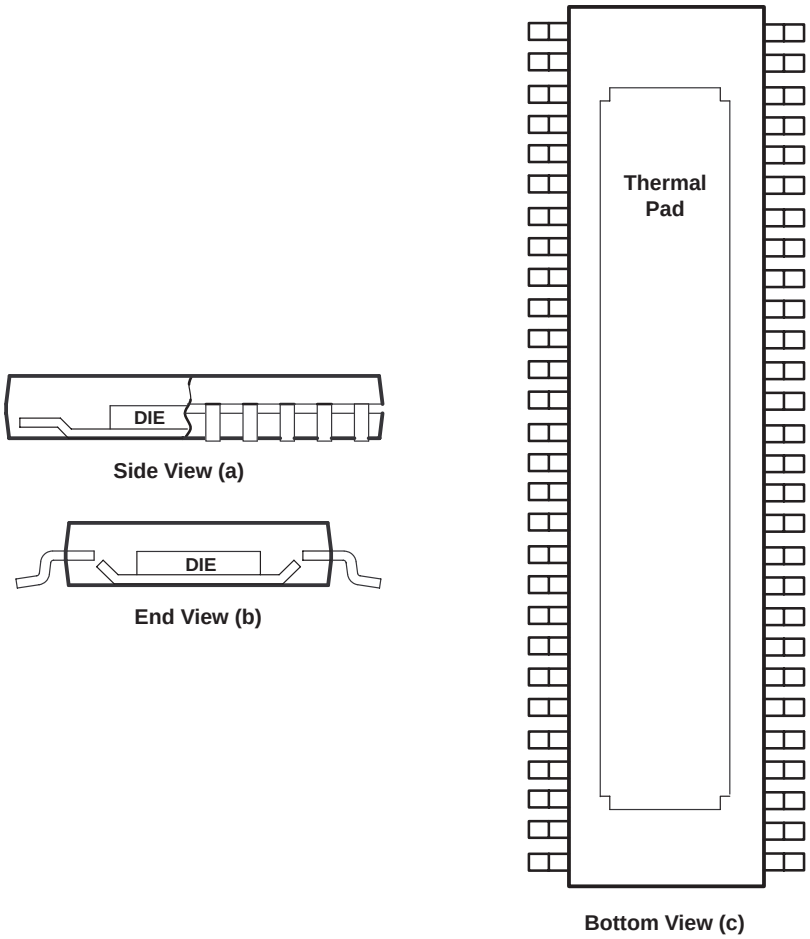
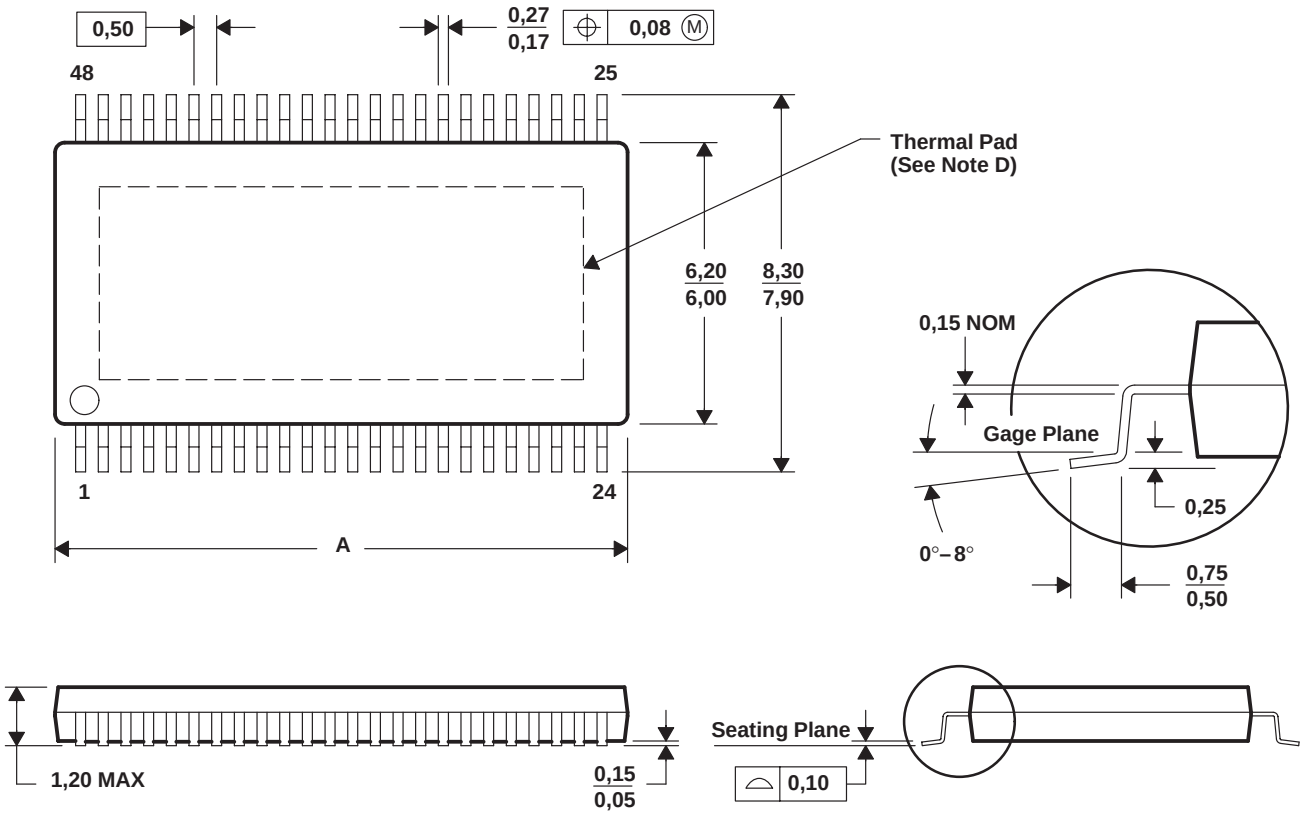


Figure 22. Views of Thermally Enhanced DCA Package

MECHANICAL DATA

DCA (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4073259/A 01/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

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