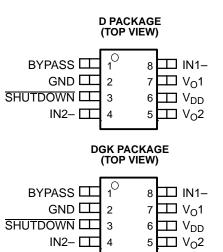




50-mW ULTRALOW VOLTAGE STEREO HEADPHONE AUDIO POWER AMPLIFIER

FEATURES

- 50-mW Stereo Output
- Low Supply Current . . . 0.75 mA
- Low Shutdown Current . . . 50 nA
- Pin Compatible With LM4881 and TPA102 (1)
- Pop Reduction Circuitry
- Internal Midrail Generation
- Thermal and Short-Circuit Protection
- Surface-Mount Packaging – MSOP and SOIC
- 1.6-V to 3.6-V Supply Voltage Range



(1) The polarity of the SHUTDOWN pin is reversed.

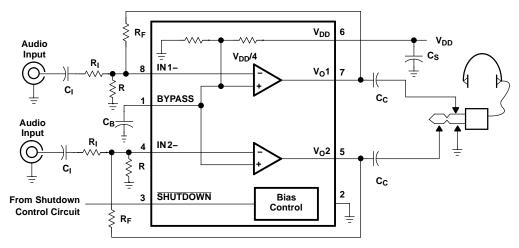
DESCRIPTION

The TPA6100A2D is a stereo audio power amplifier packaged in either an 8-pin SOIC package or an 8-pin MSOP package capable of delivering 50 mW of continuous RMS power per channel into 16- Ω loads. Amplifier gain is externally configured by a means of three resistors per input channel and does not require external compensation for settings of 1 to 10.

The TPA6100A2D is optimized for battery applications because of its low supply current, shutdown current, and THD+N. To obtain the low-supply voltage range, the TPA6100A2D biases BYPASS to $V_{DD}/4$. A resistor with a resistance equal to R_F must be added from the inputs to ground to allow the output to be biased at $V_{DD}/2$.

When driving a 16- Ω load with 45-mW output power from 3.3 V, THD+N is 0.04% at 1 kHz, and less than 0.2% across the audio band of 20 Hz to 20 kHz. For 28 mW into 32- Ω loads, the THD+N is reduced to less than 0.03% at 1 kHz, and is less than 0.2% across the audio band of 20 Hz to 20 kHz.

TYPICAL APPLICATION CIRCUIT





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS	AVA	ILABLE	OPTIONS
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т	PACKAG	ED DEVICE	MSOP
I A I	SMALL OUTLINE (D)	MSOP(DGK)	SYMBOLIZATION
–40°C to 85°C	TPA6100A2D	TPA6100A2DGK	AJL

Terminal Functions

TERMIN	4L	I/O	DESCRIPTION
NAME	NO.	1/0	DESCRIPTION
BYPASS	1	I	Tap to voltage divider for internal mid-supply bias supply. BYPASS is set at $V_{DD}/4$. Connect to a 0.1- μ F to 1- μ F low-ESR capacitor for best performance.
GND	2	Ι	GND is the ground connection.
IN1-	8	I	IN1- is the inverting input for channel 1.
IN2-	4	I	IN2- is the inverting input for channel 2.
SHUTDOWN	3	I	Active-low input. When held low, the device is placed in a low supply current mode.
V _{DD}	6	Ι	V _{DD} is the supply voltage terminal.
V ₀ 1	7	0	V ₀ 1 is the audio output for channel 1.
V _O 2	5	0	V ₀ 2 is the audio output for channel 2.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		UNIT
V_{DD}	Supply voltage	4 V
VI	Input voltage	–0.3 V to V _{DD} + 0.3 V
	Continuous total power dissipation	Internally limited
TJ	Operating junction temperature range	-40°C to 150°C
T _{stg}	Storage temperature range	–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond thoselisted under "absolute maximum ratings" may cause permanent damage to thedevice. These are stress ratings only, and functional operation of the deviceat these or any other conditions beyond those indicated under "recommendedoperating conditions" is not implied. Exposure to absolute-maximum-ratedconditions for extended periods may affect devicereliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25^{\circ}C$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
D	710 mW	5.68 mW/°C	454 mW	369 mW
DGK	469 mW	3.75 mW/°C	300 mW	244 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage		1.6	3.6	V
T _A	Operating free-air temperature		-40	85	°C
V_{IH}	High-level input voltage	SHUTDOWN	0.6 x V _{DD}		V
V_{IL}	Low-level input voltage	SHUTDOWN		$0.25 ext{ x V}_{\text{DD}}$	v

DC ELECTRICAL CHARACTERISTICS

at $T_A = 25^{\circ}C$, $V_{DD} = 3.6$ V (Unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OO}	Output offset voltage	$A_V = 2 V/V$		5	40	mV
PSRR	Power supply rejection ratio	V _{DD} = 3.0 V to 3.6 V		72		dB
I _{DD}	Supply current	SHUTDOWN = 3.6 V		0.75	2.0	mA
I _{DD(SD)}	Supply current in SHUTDOWN mode	SHUTDOWN = 0 V		50	250	nA
I _{IH}	High-level input current (SHUTDOWN)	$V_{DD} = 3.6 \text{ V}, V_{I} = V_{DD}$			1	μA
I _{IL}	Low-level input current (SHUTDOWN)	$V_{DD} = 3.6 V, V_I = 0 V$			1	μA
ZI	Input impedance (IN1-, IN2-)			> 1		MΩ

AC OPERATING CHARACTERISTICS

 $V_{DD}\,{=}\,3.3~V,\,T_{A}\,{=}\,25^{\circ}C,\,R_{L}\,{=}\,16~\Omega$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Po	Output power (each channel)	THD \leq 0.1%, f = 1 kHz		50		mW
THD+N	Total harmonic distortion + noise	P _O = 45 mW, 20 Hz–20 kHz		0.2%		
B _{OM}	Maximum output power BW	G = 1, THD < 0.5%		> 20		kHz
k _{SVR}	Supply ripple rejection	f = 1 kHz		52		dB
SNR	Signal-to-noise ratio	$P_0 = 50 \text{ mW}$		90		dB
V _n	Noise output voltage (no noise-weighting filter)			28		μV(rms)

AC OPERATING CHARACTERISTICS

 $V_{\text{DD}} = 3.3 \text{ V}, \text{ } \text{T}_{\text{A}} = 25^{\circ}\text{C}, \text{ } \text{R}_{\text{L}} = 32 \text{ } \Omega$

	PARAMETER	TEST CONDITIONS	MIN	ГҮР Ми	AX UNIT
Po	Output power (each channel)	$THD \leq 0.1\%, \ f = 1 \ kHz$		35	mW
THD+N	Total harmonic distortion + noise	P _O = 30 mW, 20 Hz–20 kHz	0	.2%	
B _{OM}	Maximum output power BW	G = 1, THD < 0.2%	>	> 20	kHz
k _{SVR}	Supply ripple rejection	f = 1 kHz		52	dB
SNR	Signal-to-noise ratio	P _O = 35 mW		91	dB
V _n	Noise output voltage (no noise-weighting filter)			28	μV(rms)



DC ELECTRICAL CHARACTERISTICS

at $T_A = 25^{\circ}C$, $V_{DD} = 1.6$ V (Unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OO}	Output offset voltage	$A_V = 2 V/V$		5	40	mV
PSRR	Power supply rejection ratio	V_{DD} = 1.5 V to 1.7 V		80		dB
I _{DD}	Supply current	SHUTDOWN = 1.6 V		1.2	1.5	mA
I _{DD(SD)}	Supply current in SHUTDOWN mode	SHUTDOWN = 0 V		50	250	nA
lін	High-level input current (SHUTDOWN)	$V_{DD} = 1.6 \text{ V}, V_I = V_{DD}$			1	μA
I _{IL}	Low-level input current (SHUTDOWN)	V _{DD} = 1.6 V, V _I = 0 V			1	μA
ZI	Input impedance (IN1-, IN2-)			> 1		MΩ

AC OPERATING CHARACTERISTICS

 $V_{DD} = 1.6~V,~T_A = 25^{\circ}C,~R_L = 16~\Omega$

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
Po	Output power (each channel)	THD≤ 0.1%, f = 1 kHz	9.5		mW
THD+N	Total harmonic distortion + noise	P _O = 9.5 mW, 20 Hz–20 kHz	0.4%		
B _{OM}	Maximum output power BW	G = 0 dB, THD < 0.4%	> 20		kHz
k _{SVR}	Supply ripple rejection	f = 1 kHz	53		dB
SNR	Signal-to-noise ratio	P _O = 9.5 mW	86		dB
V _n	Noise output voltage (no noise-weighting filter)		18		μV(rms)

AC OPERATING CHARACTERISTICS

 V_{DD} = 1.6 V, T_A = 25°C, R_L = 32 Ω

	PARAMETER	TEST CONDITIONS	MIN TY	P MAX	UNIT
Po	Output power (each channel)	THD≤ 0.1%, f = 1 kHz	7	.1	mW
THD+N	Total harmonic distortion + noise	P _O = 6.5 mW, 20 Hz–20 kHz	0.3	%	
B _{OM}	Maximum output power BW	G = 0 dB, THD < 0.3%	> 2	20	kHz
k _{SVR}	Supply ripple rejection	f = 1 kHz	Ę	63	dB
SNR	Signal-to-noise ratio	P _O = 7.1 mW	8	8	dB
V _n	Noise output voltage (no noise-weighting filter)			8	μV(rms)

APPLICATION INFORMATION

GAIN SETTING RESISTORS, R_F, R_Land R

The voltage gain for the TPA6100A2D is set by resistors R_F and R_I according to Equation 1.

Gain =
$$-\left(\frac{R_F}{R_I}\right)$$
 or Gain (dB) = $20 \log\left(\frac{R_F}{R_I}\right)$ (1)

Given that the TPA6100A2D is an MOS amplifier, the input impedance is high. Consequently, input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together, it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 k Ω and 20 k Ω . The effective impedance is calculated in Equation 2.

Effective Impedance =
$$\frac{R_F R_I}{R_F + R_I}$$
 (2)

As an example, consider an input resistance of 20 k Ω and a feedback resistor of 20 k Ω . The gain of the amplifier would be -1 and the effective impedance at the inverting terminal would be 10 k Ω , which is within the recommended range.

For high-performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 k Ω , the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F . In effect, this creates a low-pass filter network with the cutoff frequency defined in Equation 3.

$$f_{C} = \frac{1}{2\pi R_{F}C_{F}}$$
(3)

For example, if R_F is 100 k Ω and C_F is 5 pF, then f_c is 318 kHz, which is well outside the audio range.

For maximum signal swing and output power at low supply voltages like 1.6 V to 3.3 V, BYPASS is biased to $V_{DD}/4$. However, to allow the output to be biased at $V_{DD}/2$, a resistor, R, equal to R_F must be placed from the negative input to ground.

INPUT CAPACITOR, C

In the typical application, an input capacitor, C_I , is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in Equation 4.

$$f_{C} = \frac{1}{2\pi R_{I}C_{I}}$$
⁽⁴⁾

The value of C₁ is important to consider, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where R₁ is 20 k Ω and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as Equation 5.

$$C_{l} = \frac{1}{2\pi R_{l} f_{c}}$$
(5)

In this example, C_I is 0.4 μ F, so one would likely choose a value in the range of 0.47 μ F to 1 μ F. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I , C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (>10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/4$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.



APPLICATION INFORMATION (continued)

POWER SUPPLY DECOUPLING, C_s

The TPA6100A2D is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μ F, placed as close as possible to the device V_{DD} lead, works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 10 μ F or greater placed near the power amplifier is recommended.

MIDRAIL BYPASS CAPACITOR, C_B

The midrail bypass capacitor (C_B) serves several important functions. During start-up, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 55-k Ω source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in Equation 6 should be maintained.

$$\frac{1}{\left(C_{B} \times 55 \text{ k}\Omega\right)} \leq \frac{1}{\left(C_{I}R_{I}\right)}$$

(6)

As an example, consider a circuit where C_B is 1 μ F, C_I is 1 μ F, and R_I is 20 k Ω . Inserting these values into Equation 6 results in: 18.18 \leq 50 which satisfies the rule. Bypass capacitor (C_B) values of 0.47- μ F to 1- μ F ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

OUTPUT COUPLING CAPACITOR, Cc

In the typical single-supply, single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 7.

$$f_{\rm C} = \frac{1}{2\pi R_{\rm L} C_{\rm C}} \tag{7}$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 μ F is chosen and loads vary from 32 Ω to 47 k Ω . Table 1 summarizes the frequency response characteristics of each configuration.

RL	Cc	LOWEST FREQUENCY
32 Ω	68 µF	73 Hz
10,000 Ω	68 µF	0.23 Hz
47,000 Ω	68 µF	0.05 Hz

 Table 1. Common Load Impedances vs Low Frequency

 Output Characteristics in SE Mode

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is good.

The output coupling capacitor required in single-supply, SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{\left(\mathsf{C}_{\mathsf{B}}\times55\,\mathsf{k}\Omega\right)}\leq\frac{1}{\left(\mathsf{C}_{\mathsf{I}}\mathsf{R}_{\mathsf{I}}\right)}\ll\frac{1}{\mathsf{R}_{\mathsf{L}}\mathsf{C}_{\mathsf{C}}}$$

(8)

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

3.3-V VERSUS 1.6-V OPERATION

The TPA6100A2D was designed for operation over a supply range of 1.6 V to 3.6 V. There are no special considerations for 1.6-V versus 3.3-V operation as far as supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier can produce a maxium output voltage swing within a few hundred millivolts of the rails with a 10-k Ω load. However, this voltage swing decreases as the load resistance decreases and the $r_{DS(on)}$ as the output stage transistors becomes more significant. For example, for a 32- Ω load, the maximum peak output voltage with $V_{DD} = 1.6$ V is approximately 0.7 V with no clipping distortion. This reduced voltage swing effectively reduces the maximum undistorted output power.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPA6100A2D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPA6100A2DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPA6100A2DGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPA6100A2DGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPA6100A2DGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPA6100A2DGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPA6100A2DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPA6100A2DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nomina	I											
Device	-	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6100A2DGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6100A2DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6100A2DGKR	MSOP	DGK	8	2500	358.0	335.0	35.0
TPA6100A2DR	SOIC	D	8	2500	346.0	346.0	29.0

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AA.



DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



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