

TENTATIVE

TOSHIBA INTELLIGENT POWER DEVICE  
SILICON MONOLITHIC POWER MOS INTEGRATED CIRCUIT

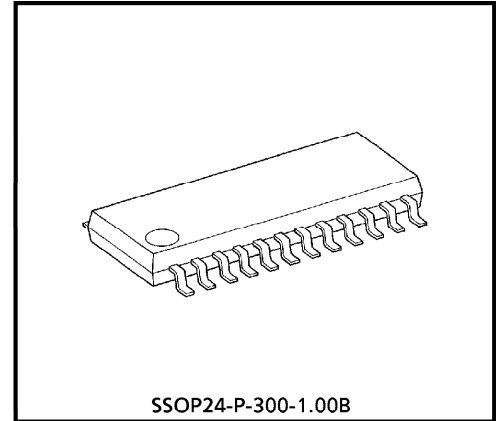
# TPD7203F

## POWER MOSFET GATE DRIVER FOR 3-PHASE DC MOTOR

TPD7203F is a power MOSFET Gate Driver for 3-Phase full-bridge circuit using charge pump system. Because this IC contains a charge pump circuit for high-side drive, it allows you to configure 3-phase full-bridge circuit.

### FEATURES

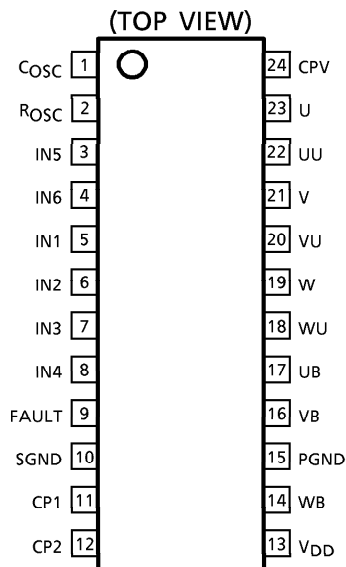
- Power MOSFET Gate Driver for 3-Phase DC Motor
- Built-in power MOSFET protection and diagnosis function: low-voltage protection
- Built-in a charge pump circuit
- Package: SSOP-24 (300 mil) with embossed-tape packing



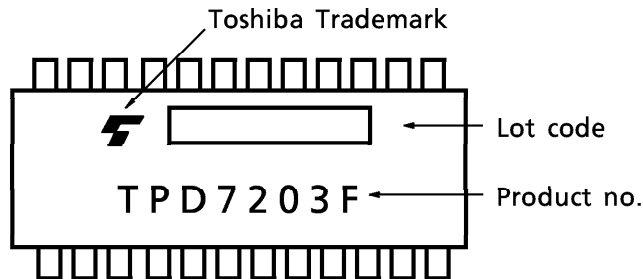
SSOP24-P-300-1.00B

Weight : 0.29 g (typ.)

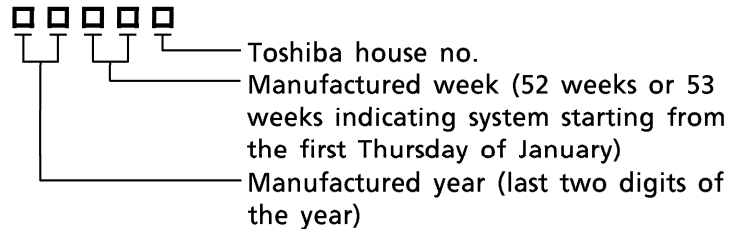
### PIN ASSIGNMENT



### MARKING



#### Lot code naming system



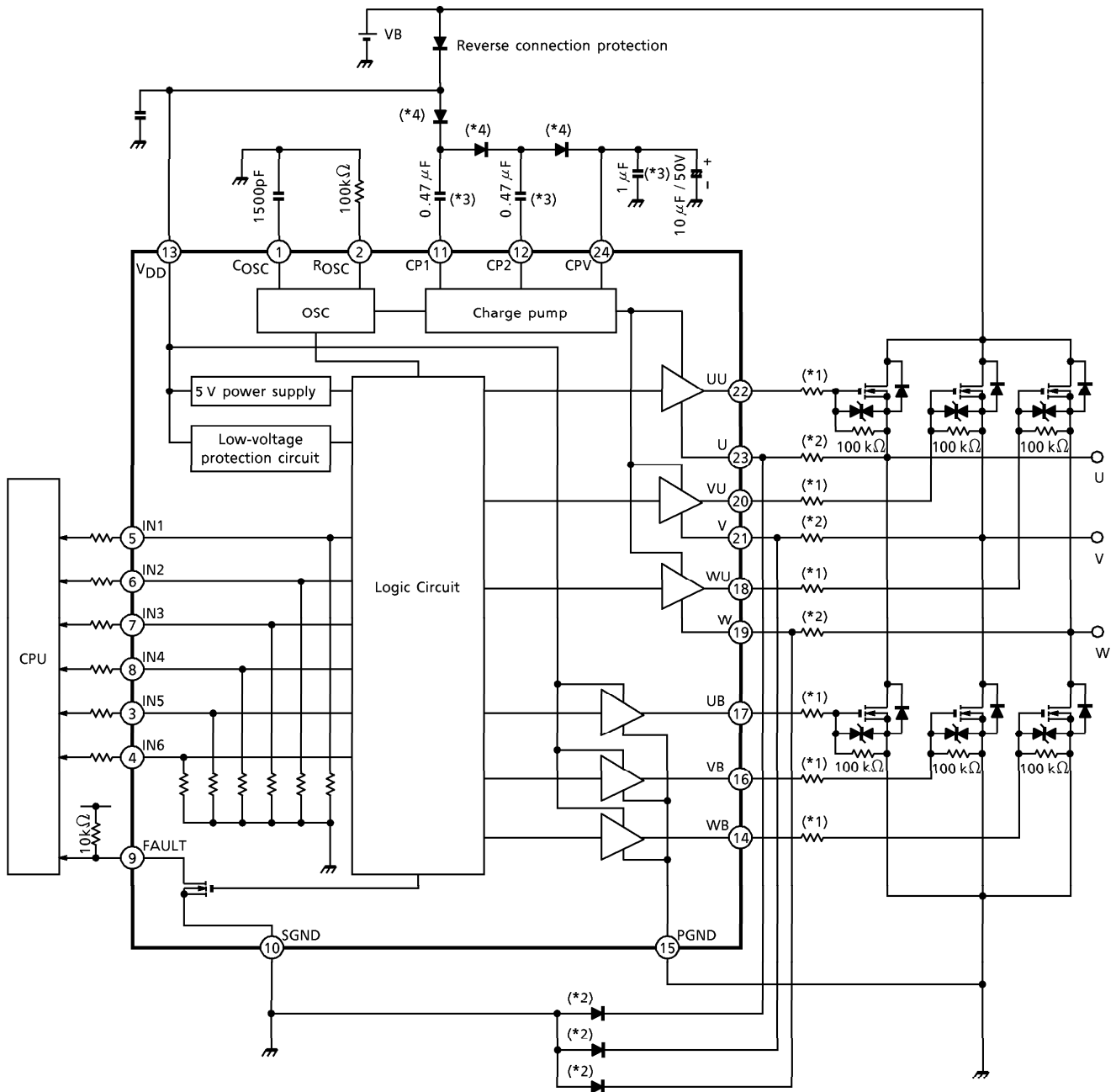
Because this product uses MOS structure, must take special care with electrostatic when handling.

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BLOCK DIAGRAM / APPLICATION CIRCUIT 1



(\*1) : Optimum conditions depend on switching loss, EMI, etc. of external MOSFET.

(\*2) : SBD  $V_F = 0.5V$  max (Recommended : CRS03)

This is needed when the U, V and W pin is biased to the negative side by more than 0.5 V.

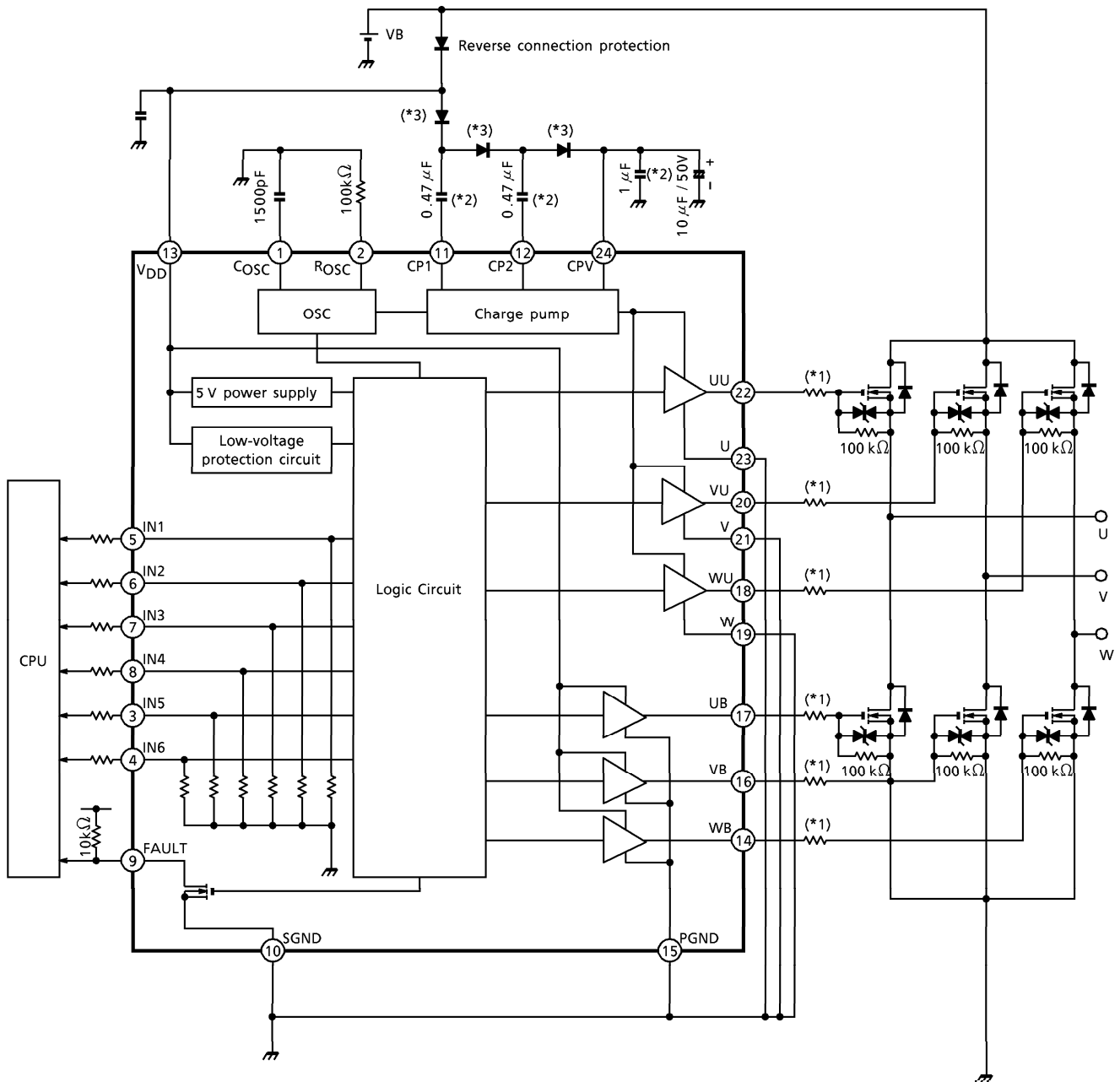
(\*3) : This is a laminated ceramic capacitor.

(\*4) : High-speed diode  $t_{rr} = 100$  ns max (Recommended : CRH01)

(Note) : When selecting external parts, please read "Method for selecting external parts" described later.

TENTATIVE

BLOCK DIAGRAM / APPLICATION CIRCUIT 2



- (\*1) : Optimum conditions depend on switching loss, EMI, etc. of external MOSFET.
- (\*2) : This is a laminated ceramic capacitor.
- (\*4) : High-speed diode  $t_{rr} = 100 \text{ ns max}$  (Recommended : CRH01)

(Note) : When selecting external parts, please read "Method for selecting external parts" described later.

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## PIN DESCRIPTION

PIN No.	SYMBOL	PIN DESCRIPTION
1	COSC	This pin sets the oscillation frequency for charge pump drive. Connect a 1500 pF (recommended) capacitor.
2	ROSC	This pin sets the oscillation frequency for charge pump drive. Connect a 100 k $\Omega$ (recommended) resistor.
3	IN5	Input pin: it controls the power MOSFET connected to VB and built-in pull-down resistor (100 k $\Omega$ typ.)
4	IN6	Input pin: it controls the power MOSFET connected to WB and built-in pull-down resistor (100 k $\Omega$ typ.)
5	IN1	Input pin: it controls the power MOSFET connected to UU and built-in pull-down resistor (100 k $\Omega$ typ.)
6	IN2	Input pin: it controls the power MOSFET connected to VU and built-in pull-down resistor (100 k $\Omega$ typ.)
7	IN3	Input pin: it controls the power MOSFET connected to WU and built-in pull-down resistor (100 k $\Omega$ typ.)
8	IN4	Input pin: it controls the power MOSFET connected to UB and built-in pull-down resistor (100 k $\Omega$ typ.)
9	FAULT	Diagnosis output pin: when low-voltage 6 V (typ.) is detected, output "H". Circuit configuration is N-ch open drain.
10	SGND	Signal block GND pin
11	CP1	Capacitor pin for charge pump Connect a 0.47 $\mu$ F (recommended) laminated ceramic capacitor.
12	CP2	Capacitor pin for charge pump Connect a 0.47 $\mu$ F (recommended) laminated ceramic capacitor.
13	VDD	Power supply pin: when low voltage (6 V typ.) is detected, all outputs are shut down.
14	WB	Drives the power MOSFET connected to the low side of W phase.
15	PGND	Power block GND pin
16	VB	Drives the power MOSFET connected to the low side of V phase.
17	UB	Drives the power MOSFET connected to the low side of U phase.
18	WU	Drives the power MOSFET connected to the high side of W phase.
19	W	W phase output pin
20	VU	Drives the power MOSFET connected to the high side of V phase.
21	V	V phase output pin
22	UU	Drives the power MOSFET connected to the high side of U phase.
23	U	U phase output pin
24	CPV	Final stage capacitor for the charge pump Connect 1 $\mu$ F (recommended) laminated ceramic capacitor and 10 $\mu$ F (recommended) aluminum electrolytic capacitor in parallel.

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**TRUTH TABLE** (All outputs go low for input in High side/Low side arm shorting mode)

MODE No.	INPUT						OUTPUT						REMARKS
	IN1 (UU)	IN2 (VU)	IN3 (WU)	IN4 (UB)	IN5 (VB)	IN6 (WB)	OUT UU	OUT VU	OUT WU	OUT UB	OUT VB	OUT WB	
01	L	L	L	L	L	L	L	L	L	L	L	L	
02	H	L	L	L	L	L	H	L	L	L	L	L	
03	L	H	L	L	L	L	L	H	L	L	L	L	
04	L	L	H	L	L	L	L	L	H	L	L	L	
05	L	L	L	H	L	L	L	L	L	H	L	L	
06	L	L	L	L	H	L	L	L	L	L	H	L	
07	L	L	L	L	L	H	L	L	L	L	L	H	
08	H	L	L	H	L	L	L	L	L	L	L	L	High side/Low side arm shorting mode (*)
09	H	L	L	L	H	L	H	L	L	L	H	L	120° square wave conducting normal mode
10	H	L	L	L	L	H	H	L	L	L	L	H	120° square wave conducting normal mode
11	L	H	L	H	L	L	L	H	L	H	L	L	120° square wave conducting normal mode
12	L	H	L	L	H	L	L	L	L	L	L	L	High side/Low side arm shorting mode (*)
13	L	H	L	L	L	H	L	H	L	L	L	H	120° square wave conducting normal mode
14	L	L	H	H	L	L	L	L	H	H	L	L	120° square wave conducting normal mode
15	L	L	H	L	H	L	L	L	H	L	H	L	120° square wave conducting normal mode
16	L	L	H	L	L	H	L	L	L	L	L	L	High side/Low side arm shorting mode (*)
17	H	H	L	L	L	L	H	H	L	L	L	L	
18	L	H	H	L	L	L	L	H	H	L	L	L	
19	H	L	H	L	L	L	H	L	H	L	L	L	
20	L	L	L	H	H	L	L	L	L	H	H	L	
21	L	L	L	L	H	H	L	L	L	L	H	H	
22	L	L	L	H	L	H	L	L	L	H	L	H	
23	H	H	L	H	L	L	L	L	L	L	L	L	High side/Low side arm shorting mode (*)
24	H	H	L	L	H	L	L	L	L	L	L	L	High side/Low side arm shorting mode (*)
25	H	H	L	L	L	H	H	H	L	L	L	H	
26	L	H	H	H	L	L	L	H	H	H	L	L	
27	L	H	H	L	H	L	L	L	L	L	L	L	High side/Low side arm shorting mode (*)
28	L	H	H	L	L	H	L	L	L	L	L	L	High side/Low side arm shorting mode (*)
29	H	L	H	H	L	L	L	L	L	L	L	L	High side/Low side arm shorting mode (*)
30	H	L	H	L	H	L	H	L	H	L	H	L	

(\*) : High side/Low side arm shorting mode is disabled by the internal logic. (FAULT is kept low.) When undervoltage (6V typ.) is detected, all outputs are pulled low regardless of input signals. At this time, FAULT output goes high (open-drain, high-impedance).

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MODE No.	INPUT						OUTPUT						REMARKS
	IN1 (UU)	IN2 (VU)	IN3 (WU)	IN4 (UB)	IN5 (VB)	IN6 (WB)	OUT UU	OUT VU	OUT WU	OUT UB	OUT VB	OUT WB	
31	H	L	H	L	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
32	H	L	L	H	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
33	H	L	L	L	H	H	H	L	L	L	H	H	
34	H	L	L	H	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
35	L	H	L	H	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
36	L	H	L	L	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
37	L	H	L	H	L	H	L	H	L	H	L	H	
38	L	L	H	H	H	L	L	L	H	H	H	L	
39	L	L	H	L	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
40	L	L	H	H	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
41	H	H	H	L	L	L	H	H	H	L	L	L	
42	L	L	L	H	H	H	L	L	L	H	H	H	
43	H	H	L	H	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
44	H	H	L	L	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
45	H	H	L	H	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
46	L	H	H	H	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
47	L	H	H	L	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
48	L	H	H	H	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
49	H	L	H	H	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
50	H	L	H	L	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
51	H	L	H	H	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
53	H	H	H	L	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
54	H	H	H	L	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
55	H	L	L	H	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
56	L	H	L	H	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
57	L	L	H	H	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
58	H	H	H	H	H	L	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
59	H	H	H	L	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
60	H	H	H	H	L	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
61	H	H	L	H	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
62	L	H	H	H	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
63	H	L	H	H	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)
64	H	H	H	H	H	H	L	L	L	L	L	L	High side / Low side arm shorting mode (*)

(\*) : High side / Low side arm shorting mode is disabled by the internal logic. (FAULT is kept low.) When undervoltage (6V typ.) is detected, all outputs are pulled low regardless of input signals. At this time, FAULT output goes high (open-drain, high-impedance).

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## MAXIMUM RATING (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT	REMARKS
Power Supply Voltage	V <sub>DD</sub>	-0.5~30	V	
Output Current	I <sub>SOURCE</sub>	1	A	Pulse width ≤ 10 μs
	I <sub>SINK</sub>	1		
Input Voltage	V <sub>IN</sub>	-0.5~7.0	V	
FAULT Pin Voltage	V <sub>FAULT</sub>	30	V	
U, V and W Pin Negative Voltage	U (-) V (-) W (-)	-0.5	V	Negative voltage that can be applied to U, V and W pins (reference to SGND pin)
PGND Pin Negative Voltage	PGND (-)	-0.5	V	Negative voltage that can be applied to PGND pin (reference to SGND pin)
Fault Pin Current	I <sub>FAULT</sub>	5	mA	
Power Dissipation	P <sub>D</sub>	0.8	W	
		1.5 (Note)		
Operating Temperature	T <sub>opr</sub>	-40~125	°C	
Storage Temperature	T <sub>stg</sub>	-40~150	°C	

## THERMAL RESISTANCE

CHARACTERISTIC	SYMBOL	RATING	UNIT
Junction to Ambient Thermal Resistance	R <sub>th(j-a)</sub>	156.3	°C/W
		83.4 (Note)	

(Note) : When a device mounted on 60 mm × 60 mm × 1.6 t glass epoxy PCB.

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ELECTRICAL CHARACTERISTICS (Unless otherwise specified,  $T_a = -40\sim 125^\circ\text{C}$ )

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARKS				
Operating Supply Voltage	$V_{DD}$	—	—	7	13.5	18	V					
Supply Current	$I_{DD(1)}$	1	$V_{DD} = 13.5\text{ V}$	—	—	10	mA	Oscillation circuit stops				
	$I_{DD(2)}$	2	$V_{DD} = 13.5\text{ V}$ , $V_{IN1}\sim V_{IN6} = 0\text{ V}$	—	—	100		When oscillation circuit is operating $f = 20\text{ kHz}$ , mean current				
Input Voltage	$V_{IH}$	2	$V_{DD} = 7\sim 18\text{ V}$ , $I_O = 0\text{ A}$	3.5	—	—	V	IN1-IN6 high-level input voltage				
	$V_{IL}$			—	—	1.5		IIN1-IN6 low-level input voltage				
Input Current	$I_{IH}$	2	$V_{DD} = 7\sim 18\text{ V}$ , $V_{IN} = 5\text{ V}$ , $I_O = 0\text{ A}$	—	—	1	mA	IN1-IN6 input current				
	$I_{IL}$			$V_{DD} = 7\sim 18\text{ V}$ , $V_{IN} = 0\text{ V}$ , $I_O = 0\text{ A}$	-10	—			10	$\mu\text{A}$		
Output Voltage	High side	2	$V_{DD} = 13.5\text{ V}$ , $V_{IN} = 5\text{ V}$ , $I_O = 0\text{ A}$	$V_{CPV-2}$	—	$V_{CPV}$	V	UU pin voltage (reference to U pin) VU pin voltage (reference to V pin) WU pin voltage (reference to W pin) $V_{CPV}$ denotes CPV pin voltage.				
								Low side	$V_{OH}$	11.5	—	13.5
	$V_{OL}$								—	—	0.1	
Charge Pump Voltage	$V_{CPV}$	2	$V_{DD} = 13.5\text{ V}$	30	—	35	V	CPV pin voltage (reference to SGND pin)				
Active Clamp Voltage (Low Side)	$V_{CLAMP}$	—	$V_{IN} = 5\text{ V}$ , $I_O = 10\text{ mA}$	—	18	—	V	UB, VB and WB pins clamp voltage (reference to PGND pin)				
Output Resistance	$R_{SOURCE}$	2	$V_{DD} = 13.5\text{ V}$ , $V_{IN} = 5\text{ V}$ , $I_O = 0.5\text{ A}$	—	7	10	$\Omega$	UU, VU, WU, UB, VB and WB output resistance pulse width $\leq 10\ \mu\text{s}$				
	$R_{SINK}$			$V_{DD} = 13.5\text{ V}$ , $V_{IN} = 0\text{ V}$ , $I_O = -0.5\text{ A}$	—	4.5			10			

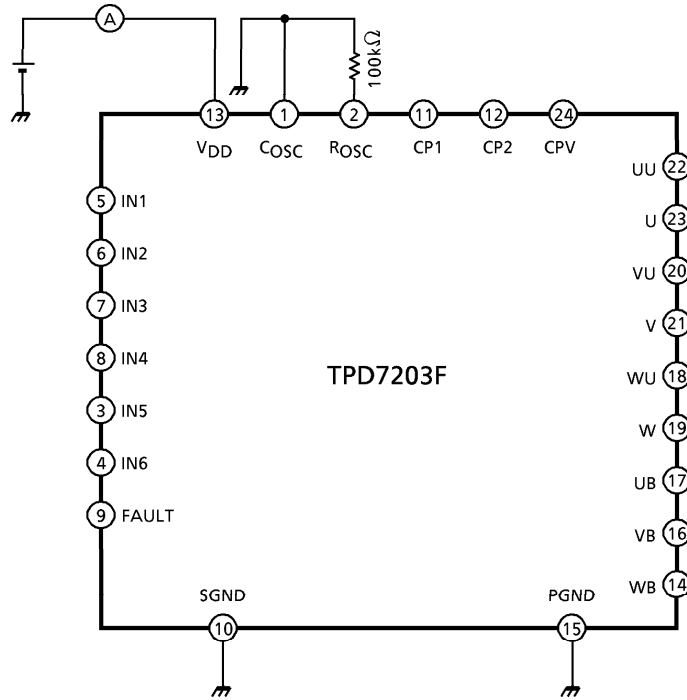


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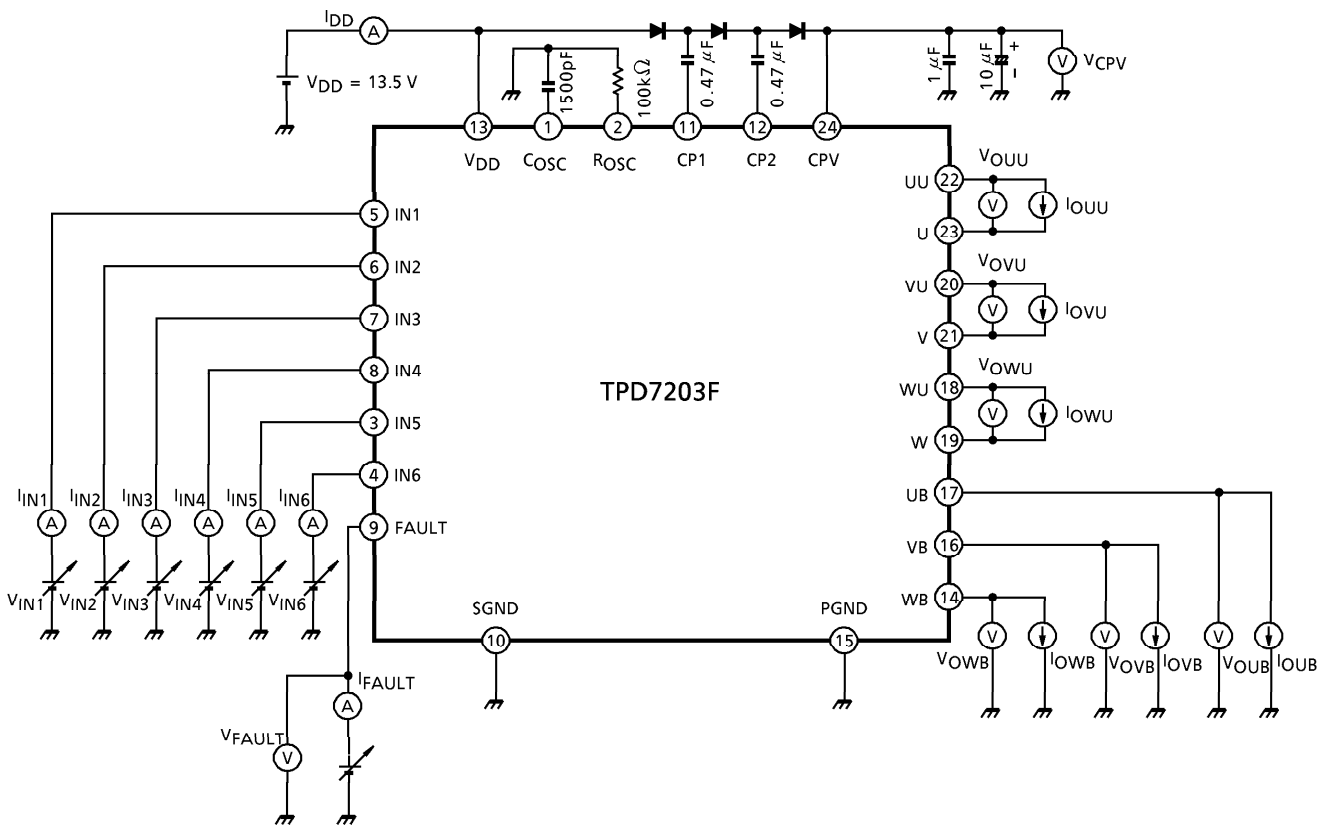
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARKS
Low-Voltage Protection	Detection	$V_{SD(L)}$	3	—	5.5	6	6.5	V	Low-voltage detection voltage and hysteresis ( $V_{DD}$ voltage detected)
	Hysteresis	$\Delta V_{SD(L)}$			—	0.5	—		
Switching Time	Turn-on delay time	$t_d(ON)$	4	$V_{DD} = 7\sim 18V,$ $C_{OUT} = 0.047\ \mu F,$ $R_G = 47\ \Omega$	—	—	4	$\mu s$	UU, VU, WU, UB, VB and WB switching time
	Turn-on time	$t_{ON}$			—	—	6		
	Turn-off delay time	$t_d(OFF)$			—	—	4		
	Turn-off time	$t_{OFF}$			—	—	6		
Oscillating Frequency		$f_{OSC}$	2	$V_{DD} = 7\sim 18V,$ $R_{OSC} = 100\ k\Omega,$ $C_{OSC} = 1500\ pF$	—	20	—	kHz	$f_{OSC}$ calculation formula $f_{OSC} = 3 / \{C_{OSC} (R_{OSC} + 2\ k)\}$ (Hz)
FAULT Pin Voltage		$V_{FAULT}$	2	$I_{FAULT} = 1\ mA$	—	—	0.8	V	FAULT pin low-level voltage (open-drain)
FAULT Delay Time		$t_{ON}$	3	$R_{FAULT} = 5.1\ k\Omega,$ $V_{FAULT} = 5V,$ (External power supply)	—	1	—	$\mu s$	Time from low voltage detection or restoration to FAULT output inversion
		$t_{OFF}$			—	1	—		

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**TESTING CIRCUIT 1**  $I_{DD} (1)$

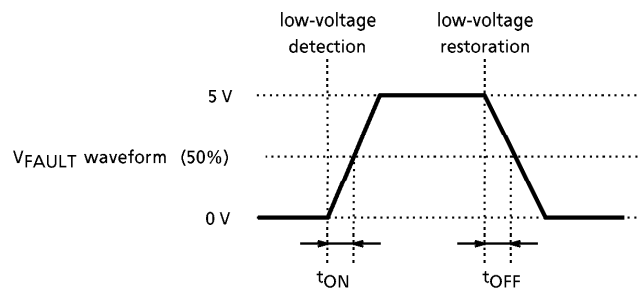
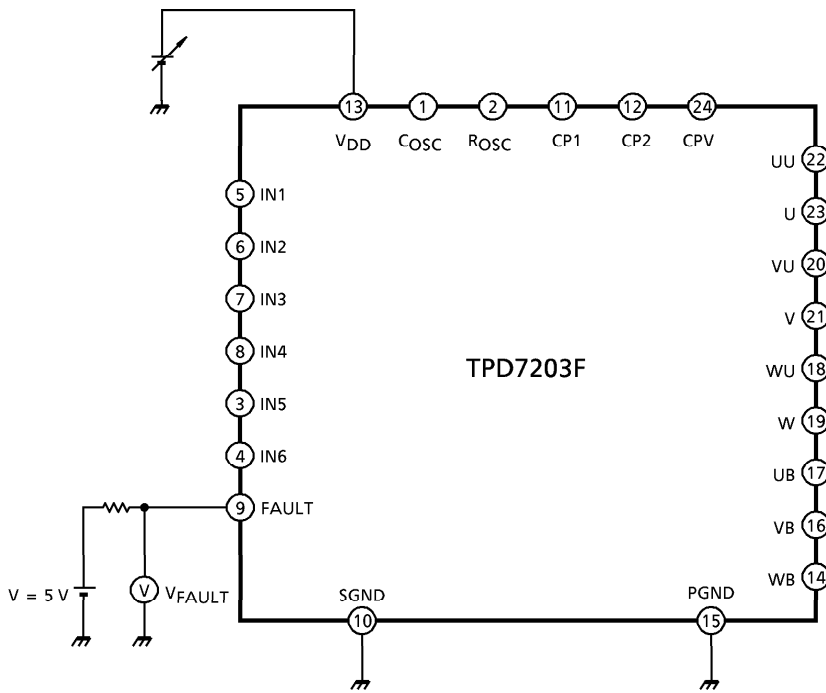


**TESTING CIRCUIT 2**  $I_{DD} (2), V_{IH}, V_{IL}, I_{IH}, I_{IL}, V_{OH}, V_{OL}, V_{CPV}, V_{FAULT}$



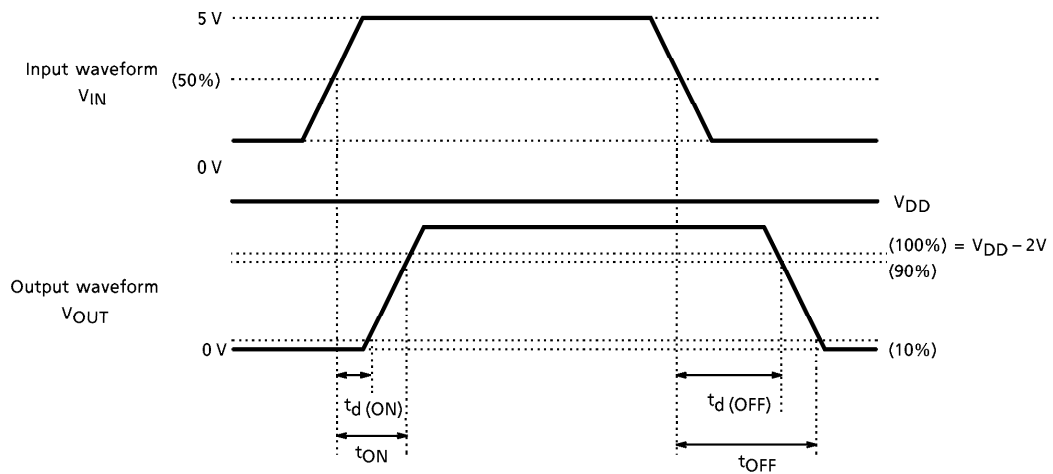
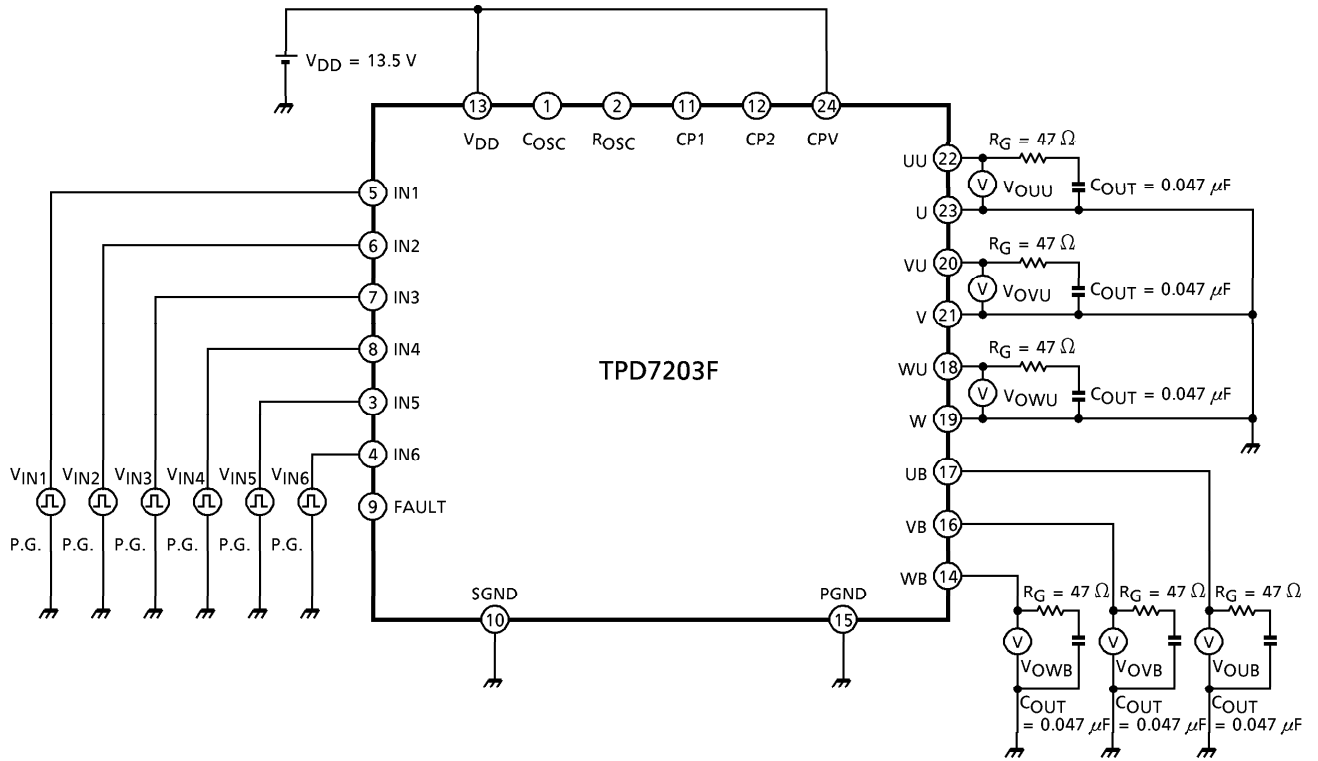
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**TESTING CIRCUIT 3**  $V_{SD}(L)$ ,  $\Delta V_{SD}(L)$ , FAULT delay time  $t_{ON}$ ,  $t_{OFF}$

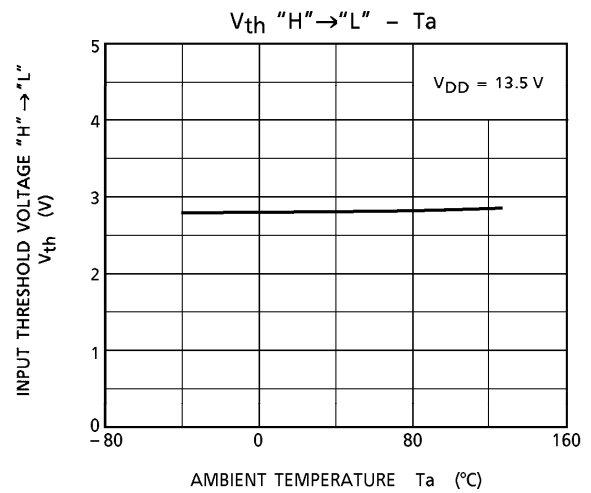
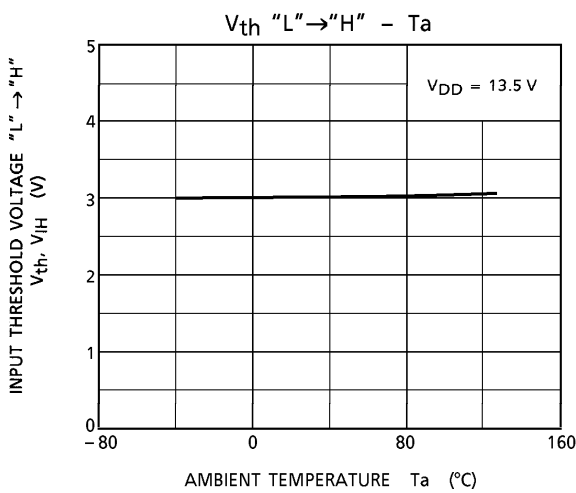
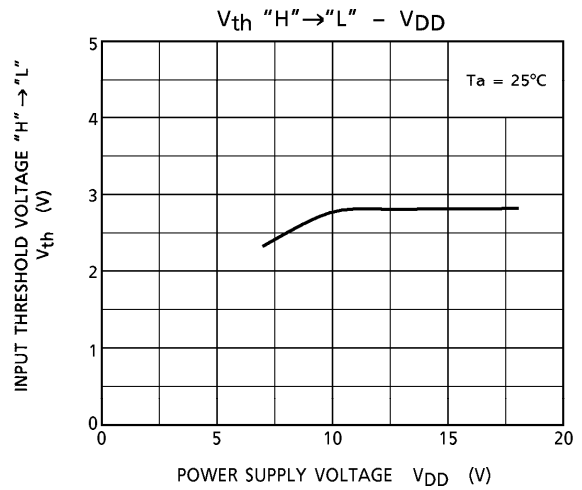
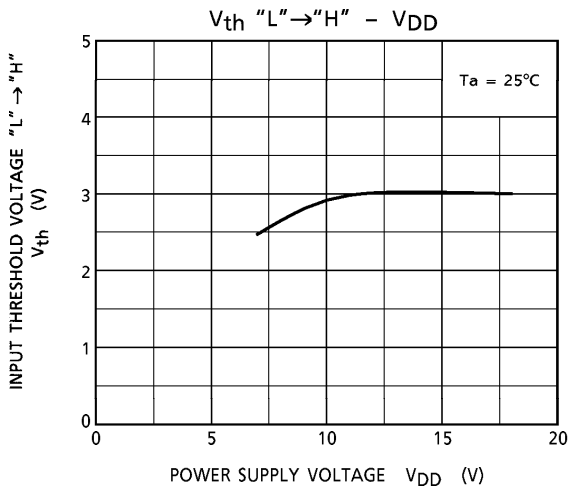
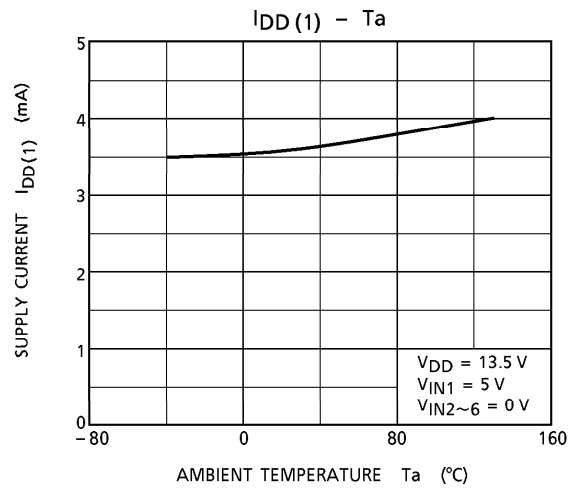
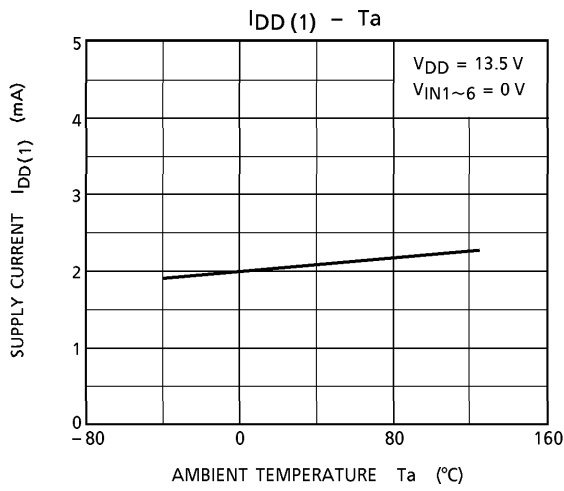


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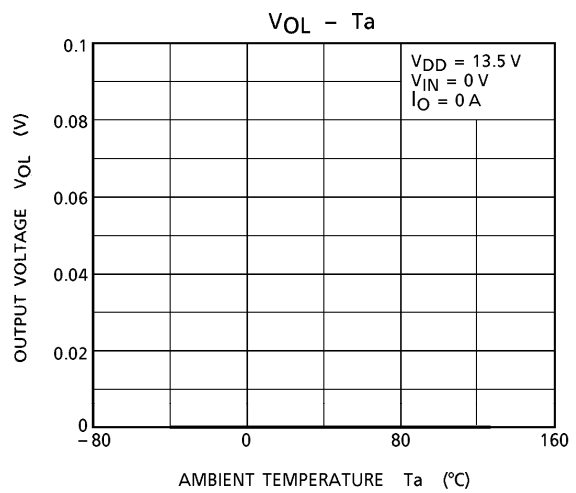
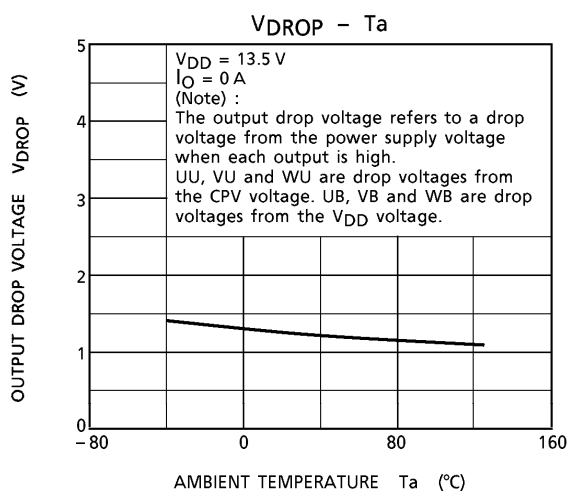
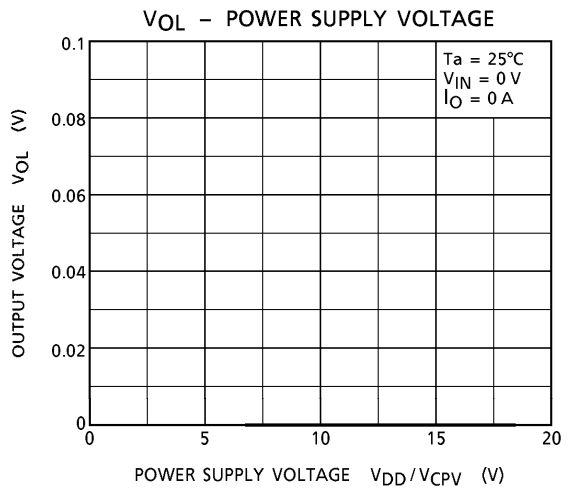
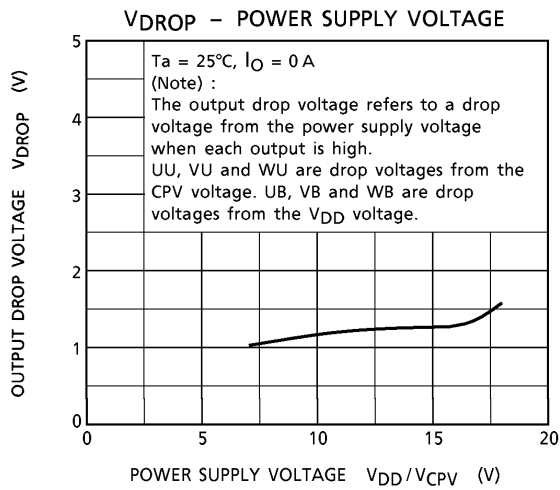
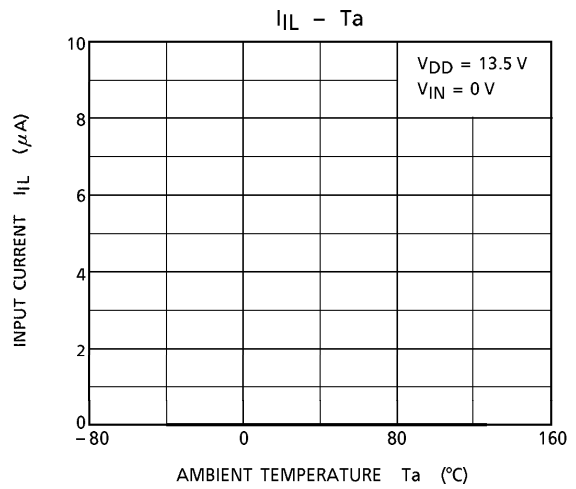
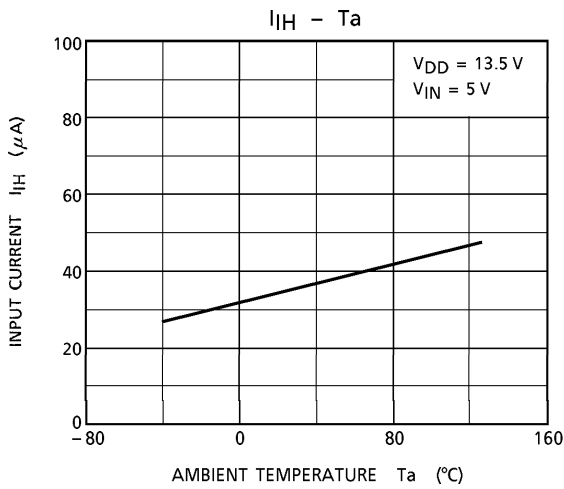
**TESTING CIRCUIT 4**  $t_d$  (ON),  $t_{ON}$ ,  $t_d$  (OFF),  $t_{OFF}$



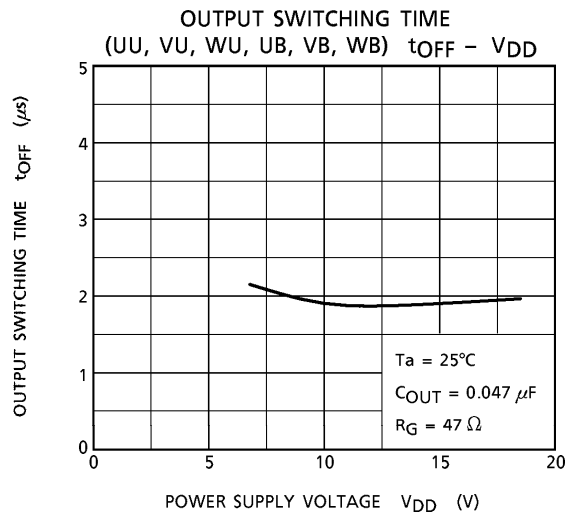
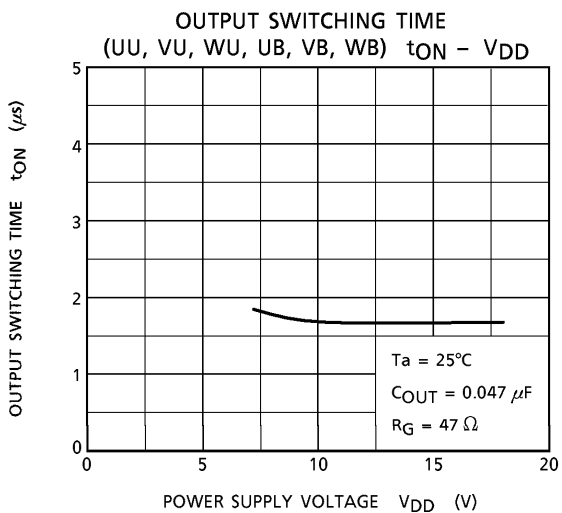
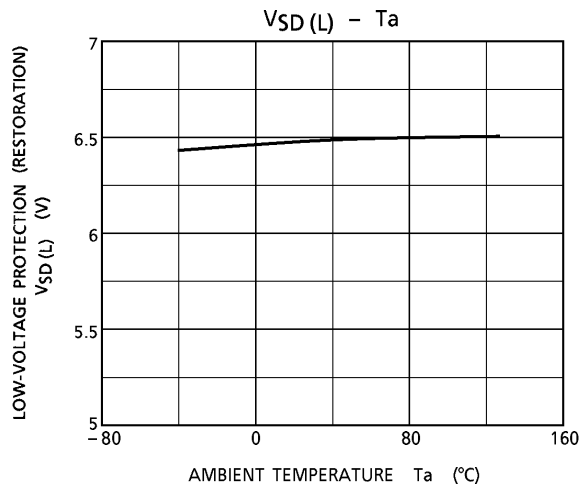
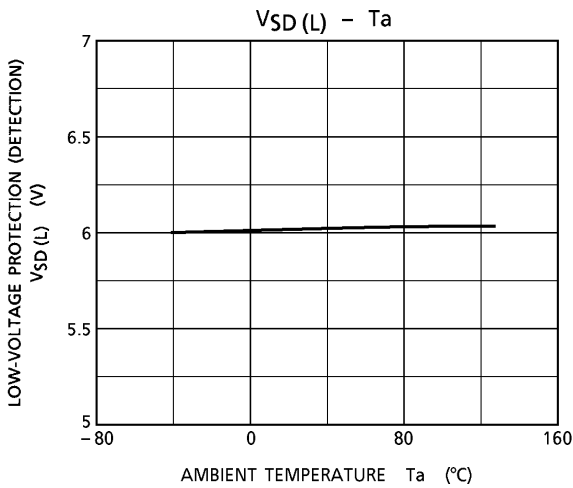
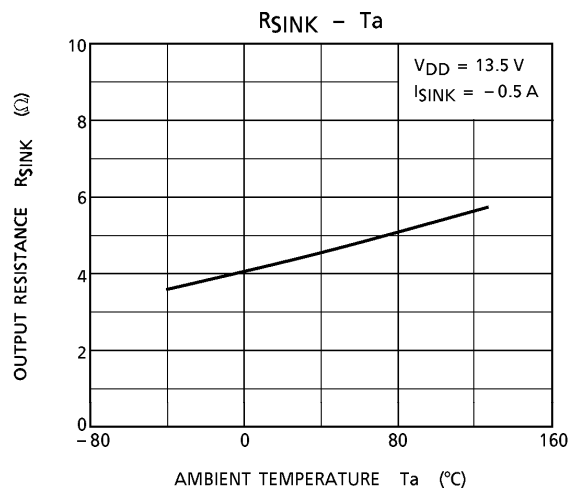
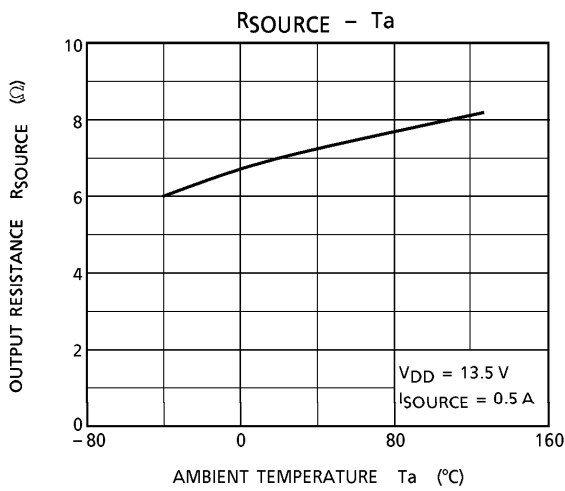
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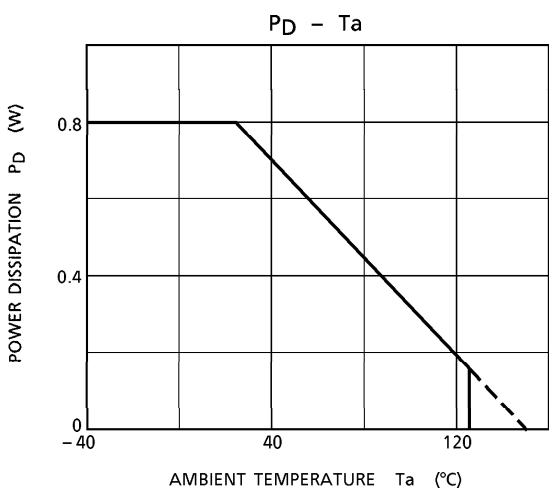
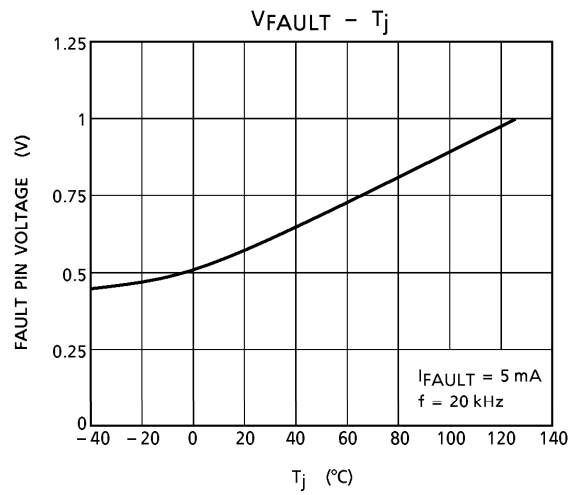
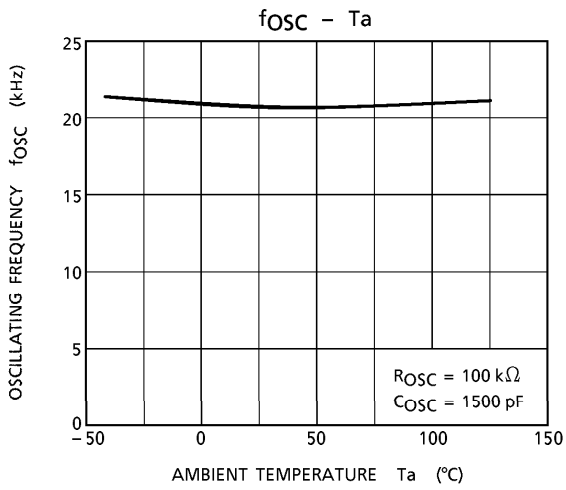
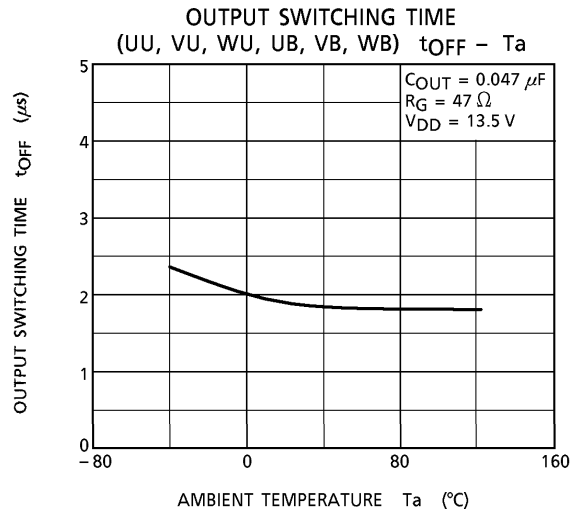
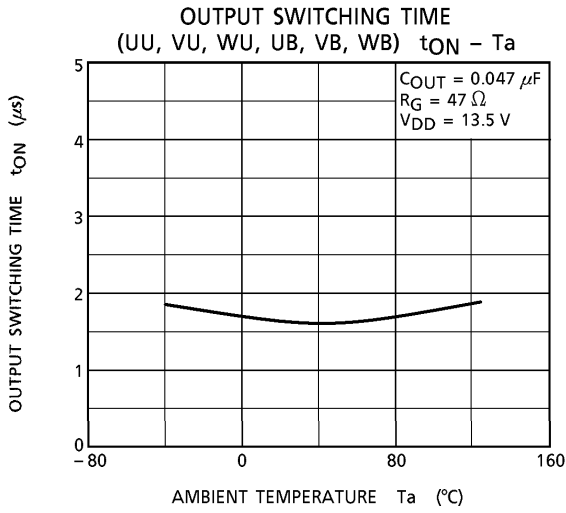
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## METHOD FOR SELECTING EXTERNAL PARTS

PIN No.	PIN NAME	TYPE	RECOMMENDED VALUE / RECOMMENDED PRODUCT	DESCRIPTION
1	COSC	Capacitor	1500 pF (ceramic)	Sets charge pump's oscillation frequency.
2	ROSC	Resistor	100 k $\Omega$	Sets charge pump's oscillation frequency.
11 12	CP1 CP2	Capacitor	0.47 $\mu$ F (laminated ceramic)	Capacitor for the charge pump. Greater this capacitance larger the charging current to the capacitor, so there is a greater loss in the IC.
24	CPV	Capacitor	1 $\mu$ F (laminated ceramic) and 10 $\mu$ F (aluminum electrolytic) connected in parallel	Greater this capacitance, larger the charge pump (CPV pin)'s current supply capacity, so there is a greater loss in the IC. Therefore, be careful not to exceed the allowable loss.
11 12 24	CP1 CP2 CPV	High-speed diode	$t_{rr} = 100$ ns (max.) CRH01 ( $t_{rr} = 35$ ns max.) recommended	Diode for the charge pump. An electric charge equal to the diode's $Q_{rr}$ component goes out of the capacitor's charged electricity. Therefore, use a high-speed diode.
22 20 18 17 16 14	UU VU WU UB VB WB	Resistor	—	Gate resistor for external power MOSFET. Choose the optimum value by considering the switching loss and EMI of the power MOSFET.
10 19 21 23	SGND W V U	SBD	$V_F = 0.5$ V (max.) CRS03 ( $V_F = 0.45$ V max. @0.7 A) recommended	This is needed when the U, V or W pin is biased to the negative side by more than 0.5 V from the SGND voltage. Because this IC operates relative to SGND, a parasitic diode exists toward each pin. When the U, V or W pin is biased to the negative side by more than 0.5 V from SGND, the parasitic diode conducts, causing the IC to operate erratically or generate abnormal heat.
19 21 23	W V U	Resistor	—	This is needed when the U, V or W pin is biased to the negative side by more than 0.5 V from the SGND voltage. This is used to limit current for external SBD.

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**USAGE PRECAUTIONS**

(Note 1) : About taking the charge pump voltage to external devices

Current can be taken out of the charge pump's final stage (CPV pin) to external devices without causing any problem. In this case, because the charge pump voltage drops, increase the capacitance of the capacitor connected to the CPV pin. However, this may cause the charging current to the capacitor and, hence, loss in the IC to increase. So be careful not to exceed the allowable loss.

(Note 2) : About heat sink design

Because this IC contains a charge pump function, loss in it affects external capacitor capacitance and diode characteristics. It is recommended that the junction temperature,  $T_j$ , be judged from the on-voltage of the FAULT pin (open-drain). When  $V_{DD}$  is within the range of operating power supply voltages, the FAULT pin outputs a low. For details about on-voltage characteristics, see  $T_j$ - $V_{FAULT}$  characteristic curves.

(Note 3) : About dead time setting

For arm-shortening input logic, all outputs (UU, VU, WU, UB, VB and WB) are pulled low. When operating in forward or reverse mode, consider the IC output switching time and the switching time (including temperature characteristic) of the external power MOSFET as you set the dead time. The dead time required for only the IC, not including the external power MOSFET, is 4  $\mu$ s (within all operating power supply voltages and all operating temperatures).

(Note 4) : Shorting between outputs, Shortcircuit of outputs and  $V_{DD}$  pin or shortcircuit of outputs GND pin may cause the IC to break down. Therefore, pay careful attention to the design of output lines and  $V_{DD}$  and GND lines.

(Note 5) : Precautions on dry packing

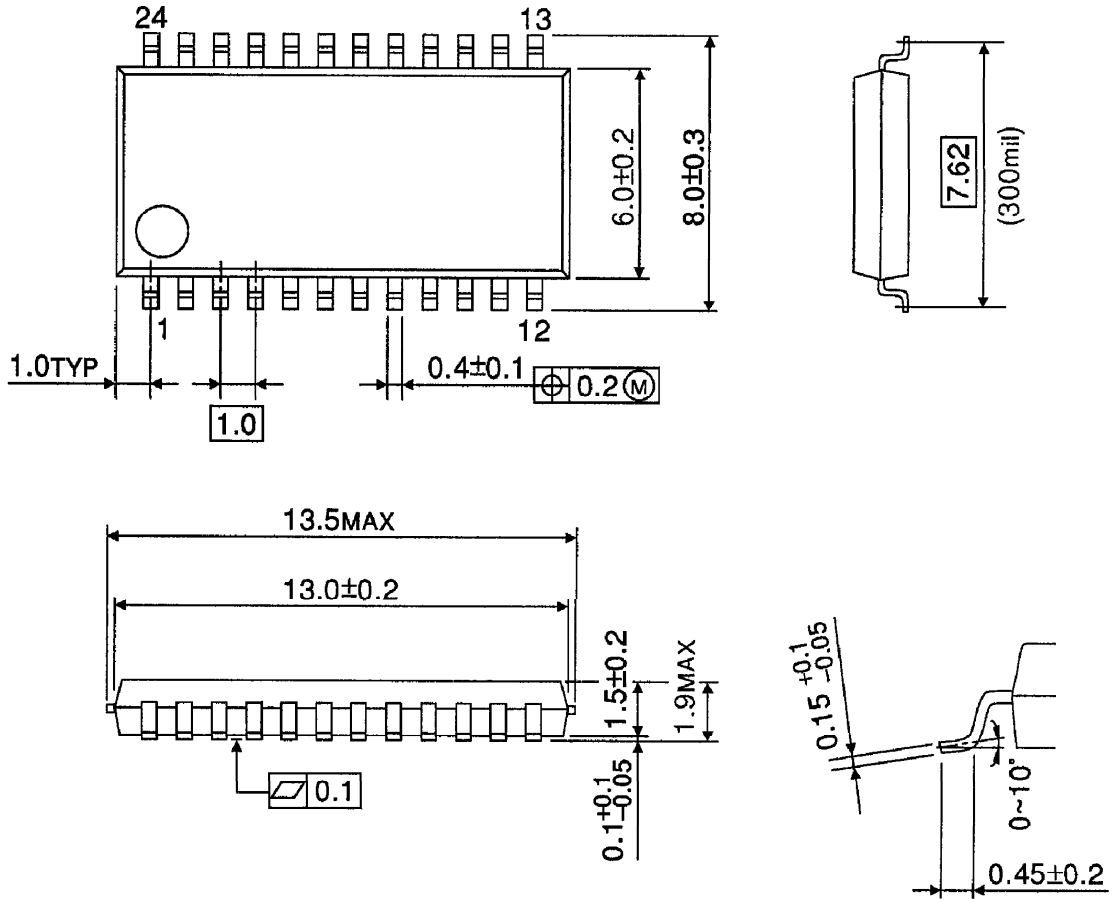
After unpacking dry or moistureproof packing, please make sure the device is mounted in place within 48 hours at temperature and humidity of 30°C and 60% RH or less. Because the device is emboss-taped and cannot be processed by baking, always be sure to use it within said allowable time after unpacking.

Tape packing quantity: 500 devices/reel (EL) or 2000 devices/reel (EL1)

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**PACKAGE DIMENSIONS**  
SSOP24-P-300-1.00B

Unit : mm



Weight : 0.29 g (typ.)

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