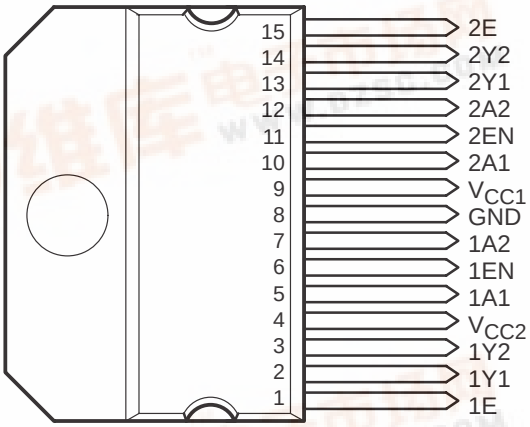
# TPIC0298
# DUAL FULL-H DRIVER

SLIS006 – D2942, JUNE 1987 – REVISED JANUARY 1990

- **Formerly TLP298**
- **2-A Output Current Capability Per Full-H Driver**
- **Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers**
- **Wide Range of Output Supply Voltage 5 V to 46 V**
- **Separate Input-Logic Supply Voltage Thermal Shutdown**
- **Internal Electrostatic Discharge Protection**
- **High Noise Immunity**
- **3-State Outputs**
- **Minimized Power Dissipation**
- **Sink/Source Interlock Circuitry Prevents Simultaneous Conduction**
- **Improved Functional Replacement for the SGS L298**

**KV PACKAGE**
**(TOP VIEW)**



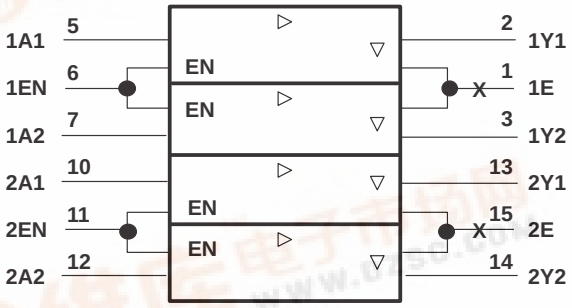

The tab is electrically connected to GND.

## description

The TPIC0298 is a dual high-current full-H driver designed to provide bidirectional drive currents of up to 2 A at voltages from 5 V to 46 V. It is designed to drive inductive loads such as relays, solenoids, dc motors, stepping motors, and other high-current or high-voltage loads in positive-supply applications. All inputs are TTL compatible. Each output (Y) is a complete totem-pole drive with a Darlington transistor sink and a pseudo-Darlington source. Each full-H driver is enabled separately. Outputs 1Y1 and 1Y2 are enabled by 1EN and outputs 2Y1 and 2Y2 are enabled by 2EN. When an EN input is high, the associated channels are active. When an EN input is low, the associated channels are off (i.e., in the high-impedance state).

Each half of the device forms a full-H reversible driver suitable for solenoid or motor applications. The current in each full-H driver can be monitored by connecting a resistor between the sense output terminal 1E and GND and another resistor between sense output terminal 2E and GND.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**FUNCTION TABLE**

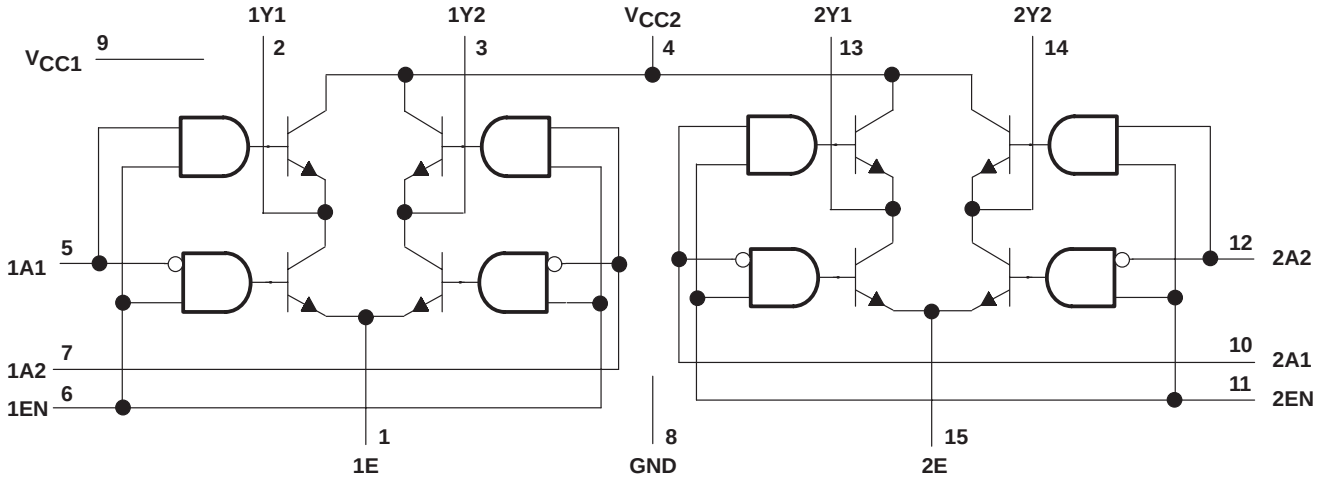
| INPUTS | | OUTPUT |
|---|---|---|
| A | EN | Y |
| H | H | H |
| L | H | L |
| X | L | Z |

H = high-level , L = low-level
X = irrelevant
Z = high-impedance (off)

External high-speed output-clamp diodes should be used for inductive transient suppression. To minimize device power dissipation, a $V_{CC1}$ supply voltage, separate from $V_{CC2}$, is provided for the logic inputs.

The TPIC0298 is designed for operation from 0°C to 70°C.

## logic diagram (positive logic)




## absolute maximum ratings over operating temperature range (unless otherwise noted)

Logic supply voltage range, $V_{CC1}$ (see Note 1) . . . . . –0.3 V to 7 V
Output supply voltage range, $V_{CC2}$ . . . . . –0.3 V to 50 V
Input voltage range at A or EN, $V_I$ (see Note 2) . . . . . –1.6 V to 7 V
Output voltage range, $V_O$ . . . . . –2 V to $V_{CC2}$ + 2 V
Emitter terminal (1E and 2E) voltage range, $V_E$ . . . . . –0.5 V to 2.3 V
Emitter terminal (1E and 2E) voltage (nonrepetitive, $t_w \le 50$ µs) . . . . . –1 V
Input current at A or EN, $I_I$ . . . . . –15 mA
Peak output current, $I_{OM}$: (nonrepetitive, $t_w \le 0.1$ ms) . . . . . ±3 A
(repetitive, $t_w \le 10$ ms, duty cycle ≤ 80%) . . . . . ±2.5 A
Continuous output current, $I_O$ . . . . . ±2 A
Peak combined output current for each full-H driver (see Note 3):
(nonrepetitive, $t_w \le 0.1$ ms) . . . . . ±3 A
(repetitive, $t_w \le 10$ ms, duty cycle ≤ 80%) . . . . . ±2.5 A
Continuous combined output current for each full-H driver (see Note 3) . . . . . ±2 A
Continuous dissipation at (or below) 25°C free-air temperature (see Note 4) . . . . . 3.575 W
Continuous dissipation at (or below) 75°C case temperature (see Note 4) . . . . . 25 W
Operating free-air, case, or virtual junction temperature range . . . . . –40°C to 150°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network GND, unless otherwise noted.
2. The maximum current limitation at this terminal generally occurs at a voltage of lower magnitude than the voltage limit. Neither the maximum current nor the maximum voltage for this terminal should be exceeded.
3. Combined output current applies to each of the two full-H drivers individually. This current is the sum of the currents at outputs 1Y1 and 1Y2 for full-H driver 1 and the sum of the currents at outputs 2Y1 and 2Y2 for full-H driver 2. The full-H drivers can carry the rated combined current simultaneously.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate linearly at the rate of 333 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

## recommended operating conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Logic supply voltage, $V_{CC1}$ | | 4.5 | 7 | V |
| Output supply voltage, $V_{CC2}$ | | 5 | 46 | V |
| Emitter terminal (1E or 2E) voltage, $V_E$ (see Note 5) | | −0.5† | 2 | V |
| | | | $V_{CC1}-3.5$ | |
| | | | $V_{CC2}-4$ | |
| High-level input voltage, $V_{IH}$ (see Note 5) | A | 2.3 | $V_{CC1}$ | V |
| | | | $V_{CC2}-2.5$ | |
| | EN | 2.3 | 7 | |
| | | | $V_{CC1}$ | |
| Low-level input voltage at A or EN, $V_{IL}$ | | −0.3† | 1.5 | V |
| Output current, $I_O$ | | | ±2 | A |
| Communication frequency | | | 40 | kHz |
| Operating free-air temperature, $T_A$ | | 0 | 70 | °C |

† The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for emitter terminal voltage and logic voltage levels.

NOTE 5: For optimum device performance, the maximum recommended voltage at any A input is 2.5 V lower than $V_{CC2}$, the maximum recommended voltage at any EN input is $V_{CC1}$, and the maximum recommended voltage at any emitter terminal is 3.5 V lower than $V_{CC1}$ and 4 V lower than $V_{CC2}$.

## electrical characteristics over recommended ranges of $V_{CC1}$, $V_{CC2}$, and $V_E$, $T_J$ = 25°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | | $I_I$ = −12 mA | | | | −0.9 | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = −1 A | | | $V_{CC2}-1.8$ | $V_{CC2}-1.2$ | | V |
| | | | $I_{OH}$ = −2 A | | | $V_{CC2}-2.8$ | $V_{CC2}-1.8$ | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 1 A | | | | $V_E+1.2$ | $V_E+1.8$ | V |
| | | | $I_{OL}$ = 2 A | | | | $V_E+1.7$ | $V_E+2.6$ | |
| $V_{drop}$ | Total source pulse sink output voltage drop | | $I_{OH}$ = −1 A, $I_{OL}$ = 1 A | | See Note 6 | | 2.4 | 3.4 | V |
| | | | $I_{OH}$ = −2 A, $I_{OL}$ = 2 A | | | | 3.5 | 5.2 | |
| $I_{OZH}$ | Off-state (high-impedance state) output current, high-level voltage applied | | $V_O = V_{CC2}$ | | | | | 500 | µA |
| $I_{OZL}$ | Off-state (high-impedance state) output current, low-level voltage applied | | $V_O$ = 0 V, $V_E$ = 0 V | | | | | −500 | µA |
| $I_{IH}$ | High-level input current | A | $V_I = V_{IH}$ | EN = H | | | 20 | 100 | µA |
| | | | | EN = L | | | | 10 | |
| | | EN | $V_I = V_{IH} \le V_{CC1} - 0.6$ V | | | | 6 | 100 | |
| $I_{IL}$ | Low-level input current | | $V_I$ = 0 V to 1.5 V | | | | | −10 | µA |
| $I_{CC1}$ | Logic supply current | | $I_O$ = 0 | All outputs at high level | | | 7 | 12 | mA |
| | | | | All outputs at low level | | | 20 | 32 | |
| | | | | All outputs at high impedance | | | 4 | 6 | |
| $I_{CC2}$ | Output supply current | | $I_O$ = 0 | All outputs at high level | | | 25 | 50 | mA |
| | | | | All outputs at low level | | | 6 | 20 | |
| | | | | All outputs at high impedance | | | | 2 | |

† All typical values are at $V_{CC1}$ = 5 V, $V_{CC2}$ = 42 V, $V_E$ = 0 V, $T_J$ = 25°C (unless otherwise noted).

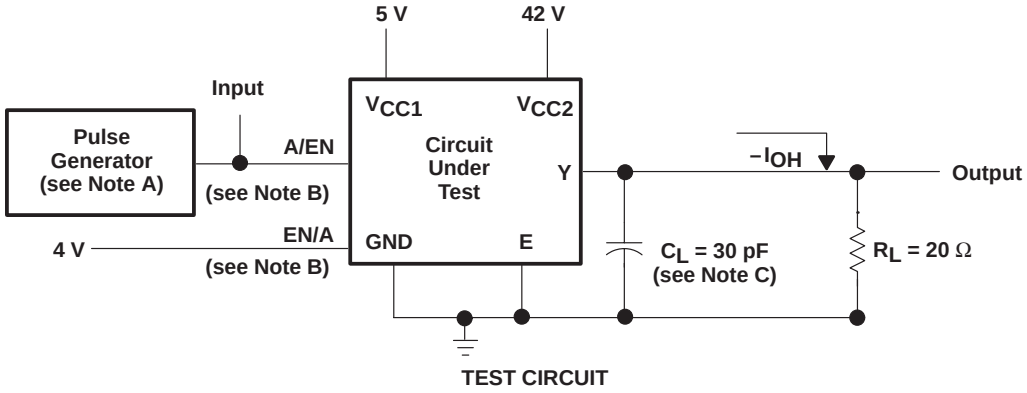
NOTE 6: The $V_{drop}$ specification applies for $I_{OH}$ and $I_{OL}$ applied simultaneously to different output channels:

$$V_{drop} = V_{CC2} - V_{OH} + V_{OL} - V_E$$

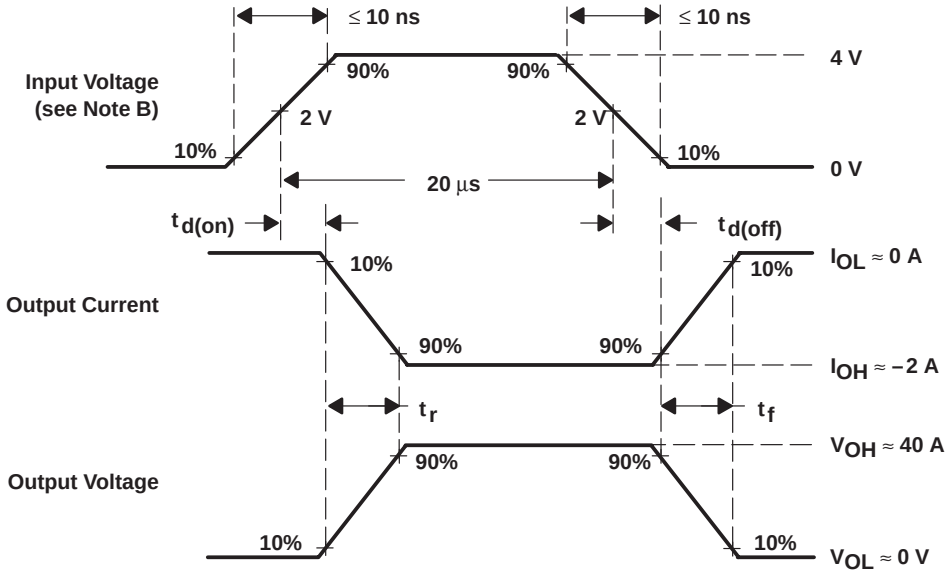
## switching characteristics, $V_{CC1}$ = 5 V, $V_{CC2}$ = 42 V, $V_E$ = 0, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time, source current from A input | $C_L$ = 30 pF, See Figure 1 | | 0.6 | | µs |
| $t_{d(off)}$ | Turn-off delay time, source current from A input | | | 0.8 | | µs |
| $t_r$ | Rise time, source current (turning on) | | | 0.8 | | µs |
| $t_f$ | Fall time, source current (turning off) | | | 0.2 | | µs |
| $t_{d(on)}$ | Turn-on delay time, source current from EN input | | | 0.5 | | µs |
| $t_{d(off)}$ | Turn-off delay time, source current from EN input | | | 2.5 | | µs |
| $t_{d(on)}$ | Turn-on delay time, sink current from A input | $C_L$ = 30 pF, See Figure 2 | | 1.3 | | µs |
| $t_{d(off)}$ | Turn-off delay time sink current from A input | | | 0.5 | | µs |
| $t_r$ | Rise time, sink current (turning on) | | | 0.2 | | µs |
| $t_f$ | Fall time, sink current (turning off) | | | 0.2 | | µs |
| $t_{d(on)}$ | Turn-on delay time, sink current from EN input | | | 0.3 | | µs |
| $t_{d(off)}$ | Turn-off delay time, sink current from EN input | | | 1 | | µs |

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT

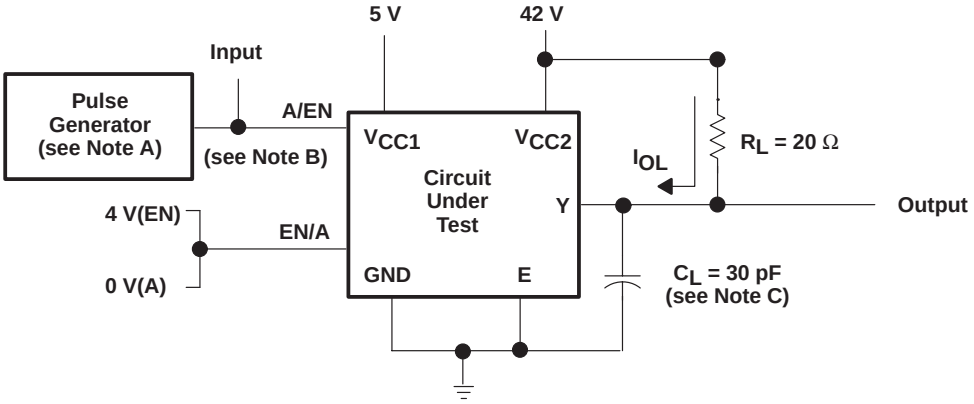



VOLTAGE AND CURRENT WAVEFORMS

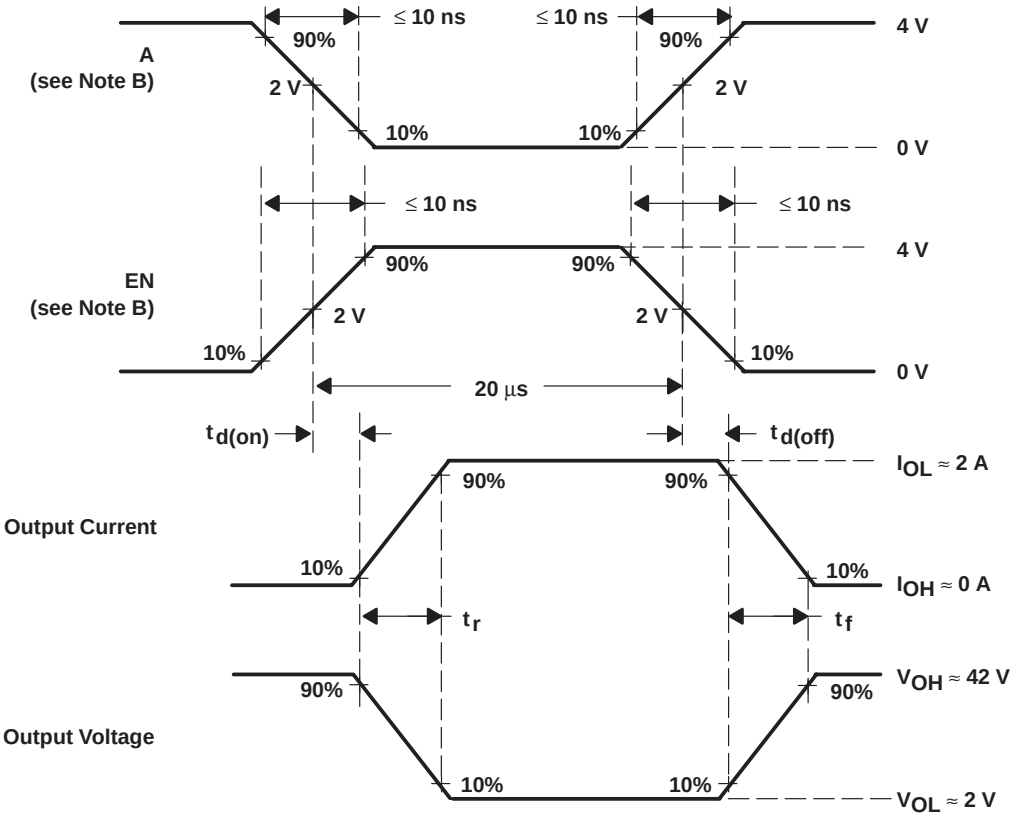
NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, $Z_O$ = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 4 V if EN is the switching input.
C. $C_L$ includes probe and jig capacitance.

**Figure 1. Source Current Test Circuit and Waveforms From Data and Enable Inputs**

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, $Z_O$ = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 0 V if EN is the switching input.
C. $C_L$ includes probe and jig capacitance.

**Figure 2. Sink Current Test Circuit and Voltage Waveforms From Data and Enable Inputs**

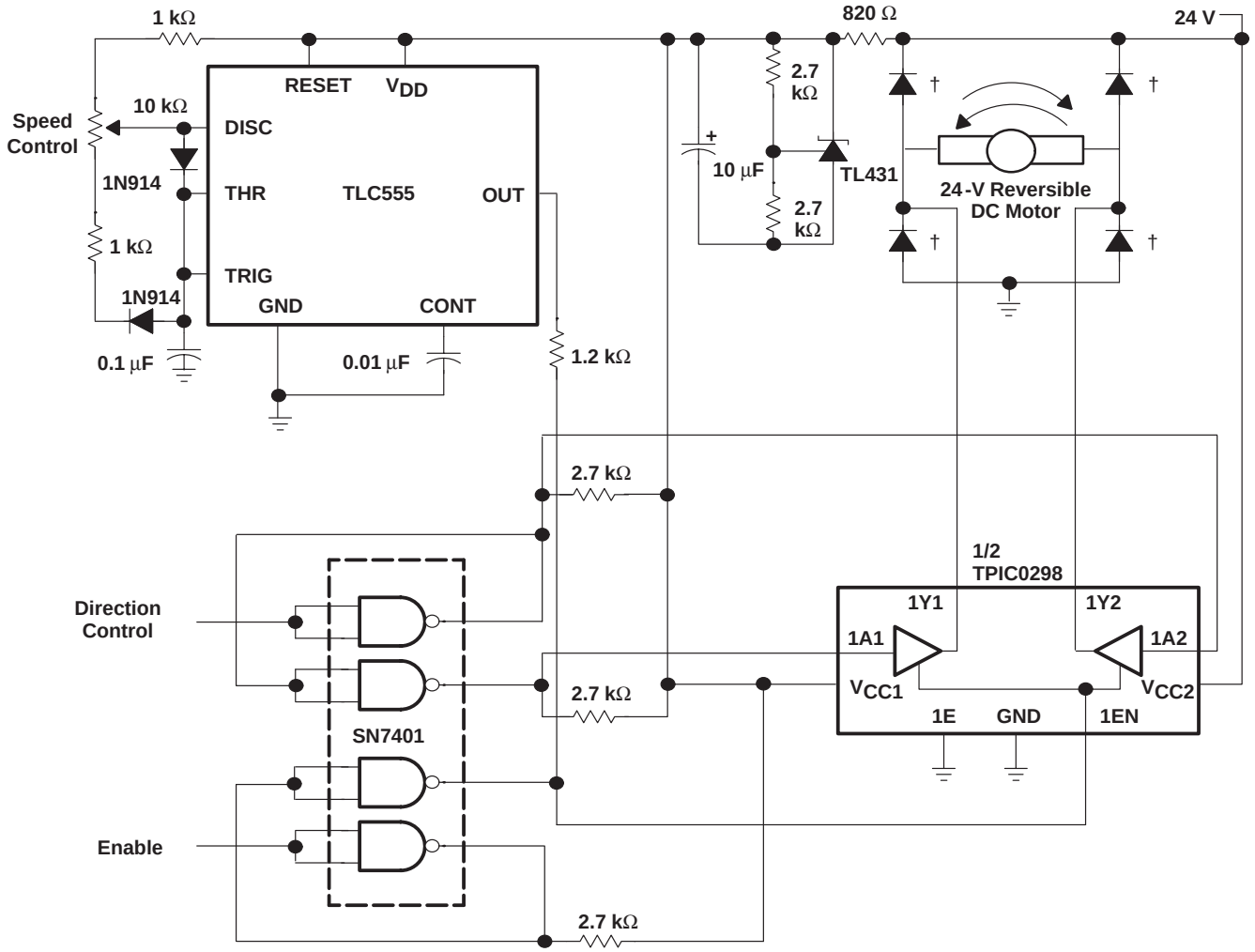
## APPLICATION INFORMATION

This circuit shows one half of a TPIC0298 used to provide full-H bridge drive for a 24-V, 2-A dc motor. Speed control is achieved with a TLC555 timer. This provides variable duty-cycle pulses to the EN input of the TPIC0298. In this configuration, the operating frequency is approximately 1.2 kHz. The duty cycle is adjustable from 10% to 90% to provide a wide range of motor speeds. The motor direction is determined by the logic level at the direction control input. The circuit can be enabled or disabled by the logic level at the EN input. A 5-V supply for the logic and timer circuit is provided by a TL431 shunt regulator. For circuit operation, refer to the function table.

**FUNCTION TABLE**

| ENABLE | DIRECTION CONTROL | 1Y1 | 1Y2 |
|---|---|---|---|
| H | H | Source | Sink |
| H | L | Sink | Source |
| L | X | Disabled | Disabled |

X = don't care  H = high level  L = low level




† Diodes are 1N4934 or equivalent.

**Figure 3. TPIC0298 as Bidirectional-DC Motor Drive**

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