

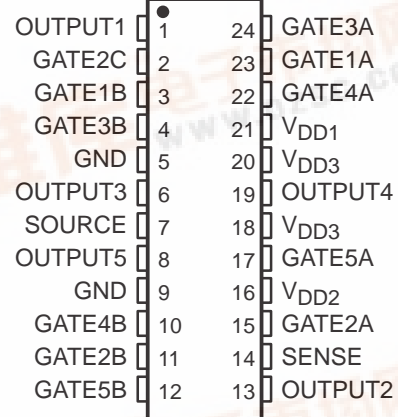
- **Low  $r_{DS(on)}$ :**  
**0.25  $\Omega$  Typ (Full H-Bridge)**  
**0.35  $\Omega$  Typ (Triple Half H-Bridge)**
- **Pulsed Current:**  
**6 A Per Channel (Full H-Bridge)**  
**4 A Per Channel (Triple Half H-Bridge)**
- **Matched Sense Transistor for Class A-B Linear Operation**
- **Fast Commutation Speed**

**description**

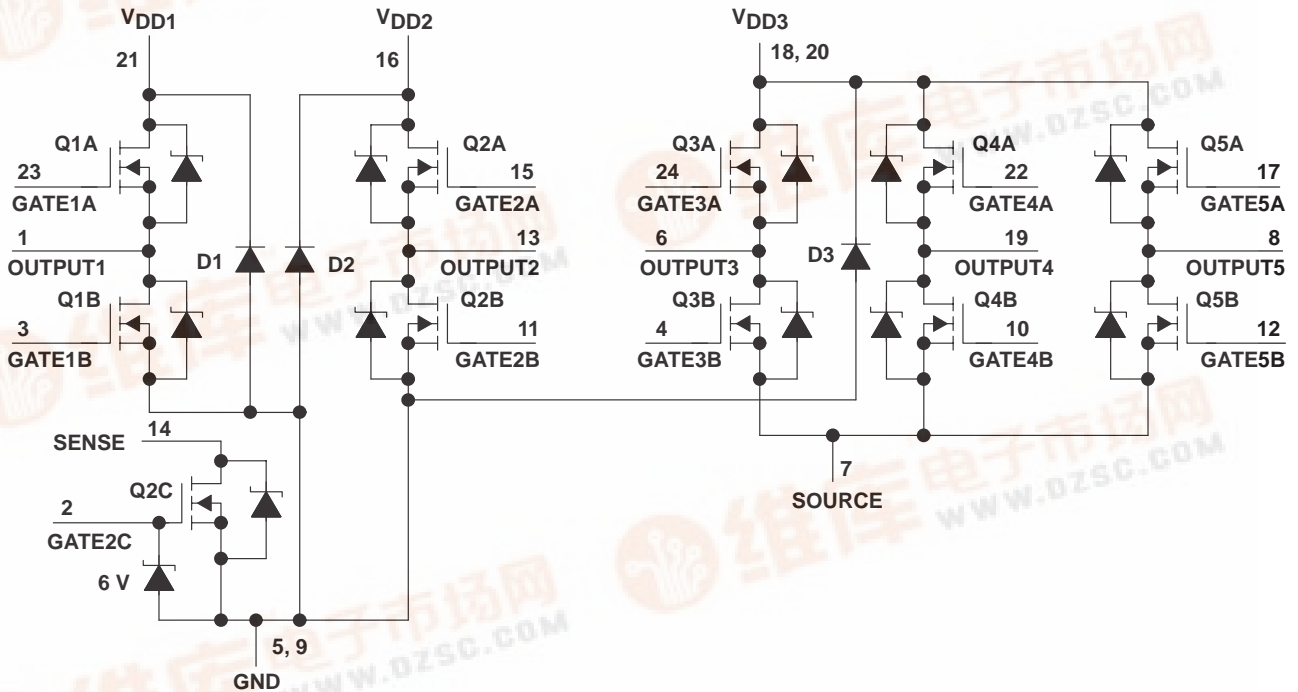
The TPIC1505 is a monolithic power array that consists of ten electrically isolated N-channel enhancement-mode power DMOS transistors, four of which are configured as a full H-bridge and six as a triple half H-bridge. The lower stage of the full H-bridge features an integrated sense FET to allow biasing of the bridge in class A-B operation.

The TPIC1505 is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

**DW PACKAGE  
(TOP VIEW)**



**schematic**



- NOTES:
- Pins 5 and 9 must be externally connected.
  - Pins 18 and 20 must be externally connected.
  - No output may be taken greater than 0.5 V below GND.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



# TPIC1505

## QUAD AND HEX POWER DMOS ARRAY

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### absolute maximum ratings, $T_C = 25^\circ\text{C}$ (unless otherwise noted)†

Supply-to-GND voltage	20 V
Source-to-GND voltage (Q3A, Q4A, Q5A)	20 V
Output-to-GND voltage	20 V
Sense-to-GND voltage	20 V
Gate-to-source voltage range, $V_{GS}$ (Q1A, Q1B, Q2A, Q2B, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	-0.5 V to 20 V
Gate-to-source voltage, $V_{GS}$ (Q2C)	-0.7 V to 6 V
Continuous gate-to-source zener-diode current (Q2C)	$\pm 10$ mA
Pulsed gate-to-source zener-diode current (Q2C)	$\pm 50$ mA
Continuous drain current, each output (Q1A, Q1B, Q2A, Q2B)	1.5 A
Continuous drain current, each output (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	1 A
Continuous drain current (Q2C)	5 mA
Continuous source-to-drain diode current (Q1A, Q1B, Q2A, Q2B)	1.5 A
Continuous source-to-drain diode current (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	1 A
Continuous source-to-drain diode current (Q2C)	5 mA
Pulsed drain current, each output, $I_{max}$ (Q1A, Q1B, Q2A, Q2B) (see Note 1 and Figure 24)	6 A
Pulsed drain current, each output, $I_{max}$ (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B) (see Note 1 and Figure 25)	4 A
Pulsed drain current, $I_{max}$ (Q2C) (see Note 1)	20 mA
Continuous total power dissipation, $T_C = 70^\circ\text{C}$ (see Note 2 and Figures 24 and 25)	2.86 W
Operating virtual junction temperature range, $T_J$	$-40^\circ\text{C}$ to $150^\circ\text{C}$
Operating case temperature range, $T_C$	$-40^\circ\text{C}$ to $125^\circ\text{C}$
Storage temperature range, $T_{stg}$	$-65^\circ\text{C}$ to $150^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	$260^\circ\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Pulse duration = 10 ms, duty cycle = 2%  
 2. Package is mounted in intimate contact with infinite heat sink.

# TPIC1505 QUAD AND HEX POWER DMOS ARRAY

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## electrical characteristics, Q1A, Q1B, Q2A, Q2B, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	20			V
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1\ \text{mA}$ , See Figure 5	1.5	1.9	2.2	V
$V_{GS(th)match}$	Gate-to-source threshold voltage matching	$I_D = 1\ \text{mA}$ , $V_{DS} = V_{GS}$			40	mV
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage	Drain-to-GND current = $250\ \mu\text{A}$ (D1, D2)	20			V
$V_{(BR)GS}$	Gate-to-source breakdown voltage, Q2C	$I_{GS} = 100\ \mu\text{A}$	6			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage, Q2C	$I_{SG} = 100\ \mu\text{A}$	0.5			V
$V_{(DS)on}$	Drain-to-source on-state voltage	$I_D = 1.5\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , See Notes 3 and 4		0.38	0.45	V
$V_F$	Forward on-state voltage, GND-to- $V_{DD1}$ , GND-to- $V_{DD2}$	$I_D = 1.5\ \text{A}$ (D1, D2), See Notes 3 and 4		1.5		V
$V_F(SD)$	Forward on-state voltage, source-to-drain	$I_S = 1.5\ \text{A}$ , $V_{GS} = 0$ , See Notes 3 and 4 and Figure 19		1	1.2	V
$I_{DSS}$	Zero-gate-voltage drain current	$V_{DS} = 16\ \text{V}$ , $V_{GS} = 0$	$T_C = 25^\circ\text{C}$	0.05	1	$\mu\text{A}$
			$T_C = 125^\circ\text{C}$	0.5	10	
$I_{GSSF}$	Forward gate current, drain short-circuited to source	$V_{GS} = 16\ \text{V}$ , $V_{DS} = 0$		10	100	nA
$I_{lkg}$	Leakage current, $V_{DD1}$ -to-GND, $V_{DD2}$ -to-GND, gate shorted to source	$V_{DGND} = 16\ \text{V}$	$T_C = 25^\circ\text{C}$	0.05	1	$\mu\text{A}$
			$T_C = 125^\circ\text{C}$	0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 1.5\ \text{A}$ , See Notes 3 and 4 and Figure 9	$T_C = 25^\circ\text{C}$	0.25	0.3	$\Omega$
			$T_C = 125^\circ\text{C}$	0.4	0.48	
$g_{fs}$	Forward transconductance	$V_{DS} = 14\ \text{V}$ , See Notes 3 and 4	$I_D = 0.75\ \text{A}$	0.7	1.1	S
$C_{iss}$	Short-circuit input capacitance, common source	$V_{DS} = 14\ \text{V}$ , $f = 1\ \text{MHz}$ , $V_{GS} = 0$ , See Figure 17		100		$\text{pF}$
$C_{oss}$	Short-circuit output capacitance, common source			75		
$C_{rss}$	Short-circuit reverse transfer capacitance, common source			60		
$\alpha_S$	Sense-FET drain current ratio	$V_{DS} = 6\ \text{V}$ , $I_{D(Q2C)} = 40\ \mu\text{A}$	100	150	200	

NOTES: 3. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

## source-to-drain diode characteristics, Q1A, Q2A, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rr}$	Reverse-recovery time	$I_S = 750\ \text{mA}$ , $V_{GS} = 0$ , $V_{DS} = 14\ \text{V}$ , $di/dt = 100\ \text{A}/\mu\text{s}$ ,		18		ns
$Q_{RR}$	Total diode charge	See Figures 1 and 23		15		nC

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### resistive-load switching characteristics, Q1A, Q1B, Q2A, Q2B, T<sub>C</sub> = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 14 V, R <sub>L</sub> = 18.7 Ω, t <sub>en</sub> = 10 ns, t <sub>dis</sub> = 10 ns, See Figure 3		11		ns
t <sub>d(off)</sub>	Turn-off delay time			16		
t <sub>r</sub>	Rise time			3		
t <sub>f</sub>	Fall time			4		
Q <sub>g</sub>	Total gate charge	V <sub>DS</sub> = 14 V, I <sub>D</sub> = 750 mA, V <sub>GS</sub> = 10 V, See Figure 4		2	2.5	nC
Q <sub>gs(th)</sub>	Threshold gate-to-source charge			0.35	0.4	
Q <sub>gd</sub>	Gate-to-drain charge			0.5	0.6	
L <sub>(drain)</sub>	Internal drain inductance			7		nH
L <sub>(source)</sub>	Internal source inductance			7		
r <sub>(gate)</sub>	Internal gate resistance			10		Ω

### electrical characteristics, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B, T<sub>C</sub> = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>(BR)DSX</sub>	Drain-to-source breakdown voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	20			V
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	I <sub>D</sub> = 1 mA, V <sub>DS</sub> = V <sub>GS</sub> , See Figure 6	1.5	1.9	2.2	V
V <sub>GS(th)match</sub>	Gate-to-source threshold voltage matching	I <sub>D</sub> = 1 mA, V <sub>DS</sub> = V <sub>GS</sub>			40	mV
V <sub>(BR)</sub>	Reverse drain-to-GND breakdown voltage	Drain-to-GND current = 250 μA (D3)	20			V
V <sub>(DS)on</sub>	Drain-to-source on-state voltage	I <sub>D</sub> = 1 A, V <sub>GS</sub> = 10 V, See Notes 3 and 4		0.35	0.48	V
V <sub>F</sub>	Forward on-state voltage, GND-to-V <sub>DD3</sub>	I <sub>D</sub> = 1 A (D3), I <sub>D</sub> = 1 A (D3), See Notes 3 and 4		1.5		V
V <sub>F(SD)</sub>	Forward on-state voltage, source-to-drain	I <sub>S</sub> = 1 A, V <sub>GS</sub> = 0, See Notes 3 and 4 and Figure 20		0.9	1.2	V
I <sub>DSS</sub>	Zero-gate-voltage drain current	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0		0.05	1	μA
		T <sub>C</sub> = 25°C				
		T <sub>C</sub> = 125°C		0.5	10	
I <sub>GSSF</sub>	Forward gate current, drain short-circuited to source	V <sub>GS</sub> = 16 V, V <sub>DS</sub> = 0		10	100	nA
I <sub>lkg</sub>	Leakage current, V <sub>DD3</sub> -to-GND, gate shorted to source	V <sub>DGND</sub> = 16 V		0.05	1	μA
		T <sub>C</sub> = 125°C		0.5	10	
r <sub>DS(on)</sub>	Static drain-to-source on-state resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1 A, See Notes 3 and 4 and Figure 10		0.35	0.48	Ω
		T <sub>C</sub> = 125°C		0.55	0.75	
g <sub>fs</sub>	Forward transconductance	V <sub>DS</sub> = 14 V, I <sub>D</sub> = 500 mA, See Notes 3 and 4	0.4	0.72		S
C <sub>iss</sub>	Short-circuit input capacitance, common source	V <sub>DS</sub> = 14 V, V <sub>GS</sub> = 0, f = 1 MHz, See Figure 18		70		pF
C <sub>oss</sub>	Short-circuit output capacitance, common source			85		
C <sub>rss</sub>	Short-circuit reverse transfer capacitance, common source			50		

NOTES: 3: Technique should limit T<sub>J</sub> – T<sub>C</sub> to 10°C maximum.

4: These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

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**QUAD AND HEX POWER DMOS ARRAY**

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**source-to-drain diode characteristics, Q3A, Q4A, Q5A,  $T_C = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rr}$	Reverse-recovery time	$I_S = 500\text{ mA}$ , $V_{DS} = 14\text{ V}$ , See Figures 2 and 23		15		ns
$Q_{RR}$	Total diode charge					

**resistive-load switching characteristics, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B,  $T_C = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 14\text{ V}$ , $R_L = 32\ \Omega$ , $t_{dis} = 10\text{ ns}$ , See Figure 3		11		ns	
$t_{d(off)}$	Turn-off delay time						16
$t_r$	Rise time						3
$t_f$	Fall time						4
$Q_g$	Total gate charge	$V_{DS} = 14\text{ V}$ , See Figure 4	$I_D = 500\text{ mA}$ ,	$V_{GS} = 10\text{ V}$ ,	1.7	2.1	nC
$Q_{gs(th)}$	Threshold gate-to-source charge				0.35	0.45	
$Q_{gd}$	Gate-to-drain charge				0.4	0.5	
$L_{(drain)}$	Internal drain inductance			7		nH	
$L_{(source)}$	Internal source inductance			7			
$r_{(gate)}$	Internal gate resistance			10		$\Omega$	

**thermal resistance**

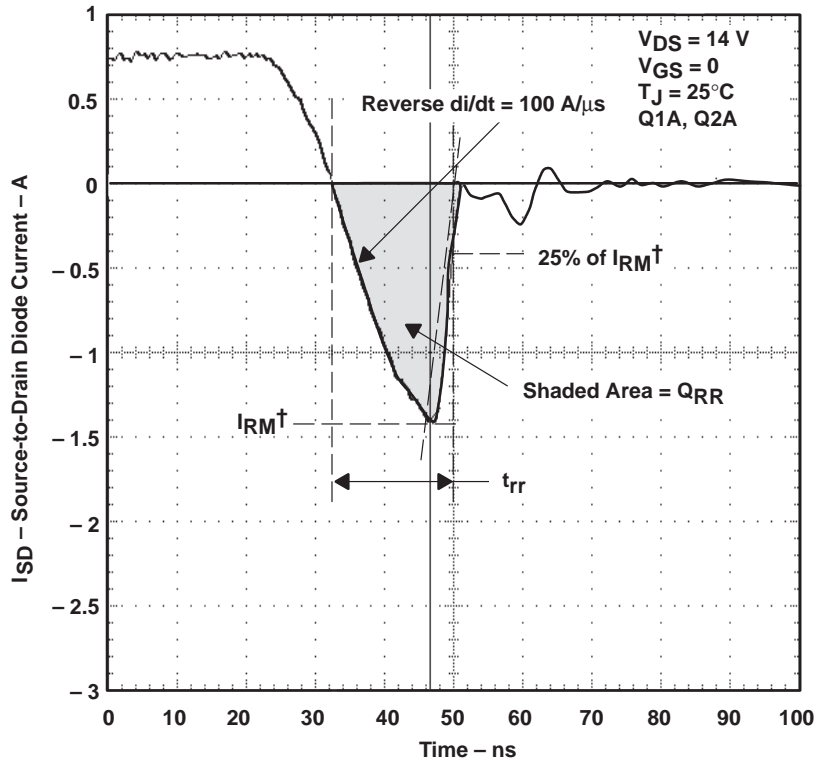
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 5 and 8		90		$^\circ\text{C/W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 6 and 8		52		
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 7 and 8		28		

- NOTES:
5. Package is mounted on a FR4 printed-circuit board with no heat sink.
  6. Package is mounted on a 24 in<sup>2</sup>, 4-layer FR4 printed-circuit board.
  7. Package is mounted in intimate contact with infinite heat sink.
  8. All outputs have equal power.

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## PARAMETER MEASUREMENT INFORMATION



$^\dagger I_{RM}$  = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diodes

PARAMETER MEASUREMENT INFORMATION

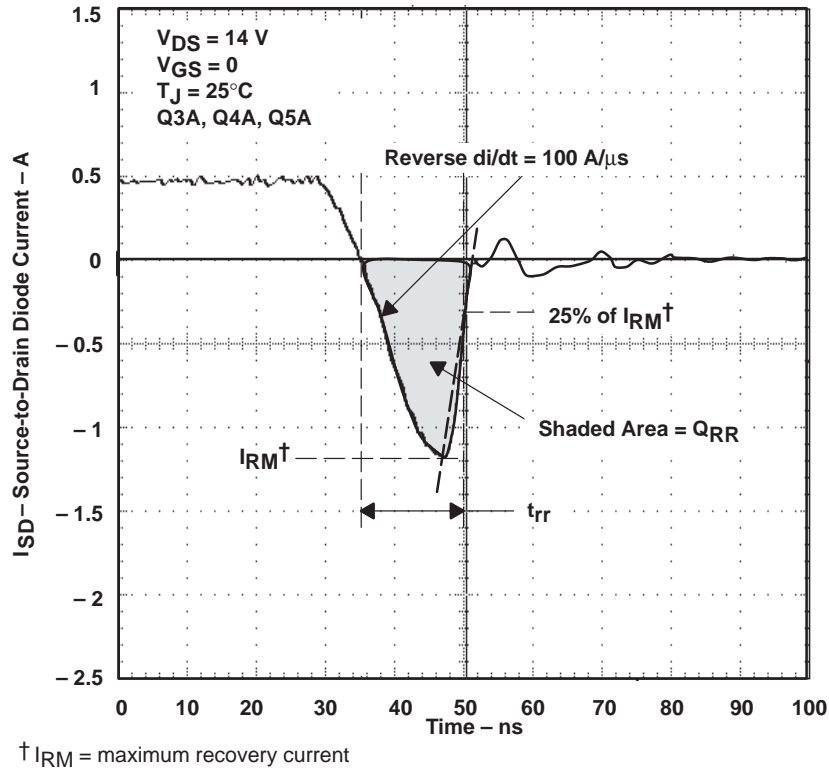
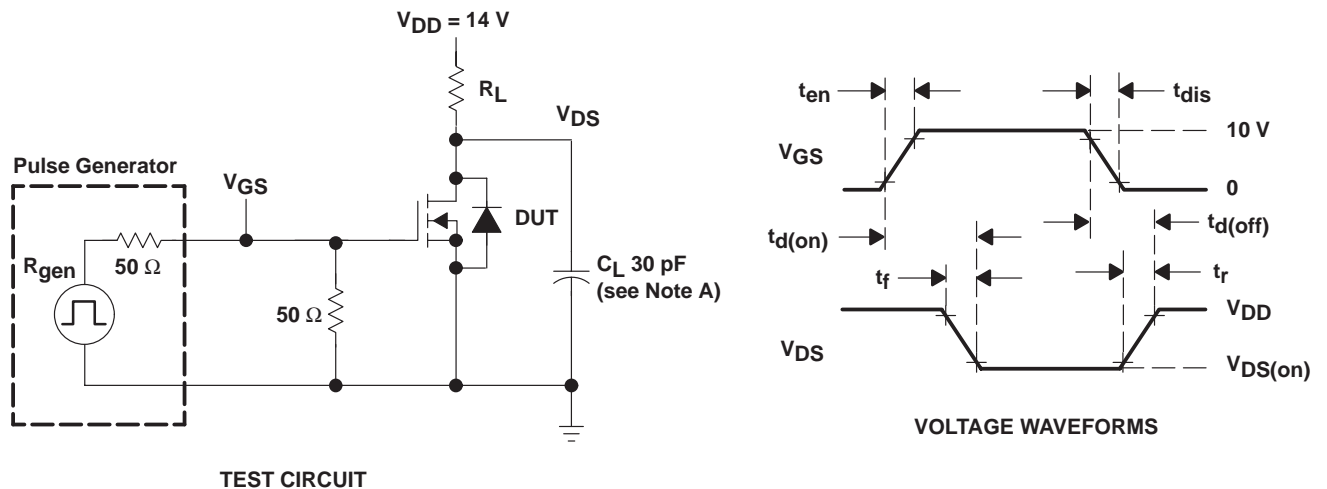


Figure 2. Reverse-Recovery-Current Waveform of Source-to-Drain Diodes



NOTE A:  $C_L$  includes probe and jig capacitance.

Figure 3. Resistive-Switching Test Circuit and Voltage Waveforms

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## PARAMETER MEASUREMENT INFORMATION

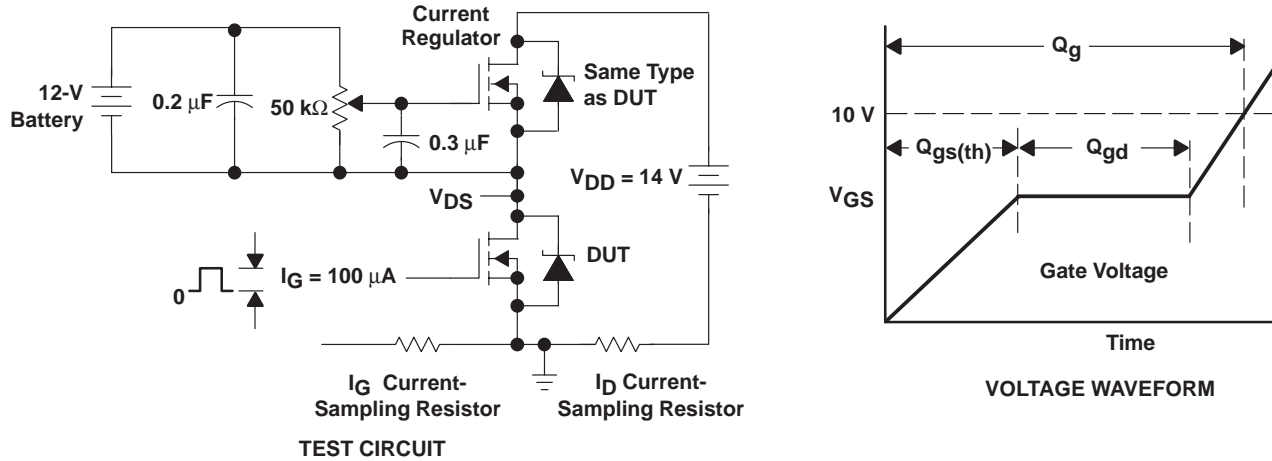


Figure 4. Gate-Charge Test Circuit and Voltage Waveform

## TYPICAL CHARACTERISTICS

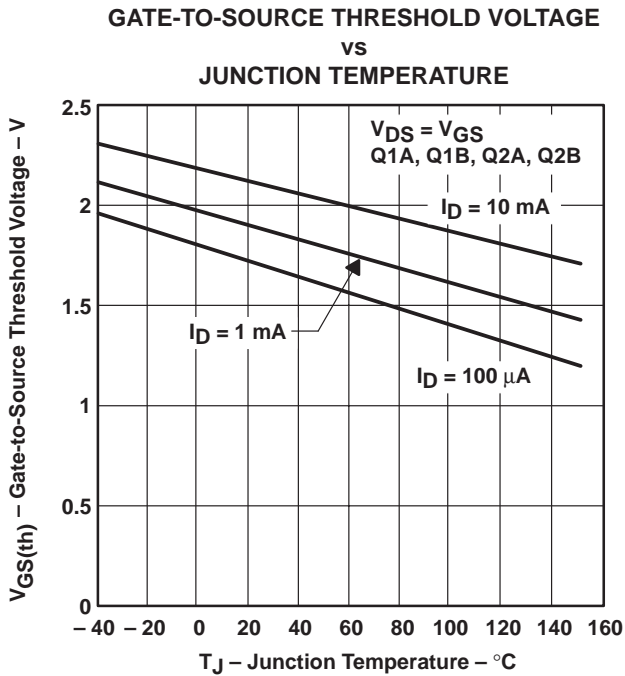


Figure 5

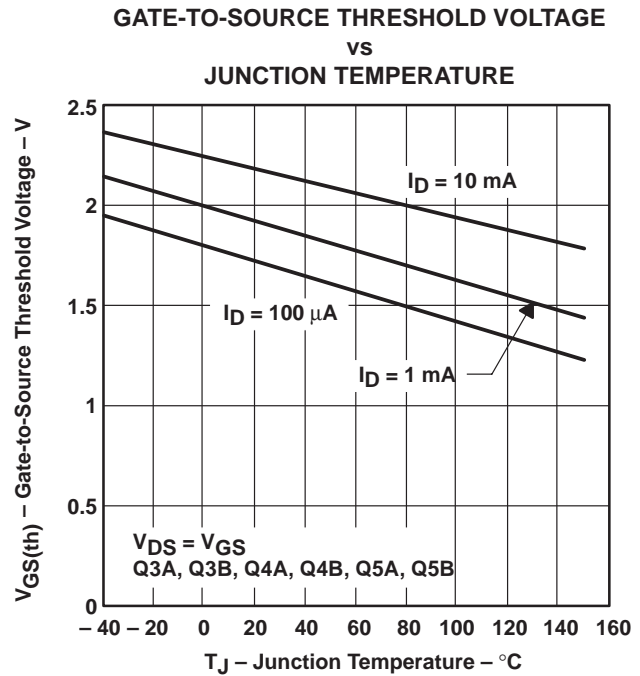


Figure 6



TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE  
 VS  
 JUNCTION TEMPERATURE

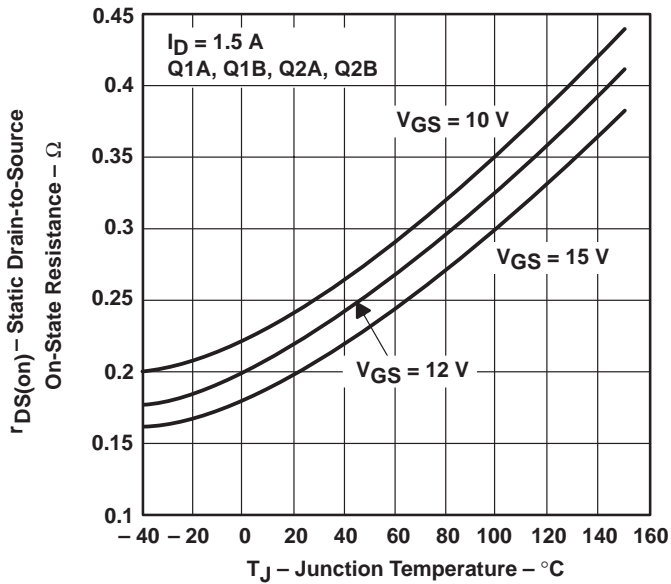


Figure 7

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE  
 VS  
 JUNCTION TEMPERATURE

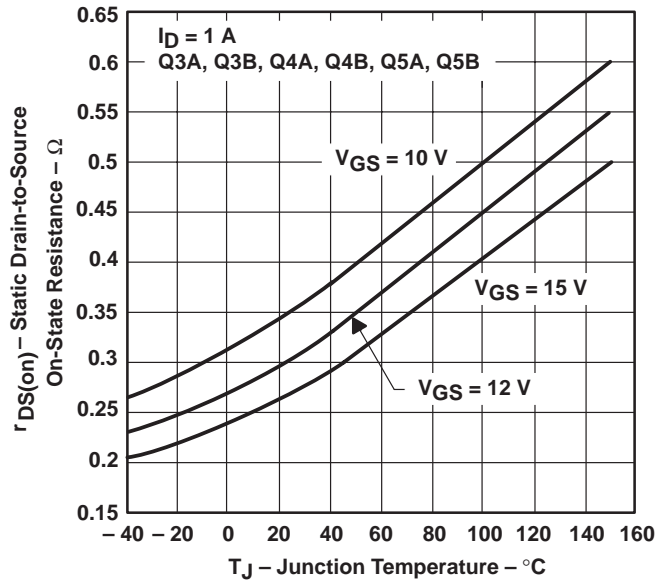


Figure 8

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE  
 VS  
 DRAIN CURRENT

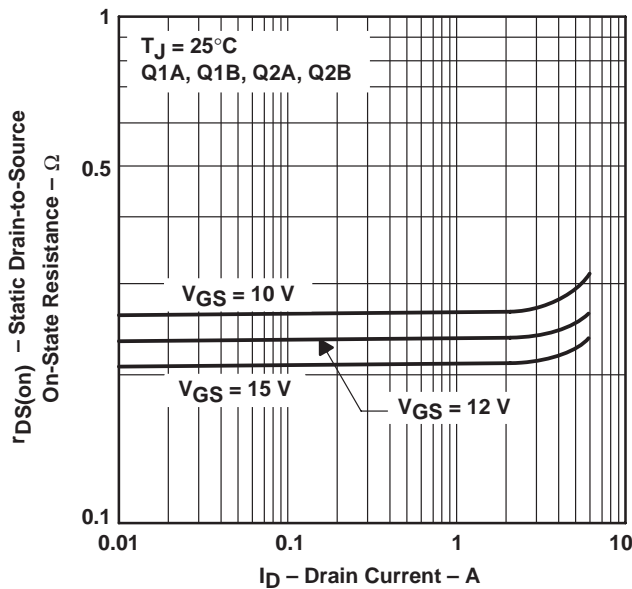


Figure 9

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE  
 VS  
 DRAIN CURRENT

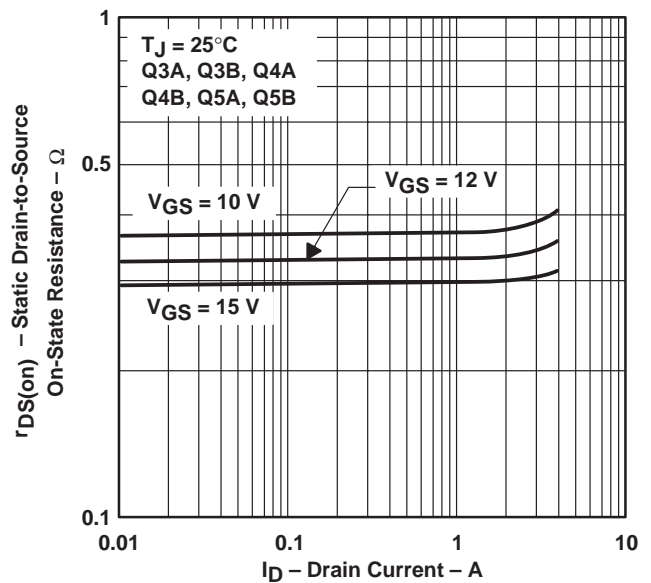
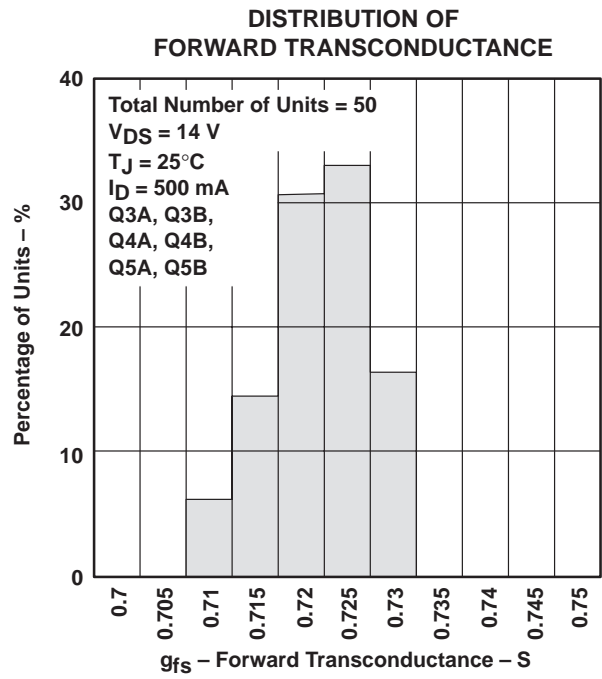
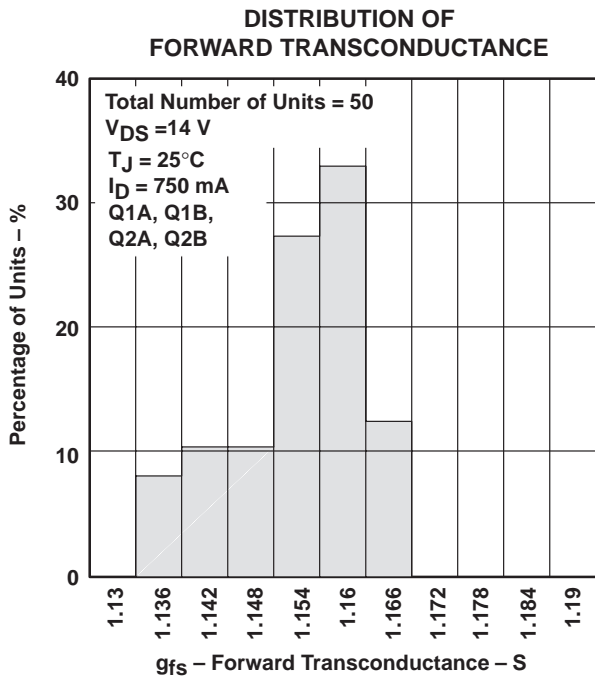
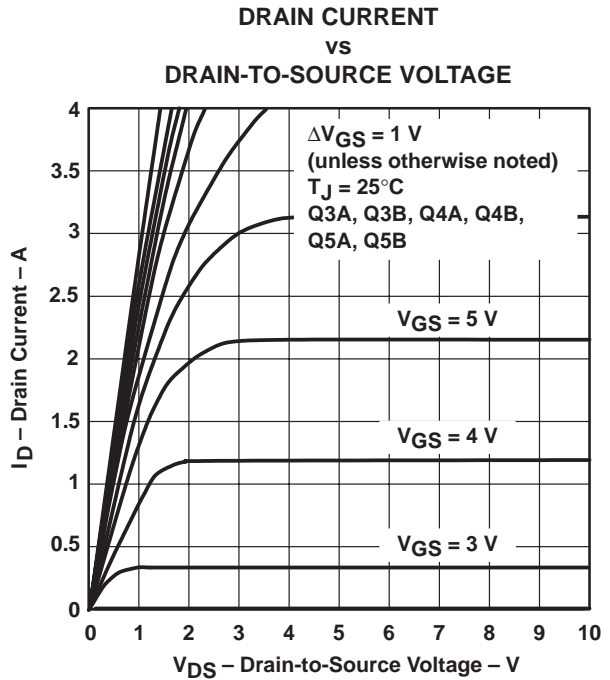
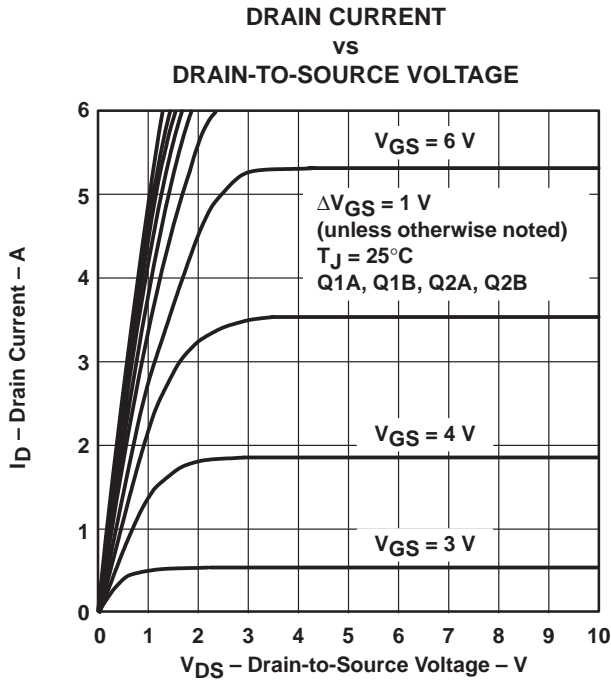


Figure 10

# TPIC1505 QUAD AND HEX POWER DMOS ARRAY

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## TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

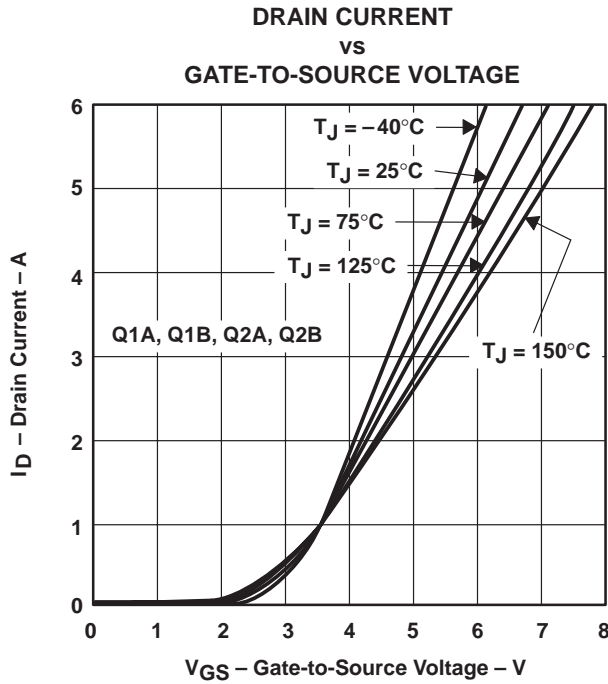


Figure 15

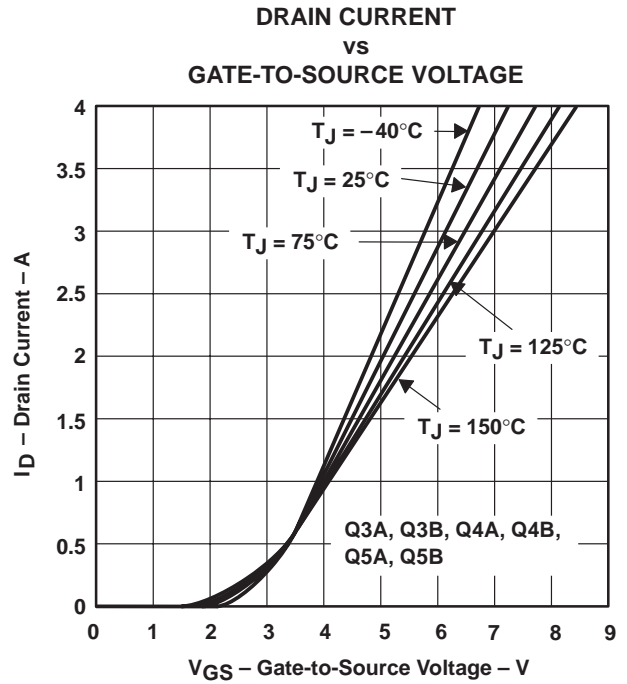


Figure 16

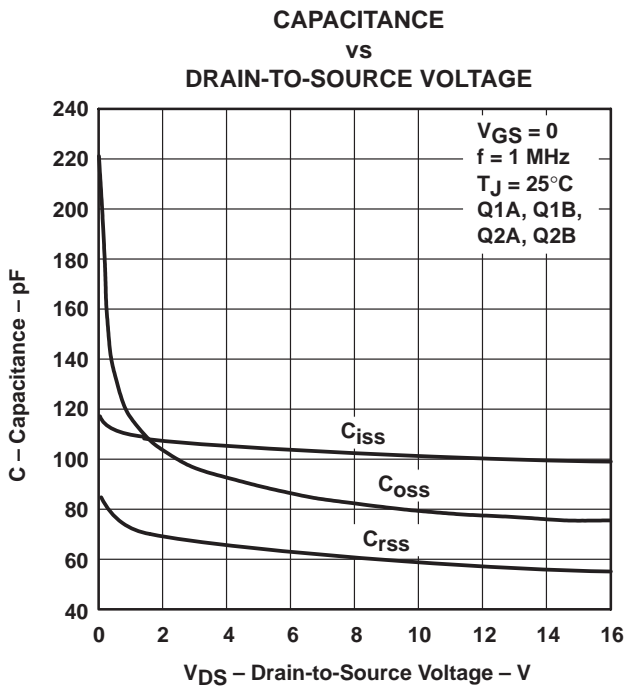


Figure 17

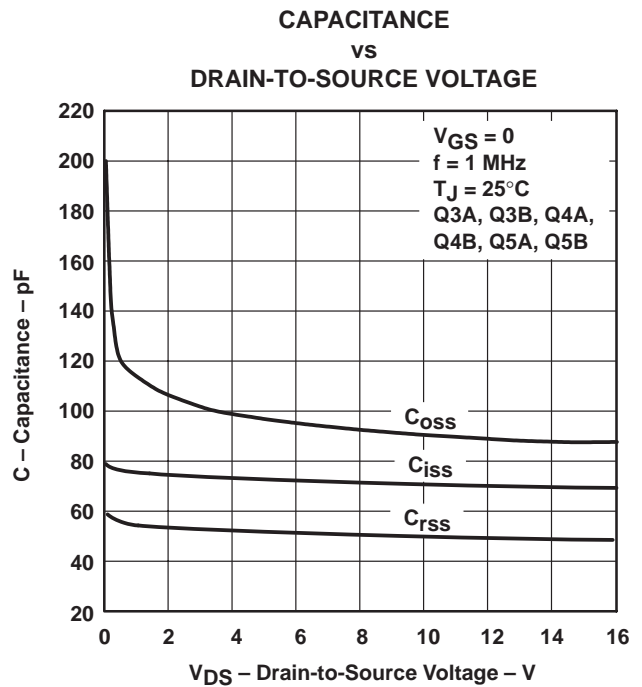


Figure 18

# TPIC1505 QUAD AND HEX POWER DMOS ARRAY

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## TYPICAL CHARACTERISTICS

SOURCE-TO-DRAIN DIODE CURRENT  
vs  
SOURCE-TO-DRAIN VOLTAGE

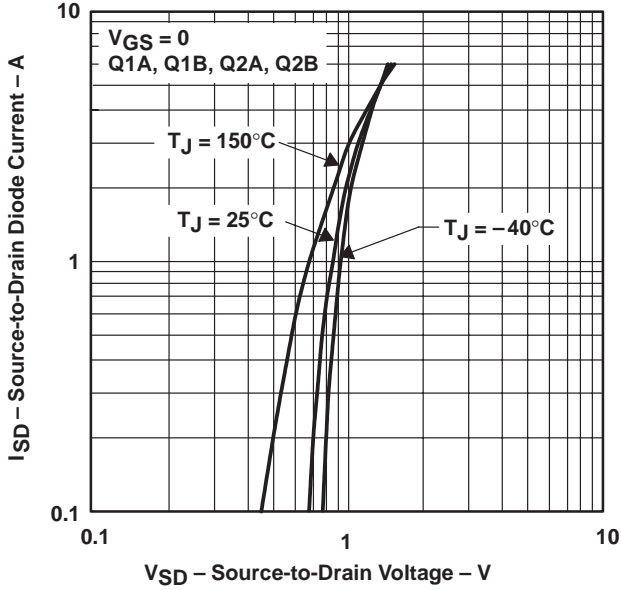


Figure 19

SOURCE-TO-DRAIN DIODE CURRENT  
vs  
SOURCE-TO-DRAIN VOLTAGE

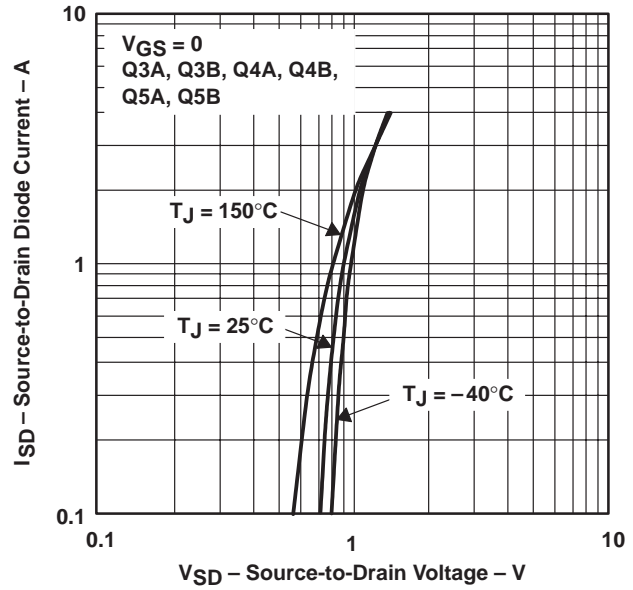


Figure 20

DRAIN-TO-SOURCE VOLTAGE AND  
GATE-TO-SOURCE VOLTAGE  
vs  
GATE CHARGE

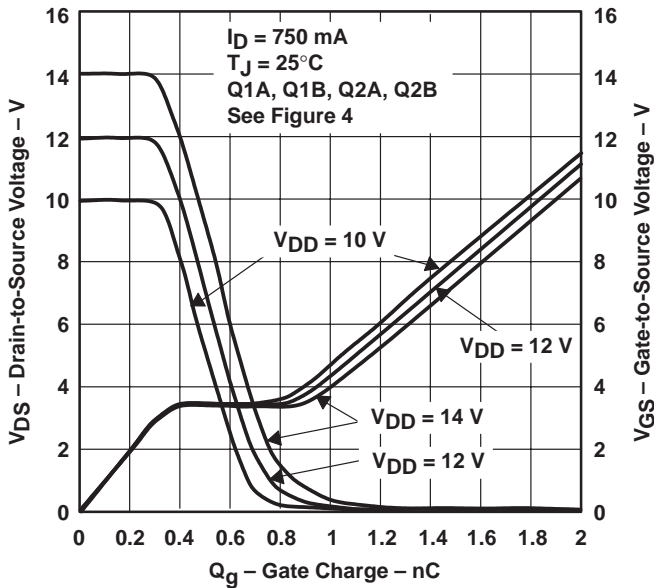


Figure 21

DRAIN-TO-SOURCE VOLTAGE AND  
GATE-TO-SOURCE VOLTAGE  
vs  
GATE CHARGE

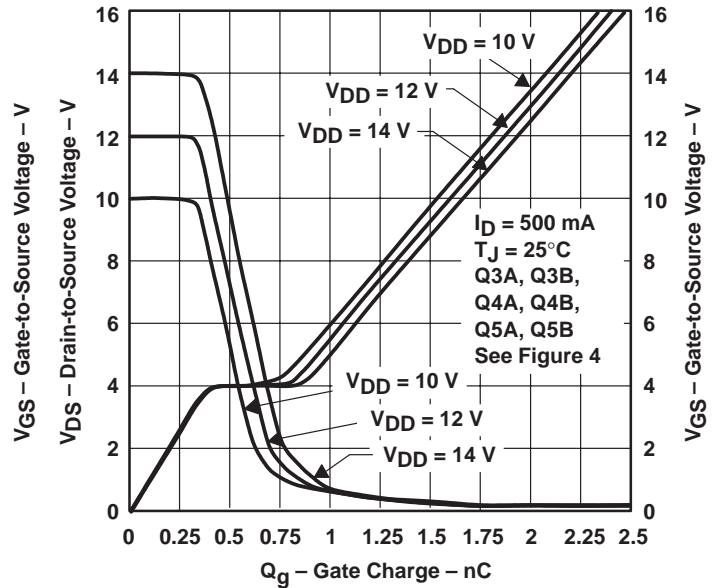


Figure 22

TYPICAL CHARACTERISTICS

REVERSE RECOVERY TIME  
vs  
REVERSE di/dt

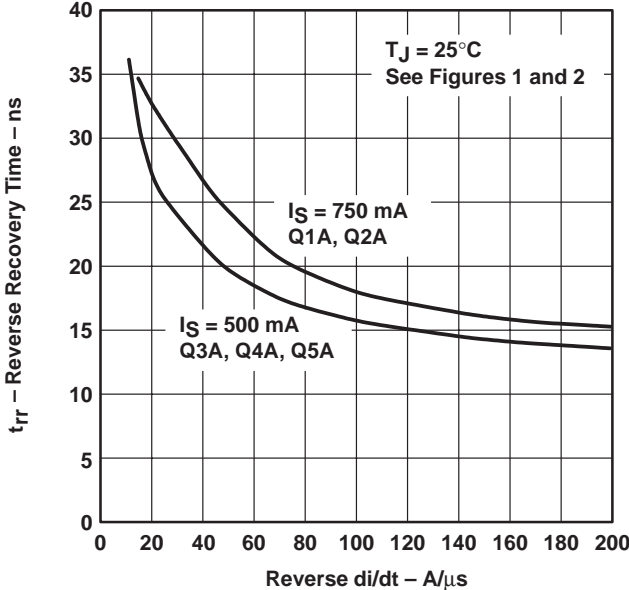


Figure 23

# TPIC1505 QUAD AND HEX POWER DMOS ARRAY

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## THERMAL INFORMATION

### MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

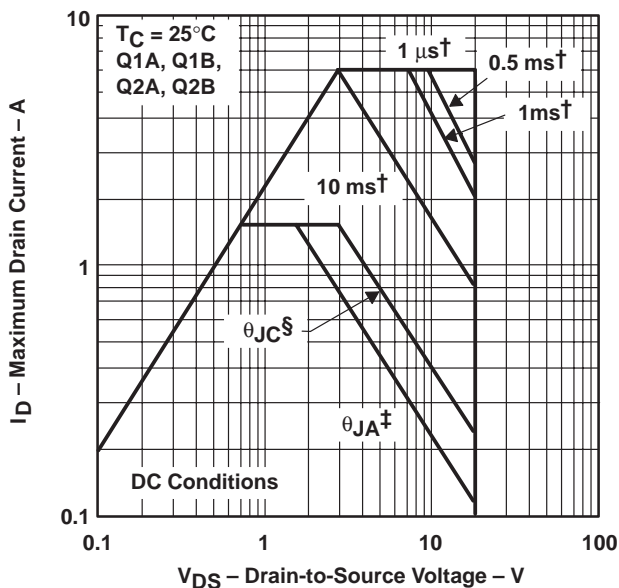


Figure 24

### MAXIMUM DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

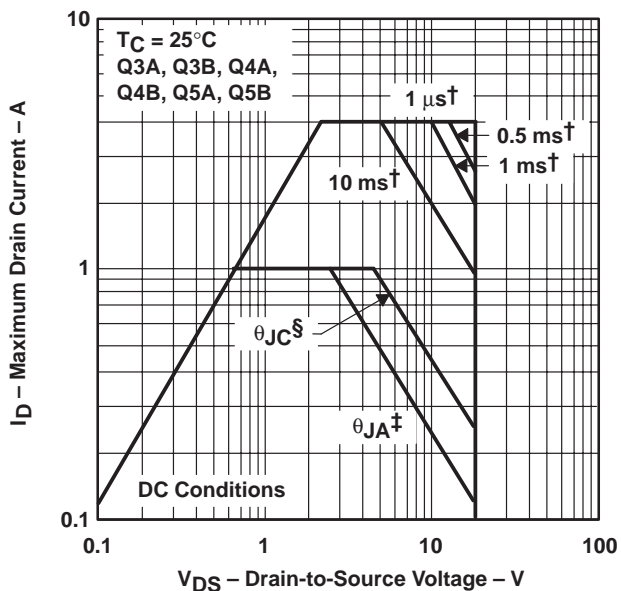


Figure 25

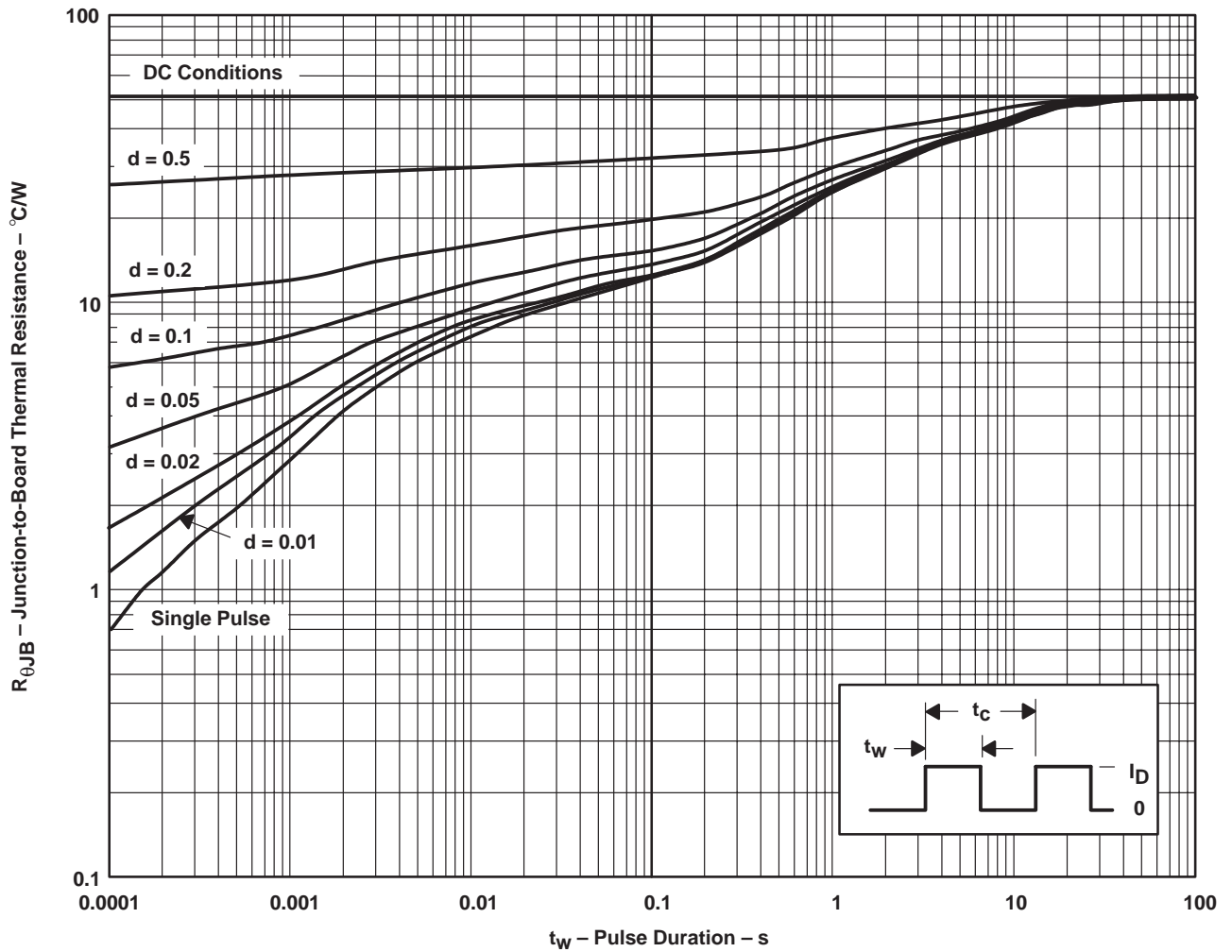
† Less than 10% duty cycle

‡ Device is mounted on a 24 in<sup>2</sup>, 4 layer FR4 printed-circuit board.

§ Device is mounted in intimate contact with infinite heat sink.

THERMAL INFORMATION

DW PACKAGE†  
 JUNCTION-TO-BOARD THERMAL RESISTANCE  
 VS  
 PULSE DURATION



† Device is mounted on 24 in<sup>2</sup>, 4-layer FR4 printed circuit board with no heat sink.

NOTE A:  $Z_{\theta B}(t) = r(t) R_{\theta JB}$   
 $t_w$  = pulse duration  
 $t_c$  = cycle time  
 $d$  = duty cycle =  $t_w/t_c$

Figure 26

## **IMPORTANT NOTICE**

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