# MICROCONTROLLER POWER SUPPLY AND MULTIPLE LOW SIDE DRIVER IC

## FEATURES

- **Eight Low-Side Drivers With Internal Clamp for Inductive Loads and Current Limiting for Self Protection**
  - **Seven Outputs are Rated at 150 mA and Controlled Through the Serial Interface**
  - **One Output Rated at 150 mA and is Controlled Through Serial and/or Parallel Input**
- **5-V ±5% Regulated Power Supply With 200-mA Load Capability at $V_{IN}$ Max of 18 V**
- **Internal Voltage Supervisory for the Regulated Output**
- **Serial Communications for Control of Eight, Low Side Drivers**
- **Enable/Disable Input for Out1**
- **5 V or 3.3 V, I/O Tolerant for Interface to Microcontroller**
- **Programmable Power On Reset Delay Before RST is Asserted High, Once the 5 V is Within Specified Range (Typically 6 ms)**
- **Programmable De-glitch Timer Before $n_{RST}$ is Asserted Low (typically 40 µs)**
- **Zero Voltage Detection Signal With Built in Filter of 20 µs**
- **Thermal Shutdown for Self Protection**

## APPLICATIONS

- **AC Unit**
- **Washing Machines**
- **Refrigeration Systems**

## DESCRIPTION

The ac-unit power supply with low side drive output provides regulated 5-V output to power the system microcontroller and drive up to eight inductive and/or resistive loads. The ac zero detect circuitry is monitoring the cross-over voltage of the mains ac supply. The resultant signal is a low frequency clock output on the ZVS terminal based on the ac line cycle. This information allows the microcontroller to reduce inrush current by powering loads on the ac-line peak voltage.

A serial communications interface controls the eight low side outputs; each output has an internal snubber circuit to absorb the energy in the inductor at turn OFF. Alternatively, the system can place a fly-back diode to $V_{IN}$ to help recirculate the energy in an inductive load at turn OFF.

PRODUCT PREVIEW

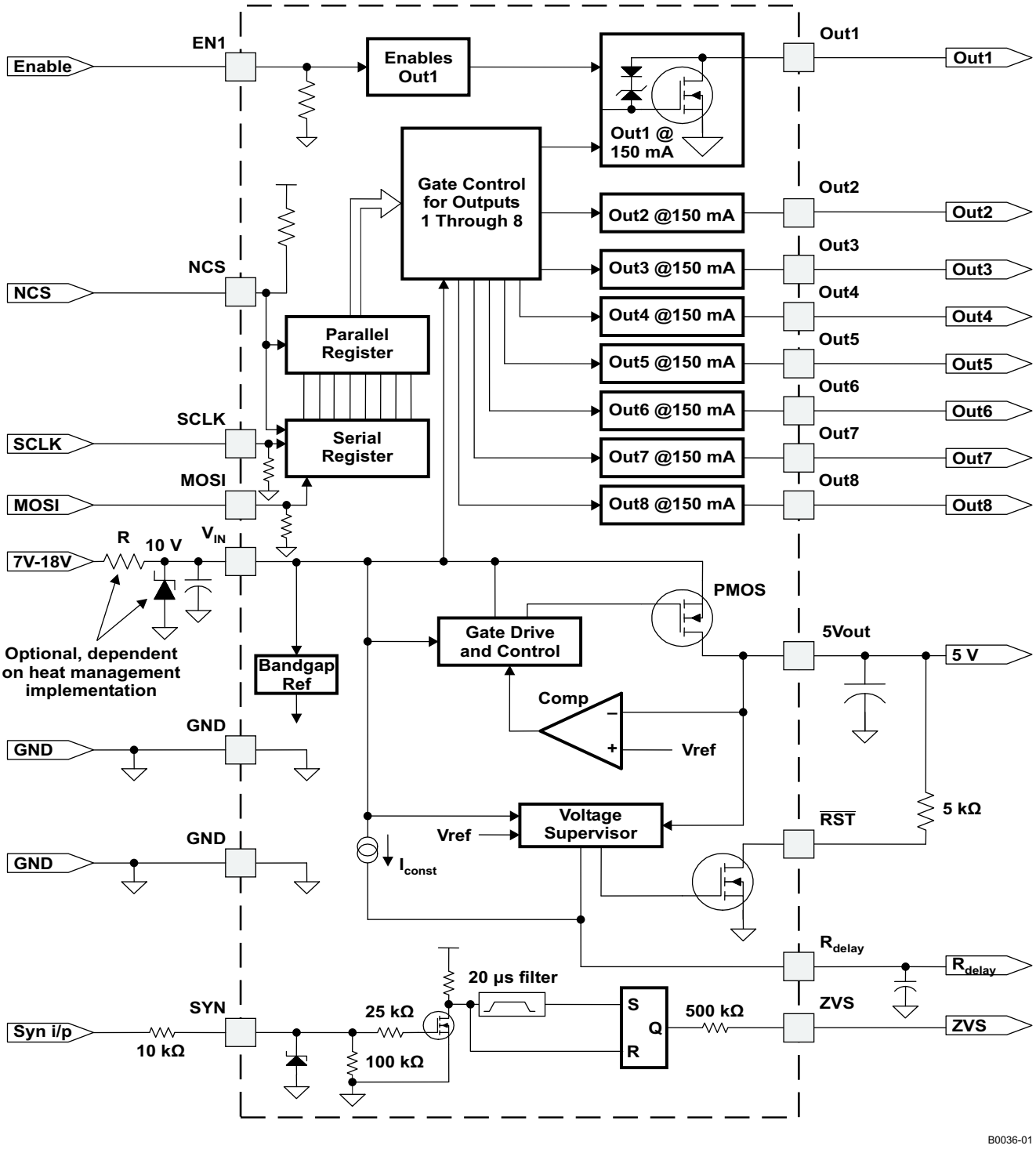
## PIN OUT CONFIGURATION

| PIN NO. | PIN LABEL | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | ZVS | O | Zero Voltage Synchronization |
| 2 | Out1 | O | Low side Output #1 |
| 3 | Out2 | O | Low side Output #2 |
| 4 | Out3 | O | Low side Output #3 |
| 5 | Out4 | O | Low side Output #4 |
| 6 | Out5 | O | Low side Output #5 |
| 7 | Out6 | O | Low side Output #6 |
| 8 | Out7 | O | Low side Output #7 |
| 9 | Out8 | O | Low side Output #8 |
| 10(1) | GND | I | IC Ground |
| 11(1) | GND | I | IC Ground |
| 12 | EN1 | I | Enable/disable for Out1 |
| 13 | $R_{delay}$ | O | Power up reset delay |
| 14 | $\overline{RST}$ | O | Power On Reset output (open drain, active low) |
| 15 | MOSI | I | Sesrial data input |
| 16 | NCS | I | Chip select |
| 17 | SCLK | I | Serial clock for data synchronization |
| 18 | 5Vout | O | Regulated output |
| 19 | $V_{IN}$ | I | Unregulated Input voltage source |
| 20 | SYN | I | AC zero detect input |

(1) Terminals 10 and 11 are internally fused in the lead frame for the 20-pin PDIP package.

PRODUCT PREVIEW

## IC FUNCTIONAL BLOCK

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The value R is chosen based on maximum 5-V out load and minimum operating voltage desired. The Zener on the $V_{IN}$ line helps limit the excess power dissipation within the IC when the operating voltage exceeds 10 V (starts conducting). For 12-V to 7-V operating input, the resistor and Zener are NOT required.

PRODUCT PREVIEW

## DESCRIPTION OF THE FUNCTION

The 5-V regulator is powered from the $V_{IN}$ line; the regulated output will be within 5 V ±5% over the operating conditions. The power on reset line (open drain) remains low until the regulator exceeds the set threshold and the timer value set by the capacitor on reset delay line expires. If both of these conditions are satisfied the POR line is asserted high. This signifies to the microcontroller that serial communications can be initiated to the IC.

The serial communications will be an 8-bit format; with data transfer synchronized using a serial clock from the microcontroller. A single register controls ALL the outputs (1-bit per output). The default value will be zero (OFF). If an output requires PWM function the register will have to be update at a rate faster than the desired PWM frequency. Out1 can be controlled by serial input bit OR the parallel input signal from EN1. The terminal will have an internal pulldown for disabling the output (Out1) in the event there is an open on this terminal.

The SYN input translates the image of the mains voltage through the secondary of the transformer. The SYN input has a resistor to protect from high currents into the IC. The zero voltage synchronization output translates the ac-line cycle frequency into a low frequency clock, which can be used for a timing reference and help power loads on the ac-line peak voltage (to reduce inrush currents).

If reset is asserted ALL outputs are turned OFF internally and the input register is reset to ALL zeroes. The microcontroller will have to write to the register to turn the outputs ON again.



## ABSOLUTE MAXIMUM RATINGS(1)(2)

| | | |
|---|---|---|
| $V_{IN}$ | Unregulated input(3)(4) | 24 V |
| SYN | Unregulated input(3)(4) | 24 V |
| EN1, MOSI, SCLK, and NCS | Logic inputs(3)(4) | 7 V |
| $\overline{RST}$ and $R_{delay}$ | See (3) and (4) | 7 V |
| OUT(1:8) | Low side outputs | 20 V |
| $\theta_{JC}$ | Thermal impedance junction-to-case(5) | 67°C/W |
| $\theta_{JA}$ | Thermal impedance junction-to-ambient(5) | 137°C/W |
| $P_D$ | Continuous power dissipation | 0.912 W |
| ESD | Electrostatic discharge(6) | 2 kV |
| $T_{OP}$ | Operating ambient temperature range | –40°C to 85°C |
| $T_S$ | Storage temperature range | –65°C to 125°C |
| $T_{LEAD}$ | Lead temperature (Soldering, 10 sec) | 260°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Absolute negative voltage on these pins not to go below -1 V
(3) All voltage values are with respect to GND.
(4) Absolute negative voltage on these pins not to go below -0.5 V
(5) The thermal data is based on using 2 oz copper trace with at least four square inches of copper footprint for heat dissipation.
(6) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

## DISSIPATION RATINGS

| PACKAGE | TC ≤ 25°C POWER RATING | DERATING FACTOR ABOVE $T_C$ = 25°C | $T_C$ = 85°C POWER RATING |
|---|---|---|---|
| N | 912.4 mW | 7.3 mW/°C | 474 mW |

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Unregulated input | 7 | | 18 | V |
| SYN | | 0 | | 15 | |
| EN1, $\overline{RST}$, and $R_{delay}$ | Logic level (I/O) | 0 | | 5.25 | V |
| MOSI, SCLK, and NCS | | 0 | | 5.25 | |
| $T_{OP}$ | Operating ambient temperature range | –40 | | 85 | °C |

## ELECTRICAL CHARACTERISTICS

$T_A$ = –40°C to 85°C, $V_{IN}$ = 7 V to 18 V (unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE AND CURRENT** | | | | | | |
| $V_{IN}$ | Input voltage | | (1)7 | | 18 | V |
| $I_{VIN}$ | Input supply current | Enable = ON, Out1–8 = OFF | | | 3 | mA |
| | | Enable = ON, Out1–8 = ON | | | 5 | |
| **LOGIC INPUT (MOSI, NCS, SCLK, and ENS)** | | | | | | |
| $V_{IL}$ | Logic input low level | $I_{IL}$ = 100 mA | | | 0.8 | V |
| $V_{IH}$ | Logic input high level | $I_{IL}$ = 100 mA | 2.4 | | | |
| **RESET ($\overline{RST}$)** | | | | | | |
| $V_{OL}$ | Logic level output | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| $V_{OH}$ | Logic level output | 5-kΩ pullup to $V_{CC}$ | $V_{CC}$– 0.8 | | | V |
| $V_H$ | Disabling reset threshold | 5-V reg ramps up | | 4.25 | 4.5 | V |
| $V_L$ | Enabling reset threshold | 5-V ramps down | 3.3 | 3.75 | | V |
| $V_{HYS}$ | Threshold hysteresis | | 0.3 | 0.5 | | V |
| **RESET DELAY ($R_{delay}$)** | | | | | | |
| $I_{OUT}$ | | | | 28 | | µA |
| $T_{DW}$ | Reset delay timer | C = 47 nF | 1 | 6 | | ms |
| $T_{UP}$ | Reset capacitor to low level | C = 47 nF | | 45 | | µs |
| **OUTPUT (OUT1 through OUT8)** | | | | | | |
| $V_{OL}$ | Output ON | $I_{OUT(x)}$ = 150 mA | | | 0.7 | V |
| $I_{OH}$ | Output leakage | $V_{OH}$ = $V_{IN}$ | | | 2 | µA |
| $I_{LIMIT}$ | Output current limit | OUT(X) = ON and shorted to $V_{IN}$ with low impedance | 350 | | | mA |
| **REGULATOR OUTPUT (5Vout)** | | | | | | |
| 5Vout | Output supply | $I_{5Vout}$ = 5 mA to 200 mA, $V_{IN}$ = 7 V to 18 V<br>$C_{5Vout}$ = 1 µF | 4.75 | 5 | 5.25 | V |
| $I_{5Vout}$ limit | Output short circuit current | 5 V = 0 V | 200 | | | mA |
| **THERMAL SHUTDOWN** | | | | | | |
| $I_{SD}$ | Thermal shutdown | | | 170 | | °C |
| $t_{HYS}$ | Hysteresis | | | 20 | | °C |
| **ZERO VOLTAGE SYNCHRONIZATION (ZVS)** | | | | | | |
| $V_{SYNTH}$ | Transition threshold | | 0.4 | 0.6 | 0.9 | V |
| $I_{SYN}$ | Input activating current | RZV = 10 kΩ and $V_{SYN}$ = 24 V | | | 2 | mA |
| $t_D$ | Transition filtering time | $V_{TF}$ = $V_{CC}$ rising and falling step | 10 | 30 | 70 | µs |

(1) There will be external high frequency noise suppression capacitors and filter capacitor on the $V_{IN}$.

## OUTPUT CONTROL REGISTER

MSB LSB

| IN8 | IN7 | IN6 | IN5 | IN4 | IN3 | IN2 | IN1 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

INX = 0; Output OFF

INX = 1; Output ON

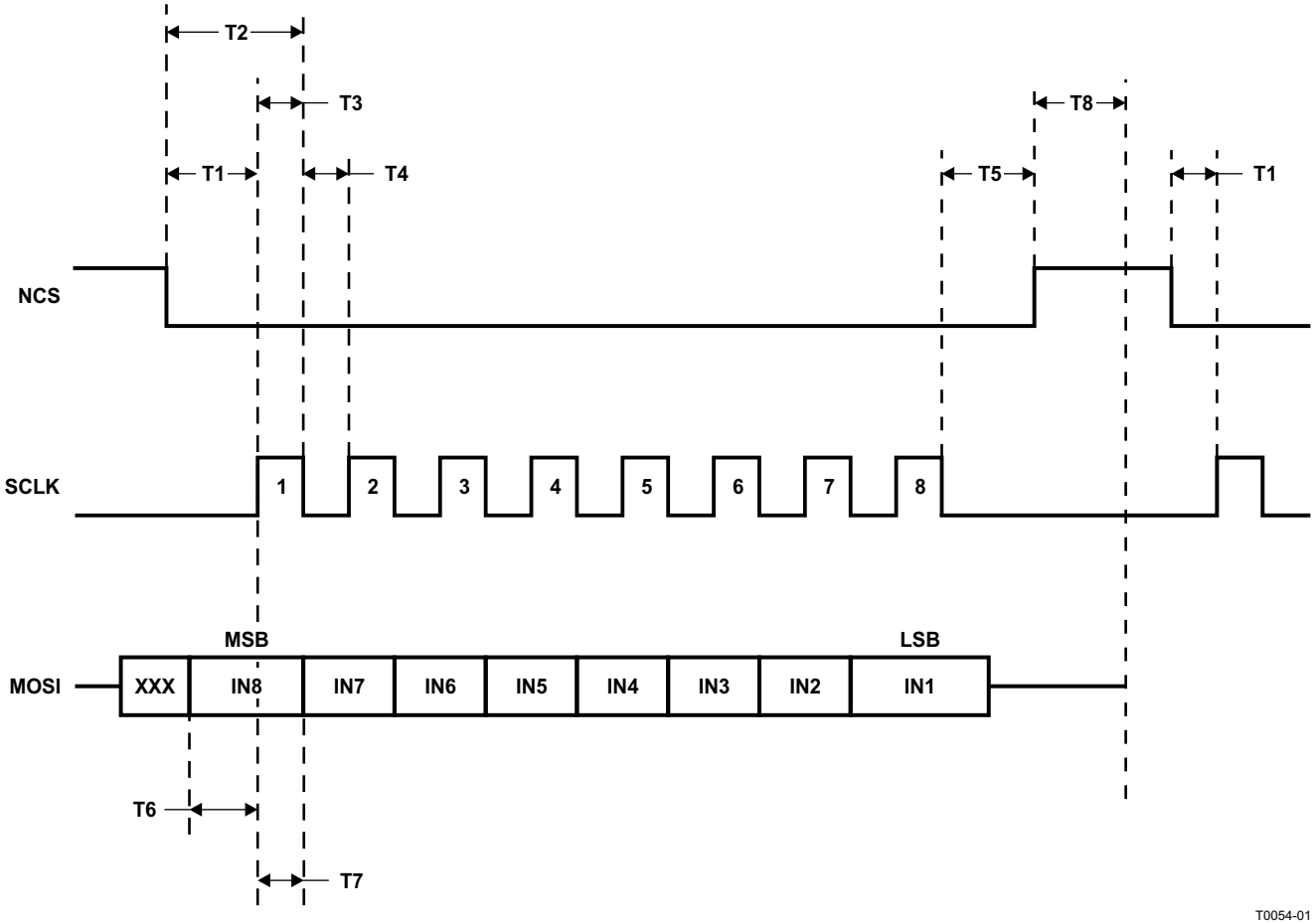
PRODUCT PREVIEW

To operate the output in a PWM mode the output control register has to be updated at a rate 2X the desired PWM frequency of the output. Maximum PWM frequency is 5 kHz. The register is updated every 100 ms.

## SERIAL COMMUNICATIONS INTERFACE

The serial communications will be an 8-bit format; with data transfer synchronized using a serial clock from the microcontroller. A single register controls all the outputs. The signal gives the instruction to control the output of TPIC9201N.

Signal NCS enables the SCLK and MOSI data when it is low. After NCS is set to low for $T_1$, synchronization clock and data begin to transmit and after the 8-bit data has been transmitted, NCS will be set to high again to disable SCLK and MOSI and transfer the serial data to the control register. SCLK must be held low when NCS is in the high state.



## TIMING REQUIREMENTS

$T_A$ = –40°C to 85°C, $V_{IN}$ = 7 V to 18 V (unless otherwise stated)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $F_{SPI}$ | SPI frequency | | 4 | | mHz |
| T1 | Time from NCS falling edge to CLK rising edge | 10 | | | ns |
| T2 | Time from NCS falling edge to CLK falling edge | 80 | | | ns |
| T3 | Time for CLK to go high | 60 | | | ns |
| T4 | Time for CLK to go low | 60 | | | ns |
| T5 | Time from last CLK falling edge to NCS rising edge | 80 | | | ns |
| T6 | SDI setup time before CLK edge | 10 | | | ns |
| T7 | SDI hold time after CLK edge | 10 | | | ns |
| T8 | Time between two words for transmitting | 170 | | | ns |

### $R_{DELAY}$

THe $R_{DELAY}$ output provides a constant current source to charge an external capacitor to approximately 6.5 V. The external capacitor is selected to provide a delay time based on the current equation for a capacitor, I = C dv/dt and a 28 µA typical output current.

Therefore, the user should select a 47-nF capacitor to provide a 6 ms delay at 3.55 V.

I = C dv/dt

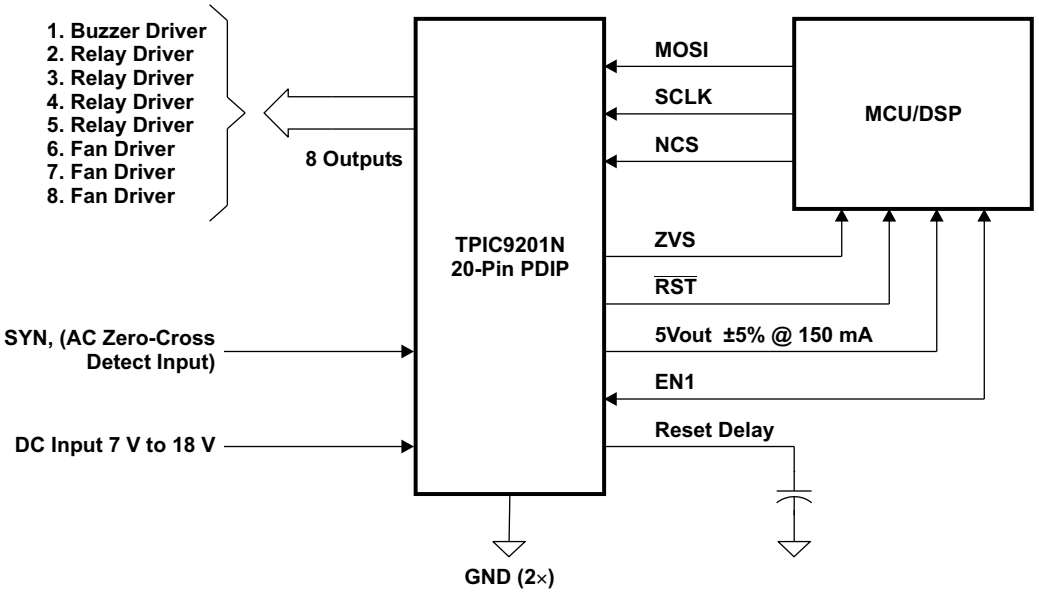
28 µA = C × (3.55 V / 6 ms)

C = 47 nF

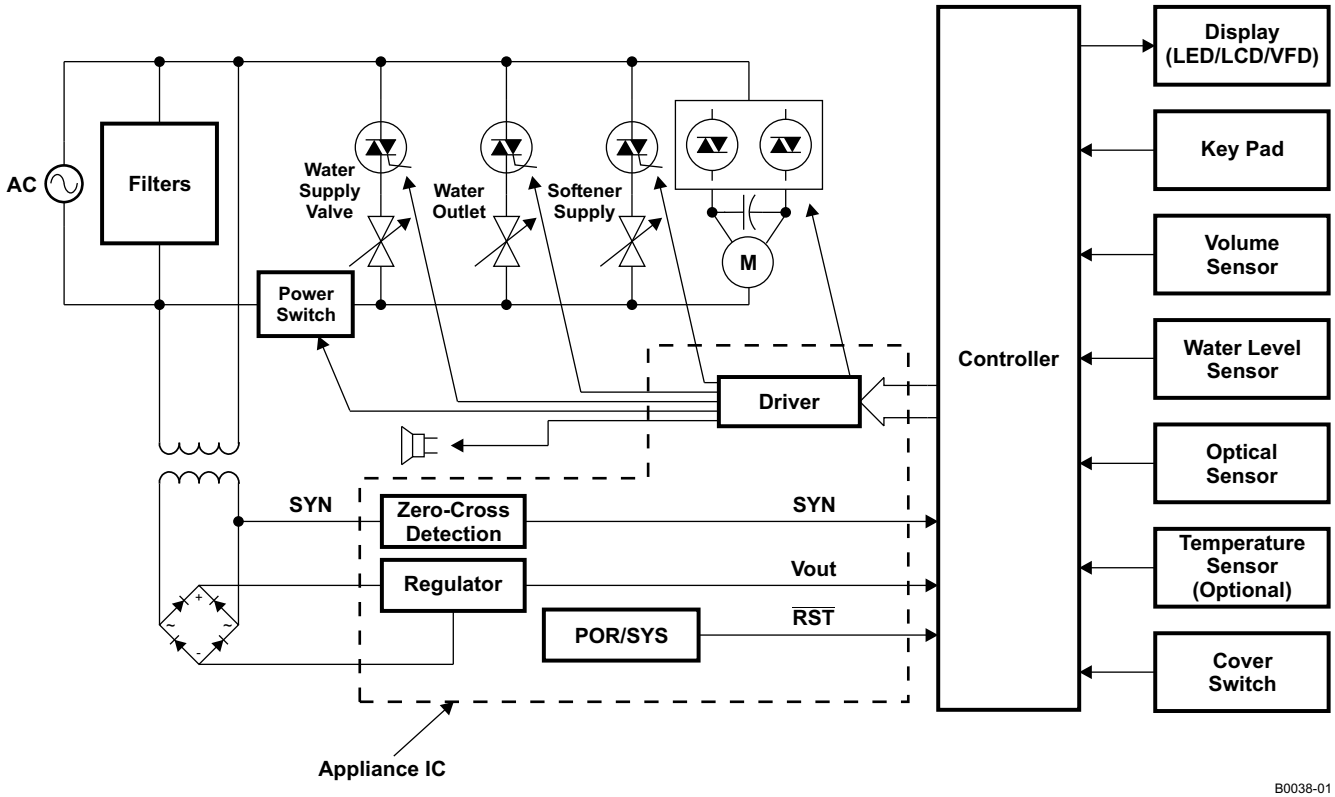
PRODUCT PREVIEW

# APPLICATION INFORMATION

## APPLICATIONS




## WASHING MACHINE APPLICATION



## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TPIC9201N | PREVIEW | PDIP | N | 20 | 20 | TBD | Call TI | Call TI |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

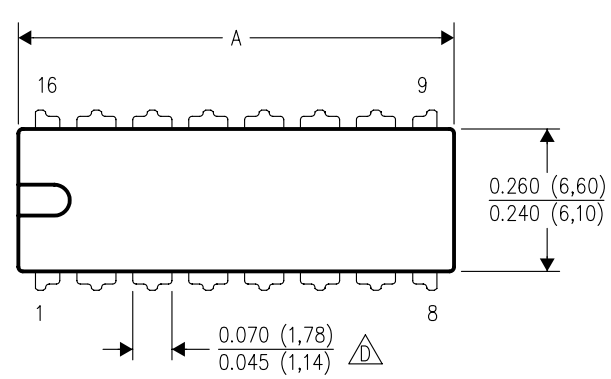
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

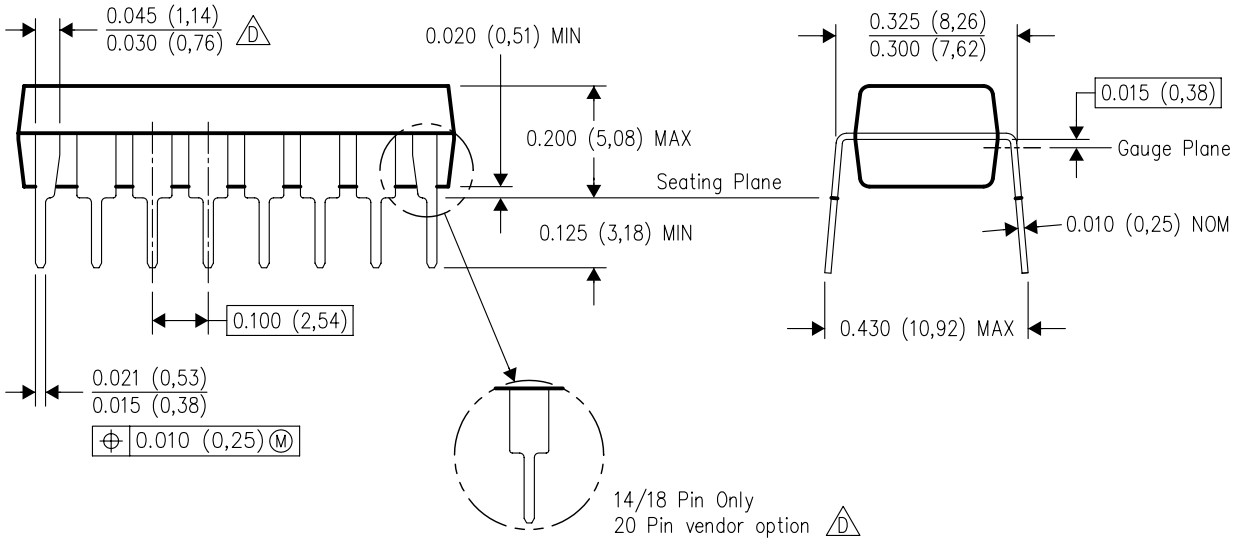
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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