TPS2342 PCIX2 Hot Plug Controller Demo System

Reference Design

TPS2342 PCIX2 Hot Plug Controller Demo System

System Power

ABSTRACT

This manual provides descriptive and operational information for the Texas Instruments TPS2342 reference design/demo board.

1 Introduction

The TPS2342 is a highly integrated hot plug controller for PCI, PCIX and PCIX2 slots. It communicates with the main system's PCI bridge slot controller over either a serial or parallel interface.

This reference design describes the TPS2342 demo module setup, GUI operation details, schematics, and parts list for the reference design/demo board system.

The demonstration system is a reference design to the user for a faster design turn. Observation of hot plug signals and system operation is convenient with test points and LED indicators. Operator interaction is through a GUI or manual switch inputs.

2 Materials Needed

2.1 TI Supplied

TPS2342 reference design/demo board kit consisting of

- TPS2342 demo board
- Load board
- Power cables for J1 and P1
- Current probe cables
- TPS2342 PCIX2 hot plug controller demo system − reference design
- TPS2342 datasheet
- TPS2342 demo system software

2.2 User Supplied

Power Supplies

- 3.3 V_{AUX}, 2 A
- 12 V, 2 A
- −12 V, 2 A
- 5 V, 14 A
- 3.3 V, 20 A

Personal Computer

- LPT1 parallel port
- Parallel port extension cable
- CD ROM drive or
- Network connection to download software

Test Equipment

- Digital oscilloscope
- Current probe

3 System Operation

The demo system has graphical user interface software (GUI) allowing the operator to manually change the state of the TPS2342 control signals. The computer's LPT1 port connects with a parallel extension cable to the demo board. The parallel data connects to a CPLD that controls timing of signals to/from the TPS2342 emulating the interface of the PCI bridge hot plug controller. Figure 1 is a block diagram of the demo module board.

There are two PCI slots on the demo board. A test load board is supplied so that full load, no load and short circuit may be applied to bus power momentarily. The user can test that the proper result occurs. Alternatively, remove the test load board and install any PCI compatible module for test. When standard PCI cards are used on the motherboard, remove the metal bracket from the PCI card because of interference with the demo circuit board.

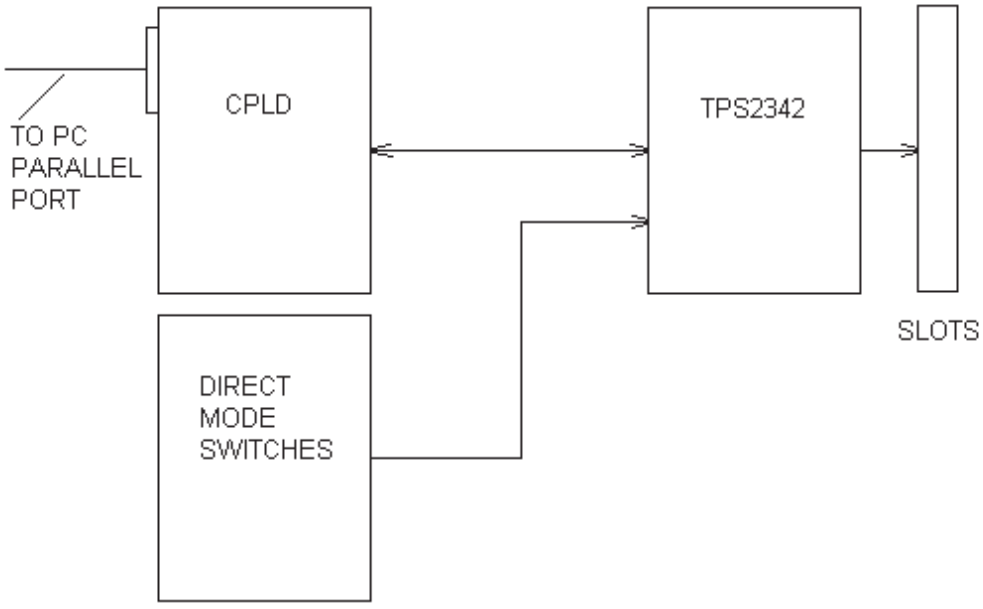


Figure 1. Demo Module Board

4 Power Connections

Power cables are supplied. Identify the power cable and locate the connector pin numbers as stamped on the demo circuit board. Connect the proper pins to power supplies with voltage and capacity as shown in Tables 1 and 2. Figure 2 is a connection diagram for the TPS2342 demo board to power supplies.

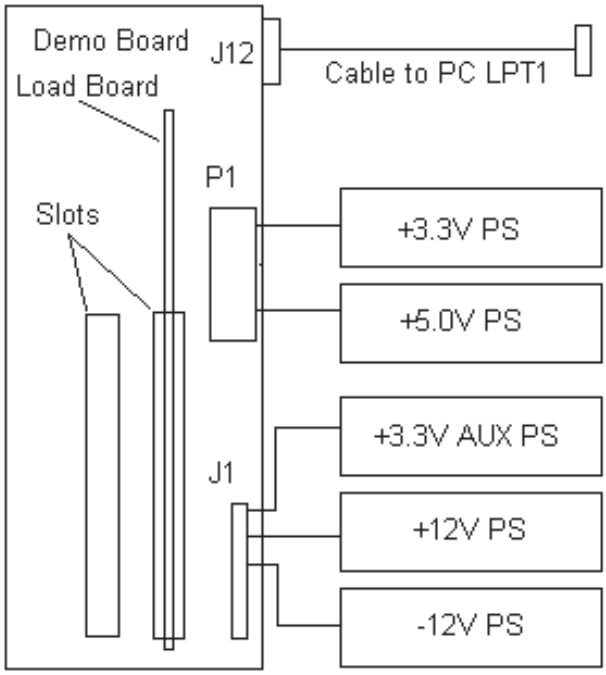


Figure 2. Connection Diagram

5 Cables

5.1 J1 Connector

Pin 1 on the J1 connector is marked on the connector body and on the printed circuit board.

Table 1.

J1	Voltage	Min Capacity
1	+3.3 VAUX	2 A
2	+12 V	2 A
3	−12 V	2 A
4	GND	
5	GND	
6	GND	

5.2 P1 Connector

Table 2.

P1	Voltage	Min Capacity	P1	Power
1	+5 V	14 A	8	GND
2	+5 V		9	GND
3	+5 V		10	GND
4	+3.3 V	20 A	11	GND
5	+3.3 V		12	GND
6	+3.3 V		13	GND
7	+3.3 V		14	GND

5.3 CPU Parallel Connector

Connect the parallel extension cable from the PC parallel port to the demo board J12 connector.

6 Software Overview

The software can be used to toggle the data presented to the TPS2342. In serial modes, the read-back condition of the data is displayed in the GUI LEDs. The GUI LED is green when the data read-back matches the data sent, red when there is a mismatch and yellow before read-back so it is invalid. In the direct mode, the read-back is invalid because many of the serial mode signals are not available. Select manual in the lower middle area of the GUI to disable read-back in direct mode.

No automatic changes are made by the GUI software. For example, a demo board fault indication does not automatically force a RST from the GUI and the other chain of events that normally follow in an actual system.

7 Demo Board Slots

There are two PCI slots on the demo module; slot A and slot B. These are standard 64-bit PCI slots that can be defined for operation from 33 MHZ to 533 MHZ by the PCIXCAP signals. PCIXCAP can be input form either the load board or the GUI. The active signals on these slots are RST, POWEN, BUSEN, CLKEN, and power pins. The address, data and other control signals are each tied to a pull-down resistor.

Although a load board is provided and discussed here, any PCI interface board can be installed and tested with respect to hot plug. The load board, when a standard PCI board is used in the slot, power is supplied to the load the when the slot power is enabled.

If the TPS2342 is soldered to the board, it utilizes the power pad package and will have good thermal conductance. Demo boards with TPS2342 sockets could reach thermal shutdown under high constant load. Unlike the load board, when a standard PCI board is used in the slot, power is supplied to the load the when the slot power is enabled.

The load board is on for a short duty cycle and will not cause the TPS2342 in a socket to overheat.

8 Demo Board Test Points and Jumpers

8.1 Test Points

The voltage across the sense resistors can be measured to determine current for each supply. Table 3 shows the test points and sense resistor values.

Table 3. Test Points and Sense Resistor Values

Voltage (V)	Sense Resistor (Ω)	Test Points	Jumpers
3.3 V_{AUXA}	0.1 Ω	TP22, TP23	J6
3.3 V_A	0.006 Ω	TP36, TP37	–
5.0 V_A	0.006 Ω	TP38, TP39	–
+12 V_A	0.1 Ω	TP30, TP31	J8
−12 V_A	0.1 Ω	TP33, TP34	J9
3.3 V_{AUXB}	0.1 Ω	TP20, TP21	J5
3.3 V_B	0.006 Ω	TP3, TP4	–
5.0 V_B	0.006 Ω	TP1, TP2	–
+12 V_B	0.1 Ω	TP9, TP10	J3
−12 V_B	0.1 Ω	TP6, TP7	J2

8.2 Jumpers

Jumpers J2, J3, J5, J6, J8 and J9 must be installed to connect the power to the slot. Any of these jumpers can be replaced by wire loops supplied in the demo board cable kit to use a current probe. The Jumpers for supplies supporting this feature are listed in Table 3

9 Demo Board Switches and Indicators

9.1 Switches

The PCIXCAP switches select the source of these signals from either the load board or the GUI. The V_{IO} switches select regulated or switched mode for the 1.5-V V_{IO}. The positions of these slide switches and their functions are silk screened on the demo board. Table 4 summarizes these switches.

Table 4. V_{IO} Slide Switches

Function	Slot A	Slot B
PCIXCAP	S3	S2
VIO switched or regulated	S4	S1

In either GUI or SLOT operation, the voltage is read by the TPS2342 and converted to an octal number for the slot controller. Below is the table of output voltage at TP28, slot A, TP12, slot B for PCIXCAP. LEDs D8, D9, D10 correspond to PCIXCAP1 thru 3 respectively for slot A and D3, D4, D5 for slot B. The LED is lit when the PCIXCAP bit is at 0 V.

Table 5.

PCIXCAP1	PCIXCAP2	PCIXCAP3	TP28/TP12	BUS SPEED
0 V	0 V	0 V	0.0 V	33/66 2.2
0 V	0 V	3 V	1.7 V	266
3 V	0 V	0 V	2.5 V	66 X
3 V	0 V	3 V	0.8 V	533
3 V	3 V	0 V	3.3 V	133

Switches S5 to S16 are switches for direct mode operation without the GUI. These are described in the Section 7, Interface Operating Modes and Section 9, Direct Mode Switches (No GUI).

9.2 Indicators

The following indicators on the front center of the demo module left to right are listed here top to bottom in Table 6.

Table 6. Indicators

Slot A		Slot B	
LED	Function	LED	Function
D10	BUSENA/PCIXCAP1A	D5	BUSENB/PCIXCAP1B
D9	CLKENA/PCIXCAP2A	D4	CLKENB/ PCIXCAP2B
D8	RESETA/ PCIXCAP3A	D3	RESETB/ PCIXCAP3B
D7	ATTLEDA	D2	ATTLEDB
D6	PWRLEDA	D1	PWRLEDB
D21	RSTA	D22	RSTB
D19	PRSNT2A/AUXFAULTA	D17	PRSNT2B/AUXFAULTB
D20	PRSNT1A/FAULTA	D18	PRSNT1B/FAULTB

10 Load Board

The load board allows the operator to apply power to the slots and check proper operation of the hot plug controller functions. Standard PCI, PCIX and PCIX2 boards can be inserted in the demo board backplane for hot plug testing.

10.1 Load Board Jumpers and Test Points

Jumpers are added to the load board to add a step capacitive load to each voltage. Table 7 shows the jumpers associated with each supply and the capacitive load added for each. For example, J6 and J7 installed add a 2000-μF load to the +5-V supply.

Table 7. Load Board Jumpers and Test Points

Voltage	Jumpers	Loading Each Jumper (μF)	SupplyTest Points	Ground Test Points
+12 V	J2, J3	150 μF	TP1	TP2
+5 V	J6, J7, J8	1000 μF	TP3	–
−12 V	J11	150 μF	TP5	TP4
+3.3 V_{AUX}	J14	150 μF	TP6	TP7
+3.3 V	J17, J18, J19	1000 μF	TP8	–
VIO	J22, J23, J24	150 μF	TP10	–

V_{PULSE} is available on TP9 and is active when switch 8 is pressed or an external trigger is applied.

11 Load Board Switches and Indicators

11.1 Switches

Each supply voltage has a DIP switch that controls the power supply loading. The switch positions for some power segments are no load, short circuit, overload, and full load. Other segments are no load, overload and full load. The following table shows the dip switch and position for loading any segment. Turn on only one switch position in a switch pack at a time.

Table 8.

Voltage	Switch	Switch Position	Function	Indicator	Test Points
+12	SW1	1	Short	D2	TP1
		2	Overload		
		3	Full load		
+5	SW2	1	Overload	D3	TP3
		2	Full load		
−12	SW3	1	Short	D4	TP5
		2	Overload		
		3	Full load		
3.3 VAUX	SW4	1	Short	D6	TP6
		2	Overload		
		3	Full load		
3.3	SW5	1	Overload	D7	TP8
		2	Full load		
VIO	SW7	1	Overload	D9 (1.5)	TP10
		2	Full load	D8 (3.3)	

The selected load is applied to the power supply for a 10-ms duration when the load push button, SW8, is pressed. When the button is held down, the load is applied for 10-ms at a 1-Hz rate. A signal can be applied to the BNC input J26 instead of pressing the manual pushbutton.

11.2 Indicators

The load board has an LED for each power supply that is on when the supply is ok. These are the indicators listed in Table 8.

DIP switch SW6 is used to switch resistors in a voltage divider to create a slot generated PCIXCAP signal. Table 9 lists switch settings for bus speed.

Table 9. Bus Speed Switch Settings

Switch On	Bus Speed MHz
S1	533
S2	266
S3	66
S4	33
All off	133

12 Software Installation

The software is distributed on a CD ROM disk in the demo package. Insert the CD ROM into a drive on your PC and copy the contents into a folder you choose.

13 Operation

Power-up the motherboard with no special sequencing of the bench power supplies. At the computer, go to the folder containing the CD ROM data. Just double click on the program icon TPSDiag1.exe.

A graphical user interface (GUI) window opens. Reference Figure 3, the GUI screen. Go to the lower middle of the GUI and select the computers parallel port setting. This is usually 0378H in the pull down menu. When you select the port address, the GUI issues a reset CPLD. If the port address is incorrect, the GUI will indicate the CPLD is not responding. The computer's port setting can be checked by going to the computer control panel and opening SYSTEM, select the PARALLEL PORT and view RESOURCES for the parallel port address. Go back to the GUI and select the correct port address.

The reset CPLD button is an available function anytime during operation. The Auto Control button enables GUI LED readback. When this button is pressed, it is labeled manual control and GUI LED readback is invalid. The SEND CMD button at the bottom middle should be selected after any button is selected, except reset CPLD, in order to send the selection

The GUI is a tool done for applications lab exercise and debug. Some of the buttons were used by the GUI author for code writing and debug and are not available to the user. These buttons include No Uart Reply Data, Canned Diag, Input Data General Status, Control Command 2, Control Command 3, and Input Data Command.

The top middle of the GUI and the left and right sides are available to the user to issue commands to the CPLD and demo module. The CPLD handles command and status information to the TPS2342 in proper timing and format in the serial modes. When you make a selection in any of the blocked areas, the radio button in the area is automatically selected. Only commands in this area are sent to the demo module when you select the SEND CMD button.

14 Auto/Manual Button

Auto control updates the GUI status readbacks while MANUAL does not.

15 Interface Operating Modes

The operating modes are described in the TPS2342 data sheet but the modes accessible with the demo module and software are:

- Direct mode (GUI or switches)
- Single slot serial mode,
- Multislot serial mode,
- Forced enabled mode.

Direct mode is the configuration where logic signals are tied directly to the TPS2342. The controller receives fault information from the TPS2342 and can control the power state with an input signal.

The serial modes of operation are used to communicate more information from the TPS2342 to serverworks compatible PCI chipsets.

The forced enable mode offers power management but is controlled only by the operator switches. The TPS2342 will not turn off power on detecting fault.

The operating mode bit settings are shown in Table 10 just for reference. These settings are made by the GUI software. The mode is entered on the rising edge of PGOOD. Once the mode settings are made, toggle the PGOOD signal. Select PGOOD de-asserted, use the SEND command to issue PGOOD de-asserted. Then select PGOOD assert and use the SEND command to issue PGOOD Asserted. Ignore GUI LED readbacks when in the direct mode. These readbacks are only valid in the serial modes.

Table 10. Bit Setting Operating Mode

PGOOD	BUTTONA	SIDB	SIDA	PWRLEDx	Operating Mode
↑	< 6 V	0	0	1	Single-slot serial mode: Using different hot-plug controllers for slot A and slot B.
↑	< 6 V	0	1	1	Multi-slot serial mode: Using the same hot-plug controller for slot A and slot B, and potentially cascading additional TPS2342.
↑	< 6 V	1	0	1	Direct mode.
↑	> 9 V	0	0	1	Tri-state test mode. In this mode, all digital pins (outputs and inputs) are tri-state; in addition, pull-ups and pull-downs are disconnected.
↑	> 9 V	0	1	1	NAND-tree test mode. In this mode, all pins are tri-state except for M66ENB.
↑	> 9 V	1	X	1	Reserved.
1	> 9 V	SIDB	SIDA	1	Normal operation, but Pwren_xo driven on PWRLEDx and Fault_xo_ driven on ATTLEDx
1	< 6 V	SIDB	SIDA	1	Normal operation.
↑	X	X	X	0	Force enable mode. The slot is forced enabled.

16 Direct Mode (GUI)

With the GUI started and the port selected, use commands listed below. Commands are found in the Control Command 1 area. SEND command and AUTO/MANUAL control are in the lower middle area. Be sure that V_{AUX} is on before you enter direct mode and turn on primary power.

- Click PGOOD asserted => PGOOD de-asserted
  - Send CMD
- Click Serial Mode => Parallel Mode
  - Send CMD
- Click PGOOD de-asserted => PGOOD asserted
  - Send CMD
- Click Auto Control => Manual Control
  - Send CMD

The TPS2342 is in direct mode. The power indicator LEDs on the load board are on in primary power and V_{AUX}. The SW for the slot controls the V_{AUX}. If V_{AUX} is off, toggle the switch to reset.

- Click Switch Closed => Switch Opened
  - Send CMD
- Click Switch Opened => Switch Closed
  - Send CMD

Primary power can be cycled from either PGOOD or Power EN asserted/de-asserted.

17 Direct Mode Switches (No GUI)

Turn off SW6 through SW15 on the demo module. Install the load board or a PCI board in slot A or B. Both slots work the same way but this write up will use the slot A. Select the direct position with the S5 switch and press the momentary button S16 to apply the PGOOD signal. Turn on SWA and this will apply V_{AUX} to the add-in module. Use the VIOSELA switch S13 to select V_{IO} for 3.3 V (Right) or 1.5 V (Left). Turn on the POWENA switch S12 to turn on main power. Cycle the main power by toggling either the PWRENA switch or the PGOOD switch. Main power must be off in order to change the VIO setting. The selected VIO turns on with the main power.

ALEDENA, S14, and PLEDENA, S15, turn on the attention LED and the power LED, respectively.

18 Multi-Slot Serial Mode (GUI Only)

Select serial mode (default at power-up) If the GUI is in parallel mode

- Click Parallel Mode => Serial Mode
  - Send CMD
- Click PGOOD asserted => PGOOD Dd-asserted
  - Send CMD
- Click PGOOD de-asserted => PGOOD asserted
  - Send CMD
- Click POWEN de-asserted => POWEN asserted

Primary power can be cycled from either PGOOD or POWEN asserted/de-asserted. SW controls V_{AUX}. If V_{AUX} is off, toggle the switch to reset.

- Click Switch Closed => Switch Opened
  - Send CMD
- Click Switch Opened => Switch Closed
  - Send CMD

19 Single Slot Serial Mode (GUI Only)

Single slot mode of operation of the TPS2342 controls two independent slots. The demo module uses only slot A and slot B is disabled. This is indicated by the GUI top middle portion (<<−Slot A || Slot B DIABLED). Set up commands are:

Select serial mode (default at power-up) If the GUI is in parallel mode

- Click Parallel Mode => Serial Mode
  - Send CMD
- Click Multi Slot Mode => Single Slot Mode
  - Send CMD
- Click PGOOD asserted => PGOOD de-asserted
  - Send CMD
- Click PGOOD de-asserted => PGOOD asserted
  - Send CMD
- Click POWEN de-asserted => POWEN asserted

Main power can be cycled from either PGOOD or POWEN asserted/de-asserted. SW controls V_{AUX}.

20 Forced Enable Mode (GUI Only)

This mode is used to turn on the output power regardless of fault conditions. It can be turned off only by the processor negating the PWREN signal. This is usually only a test and debug mode.

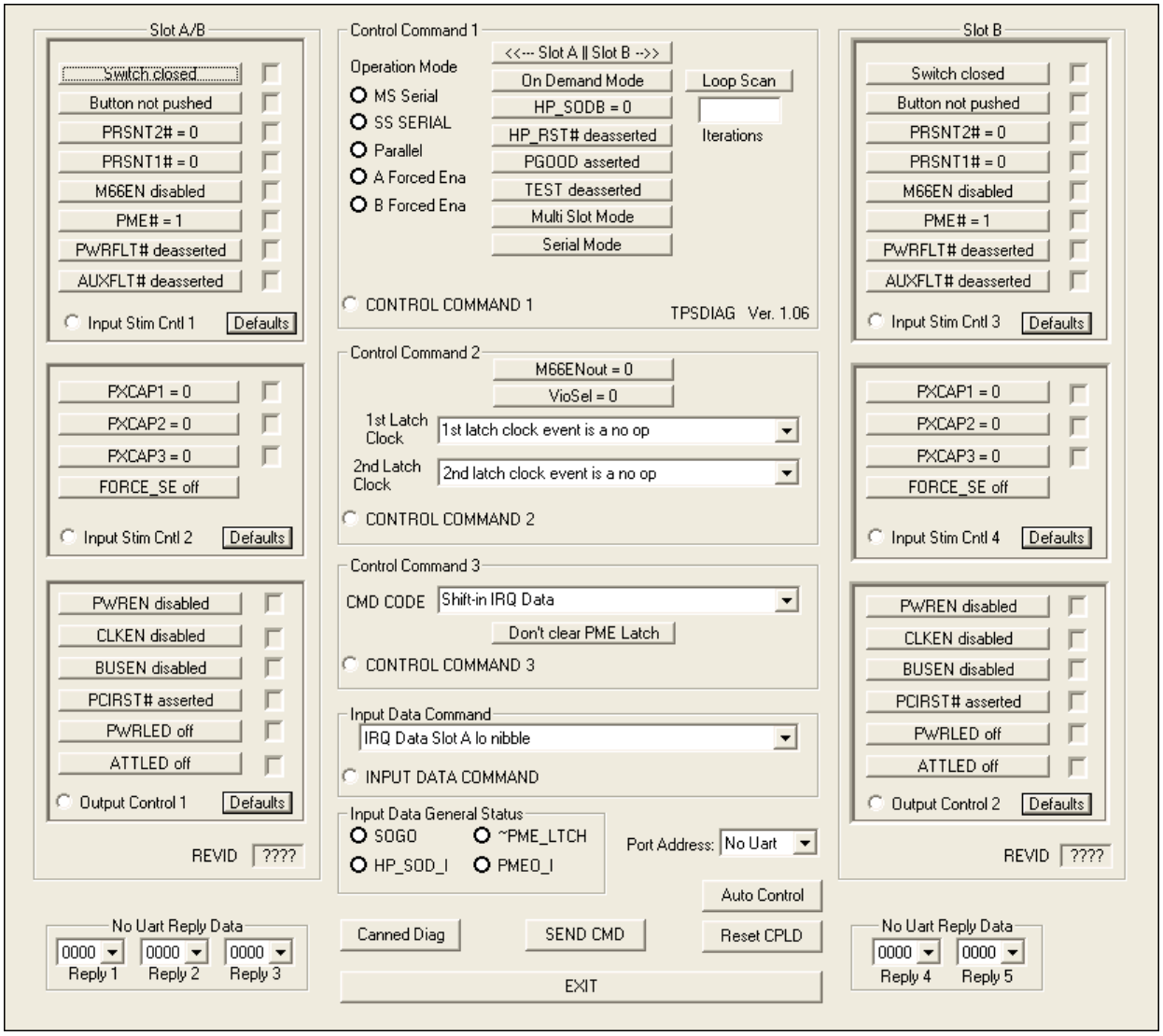


Figure 3. GUI Screen

21 Appendix A

21.1 Demo Board Schematic

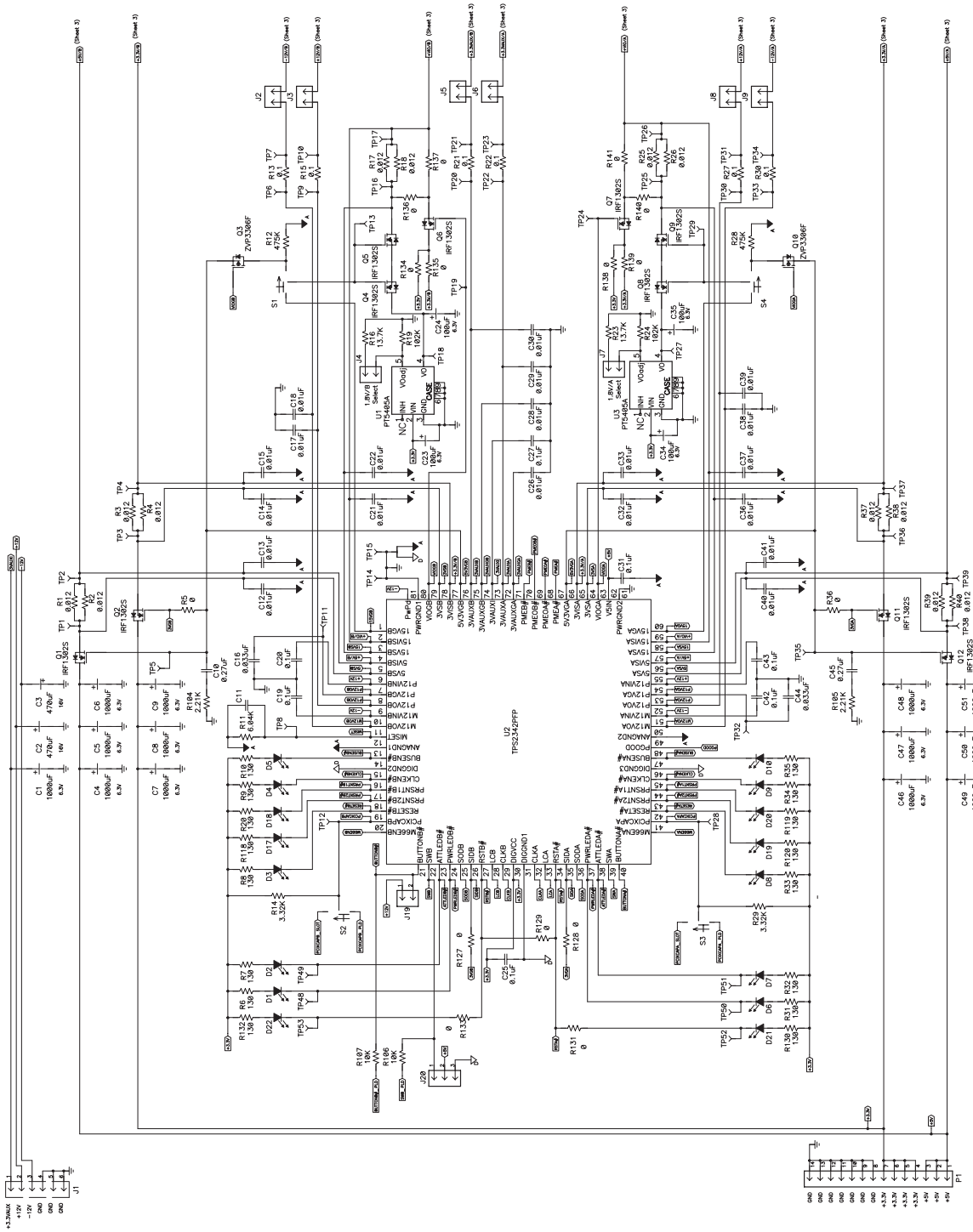


Figure 4. Reference Design/Demo Board

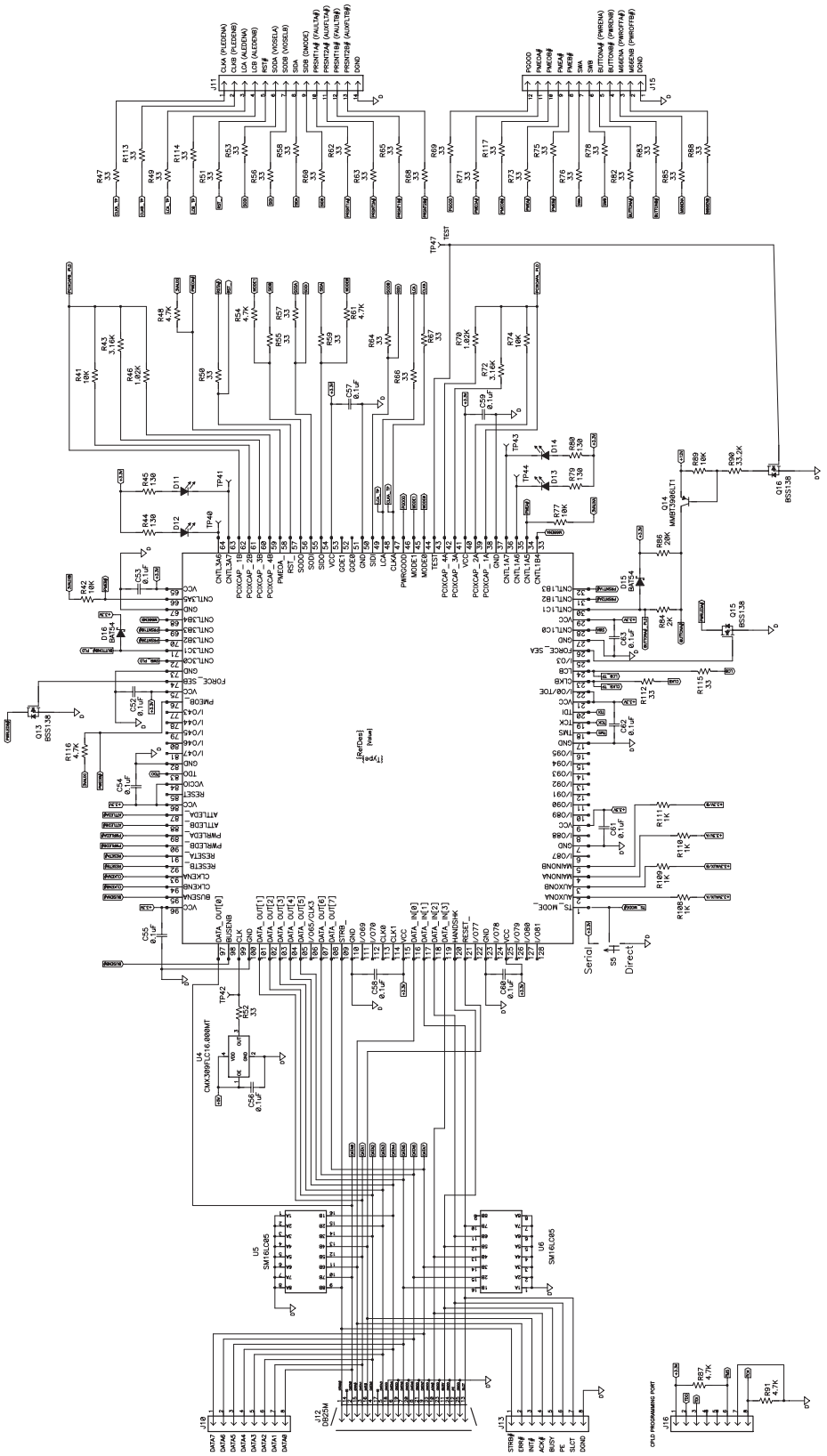


Figure 5.

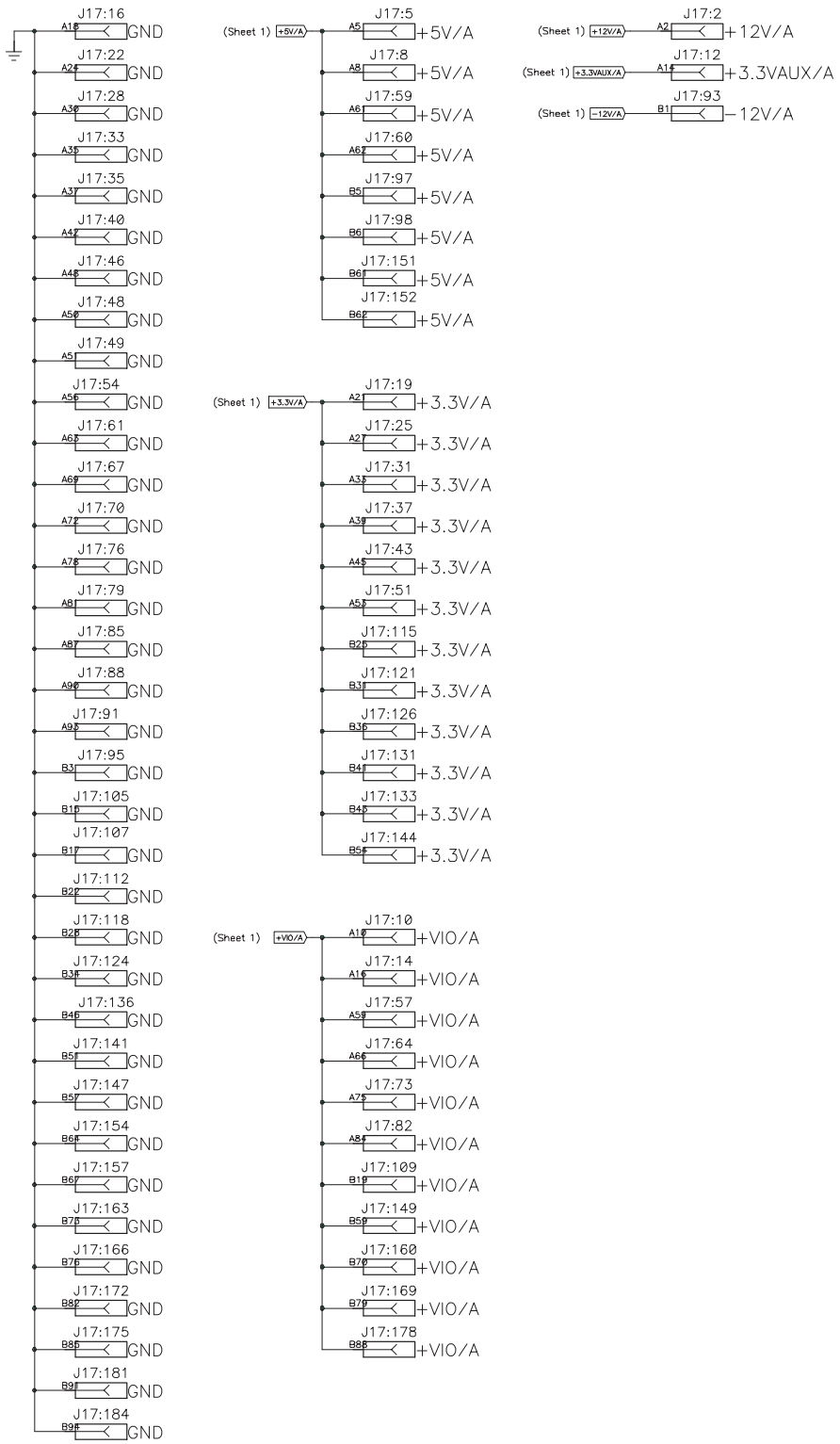


Figure 6. Slot A

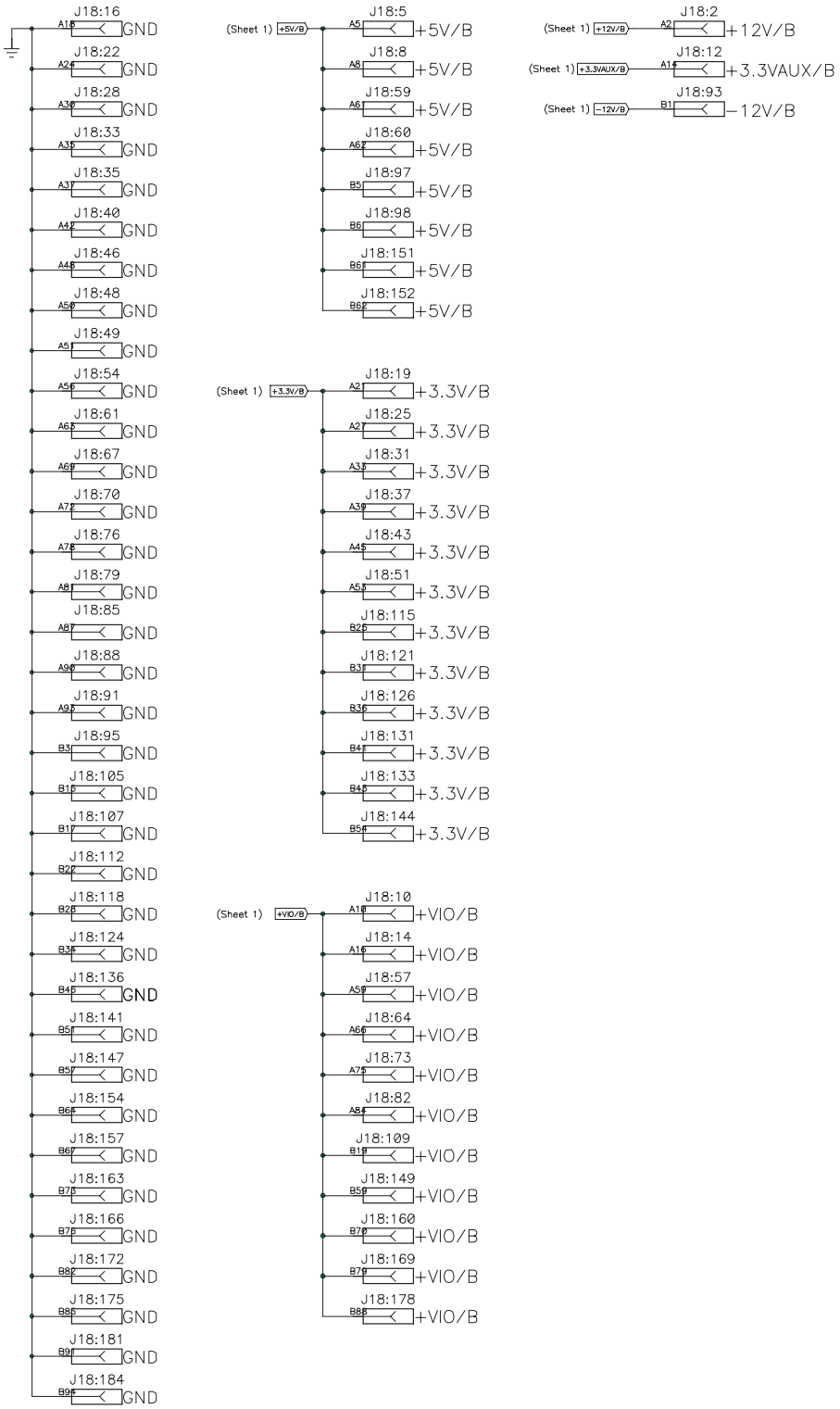


Figure 7. Slot B

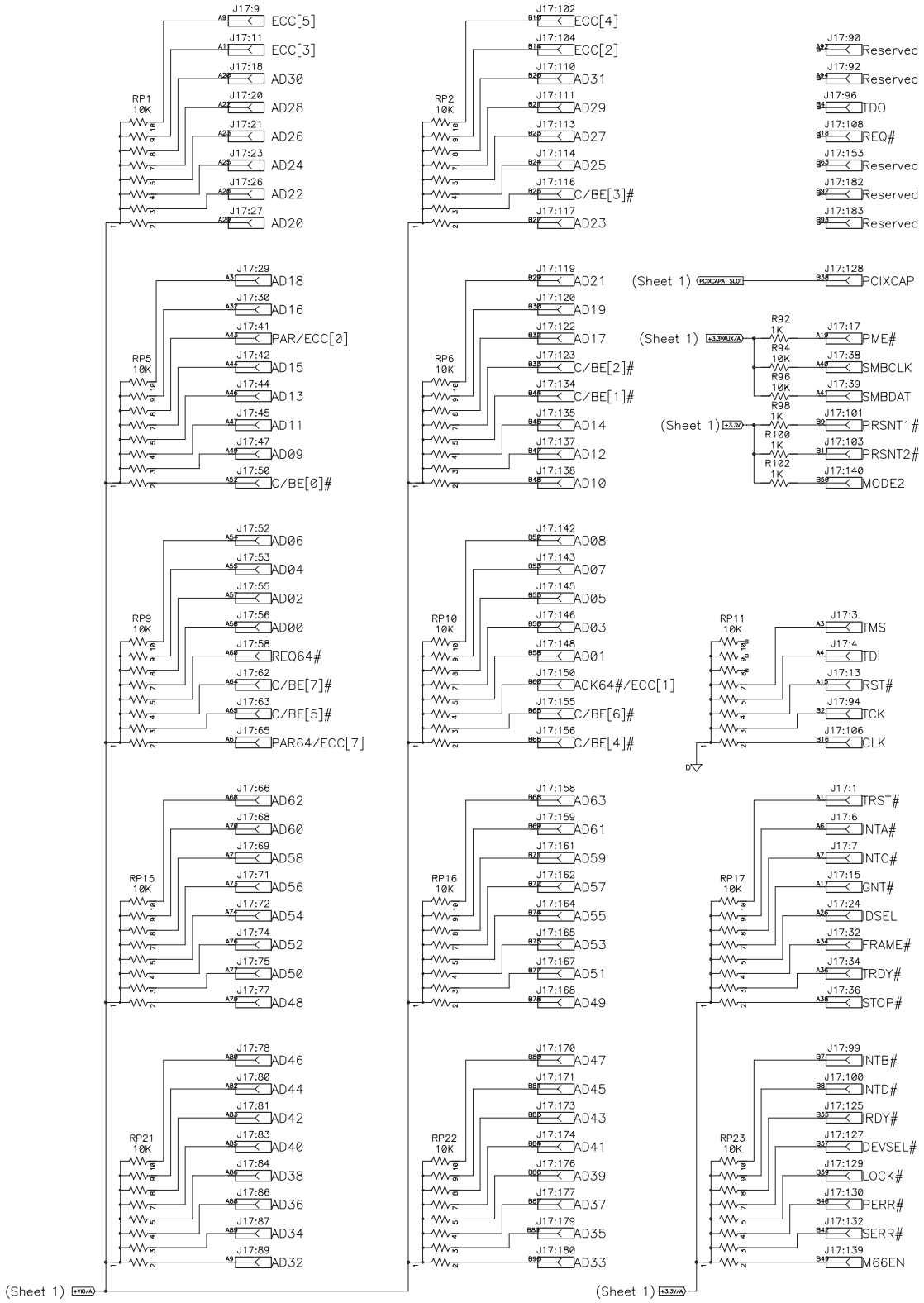


Figure 8. Slot A

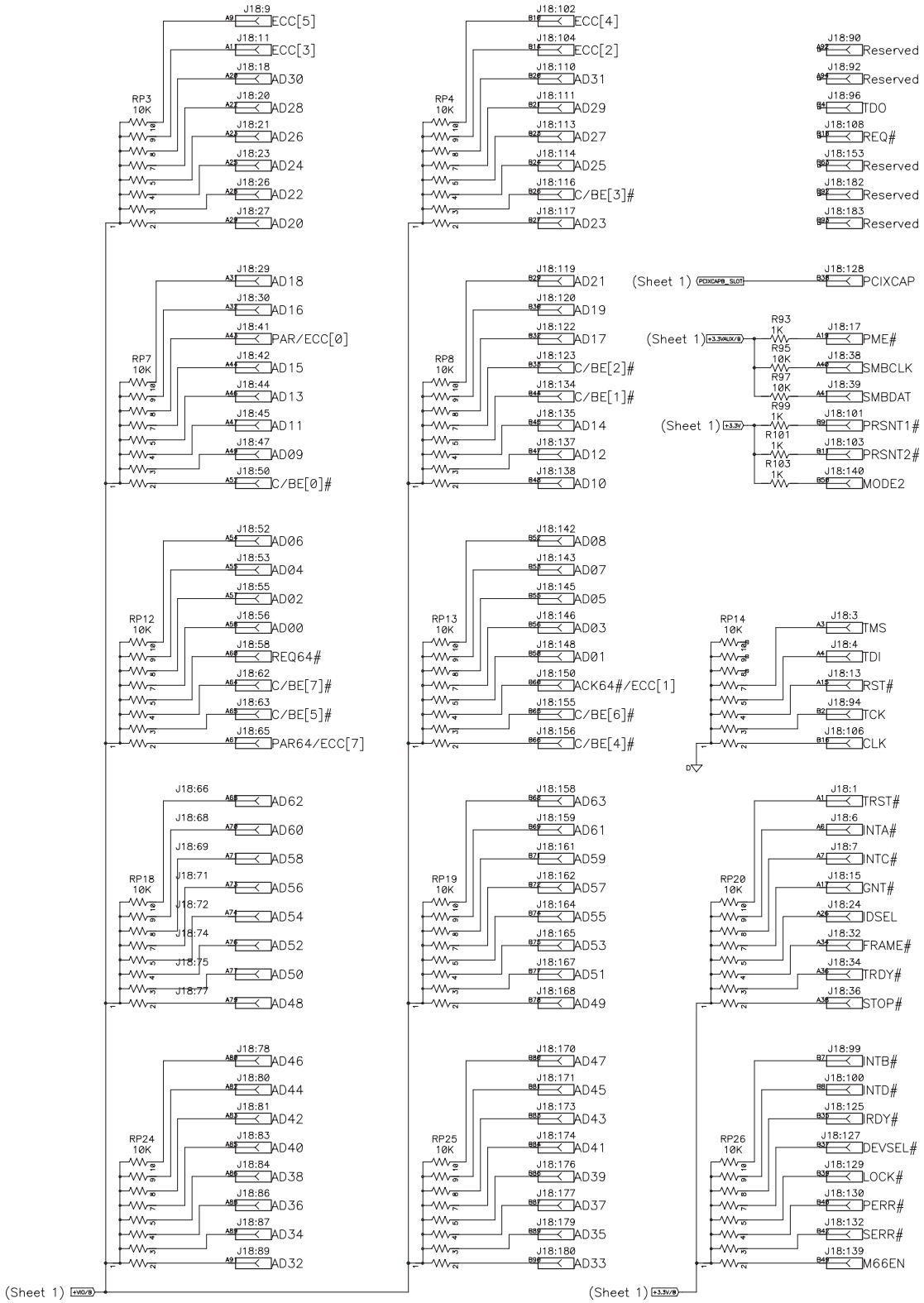


Figure 9. Slot B

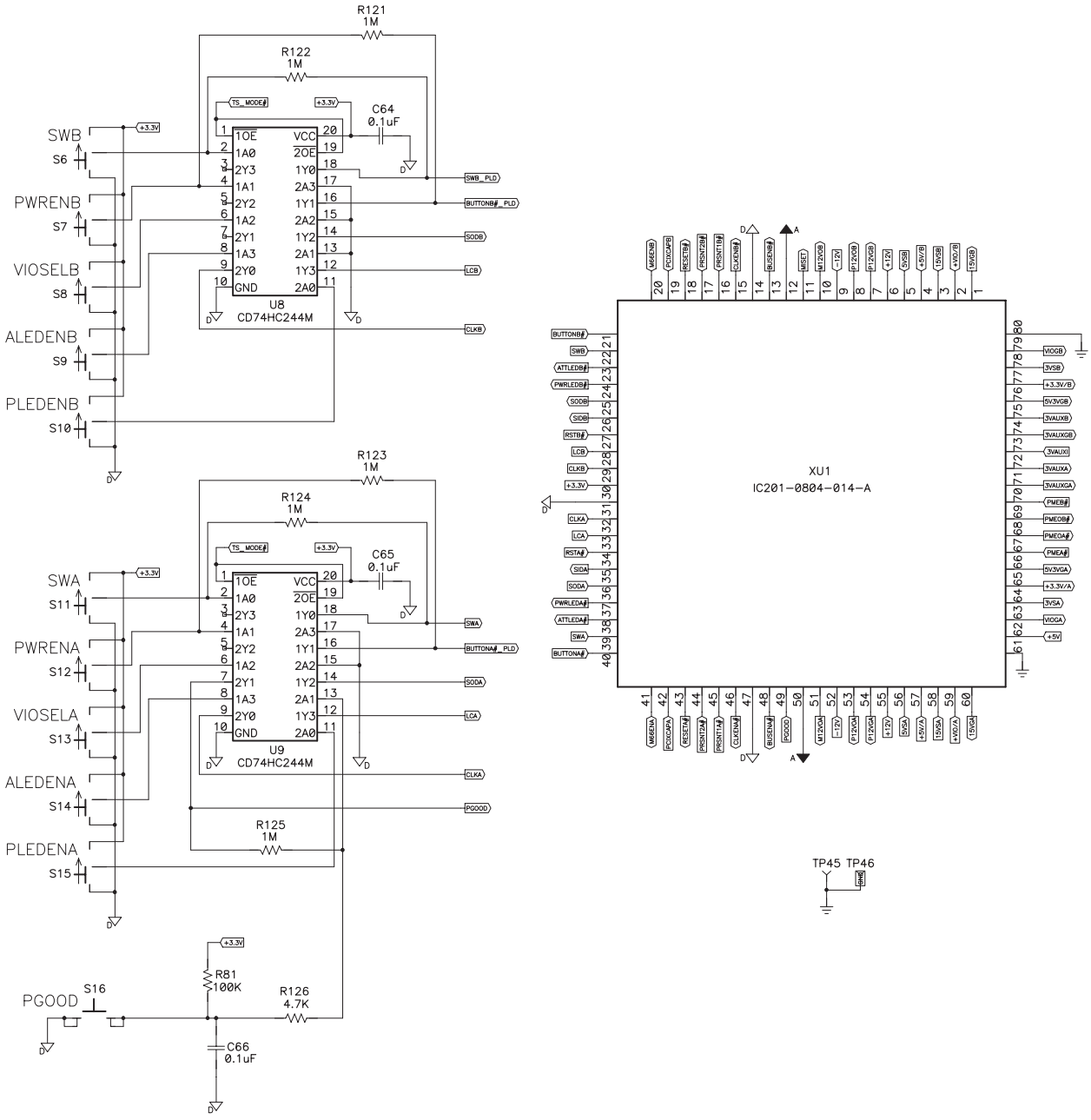

R121
1M
R122
1M
C64
0.1uF
U8
CD74HC244M
SWB
PWRENB
VIOSELB
ALEDENB
PLEDENB
S6
S7
S8
S9
S10
R123
1M
R124
1M
C65
0.1uF
U9
CD74HC244M
SWA
PWRENA
VIOSELA
ALEDENA
PLEDENA
S11
S12
S13
S14
S15
R125
1M
R81
100K
R126
4.7K
C66
0.1uF
PGOOD
S16
XU1
IC201-0804-014-A
TP45 TP46

Figure 10.

21.2 Demo Board Top Assembly

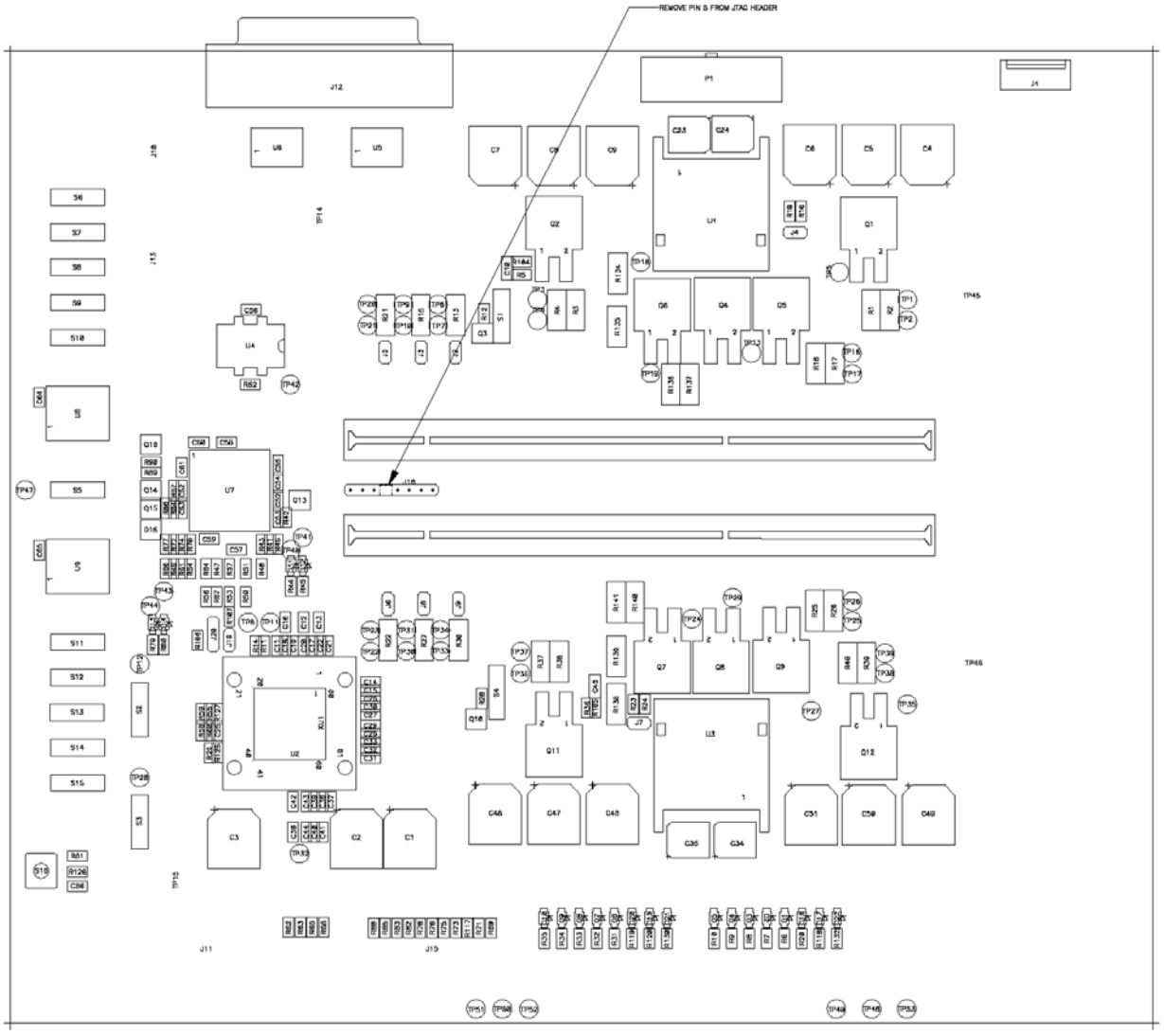


Figure 11. Top Assembly

21.3 Demo Board

Table 11. PR164 List of Materials

Reference Designator	Count	Description	MFR	Part Number
C1, C4, C5, C6, C7, C8, C9, C46, C47, C48, C49, C50, C51	13	Capacitor, aluminum, 1000 µF, 20%, 6.3 V, FC series, G case	Panasonic	EEV−FC0J102P
C10, C45	2	Capacitor, ceramic, 0.27 µF, 16 V, X7R, 10%, 1206	Panasonic	ECJ−3VB1C274K
C11, C19, C20, C25, C27, C31, C42, C43, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66	23	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 10%, 805	Panasonic	ECJ−2YB1H104K
C12, C13, C14, C15, C17, C18, C21, C22, C26, C28, C29, C30, C32, C33, C36, C37, C38, C39, C40, C41	20	Capacitor, ceramic, 0.01 µF, 50 V, X7R, 10%, 805	Panasonic	ECU−V1H103KBG
C16, C44	2	Capacitor, ceramic, 0.033 µF, 50 V, X7R, 10%, 805	Panasonic	ECJ−2VB1H333K
C2, C3	2	Capacitor, aluminum, 470 µF, 20%, 16 V, FC series, G case	Panasonic	EEV−FC1C471P
C23, C24, C34, C35	4	Capacitor, aluminum, 100 µF, 20%, 6.3 V, FC Series, D case	Panasonic	EEV−FC0J101P
D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D17, D18, D19, D20, D21, D22	20	Diode, LED, green, 20 mA, 0.9 mcd, 0.068 x 0.049	Panasonic	LN1371G−(TR)
D15, D16	2	Diode, schottky, 200 mA, 30 V, SOT23	Vishay−Liteon	BAT54
J1	1	Connector, header, vertical, 6 pin with lock, 0.600 x 0.250	Molex	22−23−2061
J10, J13, J16	3	Header, 8 pin, 100-mil spacing, (36-pin strip), 0.100 x 8”	Sullins	SAAN
J11	1	Header, 1 pin, 100-mil spacing, (36-pin strip), 0.100 x 14	Sullins	PTC36SAAN
J12	1	Connector, D sub, 25-pin male, right angle, 2.088 x 0.500”	Norcomp	182−025−112−531
J15	1	Header, 12 pin, 100-mil spacing, (36-pin strip), 0.100 x 12”	Sullins	PTC36SAAN
J17, J18	2	Coonector, PCI card, 64 bit, 188 pin, 3.3 V, 5.040 x 0.355”	Framatone	CEE2X92SCV53Z14W
J19	1	Header, 2 pin, 100-mil spacing, (36-pin strip), 0.100 x 2	Sullins	PTC36SAAN
J2, J3, J4, J5, J6, J7, J8, J9	8	Header, 2 pin, 100-mil spacing, (36-pin strip), 0.100 x 2”	Sullins	PTC36SAAN
J20	1	Header, 3 pin, 100-mil spacing, (36-pin strip), 0.100 x 3	Sullins	PTC36SAAN
P1	1	Connector, header, 14 pin, dual row, vertical, 1.200 x 0.378	Molex	39−28−1143

Reference Designator	Count	Description	MFR	Part Number
Q1, Q2, Q4, Q5, Q6, Q7, Q8, Q9, Q11, Q12	10	MOSFET, N-channel, 20 V, 174 A, 4 mΩ, SMD−220	International Rectifier	IRF1302S
Q13, Q15, Q16	3	MOSFET, N-channel, 50V, 0.17A, 3.5 Ω, SOT23	Zetex	BSS138
Q14	1	Bipolar, PNP, 40 V, 200 mA, 225 mW, SOT23	On Semi	MMBT3906LT1
Q3, Q10	2	MOSFET, P−ch, 60 V, 90 mA, 14 Ω, SOT23	Zetex	ZVP3306F
R1, R2, R3, R4, R17, R18, R25, R26, R37, R38, R39, R40	12	Resistor, chip, 12 mΩ, 1 W, 1%, 2512	Panasonic	ERJ−M1WSF12MU
R104, R105	2	Resistor, chip, 2.21 kΩ, 1/10 W, 1%, 805	Std	Std
R11	1	Resistor, chip, 6.04 kΩ, 1/10 W, 1%, 805	Std	Std
R12, R28	2	Resistor, chip, 475 kΩ, 1/10 W, 1%, 805	Std	Std
R121, R122, R123, R124, R125	5	Resistor, chip, 1 M, 1/10 W, 1%, 805	Std	Std
R127, R128, R131, R133	4	Resistor, chip, TBD Ω, 1/10 W, 1%,805	Std	Std
R13, R15, R21, R22, R27, R30	6	Resistor, chip, 100 mΩ, 1 W, 1%, 2512	Panasonic	ERJ−L1WKF10CU
R134, R135, R136, R137, R138, R139, R140, R141	8	Resistor, chip, 0 Ω, 1 W, 2512	Vishay	CRCW2512000ZZ
R14, R29	2	Resistor, chip, 3.32 kΩ, 1/10 W, 1%, 805	Std	Std
R16, R23	2	Resistor, chip, 13.7 kΩ, 1/10 W, 1%, 805	Std	Std
R19, R24	2	Resistor, chip, 102 kΩ, 1/10 W, 1%, 805	Std	Std
R41, R42, R74, R77, R89, R94, R95, R96, R97, R106, R107	11	Resistor, chip, 10 kΩ, 1/10 W, 1%, 805	Std	Std
R43, R72	2	Resistor, chip, 3.16 kΩ, 1/10 W, 1%, 805	Std	Std
R46, R70	2	Resistor, chip, 1.02 kΩ, 1/10 W, 1%, 805	Std	Std
R47, R49, R50, R51, R52, R53, R55, R56, R57, R58, R59, R60, R62, R63, R64, R65, R66, R67, R68, R69, R71, R73, R75, R76, R78, R82, R83, R85, R88, R112, R113, R114, R115, R117	34	Resistor, chip, 33 Ω, 1/10 W, 1%, 805	Std	Std
R48, R54, R61, R87, R91, R116, R126	7	Resistor, chip, 4.7 kΩ, 1/10 W, 5%, 805	Std	Std
R5, R36, R129	3	Resistor, chip, 0 Ω, 805	Std	Std

Reference Designator	Count	Description	MFR	Part Number
R6, R7, R8, R9, R10, R20, R31, R32, R33, R34, R35, R44, R45, R79, R80, R118, R119, R120, R130, R132	20	Resistor, chip, 130 Ω, 1/10 W, 1%, 805	Std	Std
R81	1	Resistor, chip, 100 kΩ, 1/10 W, 1%, 805	Std	Std
R84	1	Resistor, chip, 2 kΩ, 1/10 W, 1%, 805	Std	Std
R86	1	Resistor, chip, 20 kΩ, 1/10 W, 1%, 805	Std	Std
R90	1	Resistor, chip, 33.2 kΩ, 1/10 W, 1%, 805	Std	Std
R92, R93, R98, R99, R100, R101, R102, R103, R108, R109, R110, R111	12	Resistor, chip, 1 kΩ, 1/10 W, 1%, 805	Std	Std
RP1, RP2, RP3, RP4, RP5, RP6, RP7, RP8, RP9, RP10, RP11, RP12, RP13, RP14, RP15, RP16, RP17, RP18, RP19, RP20, RP21, RP22, RP23, RP24, RP25, RP26	26	Resistor pack, 10 kΩ, 62 mW, 5%, 8X, 0.083 x 0.158	Panasonic	EXB−E10C103J
S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, S13, S14, S15	15	Switch, SPDT, slide, PC mount, 500 mA, 0.400 x 0.100”	EAO	09−03201−02
S16	1	Switch, 1P1T, 20 mA, 15 V, 0.240 x 0.256	Panasonic	EVQPAD04M
SH1	1			
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40, TP41, TP42, TP43, TP44, TP47, TP48, TP49, TP50, TP51, TP52, TP53	49	Test point, O.062” hole, 0.25	Keystone	5012
TP14, TP15, TP45, TP46	4	Test point, SM, 0.150 x 0.090”, 0.185 x 0.135”	Keystone	5016
U1, U3	2	Module, dc-dc converter, 3.3 V/5 V, 1.5 V_{OUT}, 0.950 X 0.900	TI	PT5405A
U2	1	IC, PCI−X 2.0 dual slot power controller, PFP80	TI	TPS2342PFP
U4	1	IC, oscillator, 16.000 MHz, 5 V, 0.551 x 0.464”	Citizen	CMX309FLC16.000 MT
U5, U6	2	IC, 8-line unidirectional transorb, 5 V, SO16	Microsemi	SM16LC05
U7	1	IC, TQFP-128	Lattice	ISPLSI5256VE−HPQ1
U8, U9	2	Octal buffers/drivers with 3-state outputs, SOIC-20	TI	CD74HC244M
XU1	1	Socket, open top, 80 pin QFP, without center mounting hole, 1.14 x 1.14	Yamaichi	IC201−0804−014−A
−−	1	PCB, 8 in x 8.75 in x 0.062 I		Any
−	1	PR176B load board	TI	PR176B
	4	Rubber bumpers	SPC Technology	2567

Reference Designator	Count	Description	MFR	Part Number
Current-Sense Loop Assembly (6 per Demo Board)				
N/A	1	Terminal housing, 2 circuit N/A		Molex
N/A	2	Terminal, socket N/A		Molex
N/A		Wire, insulated	#22AWG	
N/A		Drawing, CBL001		
High-Power Cable Assembly (1 per Demo Board)				
N/A	1	Receptacle, housing	Mini–Fit Jr	14–ckt
N/A	14	Terminal, socket, copper plating, high current capable, #16 AWG, N/A	Molex	4476–3112
N/A	4	Spade lug	Voltrex	CSS–TO–1010–HT
N/A		Wire, insulated, green	Std	#16AWG
N/A		Wire, insulated, white	Std	#16AWG
N/A		Wire, insulated, black	Std	#16AWG
N/A		Tubing, heat shrinkable,flexible, 2:1 shrink ratio, 3/8 inch, diameter x 1 inch		Std
N/A		Drawing, CBL 002		
Low-Power Cable Assembly (1 per Demo Board)				
N/A	1	Terminal housing, locking ramp	6−ckt	N/A
N/A	6	Terminal, socket	tin/copperplating	#22AWG –#30AWG
N/A		Wire, insulated, black	Std	#22AWG
N/A		Wire, insulated, green	Std	#22AWG
N/A		Wire, insulated, orange	Std	#22AWG
N/A		Wire, insulated, red	Std	#22AWG
N/A		Tubing, heat shrinkable, flexible, 2:1 shrink ratio, 1/4 inch diameter x 1 inch		Std
N/A		Drawing CBL 003		Ref

NOTES: 1. These assemblies are ESD sensitive .ESD precautions shall be observed.
2 These assemblies must be clean and free from flux and all contaminants.
3 These assemblies must comply with workmanship standards IPC−A−610 Class 2.
4 Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

22 Appendix B

22.1 Load Board

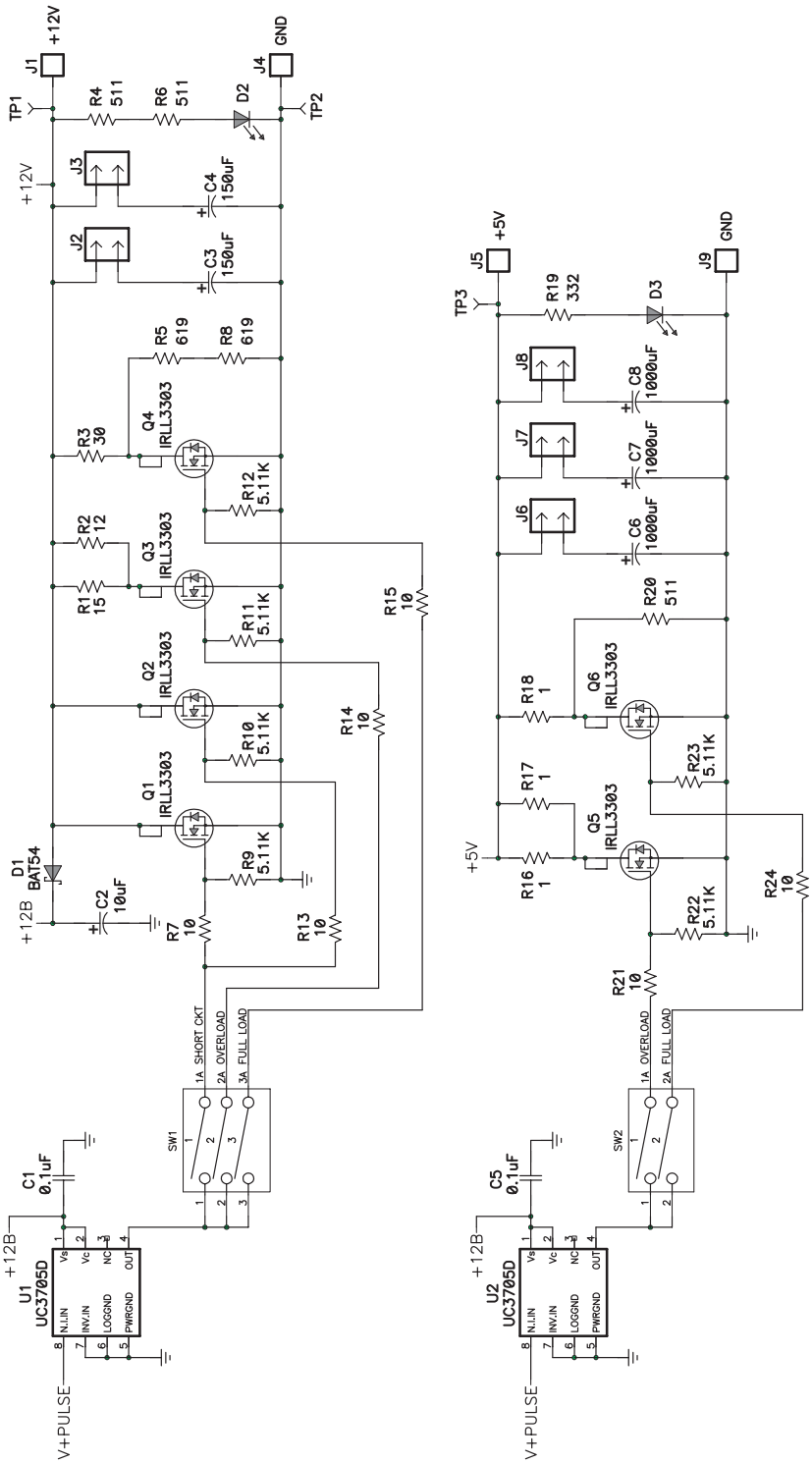


Figure 12.

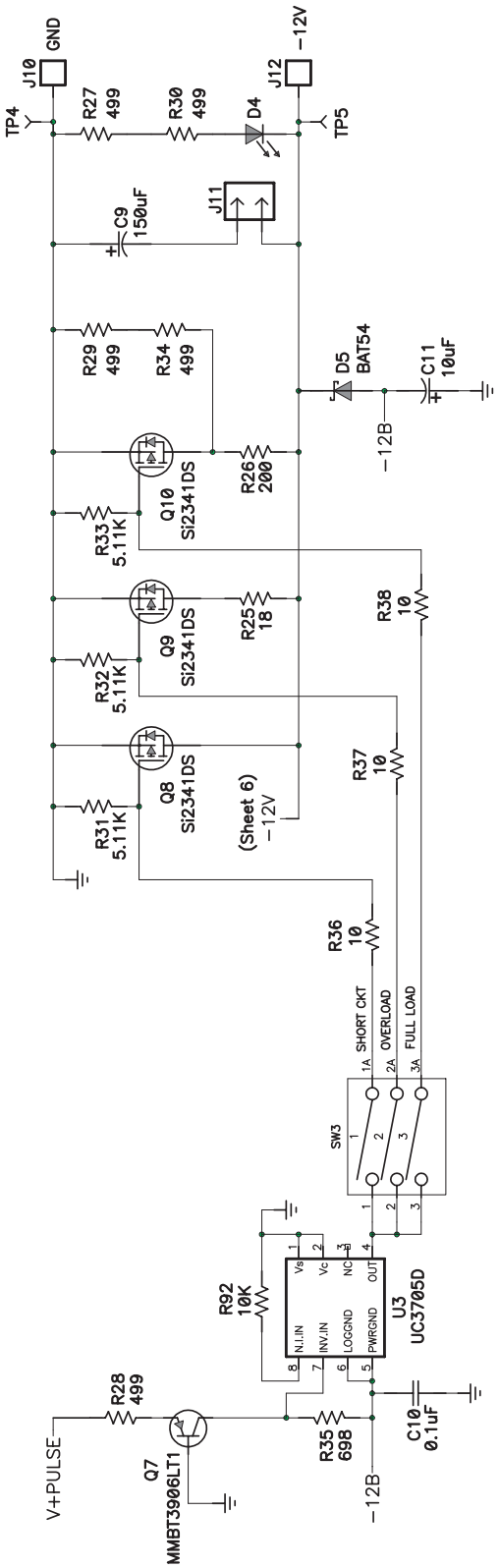

J10
GND
J12
-12V
TP4
TP5
R27
499
R30
499
D4
J11
C9
150uF
R29
499
R34
499
D5
BAT54
C11
10uF
-12B
R26
200
Q10
Si2341DS
R33
5.11K
R25
18
Q9
Si2341DS
R32
5.11K
R38
10
R37
10
Q8
Si2341DS
R31
5.11K
(Sheet 6)
-12V
R36
10
1A SHORT CKT
2A OVERLOAD
3A FULL LOAD
SW3
R92
10K
U3
UC3705D
N.I.IN
INV.IN
LOGGND
PWRGND
Vs
Vc
NC
OUT
R28
499
R35
698
C10
0.1uF
V+PULSE
Q7
MMBT3906LT1
-12B

Figure 13.

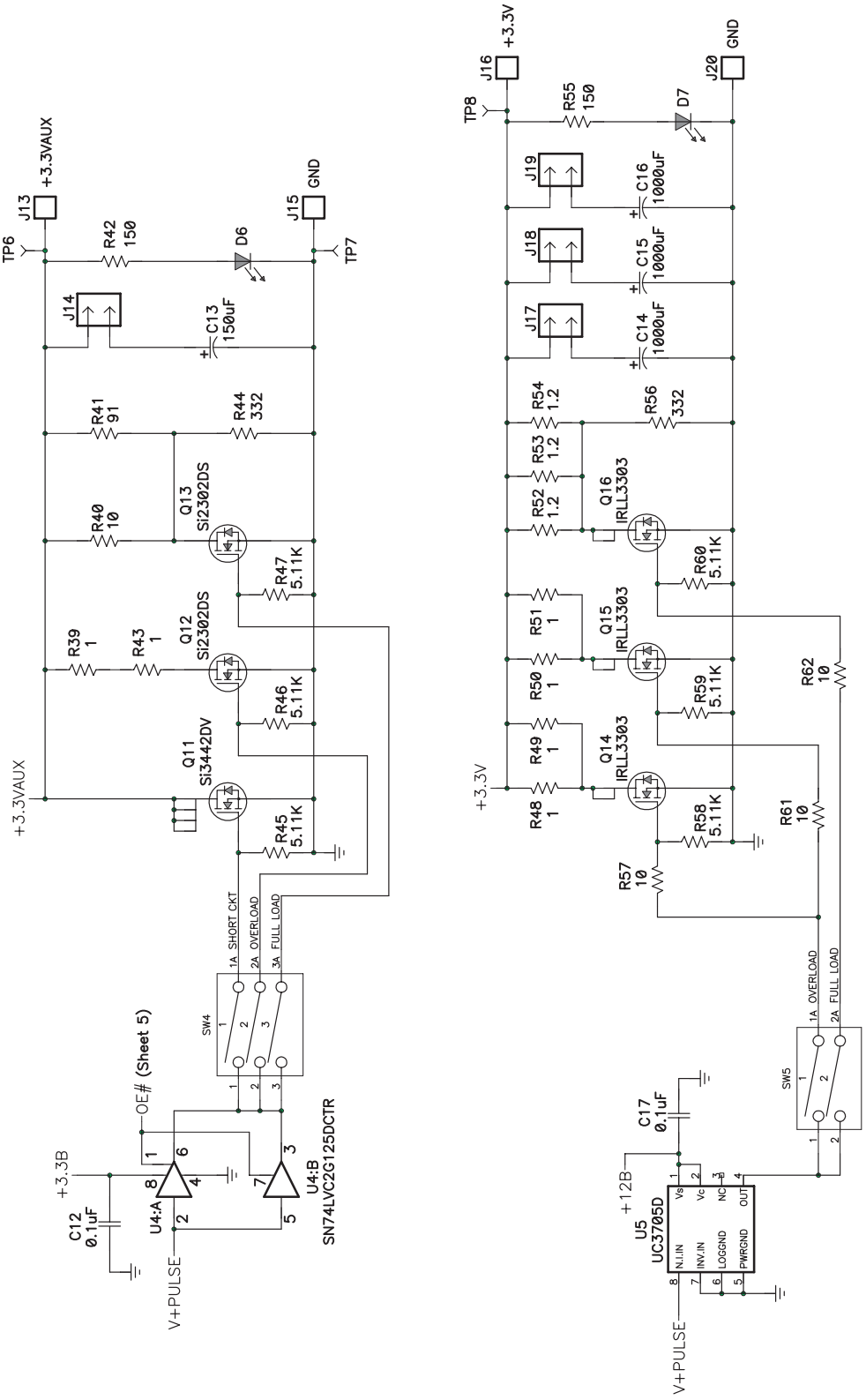

J13
+3.3VAUX
J15
GND
TP6
TP7
R42
150
D6
J14
C13
150uF
R41
91
R44
332
R40
10
Q13
Si2302DS
R47
5.11K
R39
1
R43
1
Q12
Si2302DS
R46
5.11K
Q11
Si3442DV
R45
5.11K
+3.3VAUX
1A SHORT CKT
2A OVERLOAD
3A FULL LOAD
SW4
OE# (Sheet 5)
+3.3B
C12
0.1uF
U4:A
U4:B
SN74LVC2G125DCTR
V+PULSE
J16
+3.3V
J20
GND
TP8
R55
150
D7
J19
C16
1000uF
J18
C15
1000uF
J17
C14
1000uF
R54
1.2
R56
332
R53
1.2
R52
1.2
Q16
IRLL3303
R60
5.11K
R51
1
Q15
IRLL3303
R59
5.11K
R62
10
R50
1
R49
1
Q14
IRLL3303
R48
1
R58
5.11K
R61
10
R57
10
+3.3V
1A OVERLOAD
2A FULL LOAD
SW5
C17
0.1uF
+12B
U5
UC3705D
N.I.IN
INV.IN
LOGGND
PWRGND
Vs
Vc
NC
OUT
V+PULSE

Figure 14.

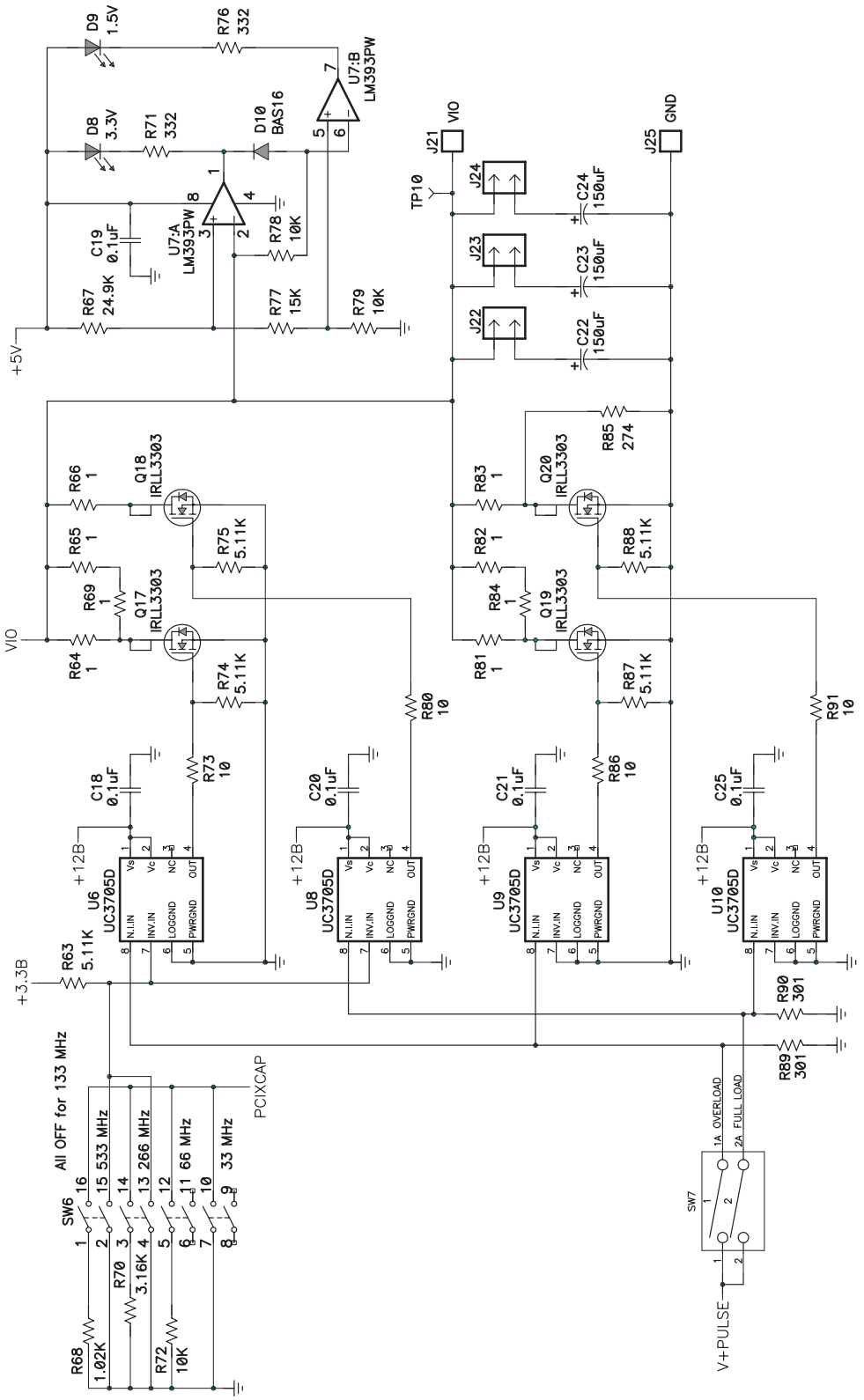

D9
1.5V
R76
332
D8
3.3V
R71
332
D10
BAS16
U7:B
LM393PW
U7:A
LM393PW
C19
0.1uF
R67
24.9K
R77
15K
R78
10K
R79
10K
+5V
J21
VIO
J25
GND
TP10
J24
J23
J22
C24
150uF
C23
150uF
C22
150uF
R85
274
R66
1
R65
1
R69
1
R64
1
Q18
IRLL3303
Q17
IRLL3303
R75
5.11K
R74
5.11K
R83
1
R82
1
R84
1
R81
1
Q20
IRLL3303
Q19
IRLL3303
R88
5.11K
R87
5.11K
VIO
R80
10
R73
10
R86
10
R91
10
C18
0.1uF
C20
0.1uF
C21
0.1uF
C25
0.1uF
+12B
U6
UC3705D
U8
UC3705D
U9
UC3705D
U10
UC3705D
N.I.IN
INV.IN
LOGGND
PWRGND
Vs
Vc
NC
OUT
R63
5.11K
+3.3B
R90
301
R89
301
All OFF for 133 MHz
SW6
15 533 MHz
13 266 MHz
11 66 MHz
9 33 MHz
R70
3.16K
R68
1.02K
R72
10K
PCIXCAP
SW7
1A OVERLOAD
2A FULL LOAD
V+PULSE

Figure 15.

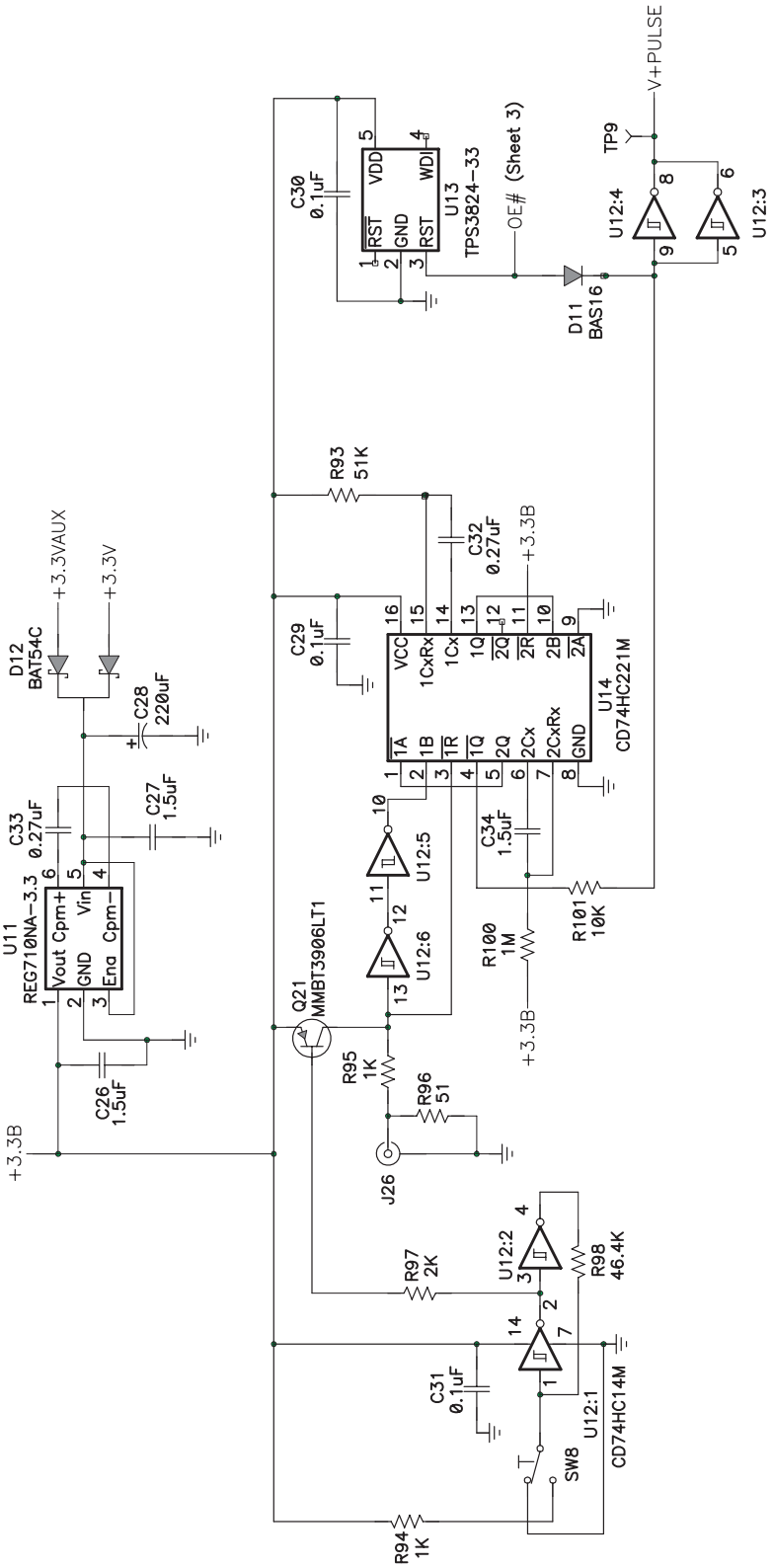
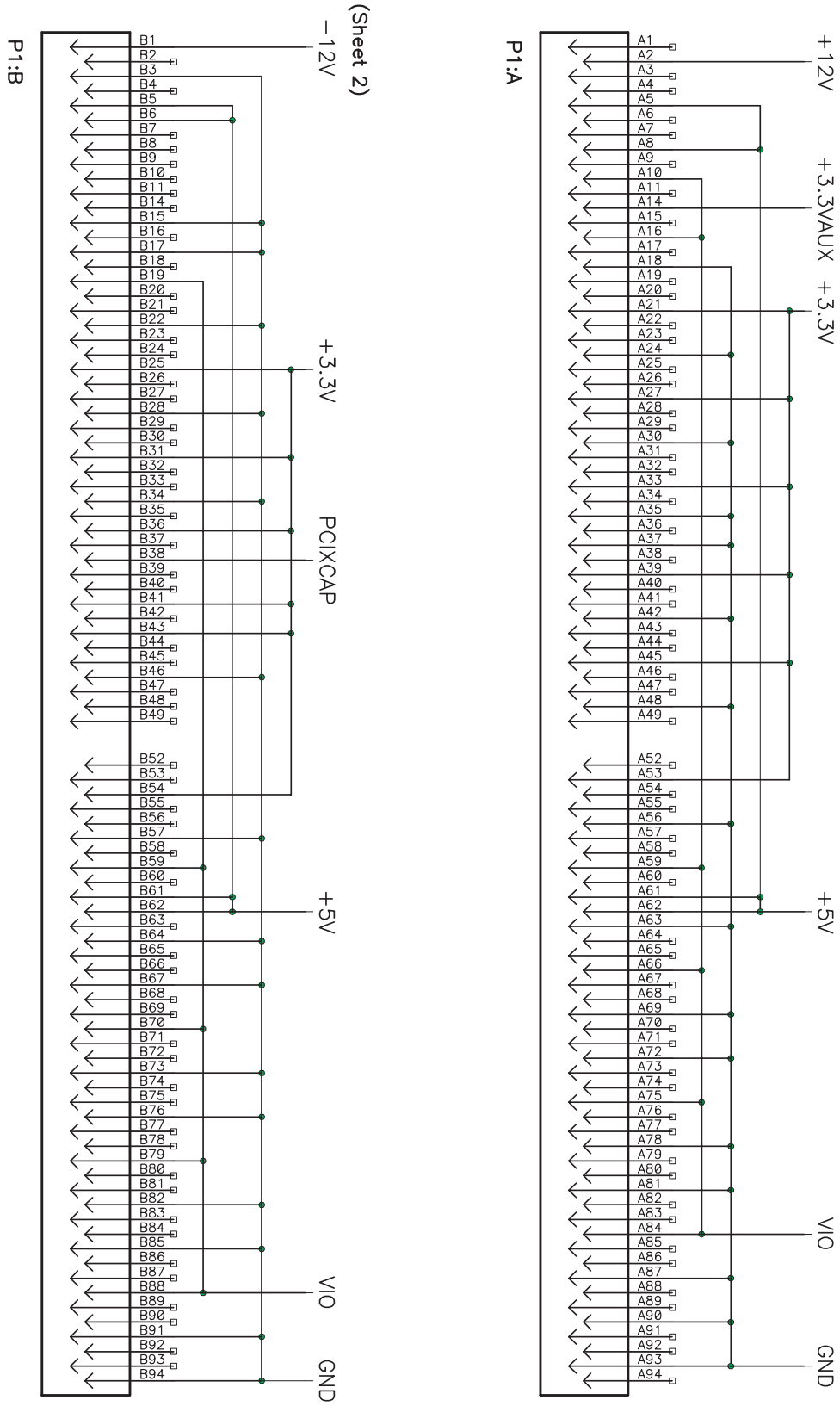

V+PULSE
TP9
U12:4
U12:3
C30
0.1uF
U13
TPS3824-33
VDD
WDI
RST
GND
RST
OE# (Sheet 3)
D11
BAS16
R93
51K
C32
0.27uF
+3.3B
C29
0.1uF
U14
CD74HC221M
VCC
1CxRx
1Cx
1Q
2Q
2R
2B
2A
1A
1B
1R
1Q
2Q
2Cx
2CxRx
GND
U12:5
U12:6
C34
1.5uF
R101
10K
R100
1M
+3.3B
Q21
MMBT3906LT1
R95
1K
R96
51
J26
+3.3VAUX
+3.3V
D12
BAT54C
C28
220uF
C27
1.5uF
C33
0.27uF
U11
REG710NA-3.3
Vout Cpm+
Vin
GND
Ena
Cpm-
C26
1.5uF
+3.3B
U12:2
R97
2K
R98
46.4K
C31
0.1uF
U12:1
CD74HC14M
SW8
R94
1K

Figure 16.


P1:B
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B14
B15
B16
B17
B18
B19
B20
B21
B22
B23
B24
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B32
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B37
B38
B39
B40
B41
B42
B43
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B79
B80
B81
B82
B83
B84
B85
B86
B87
B88
B89
B90
B91
B92
B93
B94
(Sheet 2)
– 12V
+3.3V
PCIXCAP
+5V
VIO
GND
P1:A
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A14
A15
A16
A17
A18
A19
A20
A21
A22
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A73
A74
A75
A76
A77
A78
A79
A80
A81
A82
A83
A84
A85
A86
A87
A88
A89
A90
A91
A92
A93
A94
+12V
+3.3VAUX
+3.3V
+5V
VIO
GND

Figure 17.

22.2 Load Board Top Assembly

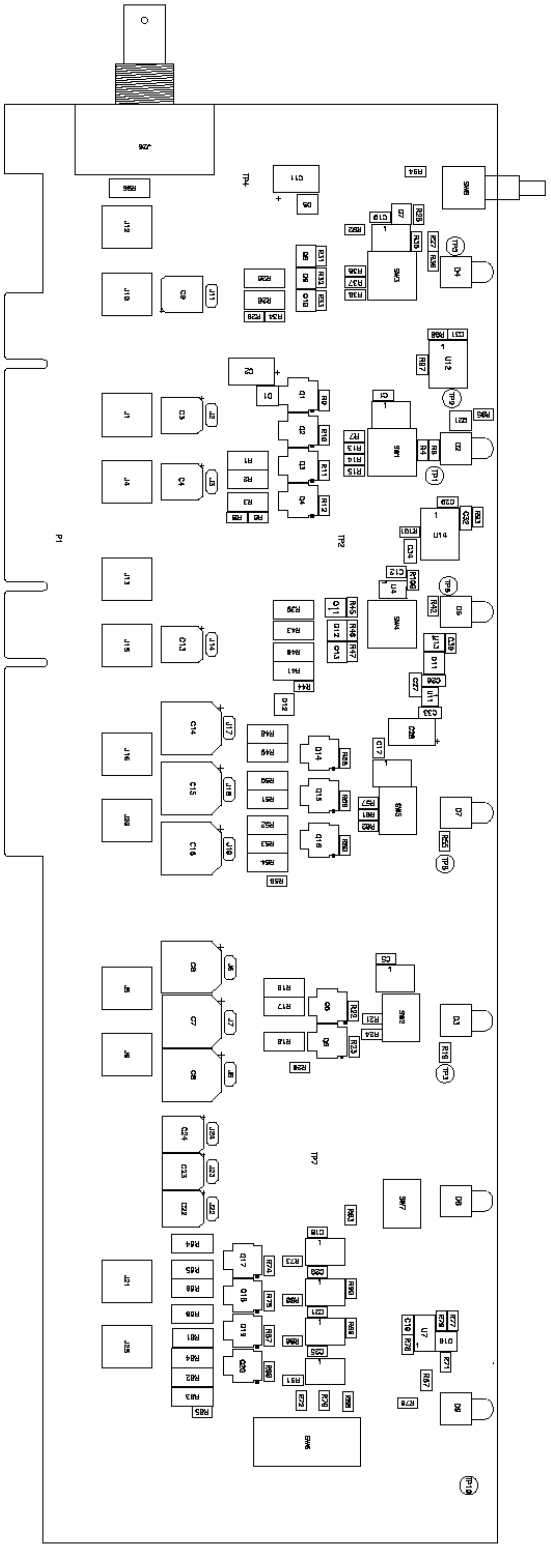

Figure 18. Top Assembly

22.3 Load Board

Table 12. PR176 List of Materials

Reference Designator	Count	Description	MFR	Part Number
C1, C5, C10, C12, C17, C18, C19, C20, C21, C25, C29, C30, C31	13	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 10%, 805	Panasonic	ECJ−2YB1H104K
C2, C11, C28	3	Capacitor, tantalum, 10 µF, 35 V, 20%, 7343 (D)	Panasonic	ECS−T1VD106R
C26, C27, C34	3	Capacitor, ceramic, 1.5 µF, 16 V, X7R, 10%, 1206	Panasonic	ECJ−3YB1C155K
C3, C4, C9, C13, C22, C23, C24	7	Capacitor, aluminum, 150 µF, 16 V, 20%, FK series, 0.268 x 0.307 (D case)	Panasonic	EEV−FK1C151XP
C32	1	Capacitor, ceramic, 0.015 µF, 50 V, X7R, 10%, 1206	Kemet	C1206C153K5RACTU
C33	1	Capacitor, ceramic, 0.27 µF, 16 V, X7R, 10%, 1206	Panasonic	ECJ−3VB1C274K
C6, C7, C8, C14, C15, C16	6	Capacitor, aluminum, SM, 1000 µF, 6.3 V, 150 mΩ, FC series, 10x12mm (G case)	Panasonic	EEV−FC0J102P
D1, D5	2	Diode, schottky, 200 mA, 30 V, SOT23	Vishay−Liteon	BAT54
D10, D11	2	Diode, switching, 10 mA, 85 V, 350 mW, SOT23	Vishay−Liteon	BAS16
D12	1	Diode, dual schottky, 200 mA, 30 V, SOT23	Vishay−Liteon	BAT54C
D2, D3, D4, D6, D7, D8, D9	7	Diode. LED, red, 2.1 V, 10 mA to 25 mA, 0.250 x 0.250”	Lumex	SSF−LXH101ID−01
J1, J4, J5, J9, J10, J12, J13, J15, J16, J20, J21, J25	12	Screw terminal, 0.310 x 0.310	Keystone	7693
J2, J3, J6, J7, J8, J11, J14, J17, J18, J19, J22, J23, J24	13	Header, 2 pin, 100-mil spacing, (36-pin strip), 0.100 x 2”	Sullins	PTC36SAAN
J26	1	Connector, right angle BNC, PCB mount, 1.15 x 0.56	AMP	226978−1
Q1, Q2, Q3, Q4, Q5, Q6, Q14, Q15, Q16, Q17, Q18, Q19, Q20	13	MOSFET, N-channel, 30 V, 4.6 A, 31 mΩ, SOT223	International Rectifier	IRLL3303
Q11	1	MOSFET, N-channel, 20 V, 4 A, 70 mΩ, TSOP−6	Vishay	Si3442DV
Q12, Q13	2	MOSFET, N-channel, 20 V, 2.8 A, 85 mΩ, SOT23	Vishay	Si2302DS
Q7, Q21	2	Bipolar, PNP, 40 V, 200 mA, 225 mW, SOT23	On Semi	MMBT3906LT1
Q8, Q9, Q10	3	MOSFET, P-channel, 30 V, 2.8 A, 72 mΩ, SOT23	Vishay	Si2341DS
R1	1	Resistor, chip, 15 Ω, 1 W, 5%, 2512	Vishay	CRCW2512−150J
R100	1	Resistor, chip, 1 MΩ, 1/10 W, 1%, 805	Std	Std
R16, R17, R18, R39, R43, R48, R49, R50, R51, R64, R65, R66, R69, R81, R82, R83, R84	17	Resistor, chip, 1 Ω, 1 W, 5%, 2512	Vishay	CRCW2512−1R0J
R19, R44, R56, R71, R76	5	Resistor, chip, 332 Ω, 1/10 W, 1%, 805	Std	Std
R2	1	Resistor, chip, 12 Ω, 1 W, 5%, 2512	Vishay	CRCW2512−120J
R25	1	Resistor, chip, 18 Ω, 1 W, 5%, 2512	Vishay	CRCW2512−180J
R26	1	Resistor, chip, 200 Ω, 1 W, 5%, 2512	Vishay	CRCW2512−201J
R27, R28, R29, R30, R34	5	Resistor, chip, 499 Ω, 1/10 W, 1%, 805	Std	Std
R3	1	Resistor, chip, 30 Ω, 1 W, 5%, 2512	Vishay	CRCW2512−300J
R35	1	Resistor, chip, 698 Ω, 1/10 W, 1%, 805	Std	Std
R4, R6, R20	3	Resistor, chip, 511 Ω, 1/10 W, 1%, 805	Std	Std
R40	1	Resistor, chip, 10 Ω, 1 W, 5%, 2512	Vishay	CRCW2512−100J

Reference Designator	Count	Description	MFR	Part Number
R41	1	Resistor, chip, 91 Ω, 1 W, 5%, 2512	Vishay	CRCW2512−910J
R42, R55	2	Resistor, chip, 150 Ω, 1/10 W, 1%, 805	Std	Std
R5, R8	2	Resistor, chip, 619 Ω, 1/10 W, 1%, 805	Std	Std
R52, R53, R54	3	Resistor, chip, 1.2 Ω, 1 W, 5%, 2512	Vishay	CRCW2512−1R2J
R67	1	Resistor, chip, 24.9 kΩ, 1/10 W, 1%, 805	Std	Std
R68	1	Resistor, chip, 1.02 kΩ, 1/10 W, 1%, 805	Std	Std
R7, R13, R14, R15, R21, R24, R36, R37, R38, R57, R61, R62, R73, R80, R86, R91	16	Resistor, chip, 10 Ω, 1/10 W, 1%, 805	Std	Std
R70	1	Resistor, chip, 3.16 kΩ, 1/10 W, 1%, 805	Std	Std
R72, R78, R79, R92, R93, R101	6	Resistor, chip, 10 kΩ, 1/10 W, 1%, 805	Std	Std
R77	1	Resistor, chip, 15 kΩ, 1/10 W, 1%, 805	Std	Std
R85	1	Resistor, chip, 274 Ω, 1/10 W, 1%, 805	Std	Std
R89, R90	2	Resistor, chip, 301 Ω, 1/10 W, 1%, 805	Std	Std
R9, R10, R11, R12, R22, R23, R31, R32, R33, R45, R46, R47, R58, R59, R60, R63, R74, R75, R87, R88	20	Resistor, chip, 5.11 kΩ, 1/10 W, 1%, 805	Std	Std
R94, R95	2	Resistor, chip, 1 kΩ 1/10 W, 1%, 805	Std	Std
R96	1	Resistor, chip, 51 Ω, 1 W, 5%, 2512	Vishay	CRCW2512−510J
R97	1	Resistor, chip, 2 kΩ, 1/10 W, 1%, 805	Std	Std
R98	1	Resistor, chip, 46.4 kΩ, 1/10 W, 1%, 805	Std	Std
SW1, SW3, SW4	3	SWITCH, 3 POS, SPST, DIP6, 0.380 * 0.385”	CTS	206−3
SW2, SW5, SW7	3	Switch, low profile 2 POS, SPST, 0.280 * 0.380	CTS	206−2
SW6	1	Switch, DPST, 4 position, 0.385 x 0.886	CTS	206−214
SW8	1	Switch, SPDT, pushbutton, momentary, 400 mA, 0.270 x 0.800	C & K	8121SD9AV2GE
TP1, TP3, TP5, TP6, TP8, TP9, TP10	7	Test point, O.062 hole, 0.25	Keystone	5012
TP2, TP4, TP7	3	Test point, SM, 0.150 x 0.090”, 0.185 x 0.135”	Keystone	5016
U1, U2, U3, U5, U6, U8, U9, U10	8	IC, high speed power driver, SO8	TI	UC3705D
U11	1	IC, switched cap, buck boost converter 1.8 V to 5.5 V in 65 μA, SOT23−6	TI	REG710NA−3.3
U12	1	IC, high-speed CMOS logic hex inverting schmitt trigger, SO14	TI	CD74HC14M
U13	1	IC, voltage supervisor, SOT23−5	TI	TPS3824−33QDBVRQ1
U14	1	IC, high-speed CMOS dual monostable multivibrator with reset, SO16	TI	CD74HC221M
U4	1	IC, dual buffer/driver with 3 state outputs, SSOP8	TI	SN74LVC2G125DCTR
U7	1	IC, dual differential comparators, 2 to 36 V_{IN}, TSSOP−8 (PW)	TI	LM393PW
−−	1	PCB, 12.25 in x 4.25 in x 0.062 in	Any	PR176B

NOTES: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3 These assemblies must comply with workmanship standards IPC−A−610 Class 2.
4 Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

23 Appendix C − TPS2342 vs TPS2340A Programming – Serial Mode

23.1 SBI2 Protocol

The hot-plug controller controls its slots and gathers status from them using a proprietary hot-plug serial bus interface (SBI2). The power controller is strictly a slave device that responds to commands issued by the hot-plug controller. Typically, the power controllers are located near the hot-plug slots. This architecture is employed to reduce the amount of signal routing between the slot and the hot-plug controller and significantly reduce pin-count impact of embedding the hot-plug controller in a bridge device, thereby reducing the cost burden of bridge customers that are not interested in PCI hot-plug functionality.

Serial data signal connections between the hot-plug and power controllers are point-to-point. The interface uses a dedicated input and output signal so no turnaround cycles are required and timing margin and loading issues are minimized. All serial data is synchronous with a common low-frequency clock. The output serial bit stream (from the hot-plug controller) consists of a command packet followed by one of more data packets for output commands. Input command packets are not followed by data packets. The power controller responds to input command by sending back-to-back 8-bit data packets. Input and output serial data packets are sent in slot order starting with the slot that is electrically closest to the hot-plug controller. There is a fixed delay of 2 clocks from the end of the command packet until the hot−plug controller receives the first bit of data. SBI2 is low frequency and is intended to service slots that are a short distance (less than 1 meter) from the hot-plug controller and does not support any error checking or error recovery mechanisms.

23.2 Hot-Plug Control Serial Bus I/F Signaling

SBI2 is used to collect status and control the slots. The SBI2 bus consists of five pins: **CLK**, **SID**, **SOD**, **LC** and $\overline{\textbf{RST}}$. When the power controller is in single-slot serial mode, two SBI2 interfaces are supported so that slots A and B are interfaced to separate hot-plug controllers. Descriptions of these pins may be found in Section 16−5. The letter “A” or “B” is appended to the pin name above to designate the slot they are associated with.

The SBI2 clock (**CLK**) frequency is typically derived from the hot-plug controller core clock and must not exceed F_{CLK}. The latch clock (**LC)** is typically synchronized to the PCI clock domain of the PCI bus that is occupied by the hot-plug slot. This signal is normally high and pulses low for no less than T_{LCPW}. **SOD** (power controller input) is valid T_{SUSOD} before the rising or falling edge of **CLK** and remains valid for T_{HSOD} after the rising edge of **CLK**. The **SID** signal is a power controller output that is an input to the hot-plug controller or an upstream power controller and must be valid within T_{COCLK} after the rising edge of **CLK** (the values can be found in the TPS2342 datasheet logic switching table).

23.3 SBI2 Serial Input and Output Commands

The hot-plug controller controls the slots using output commands and collects status using input commands. Serialized commands are sent on the **SOD** signal synchronous to **CLK**. Command packets consist of a start bit, a 4-bit command and end bit. Start bits are one clock period wide and are unique patterns that are sampled low on the falling edge of **CLK** and sampled high on the rising edge of **CLK**. All other bits within the command and data packets only change once within a **CLK** period. The 4-bit command follows the start bit and is transmitted least significant bit (lsb) first. The end bit follows the 4-bit command field and is always high. The hot-plug controller sends one or more 8-bit data packets following the end bit when the command is an output. When the command is an input, **SOD** returns to the idle (high) state until the input data has been received via the **SID** signal.

23.3.1 Serial Input Commands

Table 12 and 13 shows the command patterns of the SBI2 input commands. Typically, hot-plug controllers poll interrupt capable and non-interrupt capable inputs continuously by alternately sending the associated commands to the power controller(s). Diagnostic data commands are sent in order to verify that an output command has been executed successfully or to determine the quantity, mode, and revision level of power controllers present on the hot-plug bus segment.

Table 13. SBI Input Commands TPS2340A

Channel Address	Functional Channel Group
00	Interrupt capable inputs
01	Non–interrupt capable inputs
10	Diagnostic data #1
11	Diagnostic data #2

Table 14. SBI2 Input Commands TPS2342

Command Word msb lsb	Command Type
0000	Interrupt capable inputs
0010	Non−interrupt capable inputs
0100	Diagnostic data #1
0110	Diagnostic data #2

NOTES:All other command bit permutations not defined by this table or by Table 1−7 are Reserved.

The following diagrams illustrate SBI2 input command signaling assuming that the power controllers are in multi-slot mode. Figure 31 shows the interrupt and non-interrupt capable input commands and Figure 32 shows the diagnostic commands. In all cases, the duration (number of **CLKs** expended) of the command is a function of the number of slots supported by the platform. The **SODOB** signal is used to retransmit the command to downstream power controllers over the point-to-point serial interface. There is a 2-clock period data latency associated with each slot. Data packets are pipelined so that the hot-plug controller only sees the initial 2-bit latency associated with the first slot.

23.3.2 Interrupt Capable Input Data Packets

Table 14 and 15 indicates the serial bit order for interrupt-capable inputs. When the power controller is in multislot serial mode, the eight-bit packets associated with slots A, B, etc are referred to as packets A, B etc. Packet A signals (bit names ending in A) are associated with slot A of the power controller electrically closest to the hot-plug controller. Packet B bits are associated with slot B. When more than one power controller is used, additional 8-bit data packets (packet C and so on) are appended behind packet B in power controller slot A−B order.

The polarities of the SWITCH and BUTTON packet bits appear in the table as high true and the switch is open when asserted. The SWITCH packet bits are zero when the **SWA/B** pin is low and the switch is closed, indicating that the card is installed and ready for use. The BUTTON bits are one when the **$\overline{\text{BUTTONA/B}}$** pin is low and the momentary button is being pushed. The $\overline{\text{FAULT}}$ bits are zero when either a main or auxiliary fault is present on the associated slot. The $\overline{\text{PRSNT2}}$ and $\overline{\text{PRSNT1}}$ bits are zero when the associated **$\overline{\text{PRSNT2A/B}}$** or **$\overline{\text{PRSNT1A/B}}$** pin at the slot is low.

Table 15. TPS2340A. Channel 00 Data Group – Interrupt Capable Inputs

Bit Number	Function
0	Slot A SW (1 = interlock A open)
1	Slot A button state (1 = button A pushed)
2	Slot A power fault state (PwrfltA & AuxfltA)
3	Slot A PRSNT2
4	Slot A PRSNT1
5	Reserved
6	Reserved
7	Reserved
8	Slot B SW
9	Slot B button state
10	Slot B power fault state (PwrfltB & AuxfltB)
11	Slot B PRSNT2
12	Slot B PRSNT1
13	Reserved
14	Reserved
15	Reserved
16…47	SIDI pin data for slots C, D, E and F follows

Table 16. TPS2342 Interrupt Capable Inputs Serial Bit Order

Bit	Bit Name	Bit	Bit Name
0	SWITCHA	8	SWITCHB
1	BUTTONA	9	BUTTONB
2	$\overline{\text{FAULTA}}$	10	$\overline{\text{FAULTB}}$
3	$\overline{\text{PRSNT2A}}$	11	$\overline{\text{PRSNT2B}}$
4	$\overline{\text{PRSNT1A}}$	12	$\overline{\text{PRSNT1B}}$
5	Reserved	13	Reserved
6	Reserved	14	Reserved
7	Reserved	15	Reserved

23.3.3 Non-Interrupt Capable Input Data Packets

Table 16 and 17 defines the serial bit order for non-interrupt capable inputs. Data returned by this command indicates the bus mode capability of slot. The PCIXCAP1−3 bits follow the states and polarities described by Table 22. The M66EN bit is one when the associated slot is capable of supporting 66 MHz in conventional mode. This bit is only valid when the slot is powered but not connected. After the slot is connected, the M66EN bit indicates the current operating conventional mode of the bus segment. The $\overline{\text{AUXFLT}}$ bits indicate the state of the 3.3-V_{AUX} power rail fault latch. The $\overline{\text{AUXFLT}}$ bit is zero when an auxiliary fault is present on the associated slot.

Table 17. TPS2340AChannel 01 Data Group – Non-Interrupt Capable Inputs

Bit Number	Function
0	Slot A M66EN
1	Slot A PCI–XCAP1
2	Slot A PCI–XCAP2
3	Slot A Aux power fault state (AuxfltA)
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Slot B M66EN
9	Slot B PCI–XCAP1
10	Slot B PCI–XCAP2
11	Slot B Aux power fault state (AuxfltB)
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16…47	SIDI pin data for slots C, D, E and F follows

Table 18. TPS2342 Non-Interrupt Capable Inputs Serial Bit Order

Bit	Bit Name	Bit	Bit Name
0	M66ENA	8	M66ENB
1	PCIXCAP1A	9	PCIXCAP1B
2	PCIXCAP2A	10	PCIXCAP2B
3	PCIXCAP3A	11	PCIXCAP3B
4	Reserved	12	Reserved
5	Reserved	13	Reserved
6	Reserved	14	Reserved
7	$\overline{\text{AUXFLTA}}$	15	$\overline{\text{AUXFLTB}}$

23.3.4 Diagnostic #1 Input Data Packets

Status provided by diagnostic #1 commands indicates the current states of the hot-plug control signals at the slot. Table 18 and 19 defines the serial bit order for diagnostic #1 commands. The $\overline{\text{PWROFF}}$ bit is zero when all the main power rails of the slot are within 0.1 V of ground potential. The $\overline{\text{CLKEN}}$, $\overline{\text{BUSEN}}$, and $\overline{\text{RESET}}$ bits are zero when the respective control signals are asserted (i.e., the clock is enabled, the bus is enabled and the slot is being reset). The PWRLED and ATTLED bits are one when the associated LED is asserted (and the indicator is on).

Table 19. TPS2340A Channel 10 Data Group – Diagnostic Channel #1

Bit Number	Function
0	Device present 1 = power controller is present 0 = power controller is not installed
1	Slot A Pwren state
2	Slot A CLKEN state (0 = clock enabled)
3	Slot A BUSEN state (0 = bus enabled)
4	Slot A PCIRST state (0 = reset asserted)
5	Slot A PWRLED state (1 = power LED on)
6	Slot A ATTLED state (1 = attention LED on)
7	Reserved
8	Device present 1 = power controller is present 0 = power controller is not installed
9	Slot B Pwren state
10	Slot B CLKEN state
11	Slot B BUSEN state
12	Slot B PCIRST state
13	Slot B PWRLED state
14	Slot B ATTLED state
15	Reserved
16…47	SIDI pin data for slots C, D, E and F follows

Difference TPS2340A had device present in bit 0, TPS2342 does not and shifts all the functions back one bit.

Table 20. TPS2342 Diagnostic #1 Inputs Serial Bit Order

Bit	Bit Name	Bit	Bit Name
0	$\overline{\text{PWROFFA}}$	8	$\overline{\text{PWROFFB}}$
1	$\overline{\text{CLKEN A}}$	9	$\overline{\text{CLKENB}}$
2	$\overline{\text{BUSENA}}$	10	$\overline{\text{BUSENB}}$
3	$\overline{\text{RESETA}}$	11	$\overline{\text{RESETB}}$
4	PWRLEDA	12	PWRLEDB
5	ATTLEDA	13	ATTLEDB
6	Reserved	14	Reserved
7	Reserved	15	Reserved

23.3.5 Diagnostic #2 Input Data Packets

Status provided by diagnostic #2 commands indicates when a power controller is present on the bus and the current operating mode of that power controller. Table 20 defines the serial bit order for diagnostic #2 commands. Eight-bit data packets for slots that are not supported by the platform are reported as FFh, indicating that no power controller is present. When a power controller slot A or slot B is in single-slot mode, bits 8−15 are reported as FFh. The force enable mode bits indicate when the slot has been forced enabled by holding the **PWRLEDA/B** pin low at the rising edge of **PGOOD** (see Section 16). The Revid [3:0] bits are used to track revision changes in the power controllers that affect the SBI2 protocol, data packet definitions or other behavior that is noticeable to the hot-plug controller. The features described by this specification are associated with a power controller Revid [3:0] pattern of 0000b.

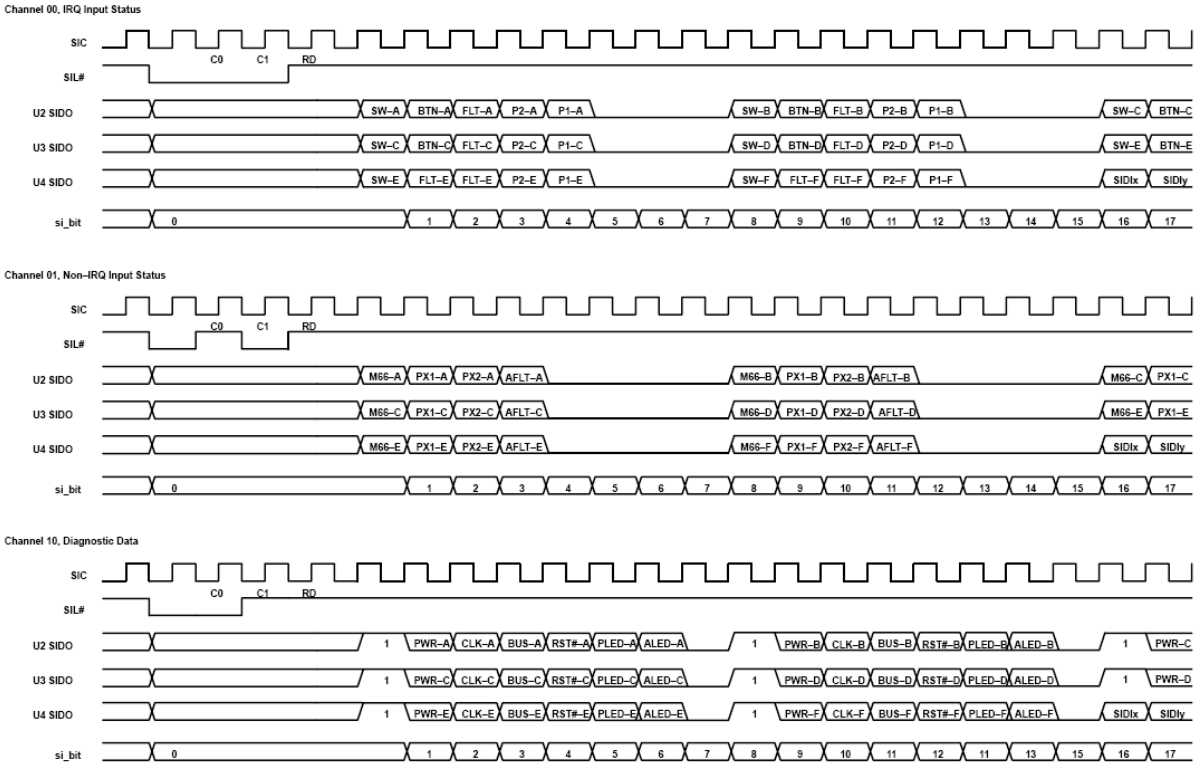

Figure 19. TPS2340A Timing

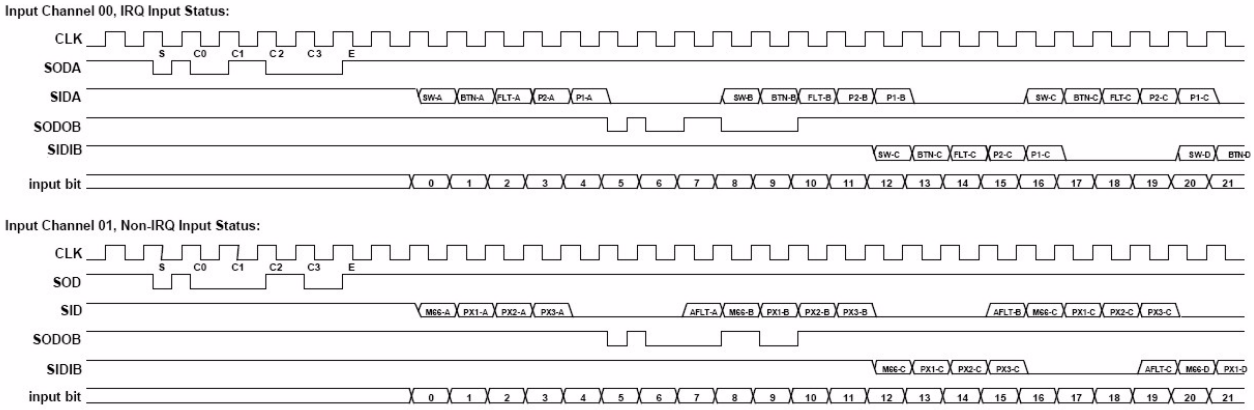

Figure 20. TPS2342 Timing

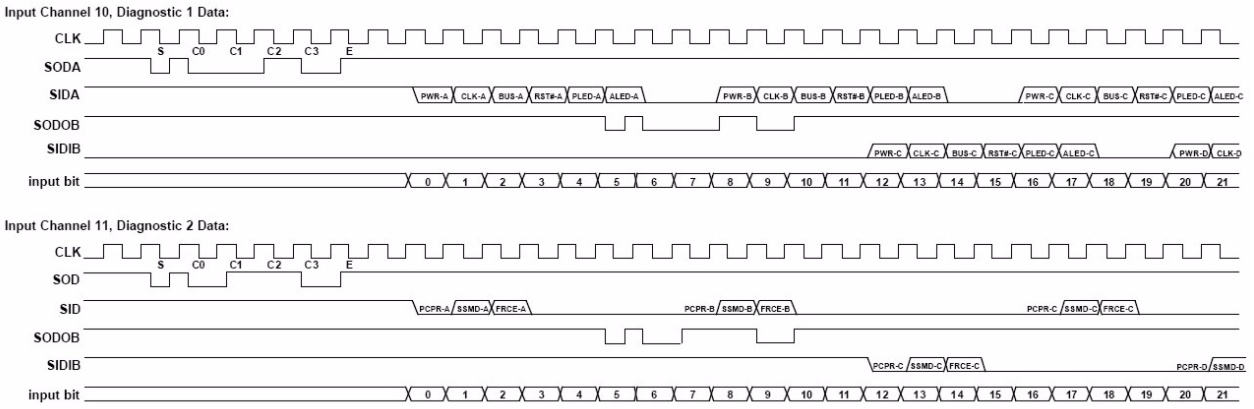

Figure 21. Diagnostic Command Signaling

Table 21. TPS2340A Channel 11 Data Group – Diagnostic Channel #2

BIT NUMBER	FUNCTION
0	Slot A latched Mode 0 bit state. This bit is latched at PGOOD
1	Slot A latched Mode 1 bit state. This bit is latched at PGOOD.
2	Must be set to 1.
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Slot B latched Mode 0 bit state. This bit is latched at PGOOD.
9	Slot B latched Mode 1 bit state. This bit is latched at PGOOD.
10	Must be set to 1.
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16…47	SIDI pin data for slots C, D, E and F follows

TPS2342 added control present from Diagnostic#1 TPS2340A to Diagnostic#2 and shifted the mode bits up.

Table 22. TPS2342 Diagnostic #2 Inputs Serial Bit Order

Bit	Function	Bit	Function
0	Slot A power controller presence detect 0 = present	8	Slot B power controller presence detect 0 = present
1	Slot A operating mode bit* state 1 = single-slot mode 0 = multi-slot mode	9	Slot B operating mode bit* state 1 = single-slot mode 0 = multi-slot mode
2	Slot A force enable mode bit* state 1 = slot is forced to enabled	10	Slot B force enable mode bit* state 1 = slot is forced to enabled
3	Reserved	11	Reserved
4	Revid [0]	12	Revid [0]
5	Revid [1]	13	Revid [1]
6	Revid [2]	14	Revid [2]
7	Revid [3]	15	Revid [3]

* – Mode bit states are platform−implementation specific and are only meaningful to diagnostic software typically provided by platform vendors.

Table 23. PCIXCAP Pin State Resolution

Slot PCIXCAP Pin State	xcapcmp 1	xcapcmp 2	xcapcmp 3	xcapcmp 4	PCIX-CAP3	PCIX-CAP2	PCIX-CAP1	Description
GND	0	0	0	0	0	0	0	Conventional PCI 2.2 operation
10 kΩ, 5% pull-down resistor	0	1	1	1	0	0	1	PCI −X 66 MHz capable
Open circuit	1	1	1	1	0	1	1	PCI −X 133 MHz capable
3.16 kΩ, 1% pull-down resistor	0	0	1	1	1	0	0	PCI −X mode 2 − 266 MHz capable
1.02 kΩ, 1% pull-down resistor	0	0	0	1	1	0	1	PCI −X mode 2 − 533 MHz capable

23.4 Commands

23.4.1 Serial Output Commands

Table 23 shows the command patterns of the SBI2 output commands. The hot-plug controller sends SHIFTOUT commands only when one or more control signals at one or more slots needs to be changed. SHIFTOUT commands always define all control signal states for all slots even when only one control signal needs to be changed. Once the SHIFTOUT command has been completed, the **LCA/B** signal is used to actually trigger a change in the control signal(s). GLOBAL commands are used to control generic bus segment signals and to describe the behavior of the **LCA/B** signal.

TPS2340A only has one output, no addressing.

Table 24. TPS2342 SBI2 Output Commands

Command Word msb lsb	Command Type
0001	SHIFTOUT command
0011	GLOBAL command

Note: All other command bit permutations not defined by this table or Table 12 and 13 are reserved.

Figure 16 and 17 show the SHIFTOUT and GLOBAL command signaling assuming the power controllers are in multi-slot mode. In all cases, the duration of the command is a function of the number of slots supported by the platform. The **SODOB** signal is used to retransmit the command and the remaining output data packet to downstream power controllers over the point-to-point serial interface. There is a 1-clock period data latency associated with each slot for SHIFTOUT commands; GLOBAL commands have a 6-clock latency per slot. GLOBAL commands have only a single 8-bit data packet that is not slot specific. The same 8-bit packet is forwarded downstream to all power controllers residing on the bus segment. Hot-plug controllers must allow time for all output commands to propagate to the last slot before issuing another command.

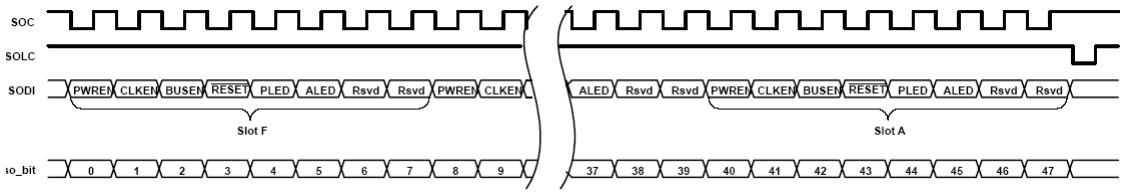

Figure 22. TPS2340A Output timing

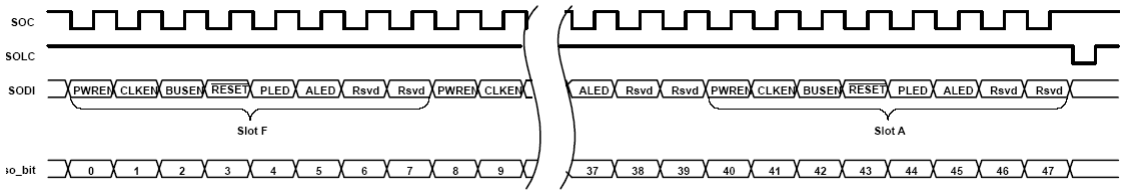

Figure 23. TPS2342 Timing Output

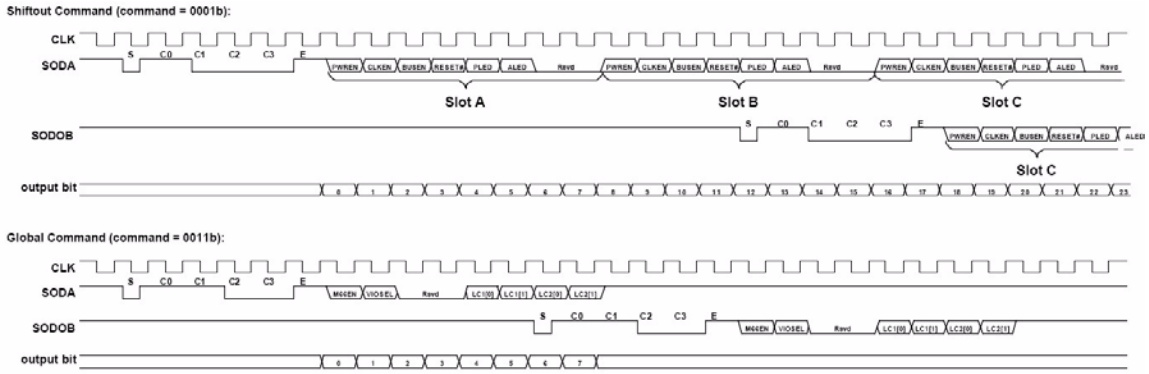

Figure 24. Shiftout and Global Command Signal

23.4.2 Shiftout Commands

Slot control data is provided by the SBI2 SHIFTOUT command. The slot-specific data packets are comprised of PWREN, CLKEN, BUSEN, $\overline{\text{RESET}}$, PWRLED and ATTLED control bits. The PWREN, CLKEN, PWRLED and ATTLED bits are one when the control signal will be changed to the asserted state. The $\overline{\text{RESET}}$ bit is zero when the slot-specific reset signal will be changed to the asserted state. Table 24 and 25 show the data packet bit order of SHIFTOUT commands.

Table 25. TPS2340A Operational Mode Output Data Bit Order

Bit Number	Function
0	Slot F Pwren state (1 = turn on power)
1	Slot F CLKEN state (1 = enable the clock)
2	Slot F BUSEN state (1 = enable the bus)
3	Slot F PCIRST state (0 = assert PCIRST)
4	Slot F PWRLED state (1 = turn on power LED)
5	Slot F ATTLED state (1 = turn on attention LED)
6	Reserved
7	Reserved
8	Slot E Pwren state
9	Slot E CLKEN state
10	Slot E BUSEN state
11	Slot E PCIRST state
12	Slot E PWRLED state
13	Slot E ATTLED state
14	Reserved
15	Reserved
16…47	SODO pin data for slots D, C, B and A follows

Table 26. TPS2342 Shiftout Command Serial Bit Order

Bit	Bit Name	Bit	Bit Name
0	PWRENA	8	PWRENB
1	CLKENA	9	CLKENB
2	BUSENA	10	BUSENB
3	$\overline{\text{RESETA}}$	11	$\overline{\text{RESETB}}$
4	PWRLEDA	12	PWRLEDB
5	ATTLEDA	13	ATTLEDB
6	Reserved	14	Reserved
7	Reserved	15	Reserved

23.4.3 Global Commands

Non slot-specific control data is provided by the SBI2 GLOBAL command. The GLOBAL command data packets are comprised of M66ENOUT and VIOSEL control bits that are recorded by power controller logic of each slot on the bus segment. The M66ENOUT bit is driven out on the power controller **M66ENA/B** pin when the **CLKENA/B** pin is asserted (see TPS2342 datasheet). The VIOSEL bit controls the state of the **Viosel_ao** and **Viosel_bo** internal digital/analog interface signals. The **Viosel_ao** and **Viosel_bo** signals change state on the next control latch clock event. The remaining GLOBAL data packet bits define the behavior of the **LCA/B** signal. The LC1_0 and LC1_1 bits define the group of signals that will be affected by the first latch clock event. The LC2_0 and LC2_1 bits define the group of signals that will be affected by the first latch clock event. Table 26 shows the data packet bit order of GLOBAL commands.

Refer to Section 15.4.4, Latch Clock Events for a detailed description of these GLOBAL command bits.

Table 27. Global Command Serial Bit Order

Bit	Bit Name
0	M66ENOUT
1	VIOSEL
2	Reserved
3	Reserved
4	LC1_0 − Arming control bit 0 for first latch clock event
5	LC1_1 − Arming control bit 1 for first latch clock event
6	LC2_0 − Arming control bit 0 for second latch clock event
7	LC2_1 − Arming control bit 1 for second latch clock event

23.4.4 Latch Clock Events

The **LCA/B** signal is normally high and pulses low in order to cause a change in the power controller control signals. Control settings that are updated by the SHIFTOUT command and the VIOSEL bit of GLOBAL command do not take effect until the hot-plug controller sends a latch clock. The rising edge of **LCA/B** causes the control signals to be update provided that they have been armed to do so. Table 27 show the definition of the GLOBAL command latch clock arming control bits. By default, all of the control signals are armed to change on the first latch clock following a SHIFTOUT command. The effect is the same as a GLOBAL command with a packet bit [7:4] pattern of 0011b. A GLOBAL command need not be issued unless the timing of the **RESETA/B** pins must be different from that of the other control signals. When a GLOBAL command is used, it defines whether the control signals will ignore that latch clock, change on the first latch clock event or change on the second latch clock event. The **RESETA/B** pins need to be controlled separately from the other control pins. Two sets of arming control bits are used so that timing of reset events can be kept separate from that of other control signals without requiring a separate SHIFTOUT command. This allows more accurate control of when the control signals change state relative to each other.

Table 28. Latch Clock Arming Controls

LC1_1	LC1_0	Description
0	0	First latch clock event has no effect on the control signals
0	1	First latch clock event affects all controls except **RESETA/B**pins
1	0	First latch clock event affects only **RESETA/B** pins
1	1	First latch clock event affects all controls signals
LC2_1	**LC2_0**	**Description**
0	0	Second latch clock event has no effect on the control signals
0	1	Second latch clock event affects all controls except **RESETA/B** pins
1	0	Second latch clock event affects only **RESETA/B** pins
1	1	Second latch clock event affects all controls signals

Hot-plug controller designs that utilize GLOBAL commands must be designed to meet the T_{GCLC} timing parameter. As is illustrated in Figure 36, GLOBAL commands are cascaded downstream by each power controller and time must be allowed for the arming controls to propagate to the slot control logic of ALL power controllers before a latch clock will operate properly.

23.4.5 Asynchronous Controls

The control signals of the power controller (see TPS2342 datasheet) can be affected by several asynchronous controls. The asynchronous controls are: **PGOOD**, **SWA/B**, **RST**, **LC**, **Pwrflt_ai_/Pwrflt_bi_**, and **Auxflt_ai_/Auxflt_bi_**.

23.4.6 PGOOD and SWA/B

When deasserted, the **PGOOD** signal initializes all flip-flops in the power controller. Main power is shut off, the slots are disconnected from the bus and PCI RST is asserted to the slot (see Table 28). When PGOOD is deasserted, the SWA/B pins cannot be sampled by an input command but continue to control the PME connections and auxiliary power state of the slot. When force enable mode is active, PGOOD deassertion and SWA/B high cause the slot to be powered off and disconnected.

Table 29. Control Signal Initial Power-On States

Control Signal/Pin	Serial Mode	Force Enable and Serial Mode, SWA/B closed
PWRLEDA/B	1	0
ATTLEDA/B	1	1
Pwren_ao/Pwren_bo	0	1
BUSENA/B	1	0
CLKENA/B	1	0
RESETA/B	0	0[1]
Viosel_ao/Viosel_bo	1	?[2]
M66ENOUT[3]	Tri-state with pullup	Tri-state with pullup

NOTES: 1. Follows the state of RSTA/B pin
2. Follows the state of mode 2 as indicated by the PCIXCAPA/B pin
3. This signal reflects the state of the M66ENOUT internal flip−flop following **PGOOD** deassertion. This signal is driven out on the **M66ENA/B**pin when **CLKENA/B** is asserted.

23.4.7 $\overline{\text{RST}}$

The **$\overline{\text{RSTA/B}}$** signal behavior closely matches that of the secondary bus reset (PCI $\overline{\text{RST}}$). When **$\overline{\text{RSTA/B}}$** asserts, the **$\overline{\text{RESETA/B}}$** pins on the power controller will asynchronously assert. When the **$\overline{\text{RSTA/B}}$** signal is asserted, SHIFTOUT commands are typically used to define new control signal states and the **$\overline{\text{RESETA/B}}$** pins are permitted to be setup to deassert. During **$\overline{\text{RSTA/B}}$** assertion, the **LCA/B** signal is ignored except as described in Section 15.4.8.

23.4.8 LC

When the **LCA/B** signal is low and the **$\overline{\text{RSTA/B}}$** signal is low, all slot control signals are asynchronously initialized to their default (**PGOOD** deasserted) state. The latch clock arming logic is also cleared so that the rising edge of the **LCA/B** signal will have no effect on the control signals. Hot-plug controllers that use this feature to disable hot-plug slots must insure that the rising edge of **LCA/B** occurs T_{RHLCH} after the rising edge of **$\overline{\text{RSTA/B}}$** to prevent timing race condition issues within the power controller.

23.4.9 Fault Conditions

When a slot is enabled or is in force enable mode, fault conditions cause the slot to be asynchronously powered down. In serial modes, the slot is also disconnected and reset. The **Pwrflt_ai_**/**Pwrflt_bi_** and **Auxflt_ai_**/**Auxflt_bi_** signals affect main power states. The **Auxflt_ai_**/**Auxflt_bi_** signals affect only auxiliary power.

Main power faults caused by **Pwrflt_ai_**/**Pwrflt_bi_** assertion are cleared by deasserting the **Pwren_ao/ Pwren_bo** signals. Main power faults caused by **Auxflt_ai_**/**Auxflt_bi_** assertion are cleared by deasserting **SWA/B**.

23.5 Special Test Logic

The power controller contains additional logic that facilitates testing by putting the device in special test modes. The **TEST** input pin (shared with the **BUTTONA** pin) is used to enter all test modes except the force enable mode. At the rising edge of **PGOOD**, the **TEST**, **PARMODE**, **MSMODE** and **PWRLEDx** pin states are latched and decoded to enable the test modes shown in the table below.

Table 30. TPS2340A Test Modes Configuration

PGOOD	TEST	SODO/MODE1	SIDO/MODE0	Operating Mode
↑	0	MODE1	MODE0	Normal operation mode, latch MODE inputs
1	0	SODO	SIDO	Normal operation mode, drive SODO and SIDO
↑	1	0	0	NAND tree test mode
↑	1	0	1	Tri-state test mode (all pins tri-stated)
↑	1	1	X	Reserved
1	1	SODO	SIDO	Normal operation, but Pwrenx driven on PWRLEDx, Faultx driven on ATTLEDx.

Table 31. TPS2342 Test Modes Configuration

PGOOD	BUTTONA	SIDB	SIDA	PWRLEDx	Operating Mode
↑	<6 V	0	0	1	Single-slot serial mode: Using different hot-plug controllers for slot A and slot B.
↑	<6 V	0	1	1	Multi-slot serial mode: Using the same hot-plug controller for slot A and slot B, and potentially cascading additional TPS2342.
↑	<6 V	1	0	1	Direct mode.
↑	>9 V	0	0	1	Tri-state test mode. In this mode, all digital pins (outputs and inputs) are tri-state; in addition, pull-ups and pull-downs are disconnected.
↑	>9 V	0	1	1	NAND-tree test mode. In this mode, all pins are tri-state except for M66ENB.
↑	>9 V	1	X	1	Reserved.
1	>9 V	SIDB	SIDA	1	Normal operation, but Pwren_xo driven on PWRLEDx and Fault_xo_ driven on ATTLEDx
1	<6 V	SIDB	SIDA	1	Normal operation.
↑	X	X	X	0	Force enable mode. The slot is forced enabled.

NOTES:1. X = do not care. The level on this signal does not affect the operating mode.
2. x = *a* or *b* as appropriate. For example, PWRLEDx refers to PWRLEDA orPWRLEDB, depending on which slot is being discussed.

23.6 Run-Time Test Mode

When **TEST** is asserted *after* **PGOOD** is asserted, the device enters a run-time test mode. When this test mode is enabled, the **PWRLEDA/B** outputs will assert when the slot's internal **Pwren_ao** or **Pwren_bo** signal is asserted. Similarly, the **ATTLEDA/B** output will assert when the corresponding **Fault_ao_** or **Fault_bo_** signal is asserted.

23.7 NAND Tree Test Mode

All bi-directional pins except **NT_OUT** (shared with the **$\overline{\text{M66ENB}}$** pin) are tri-stated to enable them to be driven by external stimulus during the NAND tree test mode. All inputs should be forced low (except for LCA that is forced high) and then switched to the opposite state, one signal at a time, in the order listed below. The NAND result is driven out on the on the **NT_OUT** bi-directional pin.

Table 32. TPS2340A NAND Tree Toggle Order

Sequence	Pin Name	Pin #
1	SIDI	20
2	SODO	19
3	SWA	46
4	SWB	14
5	PRSNT1A	37
6	PRSNT1B	24
7	PRSNT2A	36
8	PRSNT2B	25
9	BUTTONA	45
10	BUTTONB	15
11	M66ENA	34
12	M66ENB	27
13	PCI–XCAPA	50
14	PCI–XCAPB	11
15	SODI	42
16	SOC	17
17	SOR	40
18	SORR	21
19	SOLC	39
20	SORLC	22
21	BUSENA	32
22	BUSENB	29
23	CLKENA	33
24	CLKENB	28
25	RESETA	35
26	RESETB	26
27	PWRLEDA	48
28	PWRLEDB	12
29	ATTLEDA	47
30	ATTLEDB	13
31	SIL	16
32	SIC	44
33	TEST	23

Table 33. TPS2342 NAND Tree Toggle Order

Sequence	Pin Name	Pin #
1	PCIXCAPB	19
2	$\overline{\text{PRSNT2B}}$	17
3	$\overline{\text{PRSNT1B}}$	16
4	$\overline{\text{BUTTONB}}$	21
5	SWB	22
6	$\overline{\text{RESETB}}$	18
7	$\overline{\text{CLKENB}}$	15
8	$\overline{\text{BUSENB}}$	13
9	$\overline{\text{ATTLEDB}}$	23
10	$\overline{\text{PWRLEDB}}$	24
11	SIDB	26
12	SODB	25
13	$\overline{\text{RSTB}}$	27
14	LCB	28
15	CLKB	29
16	M66ENA	41
17	PCIXCAPA	42
18	$\overline{\text{PRSNT2A}}$	44
19	$\overline{\text{PRSNT1A}}$	45
20	$\overline{\text{BUTTONA}}$	40
21	SWA	39
22	$\overline{\text{RESETA}}$	43
23	$\overline{\text{CLKENA}}$	46
24	$\overline{\text{BUSENA}}$	48
25	$\overline{\text{ATTLEDA}}$	38
26	$\overline{\text{PWRLEDA}}$	37
27	SIDA	35
28	SODA	36
29	$\overline{\text{RSTA}}$	34
30	CLKA	32
31	LCA	33

23.8 Force Enable Mode

Regardless of the operational mode, slots A and/or B can be forced to the enabled state. In this state, the slots cannot be controlled but status (power controller outputs) is available from either the serial or parallel interface. The force enable mode is typically used for manufacturing test or early product development when the hot-plug controller may not be functional due to software or hardware reasons. Force enable mode is selected by holding the **PWRLEDA/B** pin low at the rising edge of **PGOOD**.

When in the force enabled state and the associated **SWA/B** pin is low, the main power is enabled (**Pwren_ao**/**Pwren_bo** is high) and the state of the **Viosel_ao**/ **Viosel_ao** signals are governed by the **PCIXCAPA/B** pin. When the power controller is in serial mode, the **BUSENA/B** and **CLKENA/B** pins are asserted and the **RESETA/B** pins follow the **RSTA/B** signal. The M66EN pin is tri-stated and pulled up with 3.3-V slot power. The **ATTLEDA/B** pin is deasserted and the **PWRLEDA/B** pin is asserted due to the external pulldown circuit. Should a power fault occur, power is shut down (**Pwren_ao**/**Pwren_bo** is deasserted), the bus is disconnected (**BUSENA/B** and **CLKENA/B** pins are deasserted) and **RESETA/B** is asserted.

When serial mode is selected, table below contrasts the difference between normal operation mode and force enable mode. The table shows the electrical power-on state (after **PGOOD** asserts) of each slot's output pins and internal analog/digital interface signals:

Table 34. Control Signal Initial Power-On States

Control Signal/Pin	Serial Mode	Force Enable and Serial Mode, SWA/B closed
PWRLEDA/B	1	0
ATTLEDA/B	1	1
Pwren_ao/Pwren_bo	0	1
BUSENA/B	1	0
CLKENA/B	1	0
RESETA/B	0	0[1]
Viosel_ao/Viosel_bo	1	?[2]
M66ENOUT[3]	Tri-state with pullup	Tri-state with pullup

NOTES: 1. Follows the state of RSTA/B pin
2. Follows the state of mode 2 as indicated by the PCIXCAPA/B pin
3. This signal reflects the state of the M66ENOUT internal flip-flop following **PGOOD** deassertion. This signal is driven out on the **M66ENA/B** pin when **CLKENA/B** is asserted.

23.9 Digital Signals

Some pins serve more than one function. Each function and its associated name are described separately, delineated by dashed lines. Output pins designated as O/I without input function descriptions utilize their input buffers to support the NAND tree mode. Refer to the TPS2342 datasheet (Texas Instruments Literature Number SLUS572) for a description of the I/O pin characteristics.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265