TPS2384 Power Sourcing Equipment Power Manager Device Errata

1 Background

Texas Instruments (TI) has recently discovered an issue with the semi-auto mode operation of the TPS2384 Power Sourcing Equipment (PSE) Power Manager product. Semi-auto mode operation is invoked when the device is connected for Auto Mode (AM)in the application circuit, but with additional control from an external host processor or controller over the available I^2C interface. When used under a specific configuration and under certain conditions (detailed below), PSE ports which are disabled via control bits within the I^2C register set will not become active again if and when the disabled state of these bits is subsequently cleared.

2 Devices Impacted

All TPS2384 devices with chip revision 01 are affected and may exhibit this issue. The chip revision is available at bits [D3:D2] in the Common Read register (Register Select address = 0000). A returned value of [D3:D2] = 01 indicates a revision 01 device. Material with a Lot Trace Code (LTC) of 66E6TET or later is revision 01 silicon. The LTC is marked on the top side of both the PowerPad™ down (PAP) and PowerPad™ up (PJD) packages. The first two characters of the LTC contain the single-digit year and month code representation, respectively, of the month and year of assembly. In the LTC, months are encoded as a progression in which “1” represents January, “2” represents February, and so on to “9” represents September, “A” represents October, “B” represents November, and “C” represents December. For example, this effectivity LTC of 66E6TET indicates a date code of June, 2006.

Earlier silicon (device revision 00) does not contain this problem.

3 Detailed Description of Failure Mode

The port re-enable issue only occurs when the TPS2384 revision 01 is used under the following configuration:

1. Device configured for auto mode operation; MS input pin low or a logic 0,
2. An external host is used in the application to further control device functions, including ports’ enabled or disabled status by setting/clearing control bits in the I^2C register map, and
3. Alternative B operation is selected; ALT_A/B pin high or a logic 1.

Device channels which are susceptible to the failure mode are those whose associated port is not already delivering power; that is, the channel/port is “searching” for a valid Powered Device (PD), or the port RJ-45 is open-circuit. These ports can be disabled by either of two control bits:

1. Writing Port Enable bit D4 of Port Control register 2 (Register Select address = 0011b) to a logic 1 (disabled), or
2. Writing the All Ports Disable bit D1 of Common Control Write register (Register Select address = 0001b) to a logic 1 (all four channels of the device disabled).

Ports disabled by either of these mechanisms will fail to become active again or re-initiate Discovery 1/Discovery 2 sequencing, and will consequently not power even valid PD’s, even when the associated control bit is subsequently cleared (set to a logic 0) by the host firmware.

4 Root Cause of Problem

In creating the revision 01 device from the original version, new logic circuits were added, and existing gate interconnect modified, to change the device AM detection function from a 2-point Discovery to a 4-point Discovery scheme. The original circuitry correctly handled the three possible outcomes of port sequencing which return function flow to the start of the Discovery/Classify/Power sequence:

1. Entry from device Power-On-Reset (POR) (application of 48-V power, PORB pin de-assertion, or software reset).
2. Return to start in Alternative A with either a valid or invalid PD indication in the logic.
3. Return to start in Alternative B, with either a valid or invalid PD indication in the logic.

The change to the new 4-point Discovery algorithm required additional logic to control launching the internal Back-off Timer, and resumption of Discovery after back-off expiration. These design changes inadvertently generated a logic error such that it no longer correctly handles return to start in Alternative B with an invalid PD result (condition 3 above).

Refer to the diagrams in Figure 1 and Figure 2 below for a graphical representation of the circuit differences between revision 00 and revision 01 devices.

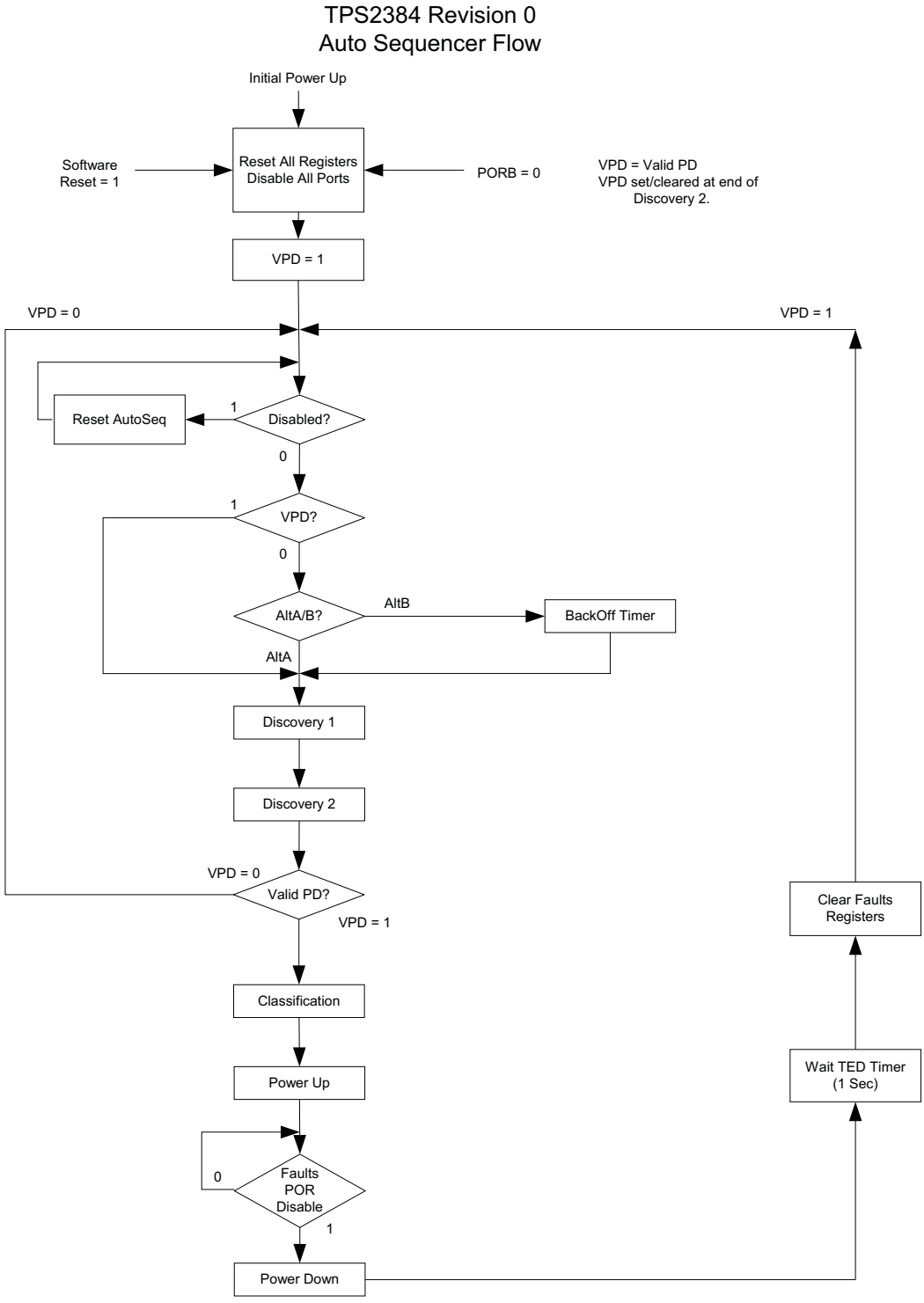

Figure 1. TPS2384 Rev. 00 Auto-Mode Sequence Flow Diagram

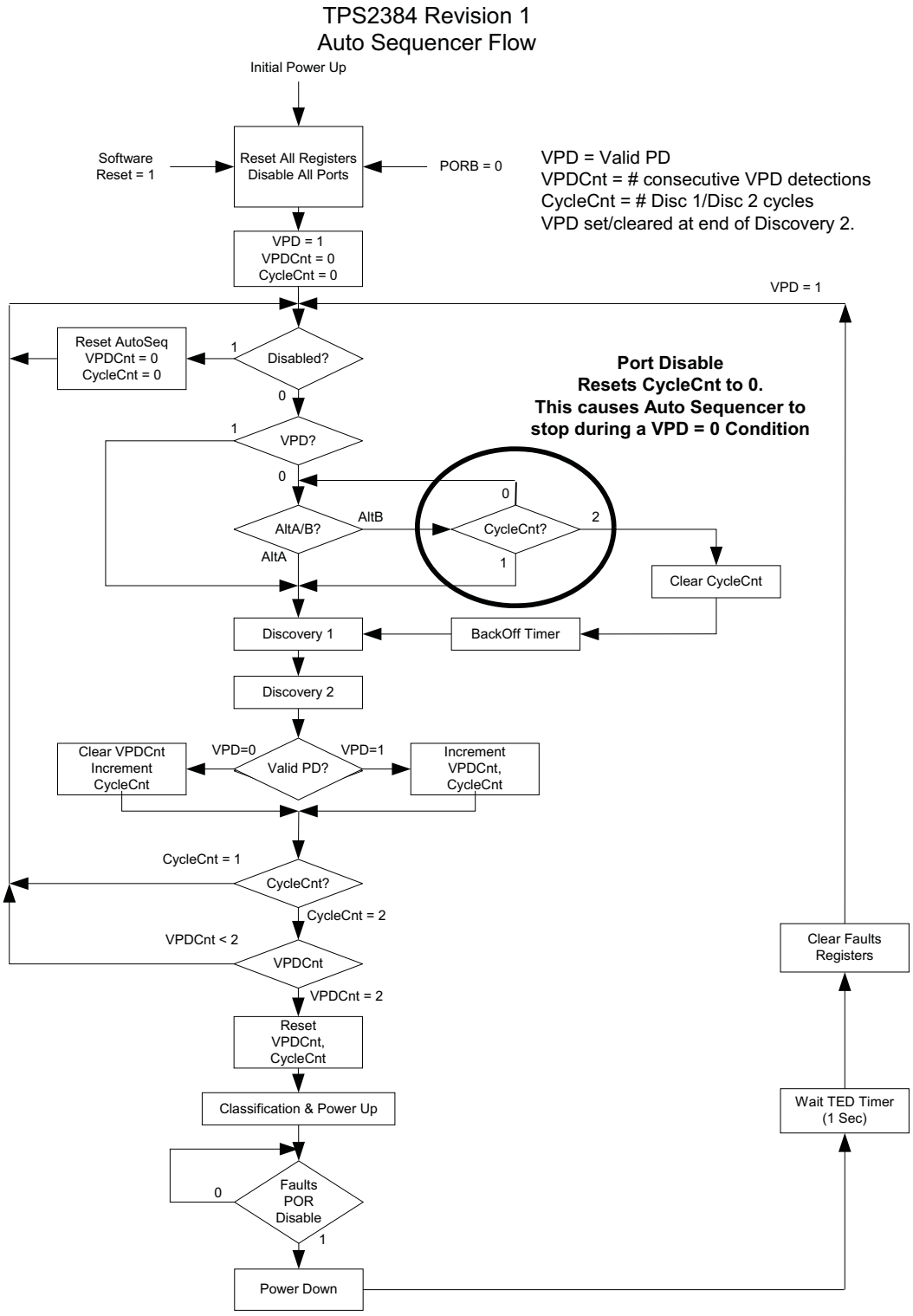

Figure 2. TPS2384 Rev. 01 Auto-Mode Sequence Flow Diagram

5 Recommended Solution

TI has discovered that a port hung as described above can be returned to normal operation without the use of a full device reset. Upon re-enable, if the ALT_A/B pin is momentarily toggled low and then high again, the device channel will recover and resume Discovery 1/Discovery 2 probing. This requires that semi-auto applications do not connect ALT_A/B directly to a supply rail (e.g., the device V3.3 pin or other logic supply), but rather connect it to some binary, logic-level drive, with at most a resistive pull-up to the local logic rail (depending on drive configuration).

For ensured operation of the port recovery mechanism, the low-going pulses at the ALT_A/B input must have a minimum pulse width of 10 μs.

TI has developed and tested an implementation of the above mechanism which requires only a wiring change (relative to the data sheet functional information for auto mode), with no additional external devices required. The solution does require some additional logic (in the form of I^2C transactions) be incorporated into the controlling PoE algorithm of the host processor.

Figure 3 shows the typical auto-mode schematic modified to incorporate the suggested fix. Note that the AC_LO pin is connected directly to drive the ALT_A/B pin. The logic-level drive circuitry of the AC_LO output is used to toggle the ALT_A/B input, according to the requirements above, via commands over the I^2C bus.

In addition to the hardware change shown above, using applications must address the following two states which may be encountered by the PoE control routine.

1. Start of PoE application from device POR.

   The reset state of the AC_LO output is a logic 0, setting the pin state to a logic low voltage. As soon as practical in the initialization sequence after I^2C POR, the controlling firmware should set AC_LO high by writing a logic 1 to bit D3 of the Common Control Write register (Register Select address = 0001b). This operation configures the TPS2384 device for Alternative B mode. Refer to the device data sheet for details on POR timing. Alternative B applications may want to add POR pin control from an available host I/O pin as shown in Figure 3, to facilitate this PSE initialization.

2. Enabling a previously disabled port.

   When, in the normal flow of the host PoE application, it is necessary to disable one or more ports for any reason, the following command sequence must be employed to subsequently re-enable those ports.

   a. Write the Port Enable bit D4 of Port Control register 2 (Register Select address = 0011b) to a logic 0 (enabled).
   b. Write the AC_LO bit D3 of Common Control Write register (Register Select address = 0001b) to a logic 0.
   c. Write the AC_LO bit D3 of Common Control Write register (Register Select address = 0001b) to a logic 1.

   Note that in the above sequence, the affected port resumes searching at the completion of step 2.b at the Alternative A rate (no back-off). Therefore, one more I^2C command sequence is required to return to Alternative B operation. At a 100-kHz I^2C SCL rate, this step takes less than 300 μs. The IEEE 802.3af specification requires Alternative B back-off behavior only after detection of an invalid PD (i.e.; after completion of at least one Discovery cycle). Therefore, specification conformance can be maintained with this recovery mechanism.

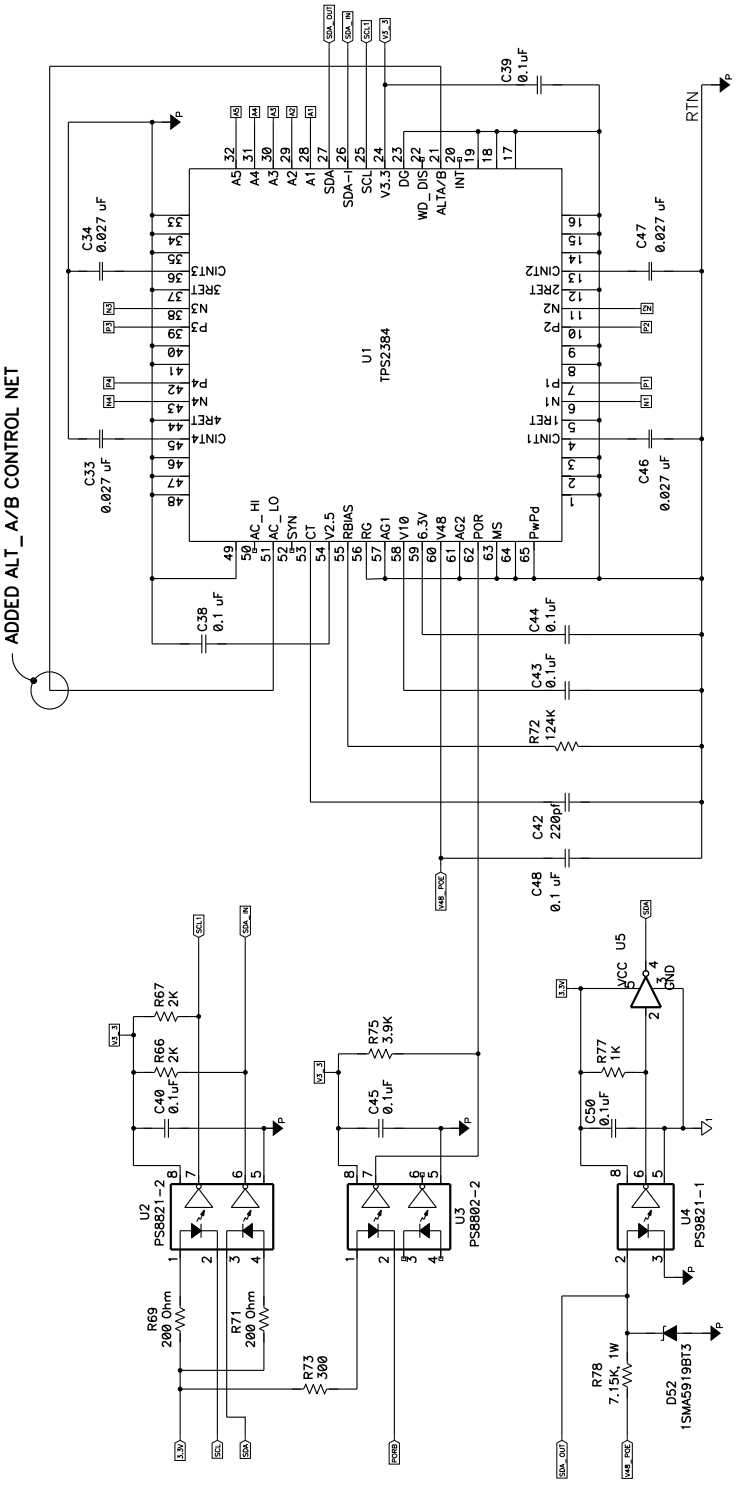

Figure 3. Semi-auto mode/Alternative B schematic for active ALT_A/B control.

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