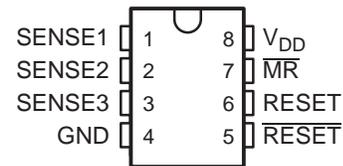


TRIPLE PROCESSOR SUPERVISORS

FEATURES

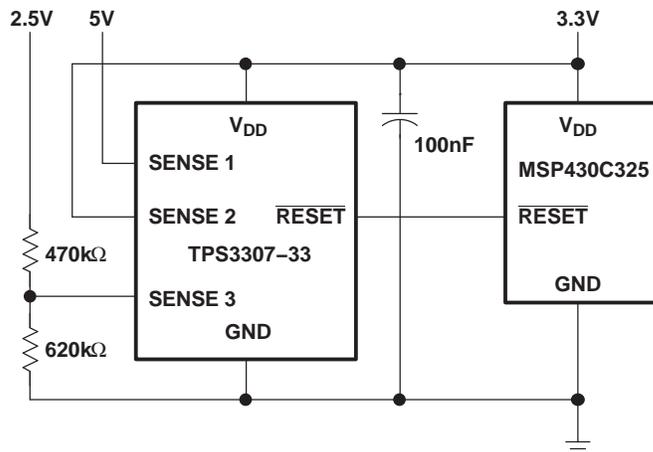
- Triple Supervisory Circuits for DSP and Processor-Based Systems
- Power-On Reset Generator With Fixed Delay Time of 200ms, No External Capacitor Needed
- Temperature-Compensated Voltage Reference
- Maximum Supply Current of 40 μ A
- Supply Voltage Range: 2V to 6V
- Defined $\overline{\text{RESET}}$ Output From $V_{\text{DD}} \geq 1.1\text{V}$
- MSOP-8 and SO-8 Packages
- Temperature Range : -40°C to $+85^{\circ}\text{C}$

D OR DGN PACKAGE
(TOP VIEW)



TYPICAL APPLICATIONS

Figure 1 lists some of the typical applications for the TPS3307 family, and a schematic diagram for a processor-based system application. This application uses TI part numbers [TPS3307-33](#) and [MSP430C325](#).



- Applications using DSPs, Microcontrollers or Microprocessors
- Industrial Equipment
- Programmable Controls
- Automotive Systems
- Portable/Battery Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Notebook/Desktop Computers

Figure 1. Applications Using the TPS3307 Family

DESCRIPTION

The TPS3307 family is a series of micropower supply voltage supervisors designed for circuit initialization primarily in DSP and processor-based systems, which require more than one supply voltage.

The product spectrum of the TPS3307-xx is designed for monitoring three independent supply voltages: 3.3V/1.8V/adj, 3.3V/2.5V/adj or 3.3V/5V/adj. The adjustable SENSE input allows the monitoring of any supply voltage $>1.25\text{V}$.

The various supply voltage supervisors are designed to monitor the nominal supply voltage as shown in the following [supply voltage monitoring table](#).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1V. Thereafter, the supply voltage supervisor monitors the SENSE_n inputs and keeps $\overline{\text{RESET}}$ active as long as SENSE_n remain below the threshold voltage $V_{\text{IT}+}$.

An internal timer delays the return of the $\overline{\text{RESET}}$ output to the inactive state (high) to ensure proper system reset. The delay time, $t_{\text{d (typ)}} = 200\text{ms}$, starts after all SENSE_n inputs have risen above the threshold voltage $V_{\text{IT}+}$. When the voltage at any SENSE input drops below the threshold voltage $V_{\text{IT-}}$, the $\overline{\text{RESET}}$ output becomes active (low) again.

The TPS3307-xx family of devices incorporates a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active. In addition to the active-low $\overline{\text{RESET}}$ output, the TPS3307-xx family includes an active-high RESET output.

The devices are available in either 8-pin MSOP or standard 8-pin SO packages.

The TPS3307-xx devices are characterized for operation over a temperature range of -40°C to $+85^{\circ}\text{C}$.

SUPPLY VOLTAGE MONITORING

| DEVICE | NOMINAL SUPERVISED VOLTAGE | | | THRESHOLD VOLTAGE (TYP) | | |
|------------|----------------------------|--------|--------------|-------------------------|--------|----------------------|
| | SENSE1 | SENSE2 | SENSE3 | SENSE1 | SENSE2 | SENSE3 |
| TPS3307-18 | 3.3V | 1.8V | User defined | 2.93V | 1.68V | 1.25V ⁽¹⁾ |
| TPS3307-25 | 3.3V | 2.5V | User defined | 2.93V | 2.25V | 1.25V ⁽¹⁾ |
| TPS3307-33 | 5V | 3.3V | User defined | 4.55V | 2.93V | 1.25V ⁽¹⁾ |

(1) The actual sense voltage has to be adjusted by an external resistor divider according to the application requirements.

AVAILABLE OPTIONS⁽¹⁾

| T_A | PACKAGED DEVICES | | MARKING DGN PACKAGE | CHIP FORM (Y) |
|--|----------------------|---------------------------------------|------------------------|------------------|
| | SMALL OUTLINE (D) | PowerPAD™ μ-SMALL OUTLINE (DGN) | | |
| -40°C to $+85^{\circ}\text{C}$ | TPS3307-18D | TPS3307-18DGN | TIAAP | TPS3307-18Y |
| | TPS3307-25D | TPS3307-25DGN | TIAAQ | TPS3307-25Y |
| | TPS3307-33D | TPS3307-33DGN | TIAAR | TPS3307-33Y |

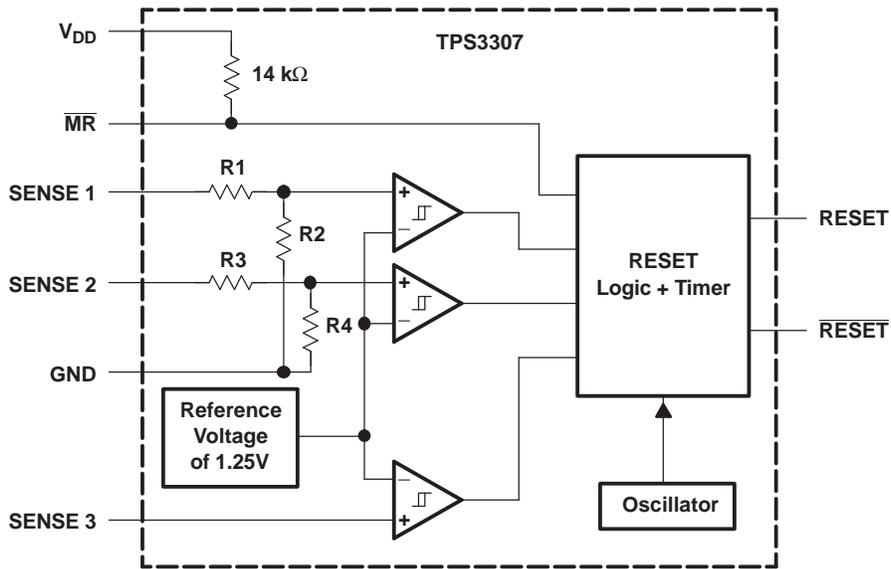
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Function/Truth Tables

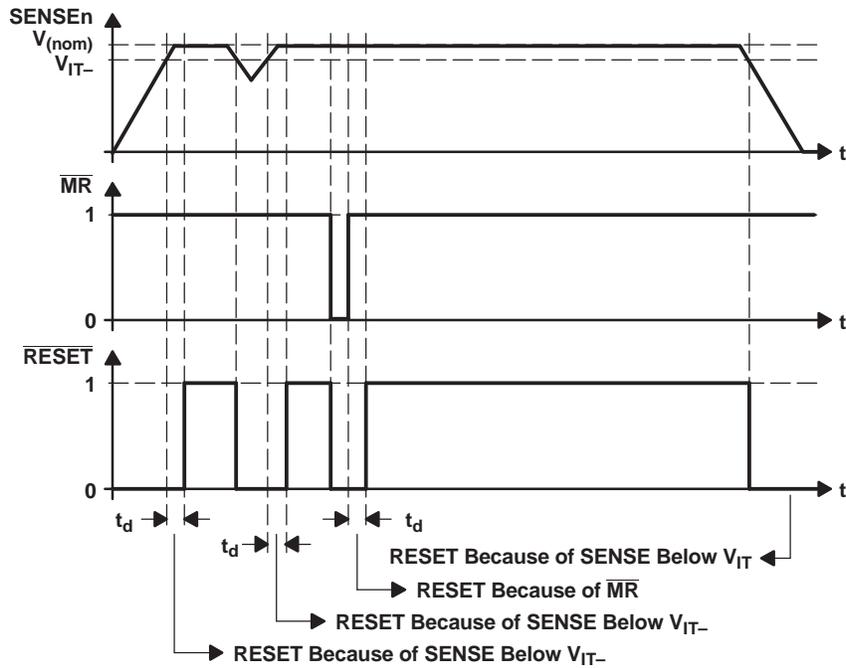
| $\overline{\text{MR}}$ | $\text{SENSE1} > V_{\text{IT1}}$ | $\text{SENSE2} > V_{\text{IT2}}$ | $\text{SENSE3} > V_{\text{IT3}}$ | $\overline{\text{RESET}}$ | RESET |
|------------------------|----------------------------------|----------------------------------|----------------------------------|---------------------------|-------|
| L | X ⁽¹⁾ | X ⁽¹⁾ | X | L | H |
| H | 0 | 0 | 0 | L | H |
| H | 0 | 0 | 1 | L | H |
| H | 0 | 1 | 0 | L | H |
| H | 0 | 1 | 1 | L | H |
| H | 1 | 0 | 0 | L | H |
| H | 1 | 0 | 1 | L | H |
| H | 1 | 1 | 0 | L | H |
| H | 1 | 1 | 1 | H | L |

(1) X = Don't care

Functional Block Diagram



Timing Diagram



TPS3307Y Chip Information

These chips, when properly assembled, display characteristics similar to those of the TPS3307. Thermal compression or ultrasonic bonding may take place on the doped aluminium bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

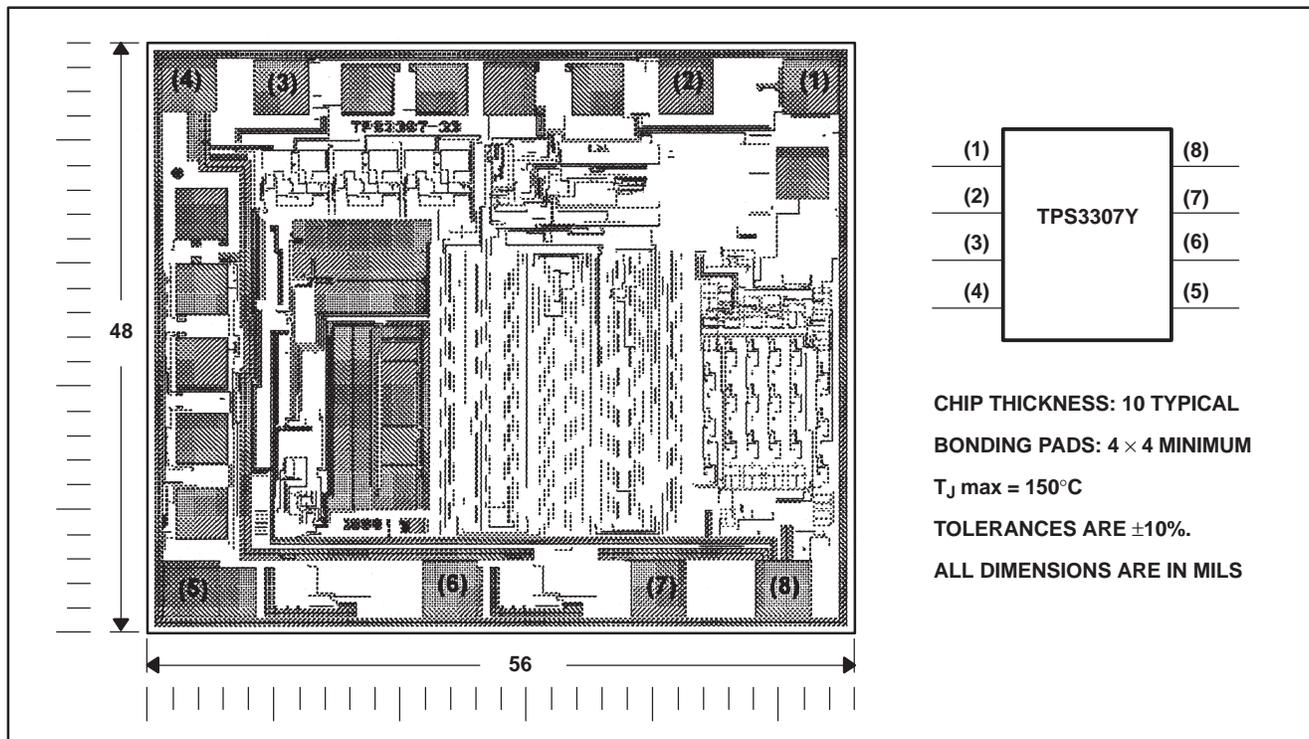


Table 2. Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---------------------------|-----|-----|--------------------------|
| GND | 4 | | Ground |
| $\overline{\text{MR}}$ | 7 | I | Manual reset |
| $\overline{\text{RESET}}$ | 5 | O | Active-low reset output |
| RESET | 6 | O | Active-high reset output |
| SENSE1 | 1 | I | Sense voltage input 1 |
| SENSE2 | 2 | I | Sense voltage input 2 |
| SENSE3 | 3 | I | Sense voltage input 3 |
| V _{DD} | 8 | | Supply voltage |

Absolute Maximum Ratings⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

| | UNIT |
|--|--|
| Supply voltage, V_{DD} ⁽²⁾ | 7V |
| \overline{MR} pin | -0.3V to $V_{DD} + 0.3V$ |
| All other pins ⁽²⁾ | -0.3V to 7V |
| Maximum low output current, I_{OL} | 5mA |
| Maximum high output current, I_{OH} | -5mA |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) | $\pm 20mA$ |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) | $\pm 20mA$ |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A | -40°C to +85°C |
| Storage temperature range, T_{stg} | -65°C to +150°C |
| Soldering temperature | +260°C |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND. For reliable operation the device must not be operated at 7V for more than $t = 1000h$ continuously.

Dissipation Rating Table

| PACKAGE | $T_A \leq +25^\circ C$ POWER RATING | DERATING FACTOR ABOVE $T_A = +25^\circ C$ | $T_A = +70^\circ C$ POWER RATING | $T_A = +85^\circ C$ POWER RATING |
|---------|--|--|-------------------------------------|-------------------------------------|
| DGN | 2.14W | 17.1mW/°C | 1.37W | 1.11W |
| D | 725mW | 5.8mW/°C | 464mW | 377mW |

Recommended Operating Conditions

At specified temperature range.

| | MIN | MAX | UNIT |
|--|---------------------|------------------------------|------|
| Supply voltage, V_{DD} | 2 | 6 | V |
| Input voltage at \overline{MR} and SENSE3, V_I | 0 | $V_{DD} + 0.3$ | V |
| Input voltage at SENSE1 and SENSE2, V_I | 0 | $(V_{DD} + 0.3)V_{IT}/1.25V$ | V |
| High-level input voltage at \overline{MR} , V_{IH} | $0.7 \times V_{DD}$ | | V |
| Low-level input voltage at \overline{MR} , V_{IL} | | $0.3 \times V_{DD}$ | V |
| Input transition rise and fall rate at \overline{MR} , $\Delta t/\Delta V$ | | 50 | ns/V |
| Operating free-air temperature range, T_A | -40 | +85 | °C |

Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | |
|---------------------------------------|---|---|---|------------------|------|------|------|---|
| V _{OH} | High-level output voltage | V _{DD} = 2V to 6V, I _{OH} = -20 μA | V _{DD} - 0.2V | | | V | | |
| | | V _{DD} = 3.3V, I _{OH} = -2mA | V _{DD} - 0.4V | | | | | |
| | | V _{DD} = 6V, I _{OH} = -3mA | V _{DD} - 0.4V | | | | | |
| V _{OL} | Low-level output voltage | V _{DD} = 2V to 6V, I _{OL} = 20μA | 0.2 | | | V | | |
| | | V _{DD} = 3.3V, I _{OL} = 2mA | 0.4 | | | | | |
| | | V _{DD} = 6V, I _{OL} = 3mA | 0.4 | | | | | |
| Power-up reset voltage ⁽¹⁾ | | V _{DD} ≥ 1.1V, I _{OL} = 20μA | 0.4 | | | V | | |
| V _{IT-} | Negative-going input threshold voltage ⁽²⁾ | V _{DD} = 2V to 6V, T _A = 0°C to +85°C | VSENSE3 | 1.22 | 1.25 | 1.28 | V | |
| | | | VSENSE1, VSENSE2 | 1.64 | 1.68 | 1.72 | | |
| | | | | 2.20 | 2.25 | 2.30 | | |
| | | | | 2.86 | 2.93 | 3 | | |
| | | | V _{DD} = 2V to 6V, T _A = -40°C to +85°C | VSENSE3 | 1.22 | 1.25 | 1.29 | V |
| | | | | VSENSE1, VSENSE2 | 1.64 | 1.68 | 1.73 | V |
| | | | | | 2.20 | 2.25 | 2.32 | |
| | | | | | 2.86 | 2.93 | 3.02 | |
| V _{hys} | Hysteresis at VSENSEn input | V _{IT-} = 1.25V | 10 | | | mV | | |
| | | V _{IT-} = 1.68V | 15 | | | | | |
| | | V _{IT-} = 2.25V | 20 | | | | | |
| | | V _{IT-} = 2.93V | 30 | | | | | |
| | | V _{IT-} = 4.55V | 40 | | | | | |
| I _H | High-level input current | \overline{MR} | $\overline{MR} = 0.7 \times V_{DD}$, V _{DD} = 6V | | | μA | | |
| | | SENSE1 | VSENSE1 = V _{DD} = 6V | | | | | |
| | | SENSE2 | VSENSE2 = V _{DD} = 6V | | | | | |
| | | SENSE3 | VSENSE3 = V _{DD} | | | | | |
| I _L | Low-level input current | \overline{MR} | $\overline{MR} = 0V$, V _{DD} = 6V | | | μA | | |
| | | SENSEn | VSENSE1,2,3 = 0V | | | nA | | |
| I _{DD} | Supply current | | 40 | | | μA | | |
| C _i | Input capacitance | V _I = 0V to V _{DD} | 10 | | | pF | | |

(1) The lowest supply voltage at which \overline{RESET} becomes active. t_r, V_{DD} ≥ 15μs/V

(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1μF) should be placed close to the supply terminals.

Timing Requirements

 At $V_{DD} = 2V$ to $6V$, $R_L = 1M\Omega$, $C_L = 50pF$, $T_A = +25^\circ C$.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-------------|---|-----|-----|-----|---------|
| t_w | Pulse width | $V_{SENSEnL} = V_{IT-} - 0.2V$, $V_{SENSEnH} = V_{IT+} + 0.2V$ | 6 | | | μs |
| | | $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$ | 100 | | | ns |

Switching Characteristics

 At $V_{DD} = 2V$ to $6V$, $R_L = 1M\Omega$, $C_L = 50pF$, $T_A = +25^\circ C$.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|--|-----|-----|-----|---------|
| t_d | Delay time | $V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$. See Timing Diagram . | 140 | 200 | 280 | ms |
| t_{PHL} | Propagation (delay) time, high-to-low level output | \overline{MR} to \overline{RESET} \overline{MR} to \overline{RESET} | | 200 | 500 | ns |
| t_{PLH} | Propagation (delay) time, low-to-high level output | \overline{MR} to \overline{RESET} \overline{MR} to \overline{RESET} | | | | |
| t_{PHL} | Propagation (delay) time, high-to-low level output | \overline{SENSEn} to \overline{RESET} \overline{SENSEn} to \overline{RESET} | | 1 | 5 | μs |
| t_{PLH} | Propagation (delay) time, low-to-high level output | \overline{SENSEn} to \overline{RESET} \overline{SENSEn} to \overline{RESET} | | | | |

Typical Characteristics

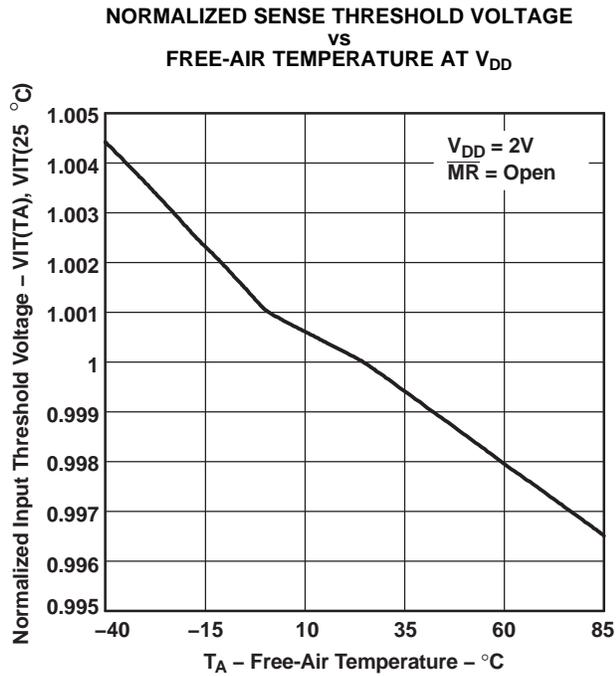


Figure 2.

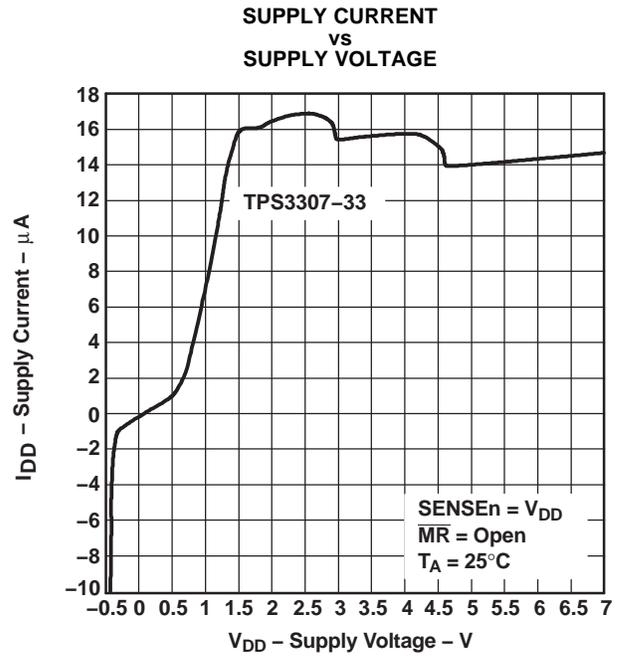


Figure 3.

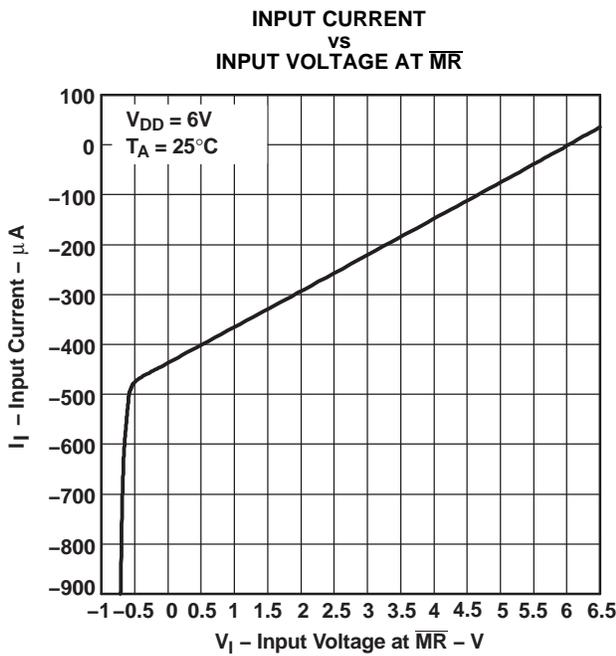


Figure 4.

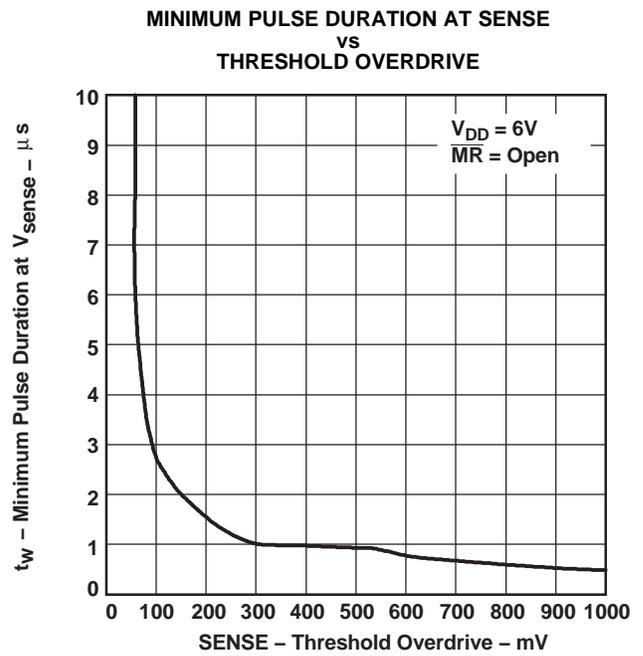


Figure 5.

Typical Characteristics (continued)

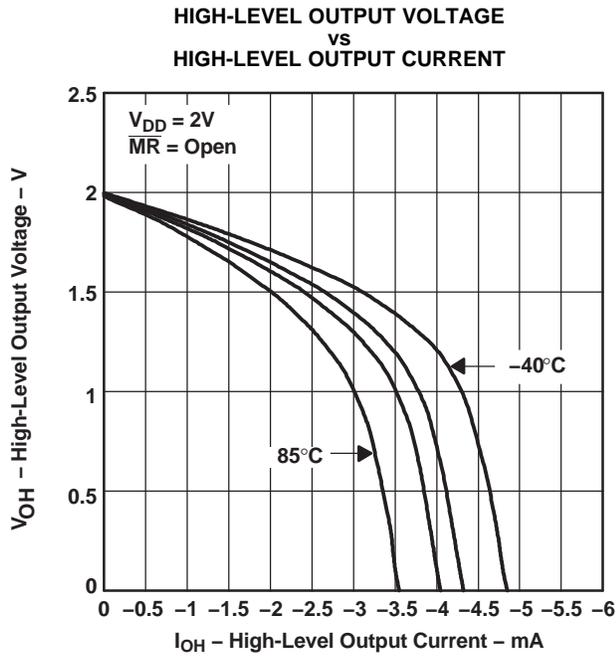


Figure 6.

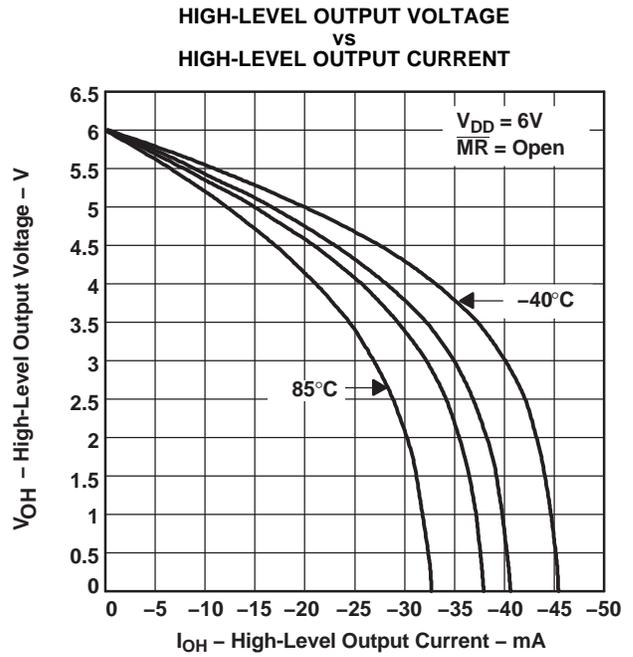


Figure 7.

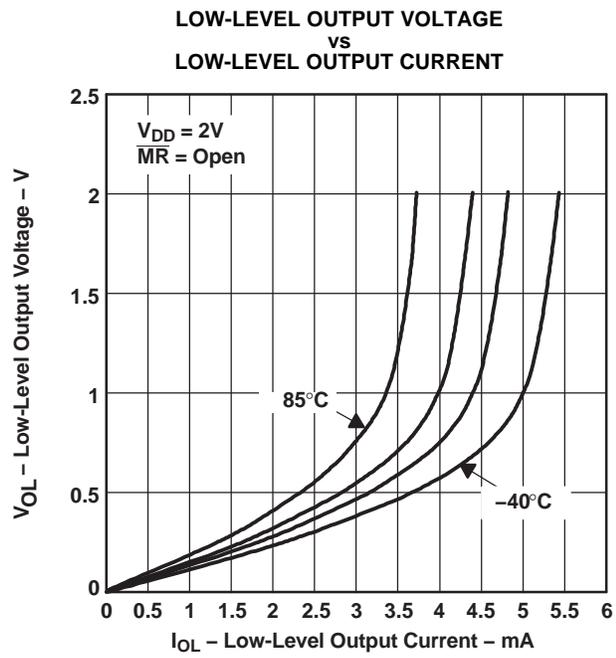


Figure 8.

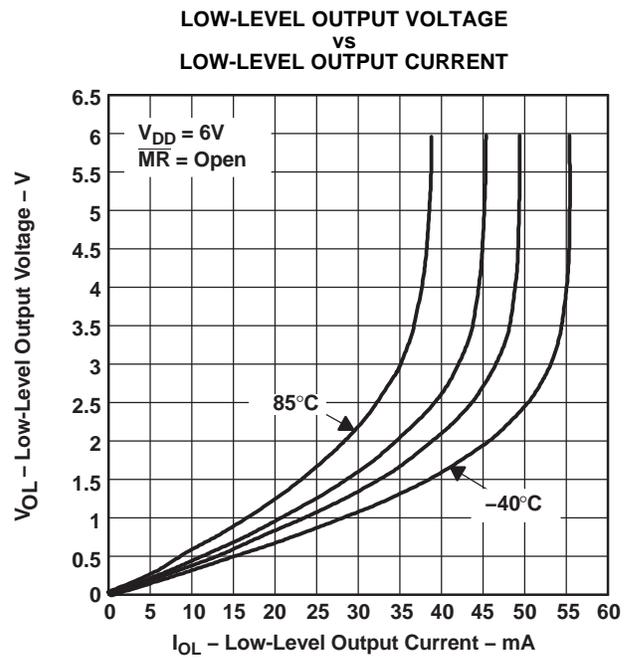


Figure 9.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|----------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TPS3307-18D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-18DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-18DGN | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-18DGNG4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-18DGNR | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-18DGNRG4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-18DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-18DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-25D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-25DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-25DGN | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-25DGNG4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-25DGNR | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-25DGNRG4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-25DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-25DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-33D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-33DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-33DGN | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-33DGNG4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-33DGNR | ACTIVE | MSOP- | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|----------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| | | Power PAD | | | | no Sb/Br) | | |
| TPS3307-33DGNRG4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-33DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS3307-33DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

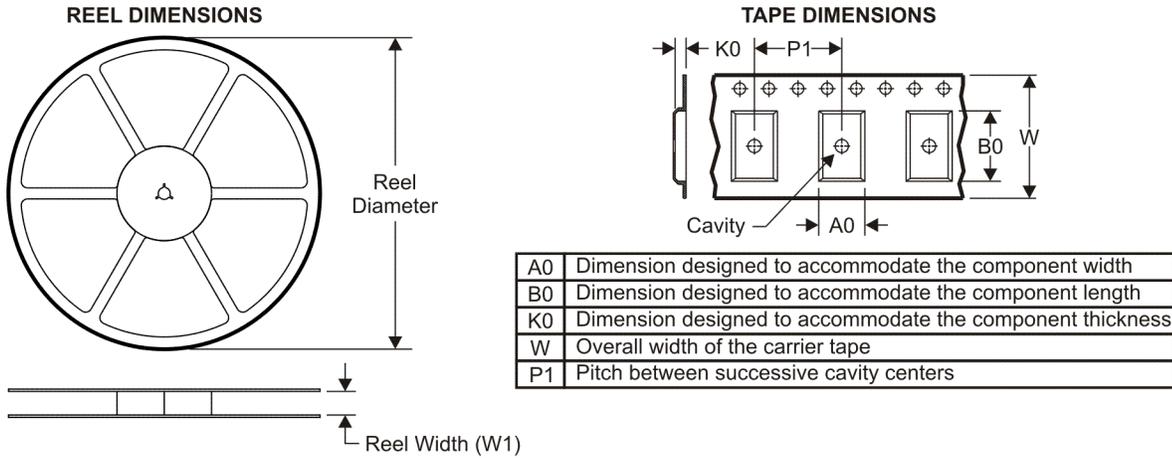
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

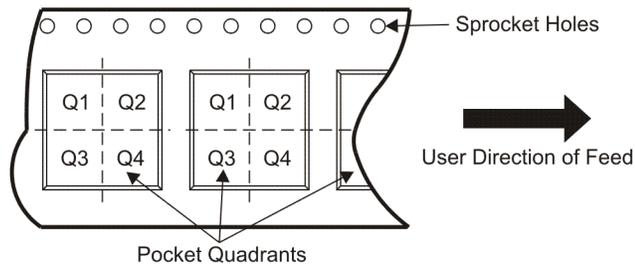
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TAPE AND REEL INFORMATION



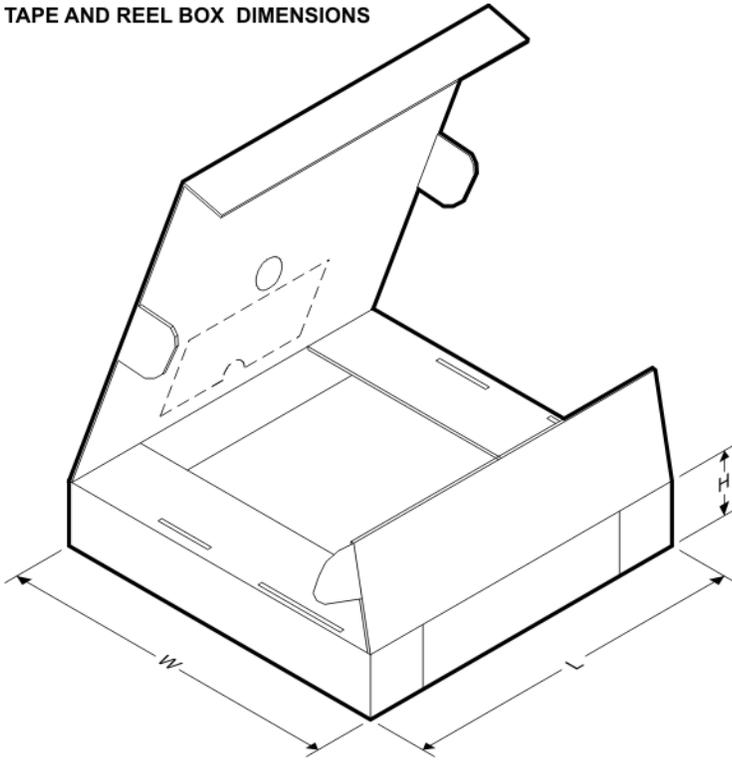
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|----------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS3307-18DGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS3307-18DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS3307-25DGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS3307-25DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS3307-33DGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS3307-33DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

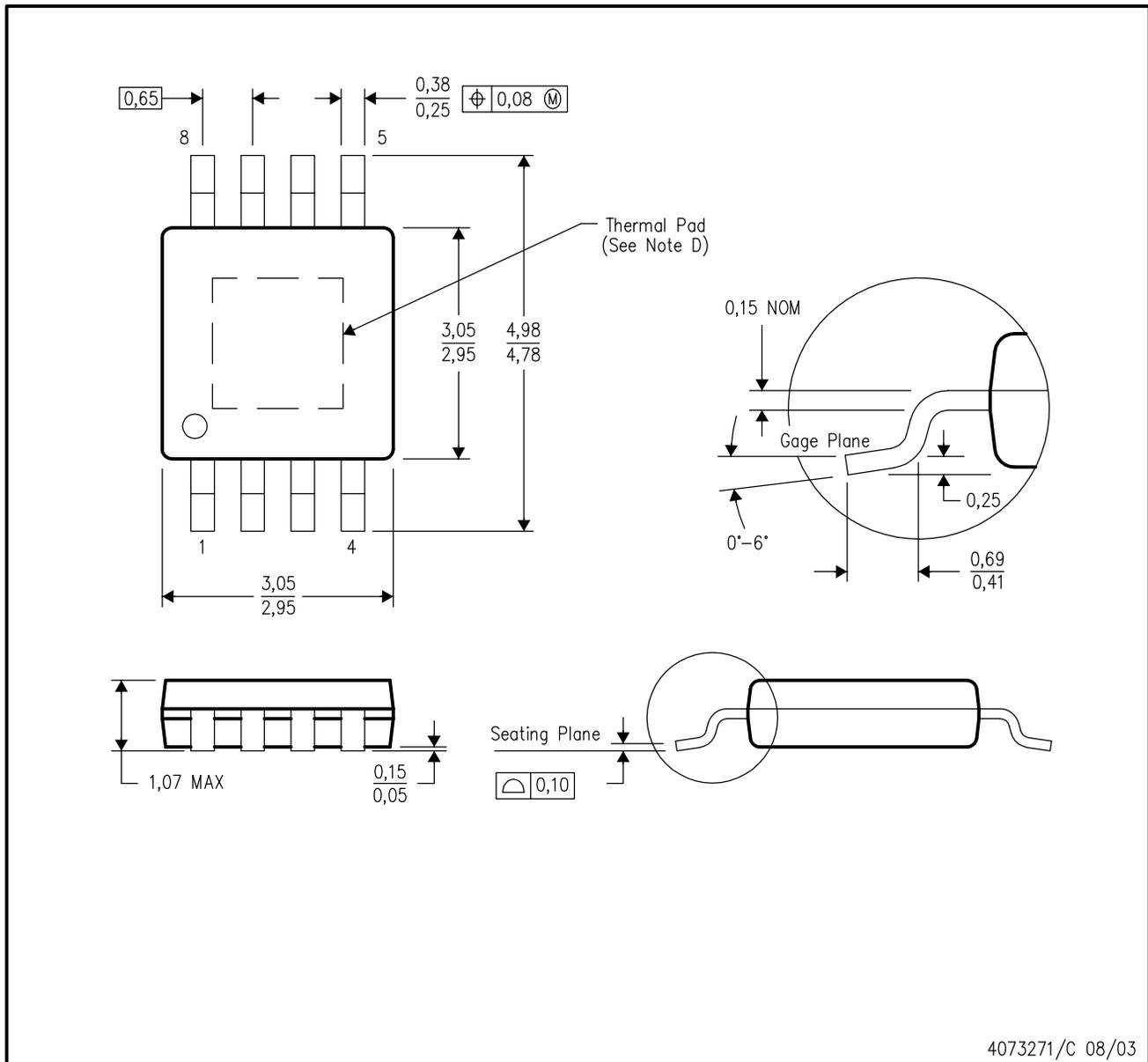


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|---------------|-----------------|------|------|-------------|------------|-------------|
| TPS3307-18DGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS3307-18DR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| TPS3307-25DGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS3307-25DR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| TPS3307-33DGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS3307-33DR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



4073271/C 08/03

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - Falls within JEDEC MO-187

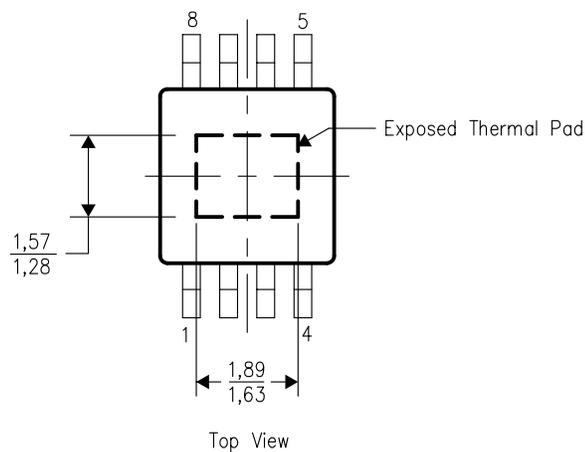
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

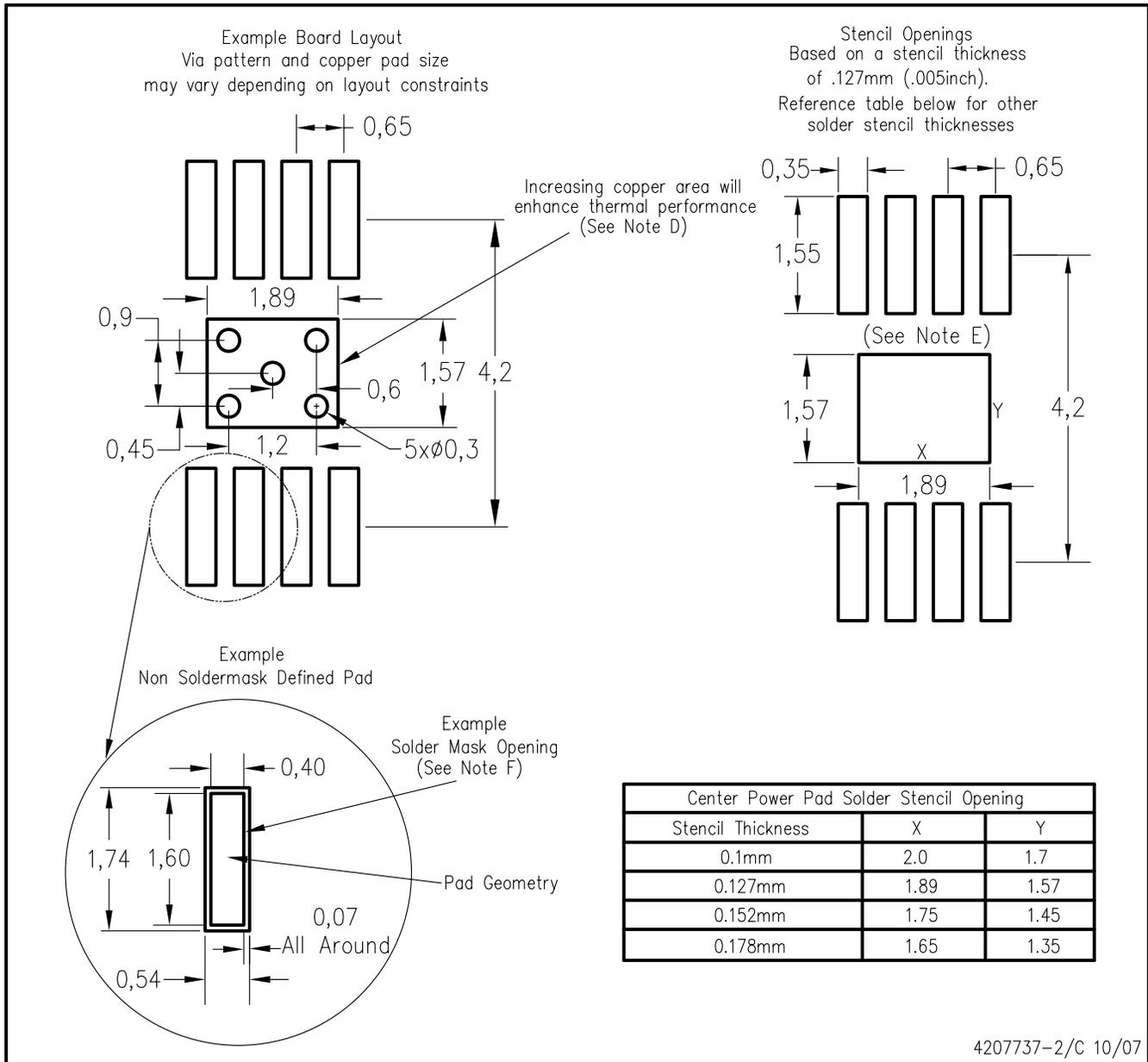
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

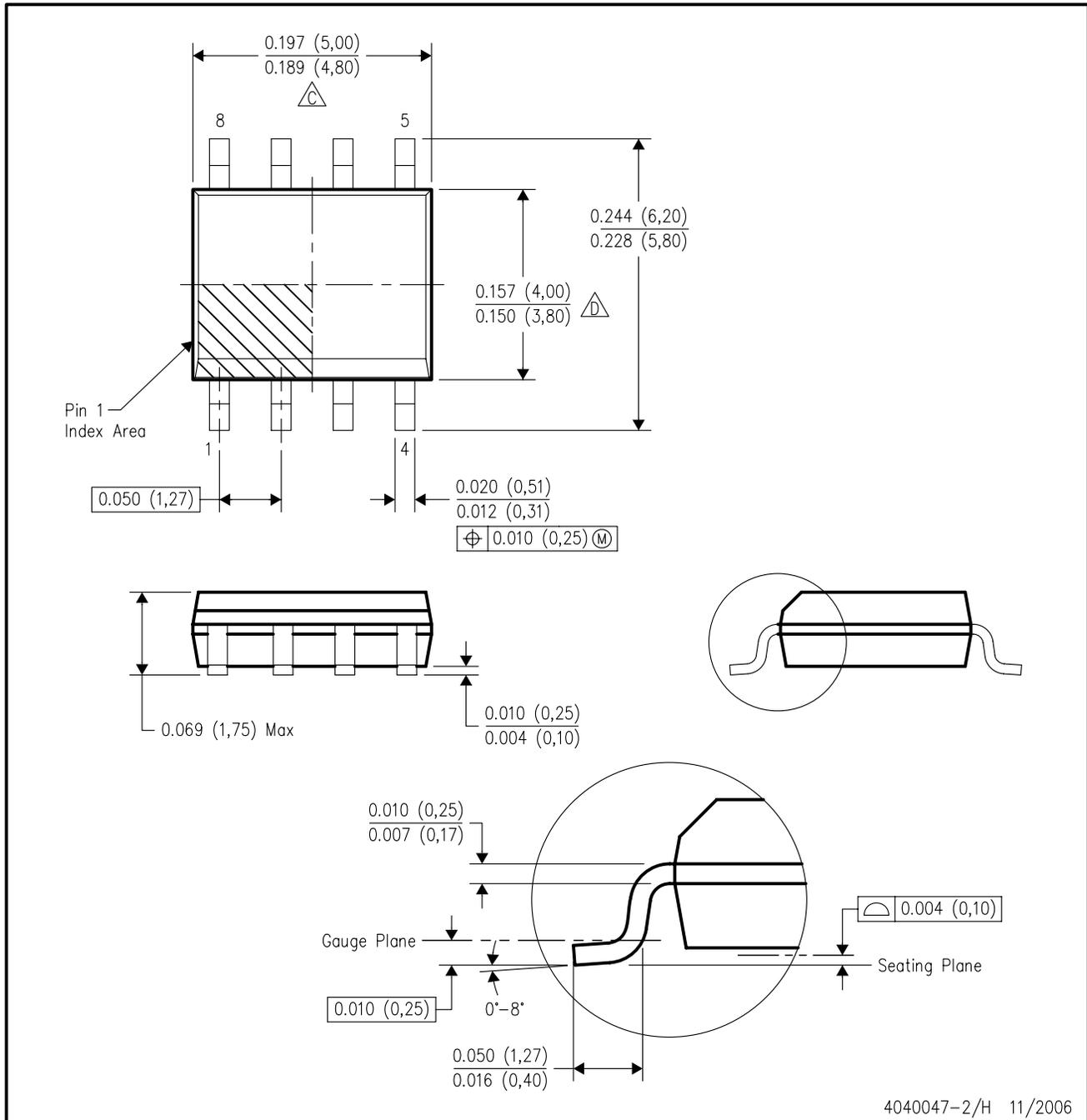
DGN (R-PDS0-G8) PowerPAD™



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

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