Under the Hood of Low-Voltage DC/DC Converters

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ABSTRACT

With the evolutionary decrease of DSP core and I/O power supply voltage levels, comes the need for efficient power conversion from existing bus voltages to newer and lower, voltages. At the same time, DC/DC converters are continuing their own evolutionary trend towards smaller size and lower cost. Caught in the middle are the circuit designers who have little experience in development of DC/DC converters, yet must incorporate them in their own systems. This topic provides a guide for engineers to follow in designing a point of use DC/DC converter. Technical challenges encountered designing for low voltage operation, and tradeoffs of different component types are presented to allow designers to make choices based on their own particular circuit or system needs. Using an example design, concepts are reviewed with attention made to underlying principals and practical ramifications.

I. INTRODUCTION

Converting one low voltage to a lower voltage provides a number of challenges to power supply design, some of which are unique. For an equivalent system power level, low voltage implies higher currents, therefore higher conduction loss and lower tolerance for voltage deviation. As a benefit, low voltage also implies lower switching loss than that found in a high voltage counterpart.

In this paper, a background discussion of basic buck converter operation creates a foundation for detailed explanation of converter operation and component selection issues. From this, the designer should be able to decide which fundamental design philosophy should be followed, whether it is to optimize for circuit performance, component cost, or power density. The interdependencies of parameters within a DC/DC converter are also discussed, allowing a designer to understand and trade off conflicting design goals. For example, if fast transient response or high power density is paramount, then a high operating frequency is in order. Conversely, if high efficiency is the most important parameter to achieve, then a low switching frequency may be the best choice.

Another fundamental issue is the method of construction and the level of manufacturing for the converter. Surface mount technology, used extensively for electronics construction, continues an ever-evolving trend towards smaller component packages. While this makes it easier to meet power density goals, it also becomes more difficult to maintain good thermal design. Small packages reduce printed circuit board parasitics, however they also may require some sort of heat sinking to keep temperatures low and reliability high.

II. TOPOLOGY OVERVIEW

A. Synchronous Buck Converter Operation

A buck converter operates by applying a pulse width modulated (PWM) waveform to an L-C filter. The filter then averages the PWM waveform, resulting in a DC output voltage. A variation on a simple buck replaces the "catch" diode with a controlled switch, or Synchronous Rectifier (SR). See Fig. 1. A synchronous rectifier generally has lower losses than a conventional or Schottky diode, and so its use is quite popular in low voltage DC/DC converters.

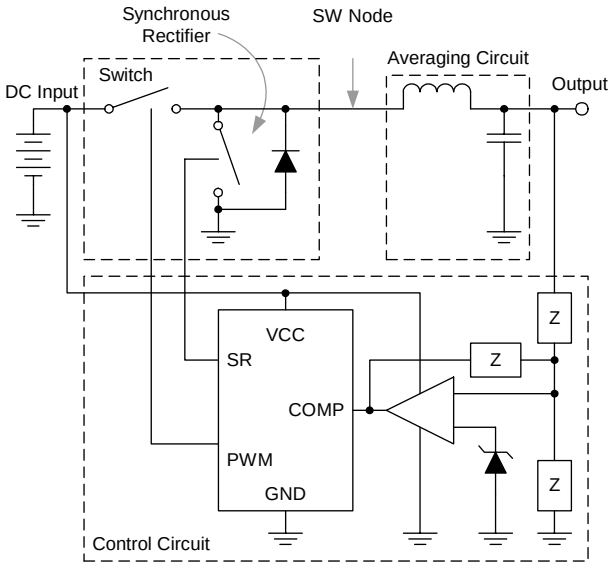

Fig. 1. Synchronous buck converter schematic.

To begin a discussion of DC/DC converters, a few fundamental relationships need understanding. In an ideal (lossless) buck converter, the input voltage and the duty cycle of the switch determine the output voltage.

$$Vout = D \bullet Vin = \frac{t_{on}}{Ts} \bullet Vin$$

Where the duty cycle is defined as the ratio of the main switch ON time to the total period. This relationship holds as long as there is continuous current flowing in the inductor.

Another important relationship relates the inductor value to the amount of AC ripple current in the converter.

$$\Delta Iout = \frac{(Vin - Vout) \bullet D \bullet Ts}{L}$$

Where ΔIout is the peak-to-peak ripple current in the output inductor. Notice the effect the input to output voltage differential has on the result.

The next step is to follow the operation of the circuit for one switching cycle. Referring to Fig. 2.

- At some time just prior to t0, a signal from the control IC turns OFF the SR.
- At t0, the PWM signal turns ON the main switch and the inductor current starts to transition from the SR to the switch.
- At t1, the SW node voltage rises above the Vout voltage level and the current in the switch and the inductor begins to increase.
- At t2, the switching transition is complete.
- At t3, the PWM signal turns OFF the switch, and the inductor current begins to transition to the body diode of the SR.
- At t4, the SW node voltage falls below Vout and the current in the SR and in the inductor begins to decrease.
- At t5, the transition is complete and the inductor current continues decreasing. At this time, the current is still fully in the SR body diode.
- At t6, the gate signal driving the SR turns ON the SR and the current transitions from the body diode of that MOSFET to its channel. Evidence of this is the SW node going closer to GND than the body diode voltage of the MOSFET had allowed. Notice that during the t6-t7 interval, the voltage across the $R_{DS(on)}$ of the SR decays because of the decay of the current in the inductor.
- At t7, the SR gate signal turns OFF the SR and the inductor current transitions from the channel back to its body diode.
- At t8, the cycle starts again with the PWM signal turning on the main switch MOSFET.

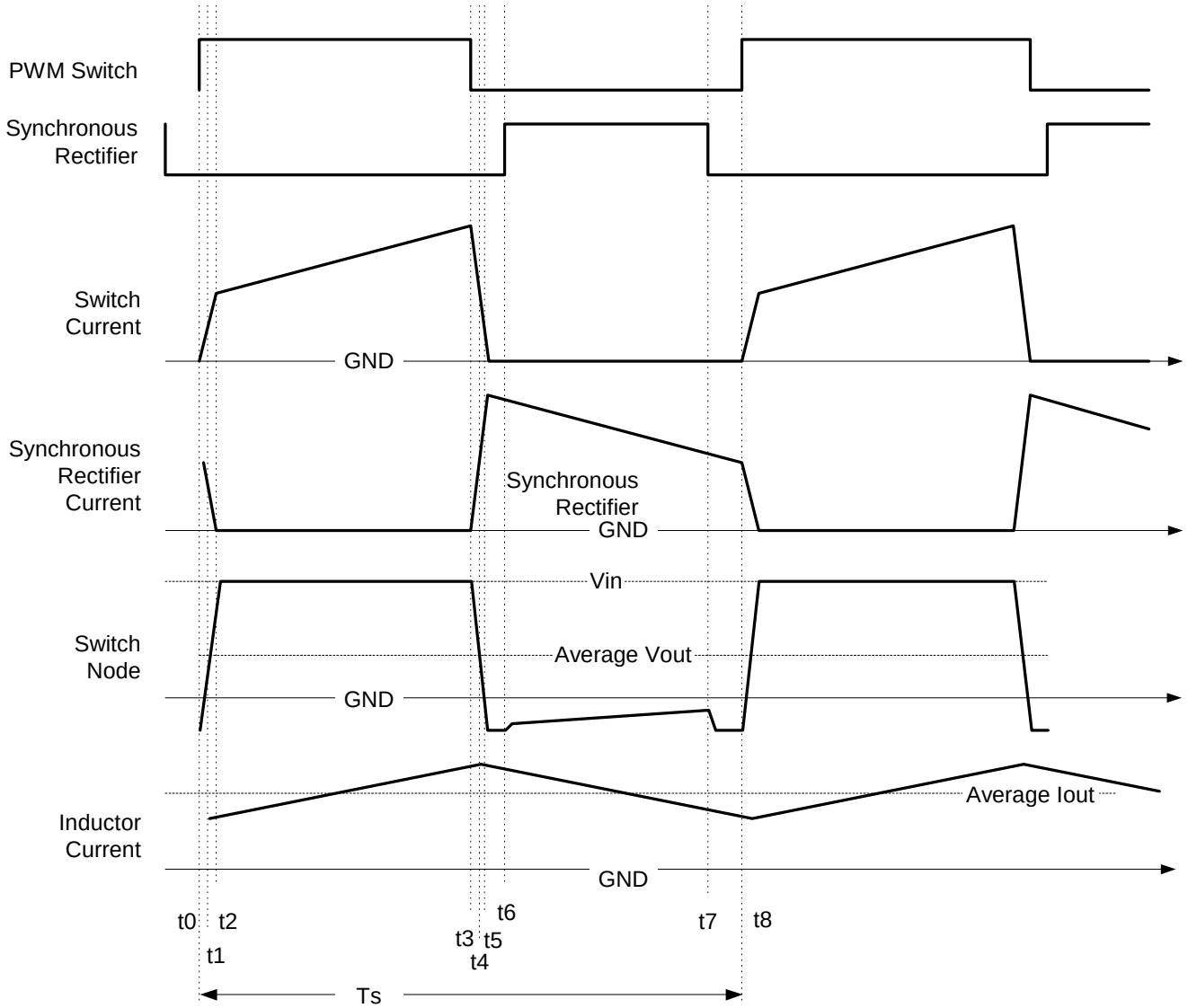

Fig. 2. Synchronous buck converter waveforms.

B. Discontinuous Current Operation

One of the key differences in circuit operation between a synchronous and a non-synchronous converter occurs at light loads when the converter's DC load current is less than half the magnitude of the peak-to-peak ripple current (ΔIout) in the output inductor. In a non-synchronous buck converter, when the inductor current valley attempts to go below zero, current no longer flows due to the rectifier diode's blocking effect (see Fig. 3). In this condition, the inductor is running "discontinuous" because current flow is interrupted. When this occurs at t4, the SW node rings up to the output voltage (t4 to t5) and settles at that level until the next switching cycle begins at t6. This low energy ringing is generated by the energy in the inductor resonating with MOSFET parasitic capacitance.

When the inductor goes discontinuous, the duty cycle required to maintain output voltage regulation is no longer simply the ratio of the output voltage to the input voltage, but is determined by the relationship:

$$D = \sqrt{\frac{2 \bullet L}{Zout \bullet Ts}\left(\frac{Vout^2}{Vin^2 - Vin \bullet Vout}\right)}$$

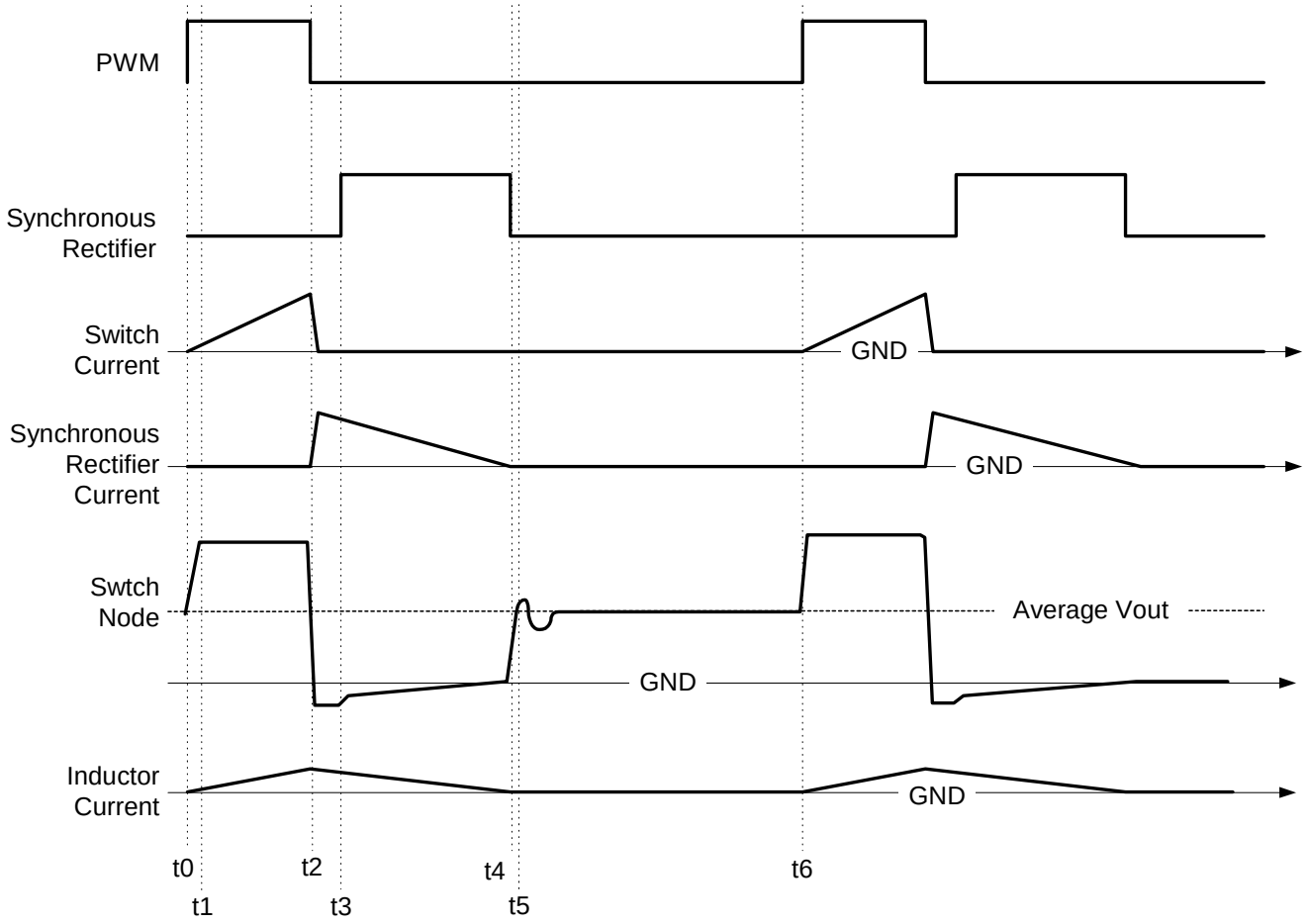

Fig. 3. Operation with discontinuous inductor current.

Notice that D is no longer a linear function of the input-to-output ratio. This is because the inductor acts as a current source feeding the output impedance of the converter. The issue that arises from this effect is that the closed loop gain of the converter is reduced, and is no longer a linear function. Care should be taken to verify loop stability and response characteristics under both conditions.

The synchronous converter can either allow current to flow in only one direction as a non-synchronous converter does, or, by allowing the synchronous rectifier to remain ON for the entire t3 to t5 interval, can operate so that current is allowed to flow in the reverse direction. The advantage is clear from the earlier discussion. If current is continuous in the output inductor then the output voltage remains a linear function of the duty cycle and the loop stability remains constant over the entire load current range. A disadvantage is that under light loads, there is now power dissipated in the channel of the SR MOSFET and in the inductor as current flows in the reverse direction.

A second advantage to allowing reverse current to flow in the SR is that the converter is now capable of sinking current from the output if the output has excess energy. As a consequence, any power absorbed at the "output" of the converter while it is sinking current is returned to the "input" of the converter. To prevent the input supply from being pumped up, the input source must be capable of absorbing this excess energy.

C. Cross Conduction and Gate Switching Delay

In a synchronous converter, where devices are turned ON and OFF alternatively, the potential exists for both devices to be momentarily turned ON at the same time, leading to a high shoot through current from the input source to the ground return and most likely, catastrophic results. To prevent this, a turn OFF to turn ON delay is added to the gate drive signals. In Fig. 4, the switch turn ON is delayed

slightly from the turn OFF of the SR, and the turn ON of the SR is delayed slightly from the turn OFF of the switch. As shown earlier, during these delayed times, current does not flow in the conduction channel of the SR, but in the parasitic body diode of the SR MOSFET. Too much time delay has the effect of increased power dissipation because the power loss in the body diode is usually much greater than the losses in the channel for a given current.

The design goal is to minimize the amount of time to delay from the turn OFF of one device to the turn ON of the other without causing cross conduction.

Unfortunately, the required delay is not a fixed requirement. Output load current, MOSFET drive capability and MOSFET device characteristics all influence delay, and so a self adjusting (or adaptive) method is necessary to avoid having to set a relatively long period of time.

In the adaptive approach, the switch node (SW) or a MOSFET gate signal is monitored for the crossing of a pre-determined voltage level. When the node crosses that level, then the device being monitored is assumed to be OFF, and so the next device is allowed to turn ON. While this approach compensates for component and load variations, it is also a reactive approach – one event has to occur before the next step can take place. There is an inherent delay in this approach, as the signal has to propagate through the control IC. When the turn-on of the MOSFET is included, this delay may be as long as 50 ns to 75 ns.

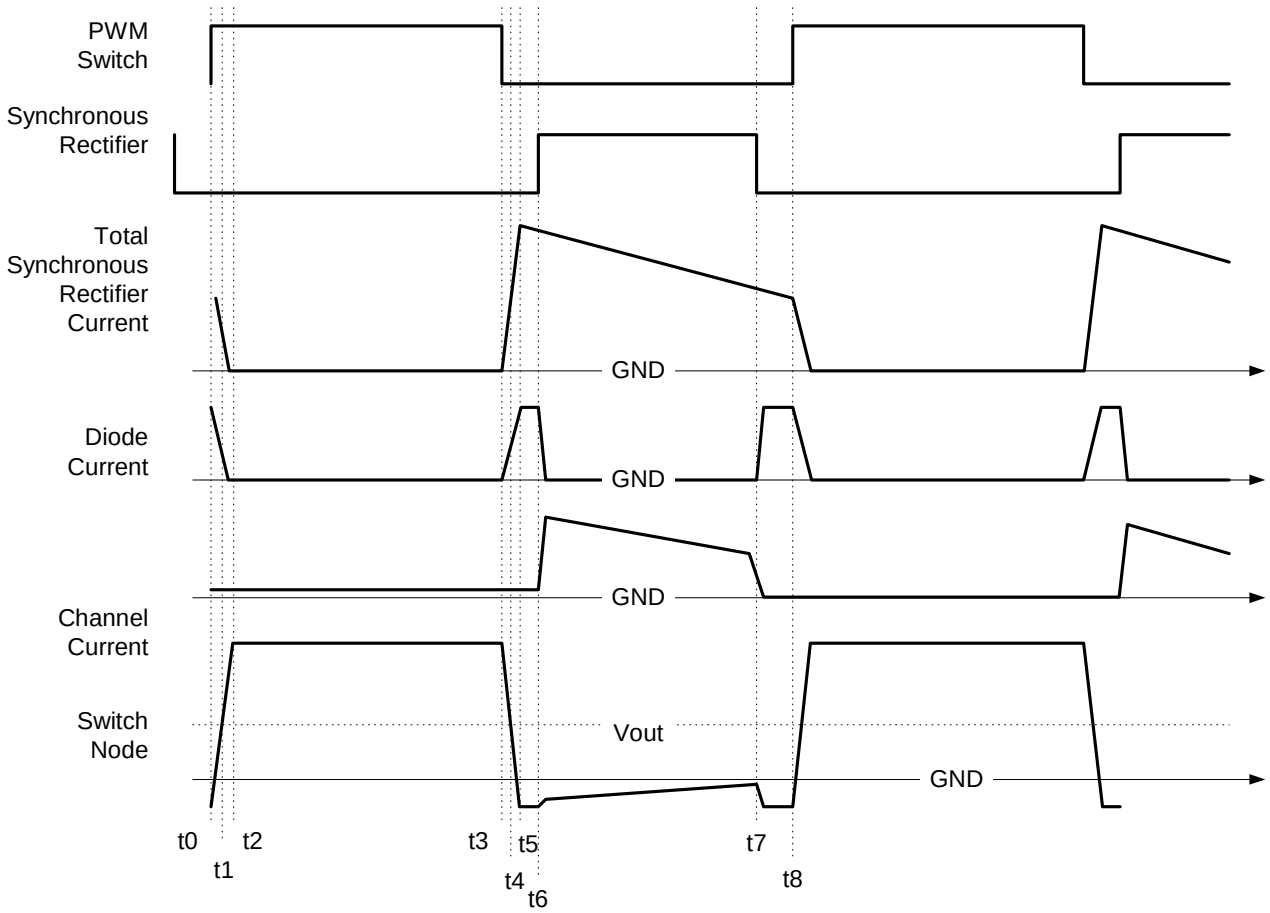

Fig. 4. Waveforms of current through MOSFET junction & body diode of synchronous rectifier.

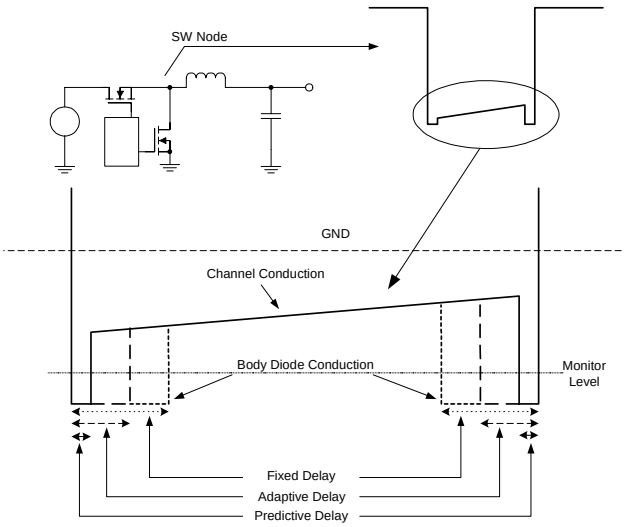

Fig. 5. Delay time for three approaches.

As switching frequencies continue to climb to the MHz range and output voltages creep lower, a new predictive approach is used to further reduce power loss. By monitoring the switch node as it transitions below a ground reference, (*monitor level* in Fig. 5) the control IC determines whether the body diode of the SR has begun to conduct. By using this information, the control IC then adjusts the delay for the next switching cycle to minimize or eliminate body diode conduction. This monitoring occurs continuously for both edges of the SR's conduction interval, assuring the "optimum" delay period is only one cycle away. Fig. 5 is a simplified illustration showing the relative delay times for the three approaches.

D. Synchronous Rectifier Parasitic Turn On

Another issue related to synchronous buck operation is parasitic turn-on of the synchronous rectifier MOSFET. Since the nature of low voltage converters requires the use of low gate threshold MOSFETs, care must be taken to insure that the SR is not turned ON inadvertently. The failure mode is this: High dv/dt on the SW node when the SR is turned OFF can raise the voltage on the SR gate (through capacitive coupling from the drain-to-gate) to the point where the SR is momentarily turned ON. Refer to Fig. 6 for the following discussion.

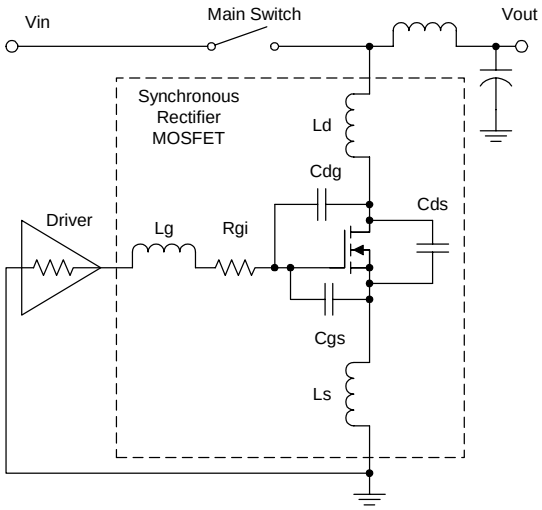

Fig. 6. Synchronous rectifier parasitic components.

In the box labeled Synchronous Rectifier MOSFET, Lg, Ld and Ls represent the inductance inherent to the device package leads. The gate resistor Rgi is the characteristic MOSFET gate resistance and is dependent on the type of MOSFET and its construction. The three "capacitors" are also inherent to the device construction and their values are found in manufacturers' data sheets.

When the SW node starts to rise, the drain voltage of the SR MOSFET rises as well. The rate of rise causes currents to flow in the parasitic MOSFET capacitors. Current through Cdg must go into either Cgs or be shunted through the gate lead and returned to GND by the driver. Current not shunted around the MOSFET causes the voltage on Cgs to rise. If this voltage rises to the threshold voltage of the MOSFET, the rectifier MOSFET turns on and shoot through current flows. The oscilloscope waveform in Fig. 7 shows an SR gate "spike" during the rising edge of the SW node.

The best line of defense to parasitic turn ON is to keep the impedance from the gate to source of the SR as low as possible. Close attention should be paid to the layout of the gate drive circuit. The circuit should be low resistance, (a wide, short track) and low inductance (a wide track with a GND return path directly beneath it). Minimize the loop area in the circuit and use a ground plane effectively. Also, use a driver or

control IC that has a very low pull down (or sinking) impedance. Also, reducing the rate of rise of the SW node with either a snubber or by limiting gate drive to the main switch can help to minimize the problem.

In Fig. 7, the gate voltage of the SR can briefly exceed the minimum specified threshold of a low Vgs MOSFET (about 0.4 V). Since the amount of time that the gate voltage spends above the threshold is small, at roughly 5 ns to 6 ns, the results are perfectly acceptable in most applications. If the SW node dv/dt were increased much beyond the above value or extended in duration, significant shoot through current could occur. Appendix E gives a simulation model helpful for predicting parasitic turn ON.

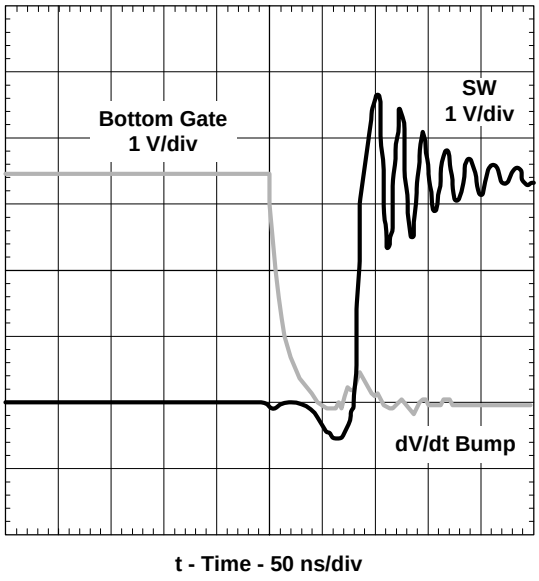

Fig. 7. SR gate waveform.

III. CONVERTER COMPONENT SELECTION

A. *Inductor Selection*

With the large number of companies competing to sell size optimized, high performance inductors for DC/DC applications, an in-depth understanding of magnetic component design is typically not required for a successful design. It is still important to consider how the operating conditions of the supply affects the inductor's performance in order to minimize losses and avoid core saturation. The optimum inductor value for a particular supply is dependent on the switching frequency, transient performance, and the conduction losses in the inductor and other components. Some of the merits for selecting a low vs. high inductor value for a given core size and geometry are summarized below:

Benefits of Lower Inductor Values

- Low DCR: lower DC inductor losses in windings
- Fewer turns: higher DC saturation current
- High di/dt: faster response to load step / dump (see Section F)
- High di/dt: fewer output capacitors required for good load transient recovery

Benefits of Higher Inductor Values

- Low ripple: lower AC inductor losses in core (flux) and windings (skin effect) (see Appendix B)
- Low ripple: lower conduction losses in MOSFETs (see Section B)
- Low ripple: lower RMS ripple current for capacitors
- Low ripple: continuous inductor current flow over wider load range (See Section B)

In general, lower inductor values are best for higher frequency converters, since the peak-to-peak ripple current decreases linearly with switching frequency. A good rule of thumb is to select an inductor that produces a ripple current of 10% to 30% of full load DC current. Too large an inductance value leads to poor loop response, and too small an inductance value leads to high AC losses.

The losses in the inductor are composed of conduction losses due to RMS current and to a lesser degree, AC losses in the wire due to skin effect, and hysteresis/eddy current losses in the core (A further discussion is in Appendix B).

The RMS conduction loss due to the winding resistance is:

$$PL_{RMS} = IL_{RMS}{}^{2} \bullet RL$$

Where $$IL_{RMS} = \sqrt{Iout^{2} + \frac{\Delta IL_{PP}{}^{2}}{12}}$$

Manufacturers offer several inductors for a particular core, where the lower inductance values have fewer turns of heavier gauge wire ($L \propto N^2$) than the higher values. Because of this relationship, lower inductor values have less winding resistance but create higher RMS currents as the ripple increases.

B. Switch MOSFET

The primary tradeoff in selecting a MOSFET is to balance package type, cost, and power loss.

These three factors are usually related, and so the designer needs to weigh the priorities. For small size, D-PAK and SO-8 packages are commonly used in on board DC/DC converters. The final choice depends on the ability for the package to adequately remove heat generated by the MOSFET die in the application, and to transfer it to the environment in order to keep the junction temperature within acceptable limits.

When selecting the MOSFETs, there is a fundamental choice of whether to use a N-channel or P-channel device for the upper switch. N-channel MOSFETs have the advantage of lower on resistance for a given die size and often have lower gate charge. They also tend to be relatively inexpensive. Their chief drawback is that they need a "bootstrapped" drive circuit or a special bias supply for the driver to work, since the gate drive must be several volts above the input voltage to the converter to enhance the MOSFET fully. Conversely, P-channel MOSFETs have simpler gate drive requirements. They require that their gate be pulled a few volts below the input voltage for them to be turned on. Their disadvantage is that their cost is higher as compared to their N-channel counterpart for an equivalent $R_{DS(on)}$, and they generally have slower switching times.

The losses in the upper switch MOSFET are found by breaking down the losses into various elements: conduction losses, switching losses, and gate losses. The conduction losses are a function of the load current, the switching frequency, and the value of the ripple current. The peak-to-peak ripple current in the output inductor is:

$$\Delta IL_{PP} = \frac{\left(Vin - Iout \bullet \left[R_{DS(on)}SW + RL\right] - Vout\right) \bullet D \bullet Ts}{L}$$

Adding the contribution to the overall current in the upper MOSFET, the RMS of this current is used in determining the AC conduction loss.

$$ISW_{RMS} = \sqrt{D \bullet \left(Iout^2 + \frac{\Delta IL_{PP}{}^2}{12}\right)}$$

and

$$PSW_{conduction} = ISW_{RMS}{}^2 \bullet R_{DS(on)}SW$$

The values of the output inductor and the switching period have a direct impact on the conduction loss. For a fixed frequency, the value of the inductor determines the amplitude of the peak-to-peak ripple current, which, as the equations indicate, affects the conduction loss. Fig. 8 shows a curve of power loss in the switch and SR for ripple current values at a single switching frequency. Notice the power loss increases by about 5% with 30% ripple current, confirming that the ripple current should be kept below 30% of the overall load current.

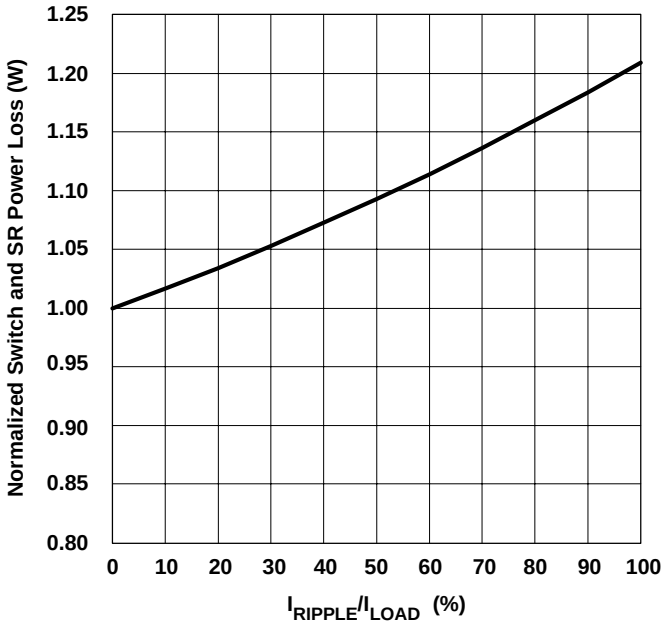

Fig. 8. MOSFET Power dissipation for various ripple current values at a single switching frequency.

The switching loss in the MOSFET is calculated by this lengthy statement.

$$PSW_{switching} = Vin \bullet Fs \bullet \left(\frac{ISW_{pk} \bullet (QgdSW + QgsSW)}{Ig} + \frac{QossSW + QossSR}{2} \right)$$

Here the impact each term has on switching loss can be seen. Notice that the Qoss of the synchronous rectifier plays a minor role in the losses of the switch.

The final power loss is associated with driving the gate:

$$PgSW = QgSW \bullet Vg \bullet Fs$$

In each of the three loss equations, there is frequency dependence. Fig. 9 shows a set of typical curves of losses in a switch MOSFET as a function of switching frequency in a typical application. Clearly, the gate losses and the switching losses show the most variation with switching frequency.

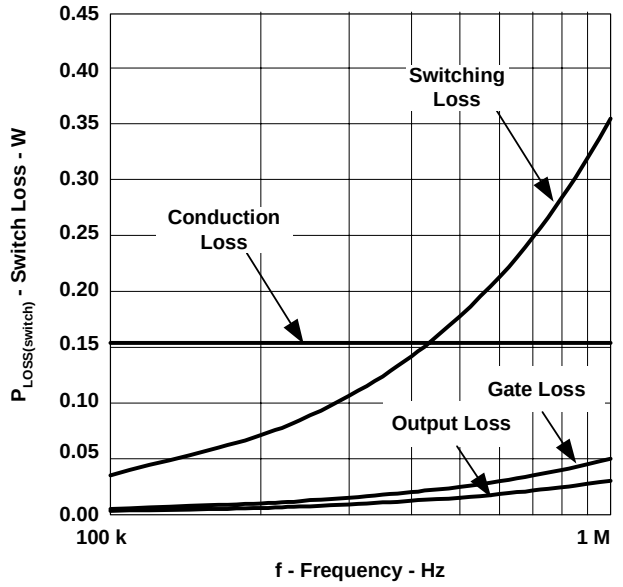

Fig. 9. Upper MOSFET losses as a function of frequency.

C. Synchronous Rectifier Selection

The conduction losses in the Synchronous Rectifier (SR) are comprised of two elements: The losses through the channel of the MOSFET, and in the parasitic body diode. In the body diode, the average power loss is

$$Pdiode_{avg} = Vfr \bullet Iout \bullet \left(\frac{Tdelay1 + Tdelay2}{Ts} \right)$$

Where Tdelay1 and Tdelay2 are the gate driver and MOSFET turn-on delay times and are the only times current flows through the body diode.

The RMS current in the SR is found in a similar fashion to that in the upper switch, however instead of using (1-D) as the duty cycle, the time delay is subtracted from the SR conduction time. This is the amount of current that is reduced in the channel of the device.

$$ISRchannel_{RMS} = \sqrt{(1 - D - \frac{Tdelay1 - Tdelay2}{Ts}) \bullet (Iout^2 + \frac{\Delta IL_{pp}^2}{12})}$$

Moreover, the loss is

$$PSRchannel_{conduction} = ISRchannel_{RMS}^2 \bullet R_{DS(on)}SR$$

While the conduction loss in the SR channel is reduced by increasing the time delays, the loss in the SR device as a whole increases because the ON loss in the SR channel is usually less than the loss in the SR body diode for the same current. The switching loss in the gate of the SR is found in a similar manner to that of the upper MOSFET.

$$PgSR = QgSR \bullet Vg \bullet Fs$$

Figure 10 shows these losses as a function of switching frequency.

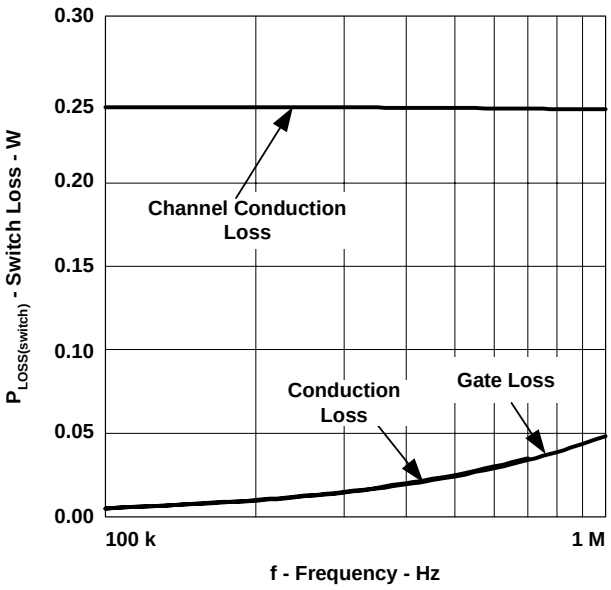

Fig. 10. SR losses as a function of switching frequency.

For illustrative purposes, the curves are plotted with a gate drive delay time of 20 ns and 10 A of current. With this delay time, the conduction losses have significant frequency dependence. The SR diode's power loss increases with frequency at a rate higher than the decrease in loss in the MOSFET's channel. By comparison, with only 2 ns of body diode conduction, the curves would be essentially flat over this frequency band.

D. PWM Controller Selection

In selecting a PWM controller IC, the overall DC/DC converter's design criteria needs to be considered. Some key parameters are:

- Operating frequency
- Voltage amplifier GBW
- Reference voltage and tolerance
- Package size
- Gate drive capability
- Phasing of the gate drive to be compatible with P-Channel/N-Channel switch selection

Plus any other features specific to the application, such as clock synchronization, power good indicators, soft-start, etc.

From a loss standpoint, the IC dissipates power in the process of driving the two MOSFETs. Reference [1] provides background information.

$$Pgtdrive = \frac{Vgtdrv \bullet Qg \bullet Fs}{2} \bullet \left(\frac{Rghi}{Rghi + Rg + Rgi} + \frac{Rglo}{Rglo + Rg + Rgi} \right)$$

The gate drive loss is a function of operating frequency, the driver's internal resistances, the MOSFET gate charge requirement and the internal MOSFET gate resistance. See Fig. 11.

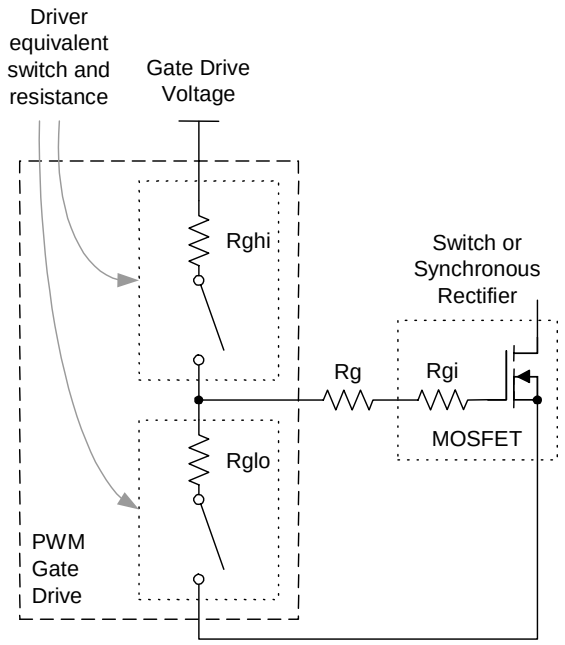

Fig. 11. Gate drive equivalent circuit.

For low voltage applications, there are a limited number of MOSFETs available that have $R_{DS(on)}$ values specified with a 2.5 Vgs. One method that opens the doors to a larger selection of MOSFETs is to use a charge pump to boost the input voltage to a higher voltage, say 4.5 V. This allows use of lower $R_{DS(on)}$ MOSFETs that have a Vgs rating at a higher voltage.

When using a charge pump, there is increased loss in the gates of the MOSFETs (because of the higher voltage) and the losses in the control IC increases due to the increased gate drive energy and the efficiency (about 80%) of the charge pump. The benefit is that the $R_{DS(on)}$ of a MOSFET is lower at a Vgs of 4.5 V than at 2.5 V, giving lower conduction loss.

Fig. 12 shows the total power loss for a DC/DC converter for two types of MOSFETs, with and without using a charge pump. Even though the losses increase with operating frequency for both cases, there is a distinct difference in losses and in the slopes for a MOSFET operated at a 2.5 Vgs and the same MOSFET operated with a higher Vgs. The tradeoff a designer must make here is to decide whether it is a better solution to use a less expensive MOSFET and a charge pump, or use a more expensive part that has a lower $R_{DS(on)}$.

The Si4836DY, which has a low $R_{DS(on)}$, benefits from the use of a charge pump only at low switching frequencies. At higher switching frequencies, the power loss in the charge pump and in driving the MOSFET gates is higher than the benefit gained by having a lower $R_{DS(on)}$.

By contrast, the Si4866DY, which has a higher $R_{DS(on)}$ and lower gate charge requirement, benefits from the use of a charge pump at all operating frequencies. This is because the decrease in losses due to driving the gate to a higher voltage, are greater than the increase in losses incurred in getting the higher gate drive voltage.

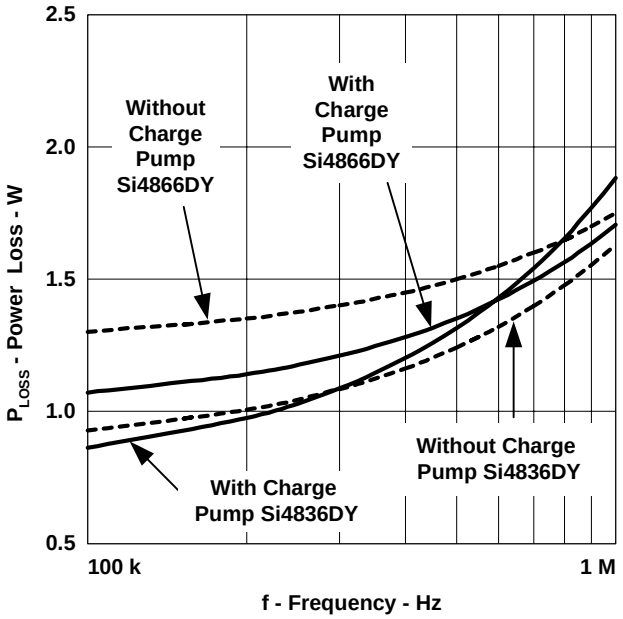

Fig. 12. Power loss comparison with and without using a charge pump.

E. Capacitor Types and Characteristics

When selecting capacitors, power loss, size and circuit noise are primary concerns. For a capacitor placed on the output, the value and type of capacitor also influences the loop bandwidth and load transient response of the converter.

The number of capacitor types available for use in power supply applications has increased over the last decade, resulting in a broad selection of parts. Common capacitor types used in low voltage DC/DC converters are aluminum electrolytic, tantalum, and ceramic. Some of the newer chemistries include solid polymer aluminum (SPA), aluminum with an organic electrolyte (OS-CON), and tantalum with organic electrolyte (POSCAP). While the variety should be viewed as a positive trend, a greater burden is placed on the power supply designer to understand the cost, availability, and performance characteristics of the various types. To make matters worse, it is often impossible to do a line-by-line comparison of parameters between different manufacturers or types, since the datasheets do not present information in a uniform matter.

Table 1 compares the performance of the various types with respect to size; ripple performance, and relative cost. It should be noted that there are several manufactures for many of these types, and the particular part number listed in Table 1 is only a representative sample. One method commonly used to quantify the effectiveness of a capacitor is the product of capacitance and voltage rating per volume (Volt x μFarad/mm^3), listed in the 4^{th} column of Table 1. Ceramic and tantalum have the best volumetric capacitance followed by conventional electrolytic.

TABLE 1. CAPACITOR TYPE RELATIVE COMPARISONS

Capacitor Type	Value (µF)	Voltage (V)	Current (A)	Case Size (mm)	Volt x µF /Volume	ESR (ESR*µF) ESL	Relative Cost/Farad
Aluminum Electrolytic/Sanyo CA/CG 06MV1000	1000	6.3	0.6	8 Dia. x 11.5	10	150 mΩ (150) 6 nH	1
OS-CON SP Series/Sanyo 4SP1000M	1000	4	5	10 Dia. x 10.5	5	12 mΩ (12) 4 nH	1.5
Solid Polymer /Cornell Dubilier ESRE181M04R	180	4	3	7.3 x 4.3 x 4.2	6	15 mΩ (2.7) 3 nH	12
POSCAP/Sanyo 4TPE220MI	220	4	2.8	7.3 x 4.3 x 1.8	16	18 mΩ (2.2) 3 nH	8
Tantalum/Kemet T495X477(1)006AS	470	6.3	1.6	7.3 x 4.3 x 4.0	23	50 mΩ (23.5) 3 nH	4
Ceramic /TDK C3225X5R0J476M	47	6.3	-	2.5 x 3.2 x 2.5	15	1 m (0.047) 0.5 nH	25
Ceramic/TDK C2012X5R0J106M	10	6.3	-	1.2 x 2.0 x 1.2	22	2m (0.02) 1 nH	25

ESR is compared in the next column using a benchmark of ESR x µF, because the capacitor values are different between types. If multiple capacitors are placed in parallel, the ESR and ESL values can generally be divided by the number of devices, although the PCB interconnect limits the improvement at some point. In the ESR category, ceramic is the clear winner followed by solid polymer and POSCAP. Conventional aluminum has relatively poor ESR performance, making its use difficult for low voltage/high current systems.

The final column is relative cost with aluminum electrolytic used as the benchmark. The cost range represents an educated guess for the technology and should not be used as a guide for a purchasing manager. As it turns out, the low ESR ceramic types have the highest cost per Farad, making their use expensive for bulk storage. Conversely, the inexpensive aluminum electrolytic types have the highest ESR and a low ripple current rating. The "correct" choice of capacitor for a particular application is on the shoulders of the designer who must weigh the various tradeoffs. It is possible in some cases to get the benefits of multiple technologies by mixing capacitor types. This can lead to a cost effective, high performance design, but may complicate the feedback analysis.

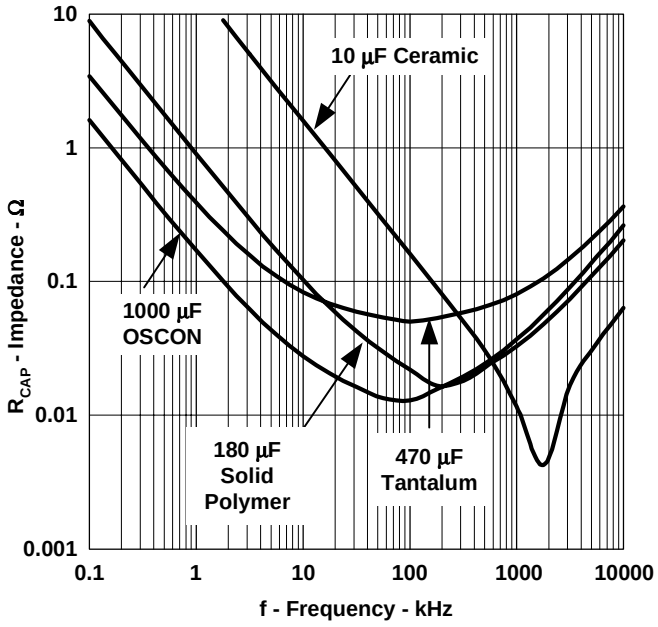

Fig. 13. Impedance curves for various capacitor types and values.

Once the capacitor types are selected, it is a good idea to "scour" the datasheet for additional information that may affect the design. This information should include (but not be limited to): leakage current, voltage coefficients, temperature and moisture effects, shelf/lifetime ratings, mechanical vibration, and failure modes. It is also a good idea to get a plot of capacitor impedance as a function of frequency as shown in Fig. 13. These graphs are found in some datasheets, but it is often necessary to use an

impedance analyzer to obtain the plot for a particular value and voltage rating. The graphs are very useful in obtaining the ESR, ESL, and resonant frequency for the capacitors.

Sizing the Input Capacitor for Ripple

Since the current delivered to the DC/DC converter is an average (DC) current and the current in the switching MOSFET is pulsating, a large capacitor is placed at the input of the converter to average the input current. To reduce conducted EMI on a system board it is advisable to contain the switching current in a small loop within the layout of the printed circuit board. (See Appendix C). The input capacitor provides a low-impedance voltage source for the converter and helps to filter the pulsating current. Important parameters in the selection process include capacitance value, ESR, ESL, and RMS current rating.

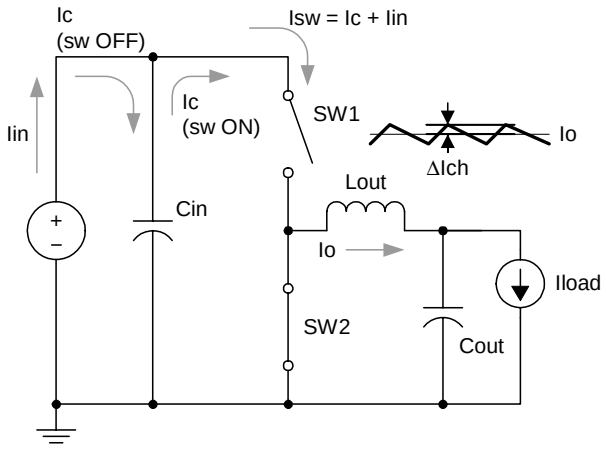

Fig. 14. Current flow in a buck converter.

The current in the input capacitor is composed of two elements. During the ON time of the switch, the capacitor current is the switch current less the DC input current, and during the switch OFF time, the capacitor is recharged by the input source. At a fixed input voltage, the steady state amp-seconds of the input capacitor balance. To find the power dissipation of the input capacitors, the two elements are combined and the RMS value is found. (See equation at bottom of page)

Using this value and the ESR of the input capacitor gives the overall loss.

$$Pincap = Iincap_{RMS}{}^{2} \bullet Resr$$

Notice that the impact the peak-to-peak contribution to the ripple current has on the overall current in the capacitor, even at high ripple current ratios, is relatively small. Smaller inductor values and/or lower switching frequencies leads to higher peak-to-peak currents, but that has little impact on the input capacitors. If a DC/DC converter is designed to operate over a wide input voltage range, then the ripple current is highest at the input voltage that places the duty cycle closest to 50%. (See Fig. 37 for a curve.)

Once the RMS input current is established and a capacitor selected, the following equation is used to calculate the input ripple voltage due to capacitance and ESR as shown in Fig 15.

$$Vin_{pp} = Iin \bullet Resr + Iin \bullet \frac{D}{Fs \bullet C} + Iin \bullet \frac{Lesl}{Tedge}$$

The first two traces in Fig. 15 show the switch and input capacitor currents for a typical buck converter. The lower traces illustrate the effects of ESR, capacitance, and ESL on input ripple voltage. The current at the switching frequency across the capacitance and the ESR generates a low frequency ripple, and the fast edges created by the SW node across the ESL creates high frequency noise spikes.

$$Iincap_{RMS} = \sqrt{\left[\left(ISW_{pk} - Iin_{avg}\right)^2 + \frac{\left(\Delta ISW_{pp}\right)^2}{12}\right] \bullet D + \left(Iin_{avg}\right)^2 \bullet (1 - D)}$$

Care must be taken to insure that the peak-to-peak ripple is not so large as to cause the UVLO circuit in the PWM controller to inadvertently shut down the converter. Also, noise spikes generated by the ESL should not be so large to cause intermittent operation of the controller or EMI.

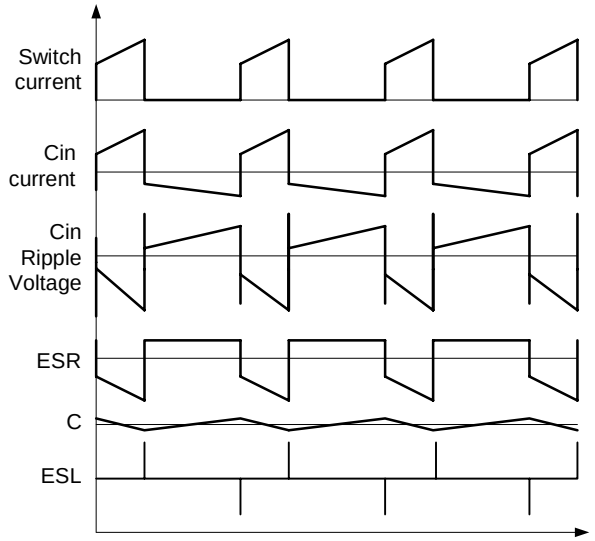

Fig. 15. Typical input current waveforms and input voltage ripple due to ESL and ESR.

F. Selecting the Output Capacitor

The output capacitor is chosen to minimize output noise voltage and to guarantee regulation during transient loads. Knowing which of these goals is predominant helps greatly in selecting the right component for the design.

Selecting based on Load Transient Response

Current transients at the output are a function of the load's characteristics and can be on the order of 100 A/µs. The value, ESR, and ESL of the output capacitor determines the magnitude of undershoot or overshoot during a transient as illustrated in Fig. 16. The top traces show the inductor and load currents on the same axis, during a sudden load step increase and decrease. The bottom trace represents the transient seen at the output of the converter.

The initial transient spike during a step load change is due to the di/dt of the load being greater than the inductor can support. The amplitude of the initial spike is given below where Istep is the magnitude of the step and di/dt is the slope. The ESR and ESL values refer to the combined effect of the output capacitors and PC board traces. The initial voltage spike can be minimized with the addition of ceramic capacitors.

$$V_{spike} = I_{STEP} \bullet Resr + \frac{di \bullet Lesl}{dt}$$

As shown in Fig. 16, the undershoot which follows the initial spike, results from the load current being supported by the output capacitor, awaiting the inductor current to catch up. The amount of time required for the current in the inductor to match the load current depends on inductor value, maximum duty cycle, and feedback loop response. If the feedback loop is designed aggressively, the buck stage can reach full duty cycle quickly, resulting in the minimal undershoot:

$$V_{under} = \frac{L \bullet I_{STEP}^2}{2 \cdot Cout \bullet D_{MAX} \bullet (Vin - Vout)}$$

The minimum overshoot during a load drop is calculated in a similar fashion. Where undershoot is affected by the difference between Vin and Vout, the overshoot is only affected by Vout.

$$V_{over} = \frac{L \bullet I_{STEP}^2}{2 \bullet Cout \bullet Vout}$$

The above equations assume that the step di/dt is longer than the inductance can support given the small Vin - Vout voltage differential, necessitating some amount of "bulk storage" capacitance at the output. If the converter has a small enough L, or a benign enough load step requirement, the bulk storage may not be necessary, in which case a design using only ceramic capacitors may be achieved.

A step increase in load is primarily supported by the output capacitors, but is partially supplied by the input. Interestingly, load drops on the output have little effect on the input capacitor since the high side switch is turned OFF during the transient. The larger effect is determined by how well the output capacitors can absorb the stored energy in the inductor when the load is suddenly removed.

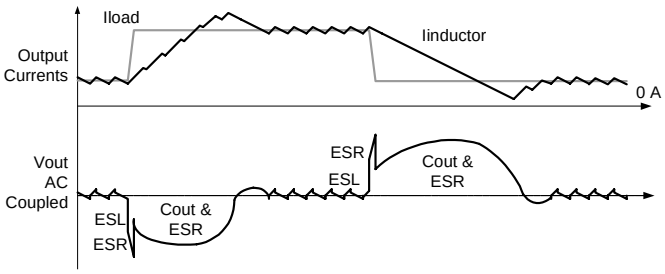

Fig. 16. Vout undershoot and overshoot during a load transient.

Output Capacitor Ripple and Power Loss

It is good design practice to compare the steady state inductor ripple current with the output capacitor's ripple current rating. As with the input capacitor, only the AC component of load current generates power loss in the output capacitor.

The voltage ripple is given by:

$$Vout_{PP} = \Delta IL \bullet Resr + \frac{Vin \bullet Lesl}{L} + \frac{\Delta IL}{Fs \bullet Cout \bullet 8}$$

The output ripple current also generates a power loss in the output capacitors. Since the ripple current is a simple saw tooth waveform, the power loss is

$$Poutcap = \frac{\Delta IL_{RMS}^2}{3} \bullet Resr$$

IV. Design Example

To illustrate the design of a synchronous buck DC/DC converter, the concepts presented are used to design a 3.3-V input, 1.2-V output converter capable of delivering up to 10 A of load current. The approach taken is to first optimize for power density and second for cost. This means low power dissipation and small size are predominantly the design goals.

The PWM controller used in this example is the TPS40003. This part is chosen for its small size, 600kHz operating frequency, its strong gate drivers, and its Predictive Delay Gate Drive™ circuitry.

The next step is to estimate the conversion duty cycle.

$$D_{est} = \frac{Vout}{Vin} = \frac{3.3}{1.2} = 36\%$$

TABLE 2. POWER LOSS CALCULATIONS

Switch MOSFET	**Si4836DY**	**FDS6574A**	**IRF7459**	**Si4866DY**	**Units**
$R_{DS(on)}$ at 100°C	0.004	0.007	0.022	0.008	Ohms
Qg	2.00E-08	4.17E-08	1.28E-08	1.17E-08	Coulombs
Qoss	9.24E-09	6.93E-09	5.61E-09	4.95E-09	Coulombs
Coss	2.80E-09	2.1E-09	1.7E-09	1.50E-09	Farads
Qgd	5.80E-09	9.44E-09	3.50E-09	1.94E-09	Coulombs
Qgs	4.44E-09	5.00E-09	3.67E-09	2.56E-09	Coulombs
Number of FETs	1	1	1	1	
Rg	1.6	1.2	1.7	1.6	Ohms
Synchronous Rectifier MOSFET	**Si4836DY**	**FDS6574A**	**IRF7459**	**Si4836DY**	
$R_{DS(on)}$ at 100°C	0.004	0.008	0.015	0.004	Ohms
Qg	2.00E-08	4.17E-08	1.28E-08	2.00E-08	Coulombs
Qoss	9.24E-09	6.93E-09	5.61E-09	9.24E-09	Coulombs
Coss	2.80E-09	2.10E-09	1.70E-09	2.80E-09	Farads
Vfr	1.1	1.1	1.1	1.1	Volts
Diode Qrr	4.40E-08	5.00E-08	7.50E-08	4.40E-08	Coulombs
Number of FETs	1	1	1	1	
Rg	1.6	1.2	1.7	1.6	Ohms
Duty cycle	38.33%	39.43%	42.57%	38.80%	
I inductor ripple peak-peak	1.91	1.94	1.94	1.90	Amperes
IswPEAK	10.96	10.97	10.97	10.95	Amperes
IswRMS	6.20	6.29	6.53	6.24	Amperes
IsrRMS	7.85	7.78	7.57	7.82	Amperes
IsrAVG	0.03	0.03	0.03	0.03	Amperes
I_incapRMS	5.34	5.37	5.44	5.35	Amperes
Switch MOSFET					
Conduction loss	0.154	0.277	0.939	0.311	Watts
Gate loss	0.030	0.063	0.019	0.018	Watts
Switching loss	0.364	0.464	0.262	0.160	Watts
Output loss	0.018	0.014	0.011	0.014	Watts
Total SW FET Losses	**0.566**	**0.817**	**1.231**	**0.503**	**Watts**
Synchronous Rectifier MOSFET					
Channel conduction losses	0.246	0.484	0.861	0.245	Watts
Diode conduction losses	0.029	0.029	0.029	0.029	Watts
Gate losses	0.030	0.063	0.019	0.030	Watts
Diode recovery loss	0.087	0.099	0.149	0.087	
Total SR FET losses	**0.392**	**0.675**	**1.057**	**0.391**	**Watts**
Inductor loss	0.250	0.250	0.250	0.250	Watts
Switch gate driver loss	0.016	0.039	0.010	0.010	Watts
SR driver loss	0.016	0.039	0.010	0.016	Watts
Output capacitor loss	0.018	0.019	0.019	0.018	Watts
Quiescent IC power loss	0.007	0.007	0.007	0.007	Watts
Snubber loss	0.007	0.007	0.007	0.007	Watts
PCB loss	0.435	0.438	0.449	0.436	Watts
Preliminary power loss	1.708	2.290	3.041	1.638	Watts
Input capacitor loss	0.199	0.202	0.207	0.200	Watts
Overall power loss	**1.91**	**2.49**	**3.25**	**1.84**	**Watts**
Converter efficiency	**86.3%**	**82.8%**	**78.7%**	**86.7%**	

A. *Inductor selection*

Using the 10-20% ripple current "rule-of-thumb", we get the following range of values for the inductor: (see equation below)

To illustrate the tradeoff between ripple current and inductor DC resistance, the converter efficiency over the load range is compared for four inductors (0.47 µH/2 mΩ, 0.68 µH/2.5 mΩ, 0.82 µH/3 mΩ, 1.0 µH/3.5 mΩ) from Vishay's IHLP-5050CE series (see Fig. 17). These low profile inductors have a case size of 13 mm x 13 mm x 3.5 mm. In this comparison, the converter with the low value/low DCR inductor has lowest overall losses at full load where the high value/high DCR inductor performs better at light load. The 0.68 µH inductor is selected for our example because it gives good efficiency over a broad load range. If a physically larger inductor were selected, then the DCR would be lower and a higher inductor value would give lower ripple and therefore lower light load losses. If the converter were designed for a nominal 6 amps of load current, then perhaps the 1.0 µH inductor would be a better choice because it yields better light load efficiency.

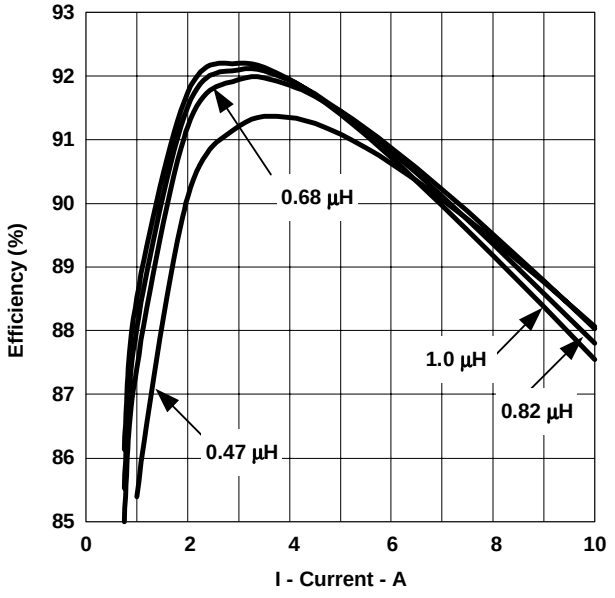

Fig. 17. Overall converter efficiency using various inductor values with a common core.

B. *MOSFET Selection*

In the earlier discussion, it was shown that the losses in the upper MOSFET, the lower MOSFET, and the gate driver were all inter-related. One method to choose the best MOSFETs for the converter is to compare the power dissipation values for a number of different MOSFET types. A survey of the industry finds a number of MOSFETs in SO-8 packages that have their $R_{DS(on)}$ values specified at 2.5-V Vgs. MOSFETs are selected from three vendors and the calculations outlined in Section 3 are entered into a spreadsheet (Table 2). Note that manufacturers specify data sheet parameters somewhat differently, causing lab results to slightly differ from the results given here.

In the upper section of the table, the MOSFETs are listed with the values used in the calculations. The same MOSFET is used as the switch and as the SR for three of the cases. In the fourth case, a low $R_{DS(on)}$ MOSFET is chosen for the SR, and a MOSFET with a low gate charge is chosen as the switch.

Comparing the MOSFETs, the Vishay Si4836 has a very low $R_{DS(on)}$ and should have the lowest conduction losses. At the other end of the spectrum is the IRF7459. This part has a higher $R_{DS(on)}$ and a much lower gate charge, and so it has lower power loss at high frequencies. The last column shows the Si4836 as the SR, and a low gate charge Si4866 as the switch. This combination (after many more comparisons than shown here) has the lowest overall power loss.

The middle portion of the table shows the results of current calculations. As expected, the higher $R_{DS(on)}$ devices create the need for higher duty cycles. By including the loss elements in the calculation of duty cycle, the effect that the $R_{DS(on)}$ and inductor resistances have is noticeable.

$$L = \frac{(Vin - Vout) \bullet D \bullet Ts}{\Delta Iout} = \frac{(3.3 - 1.2) \bullet 0.36 \bullet 1.667 \bullet 10^{-6}}{1 to 2 A} = 0.63 to 1.26 \mu H$$

$$D = \frac{Vout + Iout \bullet \left(R1 + R_{DS(on)}SR\right)}{Vin - Iout \bullet \left(R_{DS(on)}SW - R_{DS(on)}SR\right)}$$

In the bottom portion of the table, the losses are calculated and combined. Notice for each of the devices, the varying amount of power loss in each category. Taking the switching losses as an example: Because there is a finite amount of time it takes to turn OFF the upper switch, and even though the voltage across it is low, the current is relatively high and the losses significant.

The switch loss includes the loss due to driving the output of the SR. Since the Qoss is small, the voltage is low, and the operating frequency is moderate, the additional power loss is minimal.

The Predictive Gate Drive™ technology in the TPS40003 limits the body diode conduction in the SR MOSFET to almost negligible levels. This means that since the body diode conduction period is so small, on the order of 2 ns, then the power loss in the body diode is about 32 mW. By contrast, a converter operating at this frequency with 50 ns of body diode conduction time would dissipate 725 mW! Without this power loss reduction, it is unlikely that an SO-8 package could be used because the power dissipation would be too high for the package to effectively dissipate.

Interestingly, selecting the Si4866 as the switch gives the lowest overall loss. Even though the conduction losses are higher than the Si4836 (as in the first case), the lower switching, gate, output and driver losses more than compensate.

C. Input Capacitor Selection

The losses in the converter are combined and the average input current is found. With this, the RMS ripple current in the input capacitors is then calculated to be a little over 5 A. To meet the ripple current ($I_{\_incapRMS}$) requirements indicated in Table 2, two 4-V, 180-µF surface mount Solid Polymer (SP) capacitors are selected. They have a combined ripple rating of 7.2 A at 105°C, 7.5 mΩ of ESR, and 3 nH of ESL. Continuing down the table, the "Preliminary Loss" line indicates the calculation for ripple current in the input capacitor. The power loss in (Input cap loss) is about 200 mW (100 mW each).

To examine the magnitude of noise filtered by these capacitors, first look at the ripple at the fundamental switching frequency.

$$Vin_{PP} = Iin \bullet Re\,sr + \frac{Iin \bullet D}{F \bullet Cin}$$

$$= 4.2 \bullet 0.0075 + \frac{4.2 \bullet 0.39}{600\ Hz \bullet 360\ \mu F} = 39\,mV$$

With a 10 ns switching edge on the SW node, the input spike voltage is:

$$Vspike_{INPP} = Lesl \bullet \frac{ISW_{pk}}{T_{EDGE}} = 1.5\,nH \bullet \frac{12}{10\,ns}$$

$$= 1.8\,V$$

(SP capacitor only)

The major contributor to ripple is from the ESL and can be reduced by adding four 10 µF ceramic capacitors (with a combined ESL of 0.25 nH) in parallel.

$$Vin_{spikepp} = 0.25\,nH \bullet \frac{12}{10\,n} = 300\,mV$$

(SP + Ceramics)

These ceramic capacitors are placed as physically close to the switch and SR MOSFETs as possible to minimize noise.

D. Output Capacitor Selection

For this application, suppose a 2 A to 10 A load transient was possible with a 15 A/µs slope. A 470 µF output capacitor (15 mΩ ESR, 3 nH ESL) is selected because it has the same case size as the input capacitors. The resulting minimum under and overshoots are calculated below:

$$V_{under} = \frac{L \bullet I_{STEP}^2}{2 \bullet Cout \bullet D_{MAX} \bullet (Vin - Vout)}$$

$$= \frac{0.68\mu \bullet 8^2}{2 \bullet 470\,\mu \bullet 0.9 \bullet (3.3 - 1.2)} = 24.5\,mV$$

$$V_{over} = \frac{L \bullet I_{STEP}^2}{2 \bullet Cout \bullet Vout} = \frac{0.68\,\mu \bullet 8^2}{2 \bullet 470\,\mu \bullet 1.2} = 39\,mV$$

For this example, the low inductor value and high capacitance values yield a small voltage excursion. The actual values of under and overshoot may be higher depending on the response time of the feedback loop.

Two 10 µF ceramic capacitors are added, with 1 mΩ total ESR and 0.5 nH ESL, to reduce the ESL spike as shown. Note that this calculation does not include printed circuit board interconnect parasitics, which generally serve to increase the spike:

$$V_{spike} = I_{STEP} \bullet Resr + \frac{di \bullet Lesl}{dt}$$

$$= (10-2) \bullet 0.015 + {}^{15\,A}\!/_{\mu s} \bullet 3n = 165\,mV$$

(SP Only)

$$= 8 \bullet 0.0005 + 15 \bullet 0.00025 = 8\,mV$$

(SP + Ceramics)

The peak-to-peak ripple voltage during steady state operation is reduced significantly by the addition of the ceramic capacitors: The impedance of the capacitors at the switching frequency plus the ESR gives the output voltage:

$$Vout_{PP} = IL_{PP} \bullet R\,esr + \frac{IL_{PP}}{8 \bullet F \bullet Cout}$$

$$= 2 \bullet 0.01 + \frac{2}{8 \bullet 600\,k \bullet 470\,\mu} = 21mV$$

The power loss in the output capacitor is given in Table 2.

E. Thermal Design

The temperature rise of the components is the next to be determined. The temperature rise of the MOSFETs and the PWM IC is dependent on the PC board layout and the heat sinking afforded by device packaging. These are rough estimates that need to be verified by thermal imaging or direct measurement before the application is committed to production. Temperature rise in the high current traces on the board should also be predicted; this is discussed in Appendix C.

Control IC

The TPS40003 uses a 10 pin MSOP PowerPAD™ package where the die is attached to an exposed heat slug (Fig. 18) that should be soldered directly to a ground plane[2]. With an inner layer ground plane of 3 in, the specified junction to ambient thermal resistance (θja) is 60°C/Watt (the junction to case thermal resistance (θjc) is 5°C/Watt). θja is heavily dependent on the ground plane area and smaller planes results in an increased θja. As a comparison, a conventional 10 pin MSOP package has a θja of 240°C/Watt and a θjc of 40°C/Watt. The total gate drive losses are calculated to be 25 mW, and the quiescent power loss is on the order of 16 mW which results in a 2.5°C of rise. A much smaller ground plane can be used for the controller in this case.

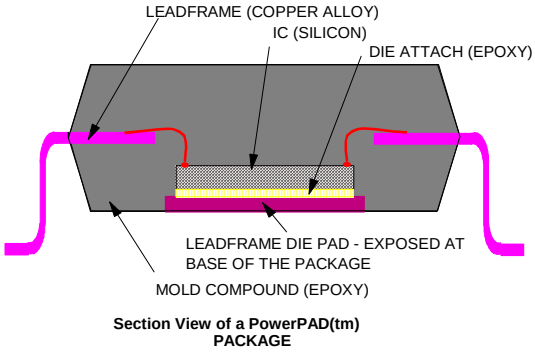

Fig. 18. PowerPAD section view.

MOSFETs

The SI4836DY and Si4866DY MOSFETs are in conventional SO-8 packages that have a θja of 67°C/Watt while mounted on a 1 in^2 plane. The main switch dissipates 503 mW at full load, resulting in a temperature rise at the junction of 33°C. The synchronous rectifier dissipates 305 mW, yielding a 20°C rise. The die of the MOSFETs and controller should be kept well below 150°C for reliability purposes, because MOSFET $R_{DS(on)}$ increases with temperature and care should be taken to avoid thermal run-away.

Capacitors

The temperature rise of a "black body" depends on many factors[3]; the placement of the component in airflow, its mounting direction, and

its surface area to name a few. To approximate the temperature rise (in degrees Centigrade), this somewhat complicated expression is used.

$$T_{rise} = \frac{\left(\frac{P \bullet \left(\frac{ht}{304.8} \right)^{0.25}}{8.8 \bullet 10^{-7} \bullet Surface\ Area} \right)^{0.8} - 32}{1.8}$$

Where P is the power dissipated, *ht* is the height of the component (in millimeters) above the plane, and *SurfaceArea* is the area of the device (in mm^2) exposed to the air.

For the input capacitors, they dissipate 100 mW at full load, the exposed surface area is 128 mm^2, resulting in a heat rise of 36°C. The actual heat rise is likely lower because the capacitor leads are connected to large power and ground traces that conduct heat from the center of the package.

Temperature rise in the output capacitor is small since it dissipates only 16 mW.

Inductor

The same formula is used to approximate the inductor loss. It dissipates 250 mW at full load, the exposed surface area is 351 mm^2, resulting in a temperature rise of 32°C.

F. Feedback Loop Design

The feedback loop is now designed for the example converter. The converter power stage frequency response characteristics are first determined, and then based on the resulting curves; a compensation network is designed to give the desired result.

A feedback model for a voltage mode buck converter is shown in Fig. 19.

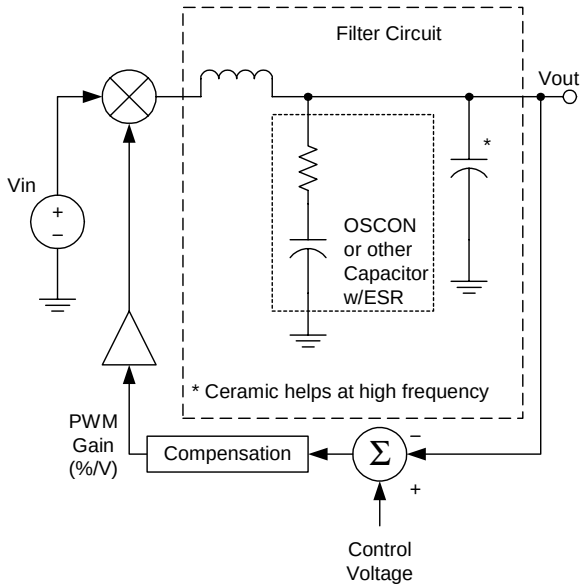

Fig. 19. Voltage mode control model.

The PWM gain is found by the relationship:

$$K_{PWM} = \frac{Vin}{Vramp}$$

Where Vramp is the 1-V peak-to-peak voltage of the ramp going to the PWM circuit. With a high input voltage of 3.6 V, the overall PWM gain is:

$$K_{PWM} = \frac{3.6}{1} = 3.6 \cong 11dB$$

The L-C filter gives the output voltage a double pole response to the output of the compensation network.

$$F_{DP} = \frac{1}{2\pi \bullet \sqrt{L_f C_f}} \cong 8.9\,kHz$$

The compensation network can be designed to have a crossover frequency either above or below the L-C filter's double pole frequency (F_{DP}). Crossing the loop below the double pole is easier to design since it only involves setting the overall gain and one pole. It does however, result in a ringing transient response because the feedback loop cannot respond as fast as the L-C filter rings. Crossing the loop above the double pole frequency requires more effort in designing the compensator but provides better transient response. In either case, good design practice dictates a phase margin of at least 45 degrees for proper damping.

A factor to consider when crossing the loop above F_{DP} is the zero introduced by the equivalent series resistance (ESR) of the filter capacitor. The main filter capacitor is an Solid Polymer type. The ESR is specified to have a maximum value of 10 mΩ. This yields a minimum ESR zero frequency of:

$$F_{ESR} = \frac{1}{2\pi \bullet C_F \bullet R_{ESR}} \cong 34\,kHz$$

Since ESR (and therefore the ESR zero frequency) can vary, the variation must be considered when designing the loop compensation. A simple but effective approach to this problem is to design the compensation so that the loop crossover frequency with a maximum ESR capacitor does not exceed 20% of the switching frequency and that adequate phase margin exists for a low ESR capacitor. The following discussion assumes that F_{DP} is at a lower frequency than the ESR zero of the output capacitor - which is usually the case.

Since the converter operates at a nominal switching frequency (Fs) of 600 kHz, then a reasonable target for a maximum loop crossover frequency is 100 kHz. This value is less than 20% of Fs and should avoid major problems. Fig. 20 shows the gain plots for the various elements of the feedback loop.

The line labeled "Filter & PWM Response" places the filter and PWM response curve flat at 11 dB until the filter double pole (F_{DP}), where it decays with a –40-dB/decade slope. At the ESR zero frequency of the output capacitor, it changes to a slope of –20 dB/decade. The maximum ESR response curve is shown by the dashed split-off from the solid (minimum ESR) response curve. It should be noted that the ceramic capacitors on the output do help to reduce the high frequency output impedance but contribute little to the compensation problem since they are not close in capacitance value to the main filter capacitor. In this example, they may be ignored for purposes of designing the feedback compensation.

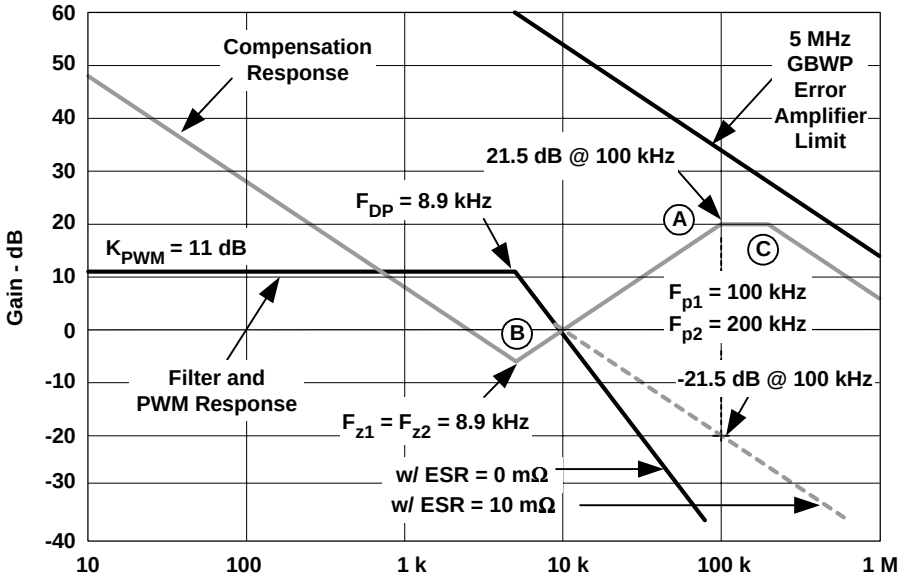

Fig. 20. Line bode plots of filter, PWM and compensation amplifier response

The line labeled *"5MHz GBWP Error Amp Limit*" shows the upper limit of gain vs. frequency the compensation network can produce if the error amplifier has a GBWP limit of 5 MHz. The compensation network gain response must stay below this line because the error amplifier imposes a limitation on how high the compensation network response can go.

With the desired maximum loop crossover frequency limited to 100 kHz, the compensation gain should be no more than 21.5 dB at 100 kHz. The response should also have a +20 dB/decade slope over the frequency range where the loop crosses zero for the range of ESR values.

To construct the line Bode plot for the compensation response begin at the max loop crossover condition of 21.5 dB at 100 kHz (Point A) and go lower in frequency at a slope of 20 dB/decade to a point about an octave below the minimum ESR zero frequency (Point B). In this case, the line is extended to F_{DP}. Placing the start of the slope here insures that the two zeros of the compensation response have a chance to get the phase response of the overall loop into a comfortable position. To minimize DC error, the compensation response is set to a –20 dB/decade slope below Point B. This provides the highest practical DC gain and the best load regulation.

At the high frequency end of the compensation response (Point A), a pole is placed at the upper loop crossover frequency limit. This turns the compensation response to a "zero" slope and insures that the loop crosses at or below this point since the PWM and filter response here is on a negative slope.

Finally, a second pole is placed at a slightly higher frequency (200 kHz at Point C) to roll off high frequency gain at a known rate. This avoids the instability that results if the output ripple voltage, when amplified through the compensation network, produces a rising slope on the output of the error amplifier, which exceeds the slope of the ramp signal at the PWM. See *Control Loop Cookbook* by Lloyd Dixon [4] for more details.

The desired loop compensation response described above is obtained using a "Type 3" compensation network as shown in Fig. 21.

The zero frequencies are given by:

$$F_{z1} = \frac{1}{2\pi \cdot R_4 C_2}, F_{z2} = \frac{1}{2\pi \cdot R_{eq} C_1},$$

$$R_{eq} = \frac{R_1 R_2}{R_1 + R_2}$$

And the poles are:

$$F_{p1} = \frac{1}{2\pi \cdot R_3 C_1}, F_{p2} = \frac{1}{2\pi \cdot R_4 C_3}$$

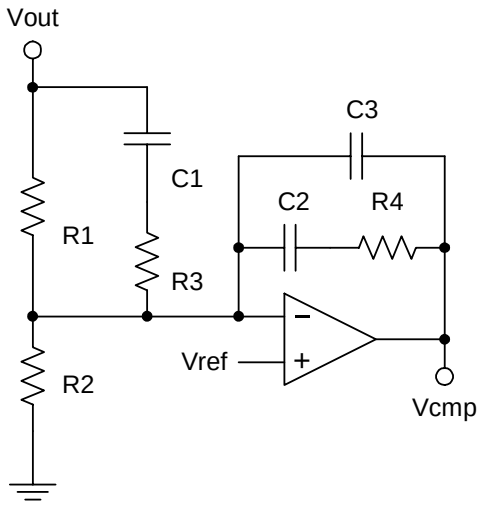

Fig. 21. Type III compensator schematic.

The gain of the compensator at the p1 is

$$\left|G_{p1}\right| = \frac{R_4}{R_{eq} \cdot R_3 / R_{eq} + R_3} = R_4 \cdot \frac{R_{eq} + R_3}{R_{eq} \cdot R_3}$$

The poles, zero, and dominant gain are set at:

$$F_{z1} = F_{z2} = 8.9\,kHz,$$
$$F_{p1} = 100\,kHz,\ F_{p2} = 200\,kHz$$
$$\left|G_{p1}\right| = 21.5\,dB = 12$$

The desired output voltage and reference voltage at the non-inverting input of the error amplifier determine the ratio of the R1-R2 voltage divider:

$$\frac{V_{ref}}{V_{out}} = \frac{R_2}{R_1 + R_2}$$

The reference voltage of the TPS40003 is 700 mV, and the desired output voltage is 1.2 V.

By arbitrarily picking the value of 10 kΩ for R2, then R1 must be 7.14 kΩ, (or 7.15 kΩ, in standard 1% values). Substituting in the above equations gives the following results: (Standard values are given in parenthesis).

$$R_{eq} = \frac{10.0\,k\Omega \cdot 7.15\,k\Omega}{10.0\,k\Omega + 7.15\,k\Omega} = 4.17\,k$$

$$C_1 = \frac{1}{2\pi \cdot R_{eq} \cdot F_{z2}} = 4.3nF \longrightarrow (4.7nF)$$

$$R_3 = \frac{1}{2\pi \cdot C_1 \cdot F_{p1}} = 370 \longrightarrow (374\,\Omega)$$

$$R_4 = G_{z1} \cdot \frac{R_{eq} \cdot R_3}{R_{eq} + R_3} = 4.08\,k \longrightarrow (4.12\,k)$$

$$C_2 = \frac{1}{2\pi \cdot R_4 \cdot F_{z1}} = 4.4nF \longrightarrow (4.7nF)$$

$$C_3 = \frac{1}{2\pi \cdot R_4 \cdot F_{p2}} = 195\,pF \longrightarrow (220\,pF)$$

The resulting compensator has the response characteristic shown in Fig. 22.

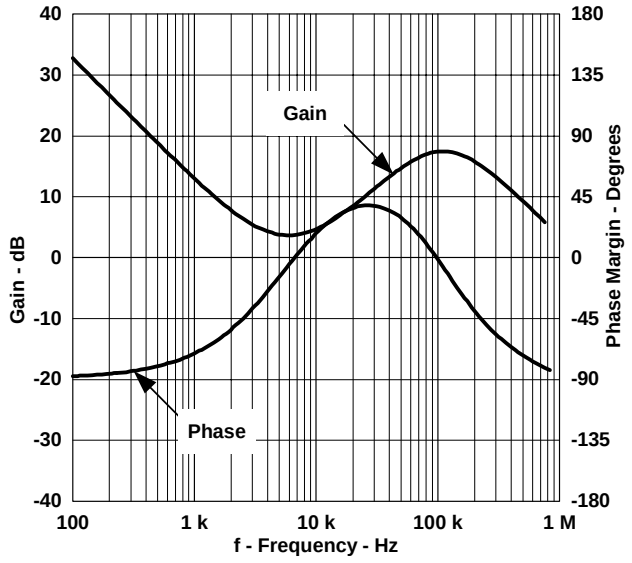

Fig. 22. Compensator gain and phase response.

The compensated system open loop response Bode plot in Fig. 23 shows the range of expected possibilities for the loop crossover frequency due to ESR variation. The minimum loop crossover frequency occurs at the minimum ESR zero frequency of the output capacitor. This is a direct result of positioning of the compensation response to limit the maximum loop crossover frequency in the maximum ESR case. In practice, the maximum crossover frequency is less than the maximum design of in the line Bode plot of Fig. 20 since that method approximates the actual frequency response with its asymptotes. If necessary, the loop bandwidth can be more tightly controlled by lowering the gain of the compensation network a few dB and shifting the double zero frequency a little lower.

The system here has a predicted crossover frequency (Fc) range of 34.4-kHz for a low ESR (2mΩ) capacitor to a maximum of 65 kHz for an output capacitor with a maximum ESR. The predicted phase margin ranges from 52° for a minimum ESR output capacitor to 79° for a maximum ESR capacitor.

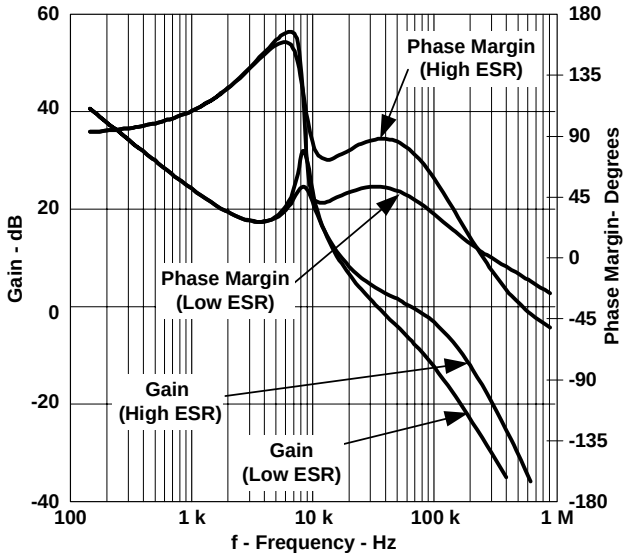

Fig. 23. System open loop gain and phase response.

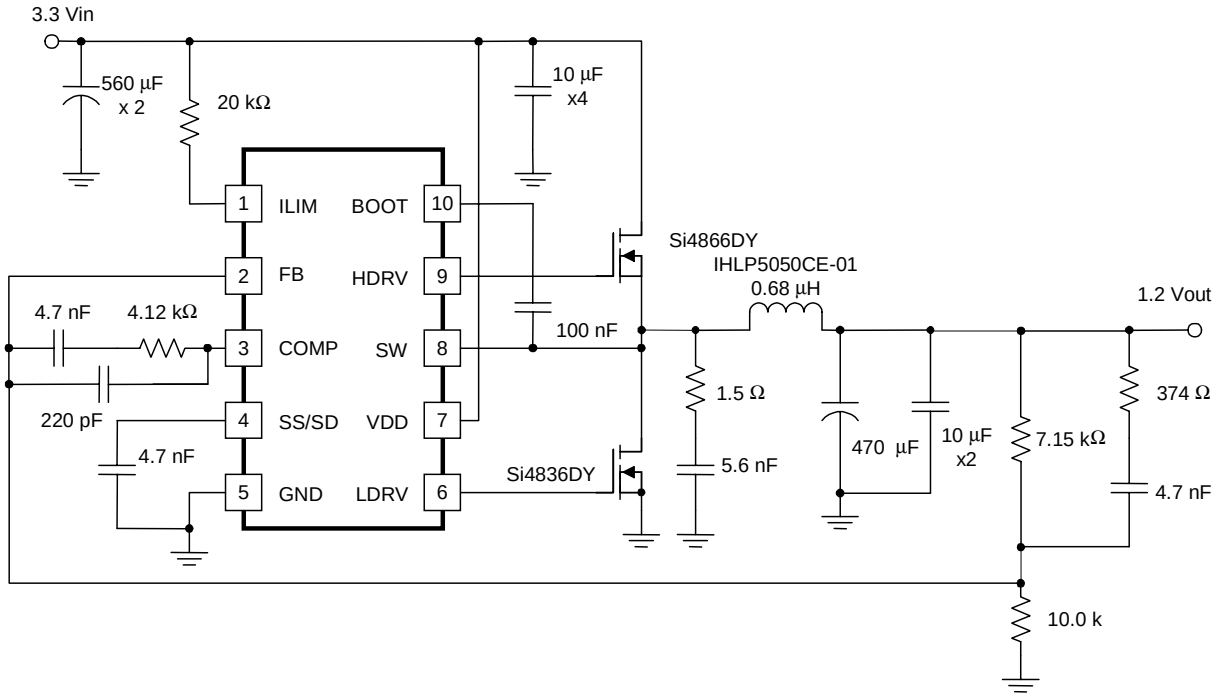

Fig. 24. Final DC/DC converter schematic.

V. Test Results

The DC/DC converter discussed in Fig. 24 was built and tested. The following waveforms show some of the issues discussed in the body of the text.

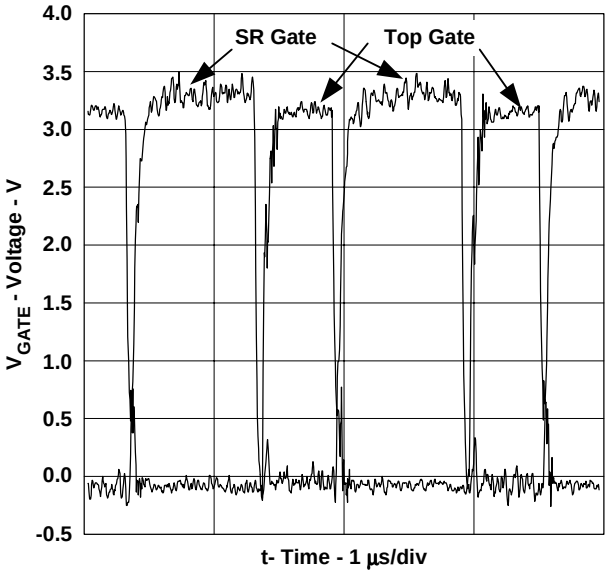

Fig. 25. Gate drive waveforms.

In Fig. 25 and Fig. 26, the relationship of the gate drive signals for the high side switch and the SR, along with the relationship to the SW node can be seen. Note the slight bump in the SR gate waveform as the SW node rises. Load current in this case is 8.5 A. SW node transition times are about 20 ns. The ringing on the SW node increases with current and is much less pronounced at lighter loads. Limiting the slew rate on this node helps to alleviate the ringing. For more information see Appendix C.

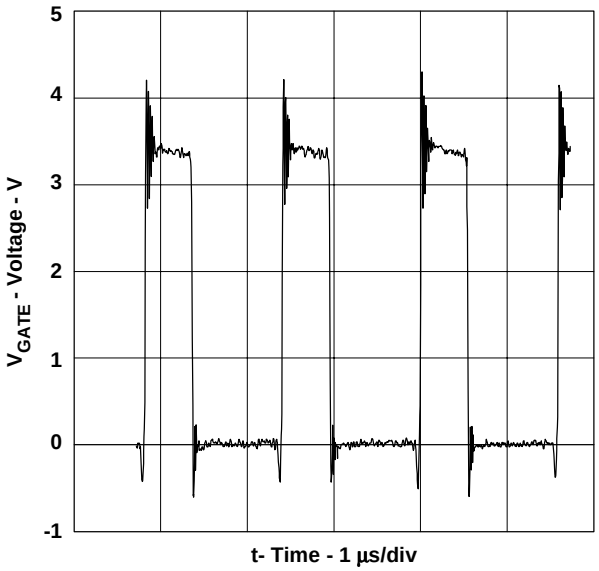

Fig. 26. Switch node waveform.

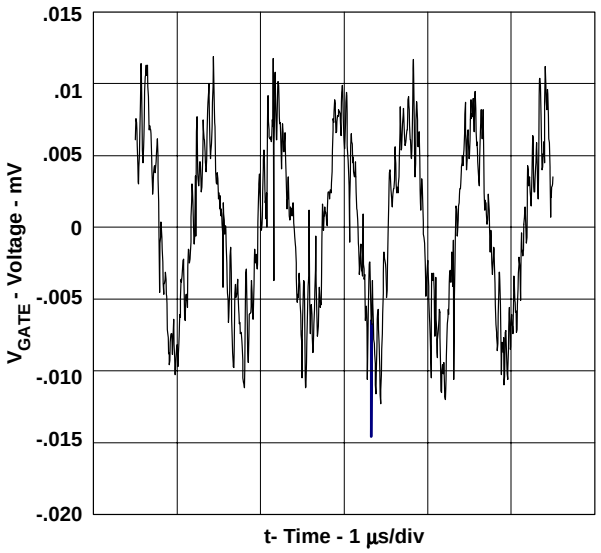

Fig. 27. Output ripple and noise.

The measured output ripple and noise at full load was about 20 mV peak-peak. Averaging out the noise on the waveform shows approximately 15 mVpk-pk ripple, well within the maximum predicted 21 mV.

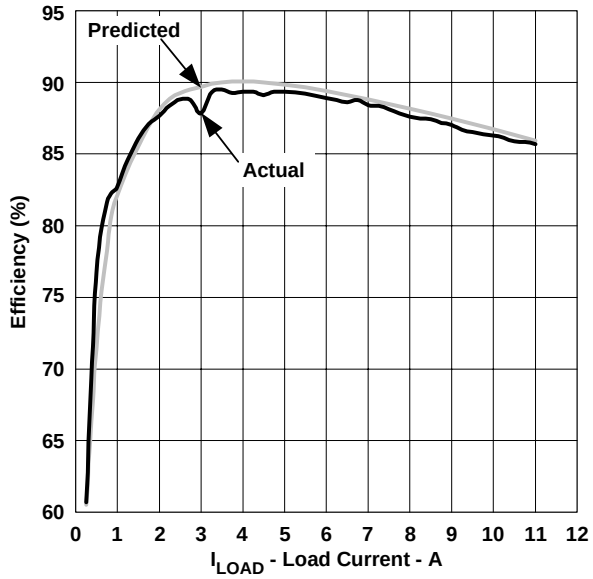

Fig. 28. Efficiency vs. load current.

The efficiency curves track fairly well. Errors in calculation may be attributed to the method of calculating MOSFET losses, and to errors associated in calculating PCB losses.

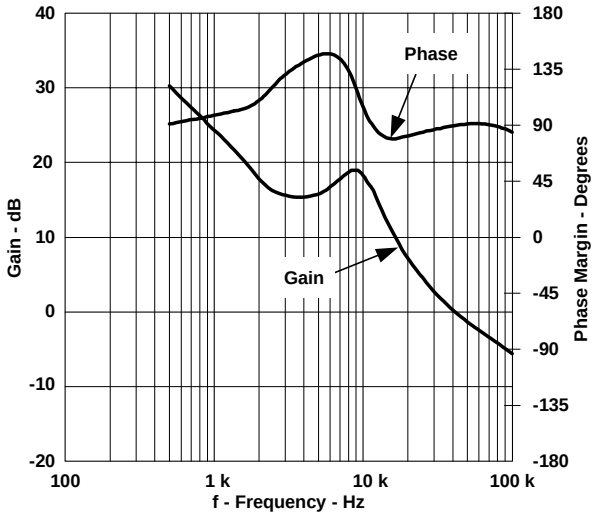

Fig. 29. Measured loop frequency response.

The measure frequency response curves also track fairly well with those predicted. The crossover frequency is approximately 45 kHz with 90° of phase margin.

VI. Conclusion

The design of low voltage DC/DC converters requires an understanding of a wide variety of issues and an understanding of how design decisions can have an effect in final converter performance. While the discussion here presented the basic concepts behind converter design, there are many other areas to expand upon. Appendix B discusses high frequency inductor issues. Appendix C describes how parasitic elements, in both the PC board layout, and in the components themselves, can contribute to causing potential circuit design problems. In Appendix D, there is a discussion of how to design a converter for very high load currents. Appendix E illustrates a schematic used to simulate the effects of parasitic turn ON.

APPENDIX A. TABLE OF VARIABLE NAMES

Cdg	Drain-to-gate (aka."Miller") capacitance of a MOSFET
Coss	Coss of a MOSFET
D	Operating duty cycle of the DC/DC converter. In an ideal converter, D=Vout/Vin In the practical case, component losses causes the duty cycle to be larger
Fs	Switching frequency of the DC/DC converter
Ig	MOSFET gate current
Δ Iout	AC Peak to peak ripple current in the output inductor.
Iout	DC output load current
Iswpk	Peak current in the upper, switch MOSFET
L	Value of output inductor
Ld	Package inductance of the drain pin of a MOSFET
Lg	Package inductance of the gate pin of a MOSFET
Ls	Package inductance of the source pin of a MOSFET
Pswconduction	Conduction loss in the switch MOSFET
Qg	MOSFET total gate charge requirement
Qgd	MOSFET gate to drain charge
Qgs	MOSFET gate to source charge
Qoss	MOSFET output charge
RL	DC winding resistance of the output inductor
$R_{DS(on)}$ sw	Static $R_{DS(on)}$ of the upper, switch MOSFET
$R_{DS(on)}$ sr	Static $R_{DS(on)}$ of the lower, synchronous rectifier MOSFET
Rg	Resistor placed in series with the gate driver and the gate of the MOSFET
Rghi	Equivalent gate driver pull up resistance
Rgi	Equivalent internal MOSFET gate resistance at the "Miller" plateau
Rglo	Equivalent gate driver pull down resistance at the "Miller" plateau
TEDGE	Transition time of the switch node (SW) edge
Ton	On time of the DC/DC converter during one switching cycle
Ts	Switching period of the DC/DC converter and is 1/Fs
Vfr	Forward voltage drop across the synchronous rectifier's body diode when it is conducting current. This current is flowing in the source pin, and out of the drain pin.
Vin	DC input voltage to the converter
Vgth	Gate turn ON threshold voltage of a MOSFET
Vout	DC output voltage of the converter
Zout	Output impedance seen by the converter. This impedance includes the impedance of the output capacitor(s) and the load

APPENDIX B. INDUCTOR CORE MATERIALS AND HIGH-FREQUENCY EFFECTS

A. Inductor Basics

Inductors require a non-magnetic gap in order to provide energy storage. In ferrite-based cores, this gap consists of a physical spacing between the core halves. The BH loop for a gapped and ungapped core is shown in Fig. 30, where field intensity (H) is plotted on the X-axis and flux density (B) is plotted on the Y-axis. The gap lowers the permeability (μ), causing the B-H curve to be stretched in the H direction, allowing higher currents to be supported without core saturation. In continuous current mode the inductor operates in a minor B-H loop as shown. The flux density in the core changes with applied voltage and time ($V_{ON} \bullet T_{ON}$ or $V_{OFF} \bullet T_{OFF}$) causing the field intensity and inductor current to change. Flux losses are proportional to the area of the minor B-H loop. Ferrite cores have low flux losses and can be used at frequencies as high as 1 MHz to 2 MHz. Most inductors used in commercial DC/DC applications are of the ferrite variety, where shielded cores are often employed to minimize external fields. Ferrite cores have some disadvantages, however, such as low flux density (B_{MAX}), sharp saturation characteristics, fringing flux losses near the air gap, and reliability issues in high shock environments.

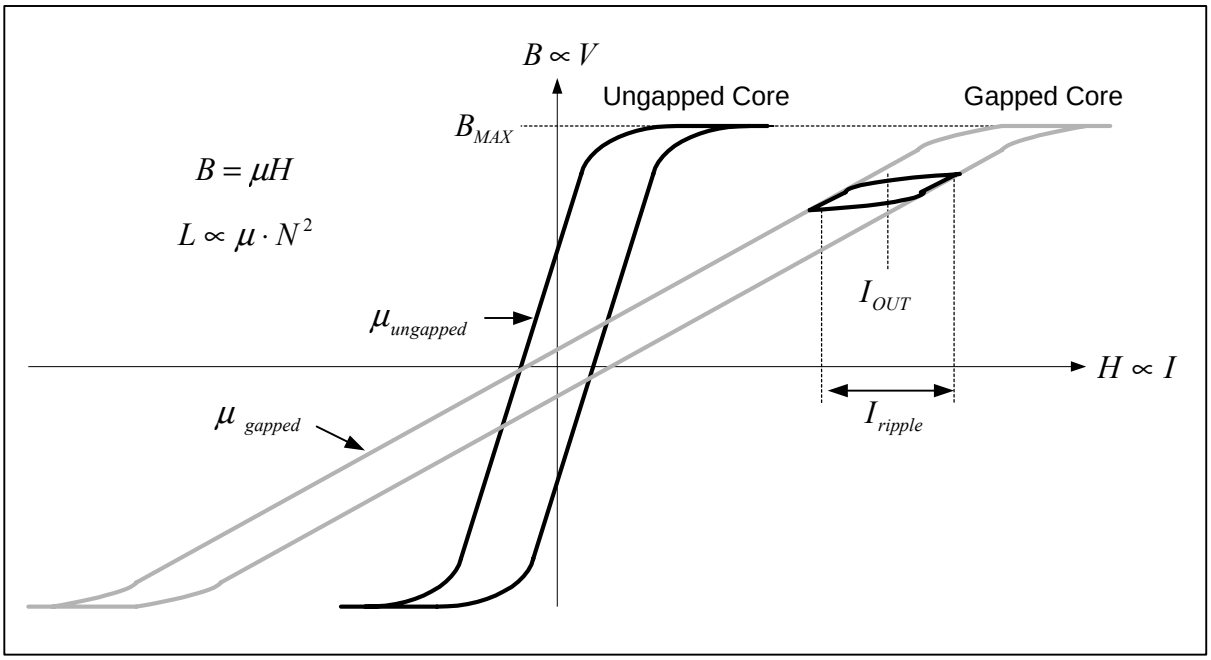

Fig. 30. B-H Curve showing minor hysteresis loop with continuous current

If a more robust and possibly size-reduced solution is required, a "distributed" gap material can be used such as powdered iron or Magnetic's Kool-Mu. With these core materials, the stored energy resides in the iron or binder material rather than the air gap. An advantage of distributed gap cores is that they have a softer saturation characteristic when compared with gapped ferrite. Cores available in these materials are often toroidal in shape, lowering the external magnetic fields and fringing losses. They also come in a choice of permeability, allowing various Inductor values and DC currents to be supported. The powered iron cores perform well with pure DC currents, but the AC core losses make their use impractical above 300 kHz. Kool-Mu cores offer lower losses with reasonable efficiencies up to about 700 kHz.

Planar magnetic inductors are often considered for low profile applications, where the printed circuit board (PCB) traces are used for windings. This technique becomes more difficult at high currents due to the thin trace thickness and heating issues with inner layers. Practical planar magnetic inductors are often built on a small section of a custom PCB with thicker copper.

B. Core Losses

Core losses in the inductor are determined by the volt-seconds flux swing in the core (see Fig. 30), the frequency of operation, and the material used. With the push for higher frequencies, the selection of core material has a greater effect on power loss. The following equations predict the core losses for magnetics traditional P-Type ferrite material (>500 kHz) with a newer high frequency K-Type:

$$PL_{PTYPE} = 0.75 \bullet 10^{-6} \bullet f^{3.5} \bullet B^{2.5} \quad \text{(P-Material)}$$

$$PL_{KTYPE} = 1.8 \bullet 10^{-9} \bullet f^{4.1} \bullet B^{3} \quad \text{(K-Material)}$$

Where PL is given in mW/cm^3, f in kHz, and B in kG. To illustrate the importance of proper core material selection, losses for P and K type ferrite materials are plotted against frequency in Fig. 31 for a 1cm^3 core with a minor B-H loop of 200 Gauss. Although inductor manufactures do not always provide information on core material, it is important to get information on core losses for high frequency designs.

C. AC Wire Losses

A portion of the AC loss in the winding of the inductor is generated by skin effect.[5] At high frequencies, the current in a conductor (in this case the inductor winding) flows at the surface of the conductor and not at the center, as if the current were flowing in a hollow tube. This means that the effective cross sectional area of a conductor at high switching frequencies is less than that at DC, and therefore the impedance at high-frequency is much higher than at DC. Fortunately, in a buck inductor, only the peak-to-peak portion of the ripple current is subject to this higher impedance.

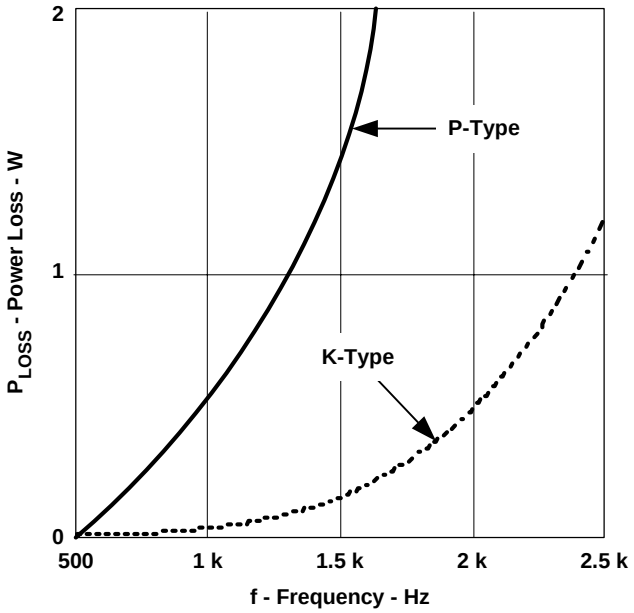

Fig. 31. P and K material losses vs. frequency for 1 cm^3 core with 200 Gauss B-H swing.

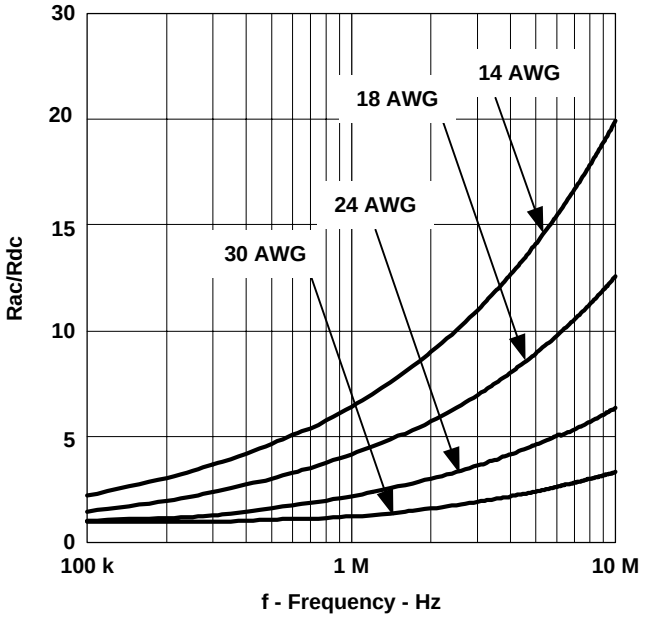

Fig. 32. Ratio of AC to DC impedance in a copper wire as a function of frequency.

The amount of increase in AC resistance depends on the diameter of the conductor, the material, and the frequency. As frequency increases, the current flows closer to the outer walls of the conductor. Fig. 32 graphs the ratio of AC resistance to DC resistance in copper vs. frequency for four common wire gauges. Notice that the larger diameter wires lose their effectiveness at relatively low operating frequencies. For higher frequency or higher ripple current applications, multiple strands of finer wire, or a thin sheet of copper foil may be used to maintain a low resistance ratio.

The following example helps describe how skin effect impacts losses. From a heating standpoint, a reasonable current density in a copper conductor is around 500 A/cm^2. For a 10-A load current, a conductor with a 0.020cm^2 cross sectional area is required. From a wire gauge table, 14AWG wire should be used (Area = 0.02cm^2, Rdc=.0083 Ω/M). With an operating frequency of 600 kHz, the equivalent AC resistance is 0.0083 • 5 = 0.0415 Ω/M. If the AC_{RMS} ripple current in the inductor is 2 A, the total loss in the conductor is (10^2 • 0.0083 + 2^2 • 0.0415) = 996 mΩ/M). If the wire is 10 cm long, then the AC wire loss due to skin effect is about 100 mW.

Although a lot of discussion in this appendix has been allotted to AC skin effect losses and AC core losses, the DC losses in the inductor dominate in most applications. The AC losses become more important at high frequencies or with high ripple currents.

For more information, two recommended sources are Unitrode's *Magnetic Design Handbook* by Lloyd Dixon[6] and the Magnetics Incorporated website at www.mag-inc.com.

APPENDIX C. LAYOUT ISSUES FOR LOW-VOLTAGE SYSTEMS

In operation, a low voltage DC-DC converter is more complicated than basic theory would lead one to believe. There are operational issues that can crop up due to the PCB layout that may have an effect on circuit function and/or reliability. A few of these issues are discussed here.

A. Trace Resistance

Despite the recent improvements in power components and controllers, the resistivity (p) of copper used in PCBs remains at 0.67 mΩ x mil at room temperature with a 0.39% increase per °C. Trace resistance is given below with the dimensions depicted in Fig. 33. Trace thickness (T) is typically specified by the number of ounces required to cover a square foot of board. For example, one ounce copper has a thickness of 1.4 mils (1mil = 0.001 inch).

$$R = \frac{\rho \bullet L}{T \bullet W}$$

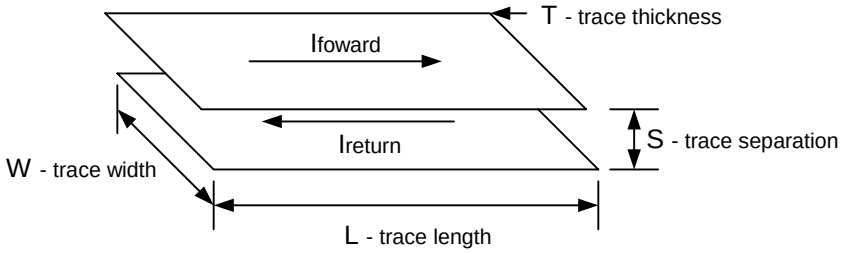

Fig. 33. Circuit trace geometry.

For the 3.3 V to 1.2 V converter discussed in the design example, 2" long x 200 mil traces on 1 ounce copper were used for the forward and return connections between the DC/DC output and load. Each trace has only 3 mΩ of resistance at room temperature. With the 10 A of load current, power loss is approximately 500 mW.

A good design practice is to check the current density in each trace to guarantee that trace temperature rise is acceptable. One standard that is commonly used to specify temperature rise in PCB traces is MIL-STD-475E. This standard is used to derive the curves of Fig. 34, which plots trace width and the maximum allowable current for a 20°C temperature rise. This graph assumes that the copper is on the top or bottom layers (inner PCB layers have much lower ratings in MIL-STD-475E) and neglects the skin effect for the AC current component. The curves tell us that for the 10 A example above, a 20° rise in the trace is expected.

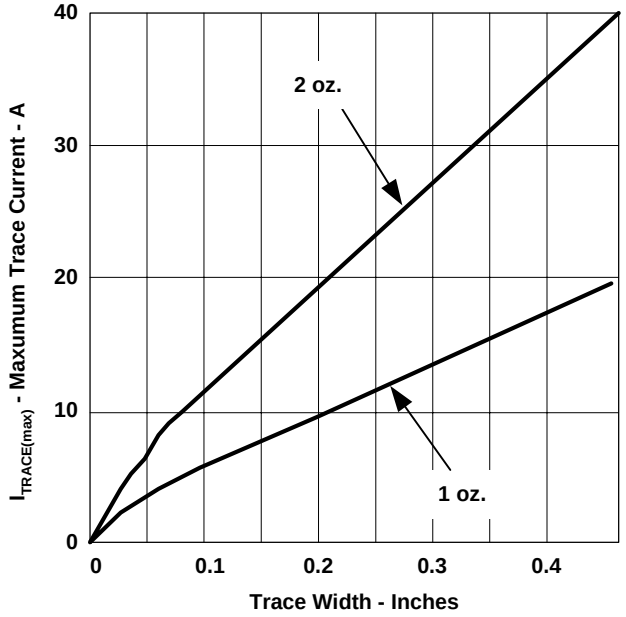

Fig. 34. Current carrying of a copper PCB trace for a 20 °C temperature rise.

B. Trace Inductance

Parasitic inductance is formed by the separation between the forward and return traces in a PCB and can be calculated using the following equation and the trace geometry in Fig. 33. Parasitic inductance is not an issue with steady state DC current, but may create noise problems during rapidly changing in input, load, or switching currents.

$$L = 32 \bullet \frac{pH}{mil} \cdot \frac{L \bullet S}{W}$$

Returning to the example that uses a 200 mil x 200mil output connection, the forward and return traces are separated by the 50 mil thickness of the board. The inductance is calculated to be 1.6 nH per connection resulting in a 128 mV transient spike between the output and load (assuming a 40 A/µs edge). Transient problems at the load can be solved with the addition of ceramic capacitors to slow the di/dt edges and reduce the transient spike.

Switch currents in a high frequency converter can easily reach 1 A/ns. The resulting voltage spikes that occur from trace and package inductance near the MOSFETs can cause a number of unwanted results including EMI issues, component stress, noise glitches at the input, and interference with upstream supplies. These issues are resolved with careful layout and adequate bypassing with low ESR/ESL capacitors.

C. High Current Layout

The proper layout of the printed circuit board (PCB) is critical in achieving acceptable efficiency and transient performance in low voltage, high current systems. Fig. 35 shows a parasitic model for a DC/DC converter, which can also be used to simulate the effects of transient behavior.

The input and output capacitors have been split into two types where an electrolytic is used for bulk storage, and a ceramic is used to filter high frequency edges. ESR and ESL effects have been included for the capacitors. The model for the MOSFETs include the drain to source capacitance, Cds, the $R_{DS(on)}$ and the package inductance, LPKG. The inductor model includes winding resistance (RW) and inter-winding capacitance (CW).

The remaining parasitic elements represent the resistance (RPCB) and inductance (LPCB) of the PCB traces. The model in has been simplified by combining PCB trace parasitics and the component models, by combining forward and return trace parasitics at the input and output, and by ignoring board capacitance. This model is a good starting point, but may need to be modified to better reflect the actual board layout if a specific problem should arise.

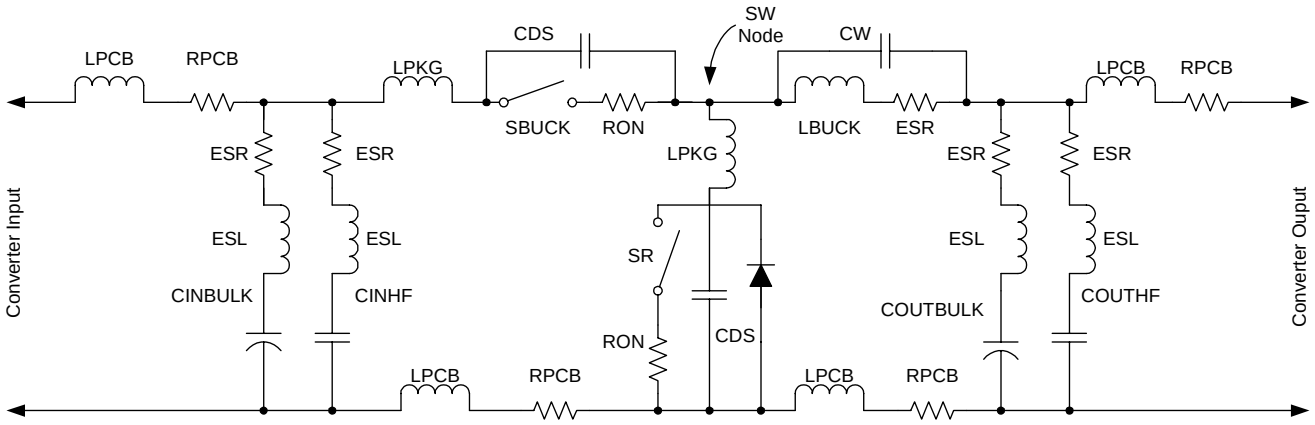

Fig. 35. Simplified parasitic model for DC/DC buck converter.

To minimize circuit noise, the loop created by the input capacitors and the two series MOSFETs should be kept as small as possible. By doing so, any noise generated by the pulsating current flowing through the input capacitors' ESR and ESL is minimized, and the switching MOSFETs has the benefit of having the "full" input voltage to work from.

The loop formed by the SR, the output inductor and the output capacitor should also be kept as small as possible to minimize ringing on the SW node

D. SW Node Ringing

What effect does this ringing have on circuit operation? The answer is - it depends. If the control scheme is looking at the SW node to determine when to take some action (possibly to sense over-current, or adjust gate drive timing) then there is a potential for mis-operation of the converter. From an EMI/RFI perspective, the energy level in the ring is relatively low and does not generally pose a problem. The fast rise and fall of the SW node at the PWM transitions are usually more cause for concern.

When the main switch MOSFET turns on, the SW node rises rapidly toward the input voltage of the converter. After a few nanoseconds, SW reaches the input voltage - and keeps right on going. The reason for this is parasitic Ls and Cs "connected" to the SW node. Referring to Fig. 35, the components that cause the ringing are the Cds of the SR MOSFET, package inductance in the switch MOSFET, and inductance in the board traces through the input bypass capacitors, and any capacitance seen looking into the buck inductor. As the SW node rises, current is flowing in the inductances to charge up the capacitance seen at the SW node. When the SW node reaches Vin, the energy stored in those inductances has to go somewhere, showing up as a ringing response on SW. Resistances in the loop determine the decay time. Since the aim is to make an efficient power converter, the parasitic resistances are typically minimized and do not do a good job of damping out the SW node ringing. Hence the ring may last up to several microseconds.

Two methods are generally used to reduce the ringing: Minimize the excess inductive energy buildup as SW rises; or provide a means to dissipate the energy in a controlled fashion

Limiting the rise time on the SW node minimizes the excess inductive energy buildup. This amounts to purposely slowing the switching time of the main switch MOSFET by adding some resistance in between the MOSFET gate and its driver circuit. The effectiveness of this depends on how much the SW node dv/dt can be reduced, what the effective capacitance of the SW node is and what the inductor current is at the time the SW node reaches Vin. The closer that the current in the buck inductor is to what the SW capacitance needs to charge at a certain dv/dt, the less the ringing problem will be. There is a trade off though. The slower the SW node dv/dt, the more switching loss occurs in the switch and the SR.

The other common method to control ringing is to use a snubber circuit. A simple series R-C network around the SR can control ringing effectively in most cases. A general approach to determining snubber component values is to add capacitance around the rectifier device until the observed ring frequency is approximately halved from its original value. The resistor value to put in series with this capacitor should be something near the impedance of the capacitor at the new ring frequency. A caution here is that a snubber can increase losses in the converter if components are not chosen wisely. For a more detailed discussion see Snubber Circuits: Theory Design and Application, Unitrode SEM-900 by Philip Todd.[7]

APPENDIX D. INTERLEAVED CONVERTERS

When an application's load current requirement grows to a level too high for a single converter to easily handle, often the solution is to parallel power stages. By phase shifting the PWM signals to the converter power stages, or "channels", there is an added benefit of reducing the RMS ripple current in the input capacitors. This is because for each converter channel, the effective current is 1/n that of a single channel power stage. The effective duty cycle of the converter is also n times that of a single channel power stage. Fig. 36 illustrates this concept for paralleling two power stages.

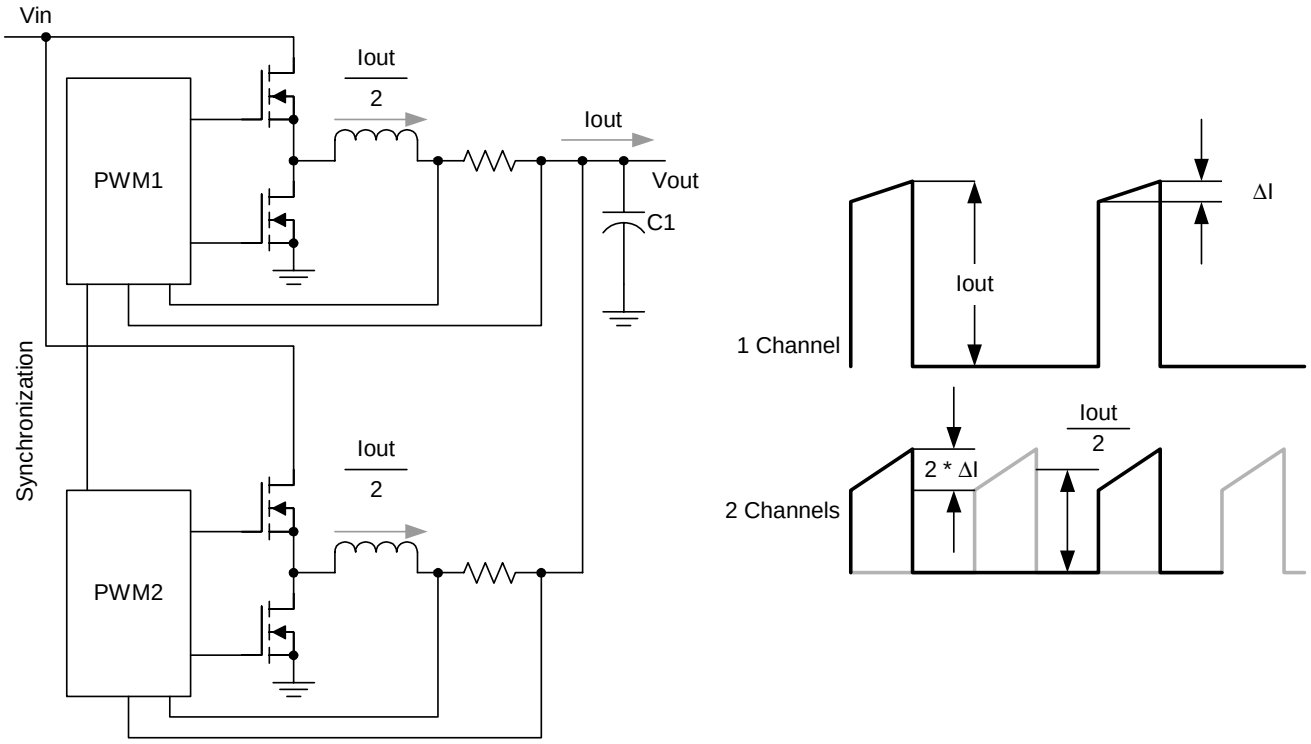

Fig. 36. Interleaving.

The RMS current improvement in the input capacitor for a single, a two, and a four-phase converter is shown in Fig. 37. The ripple current (and therefore the power loss) in the input capacitors reaches a maximum where the sum of the duty cycles equals 0.5, and reaches a minimum where the sum of the duty cycles approaches 100%.

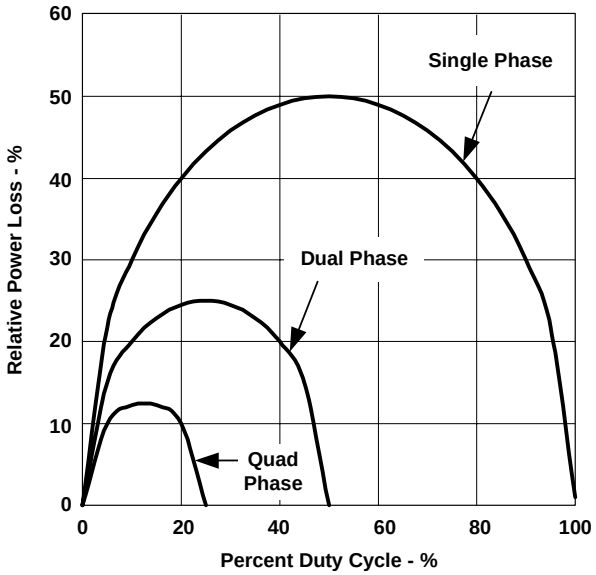

Fig. 37. Input capacitor RMS ripple current in an interleaved converter.

One other benefit to interleaving multiple synchronous buck regulators is the improved effect on transient response. Why is that? Fig. 38 shows the magnitude of DC and ripple current for single phase, two phase, three phase, and four-phase converters. Notice that the average level of the current is decreased by the addition of phases, and the magnitude of the ripple is allowed to be increased.

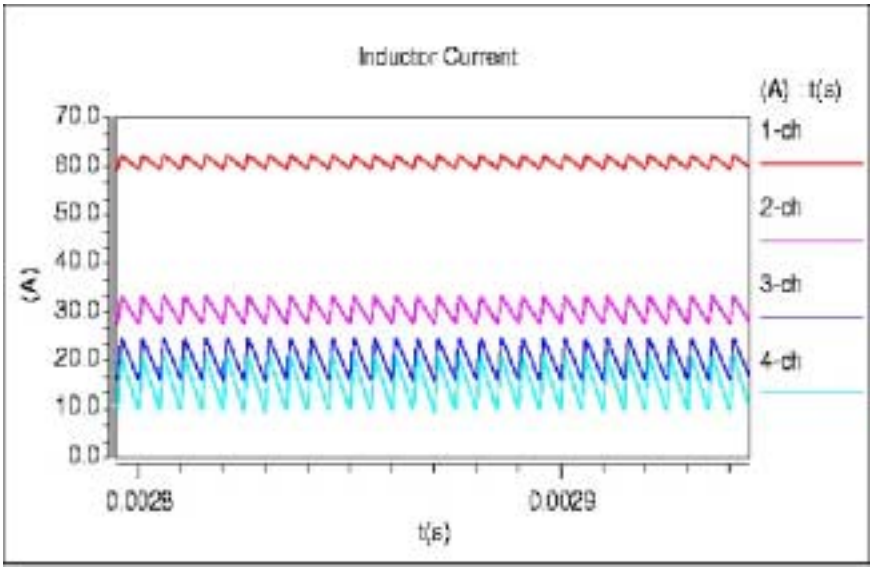

Fig. 38. Increase in ripple current.

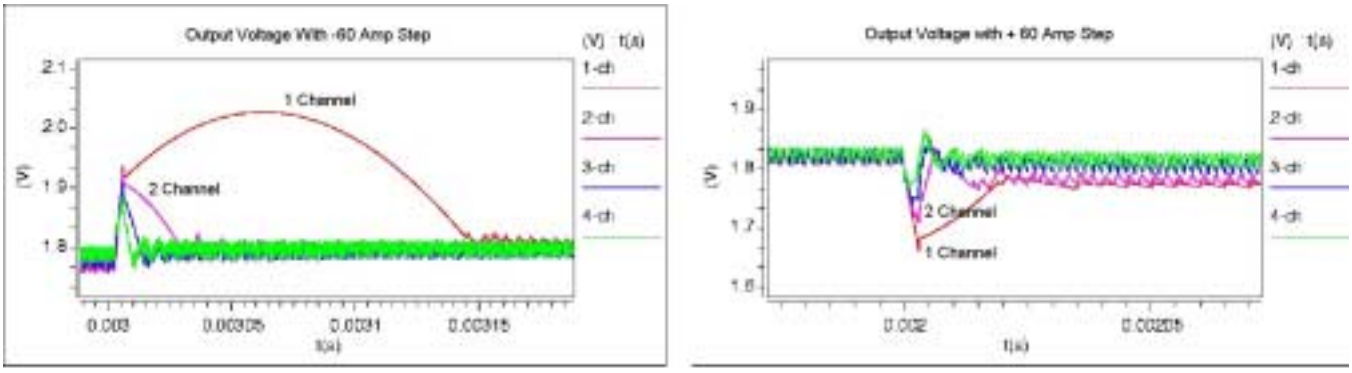

Fig. 39. Transient response waveforms for multi-phase converter.

A smaller inductor gives the greatest benefit in transient response recovery. Fig. 39 shows the output voltage response for a one, two, three and a four-phase converter.

On the left side of the figure, where a load drop is being viewed, there is a large amount of energy in the inductor transferred into the output capacitors. When more phases are added, there is less energy to "ring" the output voltage higher because the energy storage decreases as the square of the current through it. By increasing the number of phases, the current per phase drops by 1/n.

During a load step increase, the single-phase converter has a response time quite a bit slower than the other cases because the output inductance is the highest.

APPENDIX E. PARASITIC TURN-ON MODELING

The simulation results discussed in Section II.D were generated from a simulation based on the circuit in Fig. 40. This schematic can be used for initial modeling to determine if a potential problem exists with parasitic turn on of the SR MOSFET.

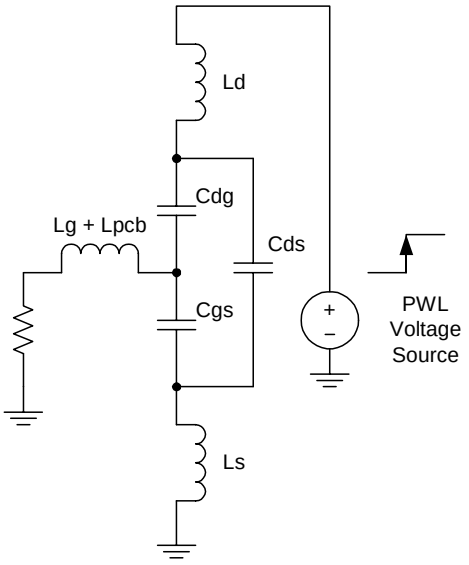

Fig. 40. Parasitic turn on model.

In this model, the actual gate voltage is measured across Cgs. The PWL voltage source is set to ramp from 0 V to the input voltage of the converter in the expected switching time of the actual converter. Since many FET manufacturers give the parasitic capacitances in terms of Coss, Crss and Ciss, the following can be used to convert to the model capacitances:

Coss = Cds + Cdg

Ciss = Cgs + Cdg

Crss = Cdg

In general, for a multi-pin MOSFET such as an SO-8, the values of Ld and Ls are significantly smaller than that of Lg. This is due to at least three bonding wires being used for the source lead, either four bonding wires or direct bonding to the lead frame for the drain, and only one bonding wire for the gate. A typical bonding wire has an inductance of around 1 nH. As an approximation, an SO-8 MOSFET can be assumed to have 250 pH in the drain, 350 pH in the source and about 1 nH in the gate lead. PCB wiring also contributes both resistance and inductance in the gate circuit. This is lumped together with the driver impedance as shown in Fig. 40.

The model shows a first order approximation of the rise that can be expected at the gate of the SR FET for a given input voltage and rise time. It does not take into account the effect of actual parasitic turn on limiting the dv/dt of the SW node. When this starts to occur, some of the current that was charging capacitance at the SW node is shunted through the channel of the FET, leaving less available to charge SW node capacitance reducing the actual dv/dt. If this model shows that there might be parasitic turn on, it is best to actually evaluate a real power circuit to determine if the amount is acceptable or not.

Simulation shows that for a 3.3 V supply, 10 ns rise time of the SW node, typical values for a Si4836DY FET (Cgs = Cdg = 1.5 nF, Cds = 4.5 nFa lumped driver/board resistance of 1.5 Ω and a lumped driver/board inductance of 2 nH, the peak gate voltage is about 850 mV. Since the amount of time that the gate voltage spends above the gate threshold is small, at roughly 5 ns to 6 ns, in most applications the results are perfectly acceptable.

APPENDIX F. REFERENCES

[1] Balogh, Laszlo, *A design and Application Guide for High Speed Power MOSFET Gate Drive Circuits*, SEM-1400, Unitrode Power Supply Design Seminar, 2001. Topic II, TI Literature No. SLUP133

[2] *PowerPAD Thermally Enhanced Package*, Technical Brief, TI Literature No. SLMA 2002

[3] Tarter, Ralph E., *Principals Of Solid State Power Conversion*, Howard Sams & Co., Inc., 1985. pp480, 481

[4] Dixon, Lloyd H., *Control Loop Cookbook*, SEM-1100 Unitrode Power Supply Design Seminar, 1996. Topic V, TI Literature No. SLUP113

[5] Reference Data for Radio Engineers, Sixth Edition, Howard Sams & Co.,Inc., 1977. pp 6-4 through 6-8

[6] Dixon, Lloyd H., MAG-100A Unitrode Magnetics Design Handbook, 1999, TI Literature No. SLUP123

[7] Todd, Philip C, *Snubber Circuits: Theory, Design, and Application*, SEM-900 Unitrode Power Supply Design Seminar, 1994. Topic II , TI Literature No. SLUP100

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