# TPS40130 Enable Reference Voltage Interaction Errata

## 1 Problem Description

In applications where BP5 and UVLO are initially powered while the TPS40130 is disabled through the EN/SYNC pin, it is possible for the TPS40130 to experience a small offset in the reference voltage. The small offset is a discrete -3 mV or -5 mV offset due to the discrete nature of the trim circuitry. Approximately 5% of TPS40130's exhibits a read error on the EEPROM, resulting in an IC reference voltage trimmed 3 mV or 5 mV low. While this is within the reference tolerance of the device, it may fall below the specified tolerances at temperature extremes. A given device's reference shift (0 mV, 3 mV or 5 mV) is consistent and poses no device reliability or latent failure issue.

## 2 Interim Containment Solutions

Existing applications require no changes if:

- EN/SYNC is biased by a resistor from BP5 and is not held low while the device leaves UVLO.
- If EN/SYNC is biased from an external 5-V supply and is held high while the device leaves UVLO.
- If EN/SYNC is brought HIGH (>2 V) then Low (< 0.3 V) then HIGH on first Enable (EN/SYNC should be high for more than 1 μs and less than four switching periods to ensure a proper read and no gate drive activity).
- If the application can support a -0.7% shift in reference voltage and regulated output voltage on initial power-up (shift is removed if TPS40130 is disabled and enabled through the EN/SYNC pin)

If a design does not meet these requirements, a design change should be implemented to either meet one of the above design requirements or screen TPS40130's for a 3 or 5mV shift in reference voltage between first Enable and second Enable.

## 3 Root Cause

The EEPROM of the TPS40130 is read each time EN/SYNC is pulled high. If BP5 is present when EN/SYNC is pulled high, an internal race condition can cause the EEPROM read cycle to initiate before the output flip-flops are initialized, causing the EEPROM read cycle to generate error bits, resulting in a small shift in the trimmed output voltage.

## 4 Permanent Corrective Action

TI is in the process of making a metal layer only change to the TPS40130 to delay the EEPROM read cycle from EN/SYNC by 32 clock cycles to ensure the EEPROM flip-flop is initialized prior to the read cycle.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265