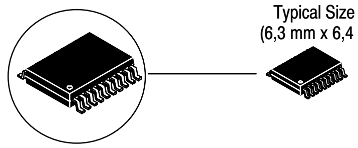


3-V TO 6-V INPUT, 3-A OUTPUT SYNCHRONOUS-BUCK PWM SWITCHER WITH INTEGRATED FETs (SWIFT™)

FEATURES

- 60-mΩ MOSFET Switches for High Efficiency at 3-A Continuous Output Source or Sink Current
- 0.9-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.3-V Fixed Output Voltage Devices With 1% Initial Accuracy
- Internally Compensated for Low Parts Count
- Fast Transient Response
- Wide PWM Frequency: Fixed 350 kHz, 550 kHz, or Adjustable 280 kHz to 700 kHz
- Load Protected by Peak Current Limit and Thermal Shutdown
- Integrated Solution Reduces Board Area and Total Cost

APPLICATIONS

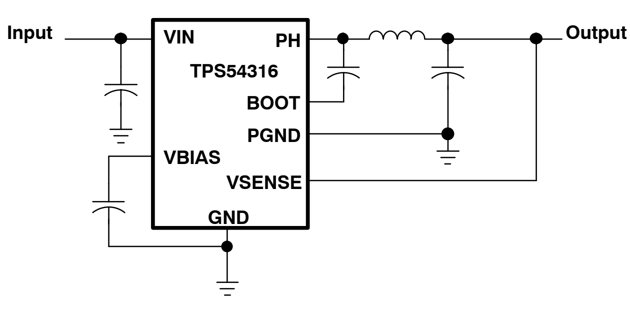
- Low-Voltage, High-Density Systems With Power Distributed at 5 V or 3.3 V
- Point of Load Regulation for High Performance DSPs, FPGAs, ASICs, and Microprocessors
- Broadband, Networking and Optical Communications Infrastructure
- Portable Computing/Notebook PCs

DESCRIPTION

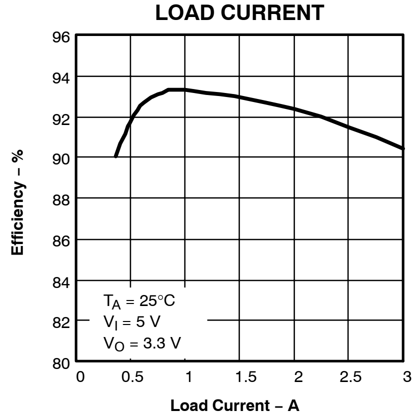
As members of the SWIFT family of dc/dc regulators, the TPS54311, TPS54312, TPS54313, TPS54314, TPS54315 and TPS54316 low-input-voltage high-output-current synchronous-buck PWM converters integrate all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that provides high performance under transient conditions; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a power good output useful for processor/logic reset, fault signaling, and supply sequencing.

The TPS54311, TPS54312, TPS54313, TPS54314, TPS54315 and TPS54316 devices are available in a thermally enhanced 20-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks. TI provides evaluation modules and the SWIFT designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

Simplified Schematic



EFFICIENCY
vs
LOAD CURRENT



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	OUTPUT VOLTAGE	PACKAGED DEVICES PLASTIC HTSSOP (PWP)(1)(2)	T_A	OUTPUT VOLTAGE	PACKAGED DEVICES PLASTIC HTSSOP (PWP)(1)(2)
−40°C to 85°C	0.9 V	TPS54311PWP	−40°C to 85°C	1.8 V	TPS54314PWP
	1.2 V	TPS54312PWP		2.5 V	TPS54315PWP
	1.5 V	TPS54313PWP		3.3 V	TPS54316PWP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2)) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54316PWPR). See application section of data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TPS54310
Input voltage range, V_I	VIN, SS/ENA, SYNC	−0.3 V to 7 V
	RT	−0.3 V to 6 V
	VSENSE	−0.3 V to 4 V
	BOOT	−0.3 V to 17 V
Output voltage range, V_O	VBIAS, PWRGD, COMP	−0.3 V to 7 V
	PH	−0.6 V to 10 V
Source current, I_O	PH	Internally Limited
	COMP, VBIAS	6 mA
Sink current	PH	6 A
	COMP	6 mA
	SS/ENA,PWRGD	10 mA
Voltage differential	AGND to PGND	±0.3 V
Operating virtual junction temperature range, T_J		−40°C to 125°C
Storage temperature, T_{stg}		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage range, V_I	3		6	V
Operating junction temperature, T_J	−40		125	°C

PACKAGE DISSIPATION RATINGS(1) (2)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
20-Pin PWP with solder	26.0°C/W	3.85 W(3)	2.12 W	1.54 W
20-Pin PWP without solder	57.5°C/W	1.73 W	0.96 W	0.69 W

(1) For more information on the PWP package, refer to TI technical brief (SLMA002).
(2) Test board conditions:
1. 3” × 3”, 2 layers, Thickness: 0.062”
2. 1.5 oz copper traces located on the top of the PCB
3. 1.5 oz copper ground plane on the bottom of the PCB
4. Ten thermal vias (see recommended land pattern in application section of this data sheet)

(3) Maximum power dissipation may be limited by overcurrent protection.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, VIN = 3 V to 6 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN					
VIN input voltage range		3		6	V
Quiescent current	f_s = 350 kHz, FSEL = 0.8 V, RT open		6.2	9.6	mA
	f_s = 550 kHz, FSEL ≥ 2.5 V, RT open, Phase pin open		8.4	12.8	
	Shutdown, SS/ENA = 0 V		1	1.4	
UNDER VOLTAGE LOCK OUT					
Start threshold voltage, UVLO			2.95	3	V
Stop threshold voltage, UVLO		2.70	2.80		
Hysteresis voltage, UVLO		0.14	0.16		V
Rising and falling edge deglitch, UVLO(1)			2.5		µs
BIAS VOLTAGE					
Output voltage, VBIAS	$I_{(VBIAS)}$ = 0	2.70	2.80	2.90	V
Output current, VBIAS(2)				100	µA
OUTPUT VOLTAGE					
V_O Output voltage, TPS54311	T_J = 25°C, VIN = 5 V		0.9		V
	3 ≤ VIN ≤ 6 V, 0 ≤ IL ≤ 3 A, –40 ≤ T_J ≤ 125	–2.5%		2.5%	
TPS54312	T_J = 25°C, VIN = 5 V		1.2		V
	3 ≤ VIN ≤ 6 V, 0 ≤ IL ≤ 3 A, –40 ≤ T_J ≤ 125	–2.5%		2.5%	
TPS54313	T_J = 25°C, VIN = 5 V		1.5		V
	3 ≤ VIN ≤ 6 V, 0 ≤ IL ≤ 3 A, –40 ≤ T_J ≤ 125	–2.5%		2.5%	
TPS54314	T_J = 25°C, VIN = 5 V		1.8		V
	3 ≤ VIN ≤ 6 V, 0 ≤ IL ≤ 3 A, –40 ≤ T_J ≤ 125	–2.5%		2.5%	
TPS54315	T_J = 25°C, VIN = 5 V		2.5		V
	3 ≤ VIN ≤ 6 V, 0 ≤ IL ≤ 3 A, –40 ≤ T_J ≤ 125	–2.5%		2.5%	
TPS54316	T_J = 25°C, VIN = 5 V		3.3		V
	3 ≤ VIN ≤ 6 V, 0 ≤ IL ≤ 3 A, –40 ≤ T_J ≤ 125	–2.5%		2.5%	
REGULATION					
Line regulation(1) (3)	I_L = 1.5 A, 350 ≤ f_s ≤ 550 kHz, T_J = 85°C		0.21		%/V
Load regulation (1) (3)	I_L = 0 A to 3 A, 350 ≤ f_s ≤ 550 kHz, T_J = 85°C		0.21		%/A
OSCILLATOR					
Internally set free-running frequency range	FSEL ≤ 0.8 V, RT open	280	350	420	kHz
	FSEL ≥ 2.5 V, RT open	440	550	660	
Externally set free-running frequency range	RT = 180 kΩ (1% resistor to AGND)(1)	252	280	308	kHz
	RT = 100 kΩ (1% resistor to AGND)	460	500	540	
	RT = 68 kΩ (1% resistor to AGND)(1)	663	700	762	
High-level threshold voltage at FSEL		2.5			V
Low-level threshold voltage at FSEL				0.8	V
Ramp valley(1)			0.75		V
Ramp amplitude (peak-to-peak)(1)			1		V
Minimum controllable on time(1)				200	ns
Maximum duty cycle		90%			

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 10.

TEXAS INSTRUMENTS
www.ti.com

ELECTRICAL CHARACTERISTICS (continued)

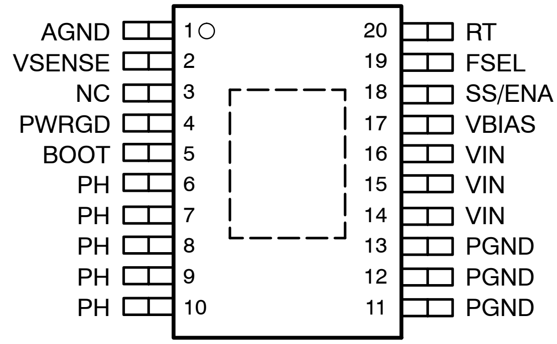
T_J = –40°C to 125°C, VIN = 3 V to 6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
Error amplifier open loop voltage gain(1)				26		dB
Error amplifier unity gain bandwidth(1)			3	5		MHz
PWM COMPARATOR						
PWM comparator propagation delay time, PWM comparator input to PH pin (excluding dead time)		10 mV overdrive(1)		70	85	ns
SLOW-START/ENABLE						
Enable threshold voltage, SS/ENA			0.82	1.20	1.40	V
Enable hysteresis voltage, SS/ENA(1)				0.03		V
Falling edge deglitch, SS/ENA(1)				2.5		µs
Internal slow-start time(1)	TPS54311		2.6	3.3	4.1	ms
	TPS54312		3.5	4.5	5.4	
	TPS54313		4.4	5.6	6.7	
	TPS54314		2.6	3.3	4.1	
	TPS54315		3.6	4.7	5.6	
	TPS54316		4.7	6.1	7.6	
Charge current, SS/ENA		SS/ENA = 0 V	3	5	8	µA
Discharge current, SS/ENA		SS/ENA = 0.2 V, V_I = 1.5 V	1.5	2.3	4	mA
POWER GOOD						
Power good threshold voltage		VSENSE falling		90		$\%V_{ref}$
Power good hysteresis voltage(1)				3		$\%V_{ref}$
Power good falling edge deglitch(1)				35		µs
Output saturation voltage, PWRGD		$I_{(sink)}$ = 2.5 mA		0.18	0.30	V
Leakage current, PWRGD		V_I = 5.5 V			1	µA
CURRENT LIMIT						
Current limit trip point		V_I = 3 V, output shorted(1)	4	6.5		A
		V_I = 6 V, output shorted(1)	4.5	7.5		
Current limit leading edge blanking time		(1)		100		ns
Current limit total response time		(1)		200		ns
THERMAL SHUTDOWN						
Thermal shutdown trip point(1)			135	150	165	°C
Thermal shutdown hysteresis(1)				10		°C
OUTPUT POWER MOSFETS						
$r_{DS(on)}$ Power MOSFET switches		V_I = 6 V(2)		59	88	mΩ
		V_I = 3 V(2)		85	136	

(1) Specified by design
(2) Matched MOSFETs, low side $r_{DS(on)}$ production tested, high side $r_{DS(on)}$ specified by design

PIN ASSIGNMENTS

**PWP PACKAGE
(TOP VIEW)**

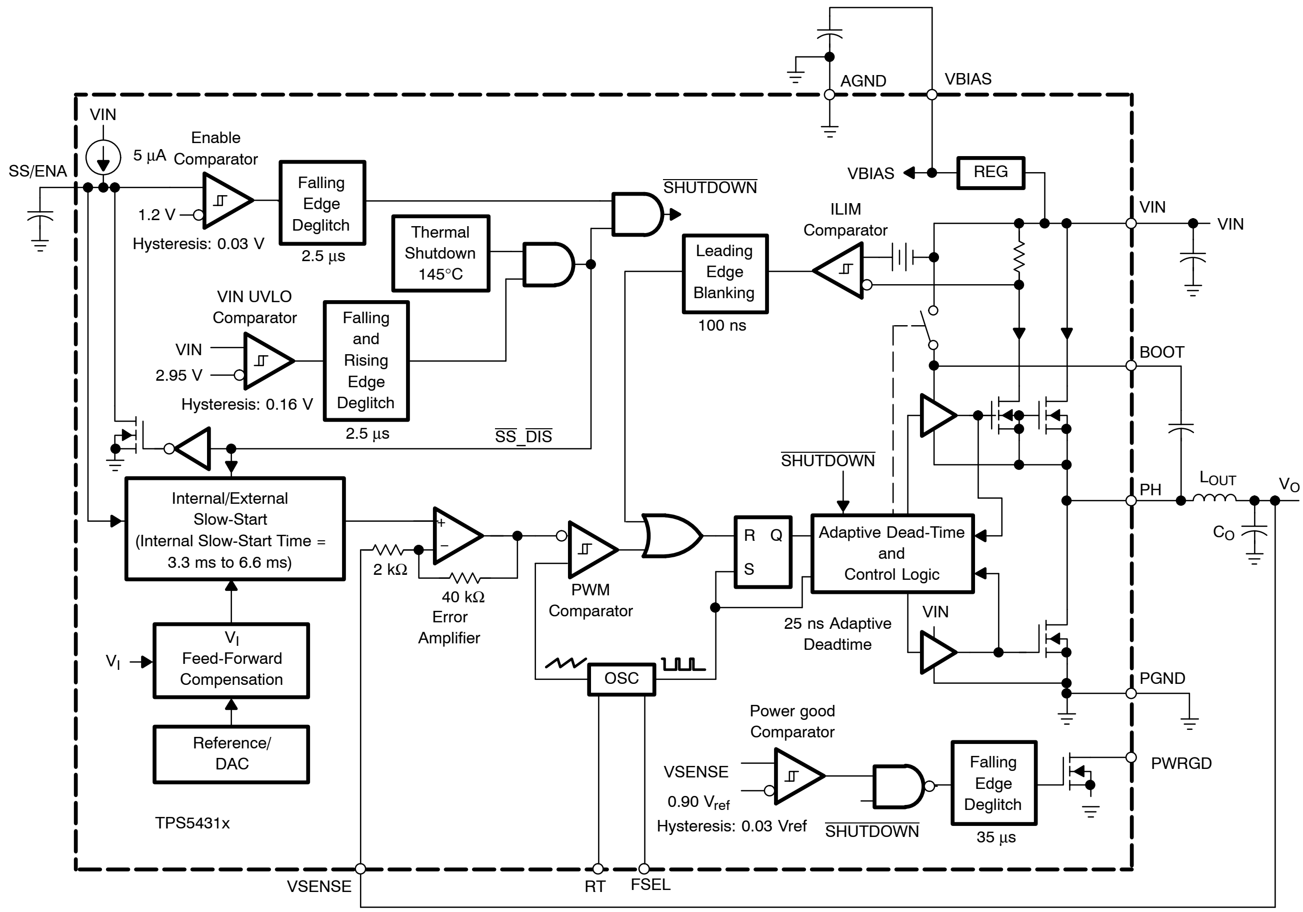


NC − No internal connection

Terminal Functions

TERMINAL NAME	NO.	DESCRIPTION
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, RT resistor and FSEL pin. Make PowerPAD connection to AGND.
BOOT	5	Bootstrap input. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
FSEL	19	Frequency select input. Provides logic input to select between two internally set switching frequencies.
NC	3	No connection
PGND	11−13	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors.
PH	6−10	Phase input/output. Junction of the internal high and low-side power MOSFETs, and output inductor.
PWRGD	4	Power good open drain output. Hi-Z when VSENSE ≥ 90% V_{ref}, otherwise PWRGD is low. Note that output is low when SS/ENA is low or internal shutdown signal active.
RT	20	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, f_s.
SS/ENA	18	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
VBIAS	17	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low ESR 0.1-µF to 1.0-µF ceramic capacitor.
VIN	14−16	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high quality, low ESR 1-µF to 10-µF ceramic capacitor.
VSENSE	2	Error amplifier inverting input. Connect directly to output voltage sense point.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

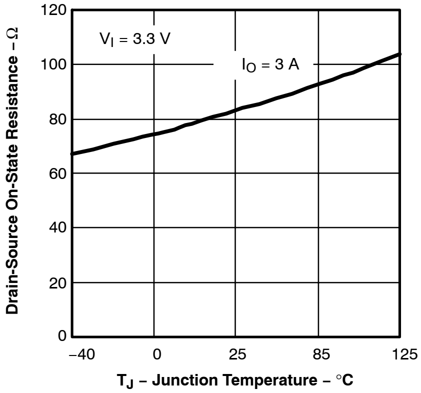


Figure 1

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

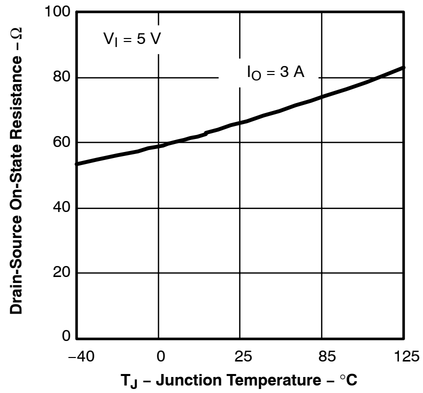


Figure 2

INTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

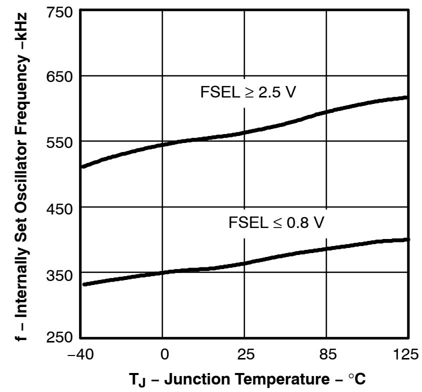


Figure 3

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

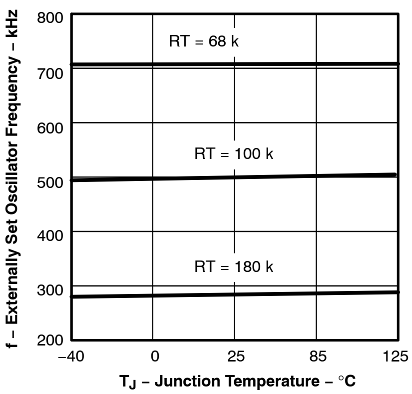


Figure 4

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

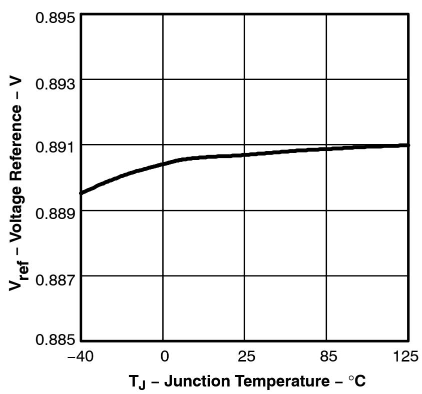


Figure 5

OUTPUT VOLTAGE REGULATION vs INPUT VOLTAGE

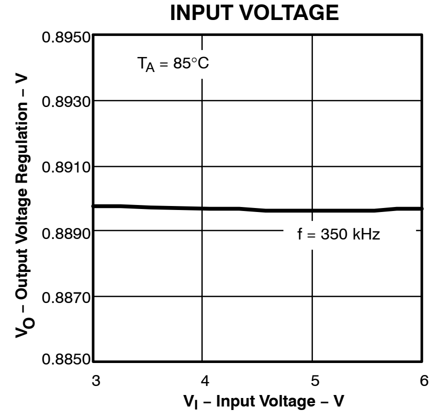


Figure 6

ERROR AMPLIFIER OPEN LOOP RESPONSE

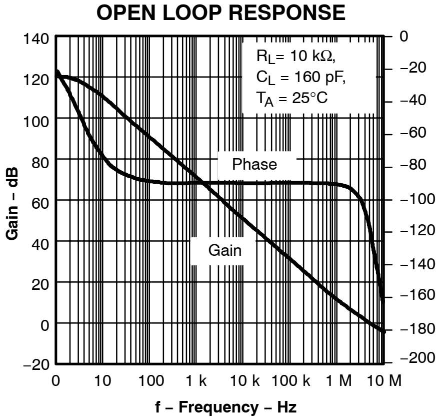


Figure 7

INTERNAL SLOW-START TIME vs JUNCTION TEMPERATURE

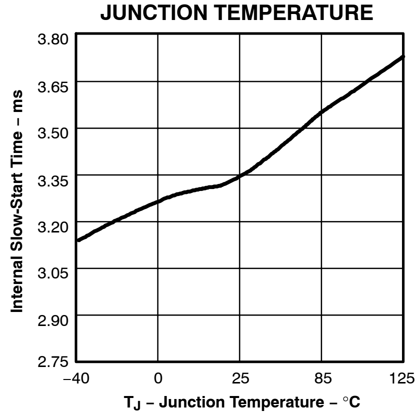


Figure 8

DEVICE POWER LOSSES vs LOAD CURRENT

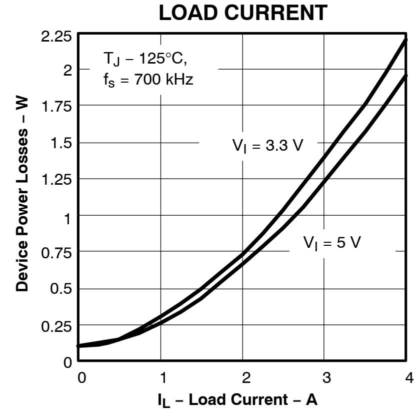


Figure 9

APPLICATION INFORMATION

Figure 10 shows the schematic diagram for a typical TPS54314 application. The TPS54314 (U1) can provide up to 3 A of output current at a nominal output voltage of 1.8 V. For proper thermal performance, the PowerPAD underneath the TPS54314 integrated circuit needs to be soldered to the printed circuit board.

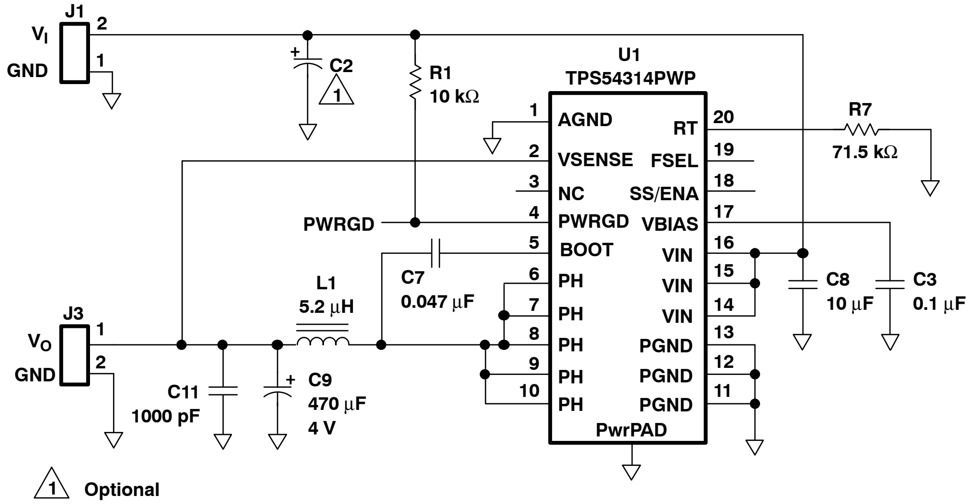


Figure 10. TPS54314 Schematic

INPUT VOLTAGE

The input to the circuit is a nominal 5 VDC, applied at J1. The optional input filter (C2) is a 220-µF POSCAP capacitor, with a maximum allowable ripple current of 3 A. C8 is the decoupling capacitor for the TPS54314 and must be located as close to the device as possible.

FEEDBACK CIRCUIT

The output voltage of the converter is fed directly into the VSENSE pin of the TPS54314. The TPS54314 is internally compensated to provide stability of the output under varying line and load conditions.

OPERATING FREQUENCY

In the application circuit, a 700 kHz operating frequency is selected by leaving FSEL open and connecting a 71.5 kΩ resistor between the RT pin and AGND. Different operating frequencies may be selected by varying the value of R3 using equation 1:

$$R = \frac{500\ \text{kHz}}{\text{Switching Frequency}} \times 100\ \text{k}\Omega \tag{1}$$

Alternately, preset operating frequencies of 350 kHz or 550 kHz my be selected by leaving RT open and connecting the FSEL pin to AGND or VIN respectively.

OUTPUT FILTER

The output filter is composed of a 5.2-µH inductor and 470-µF capacitor. The inductor is a low dc resistance (16-mΩ) type, Sumida CDRH104R−5R2. The capacitor used is a 4-V POSCAP with a maximum ESR of 40 mΩ. The output filter components work with the internal compensation network to provide a stable closed loop response for the converter.

PCB LAYOUT

Figure 11 shows a generalized PCB layout guide for the TPS54311−16.

The VIN pins should be connected together on the printed circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS54311−16 ground pins. The minimum recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the PGND pins.

The TPS54311−16 has two internal grounds (analog and power). Inside the TPS54311−16, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. Noise injected between the two grounds can degrade the performance of the TPS54311−16, particularly at higher output currents. Ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground traces are recommended. There should be an area of ground one the top layer directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The AGND and PGND pins should be tied to the PCB ground by connecting them to the ground area under the device as shown. The only components that should tie directly to the power ground plane are the input capacitors, the output capacitors, the input voltage decoupling capacitor, and the PGND pins of the TPS54311−16. Use a separate wide trace for the analog ground signal path. This analog ground should be used for the timing resistor RT, slow-start capacitor and bias capacitor grounds. Connect this trace directly to AGND (pin 1).

The PH pins should be tied together and routed to the output inductor. Since the PH connection is the switching node, inductor should be located very close to the PH pins and the area of the PCB conductor minimized to prevent excessive capacitive coupling.

Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths.

Connect the output filter capacitor(s) as shown between the VOUT trace and PGND. It is important to keep the loop formed by the PH pins, Lout, Cout and PGND as small as practical.

Connect the output of the circuit directly to the VSENSE pin. Do not place this trace too close to the PH trace. Do to the size of the IC package and the device pinout, they will have to be routed somewhat close, but maintain as much separation as possible while still keeping the layout compact.

Connect the bias capacitor from the VBIAS pin to analog ground using the isolated analog ground trace. If a slow-start capacitor or RT resistor is used, or if the SYNC pin is used to select 350-kHz operating frequency, connect them to this trace as well.

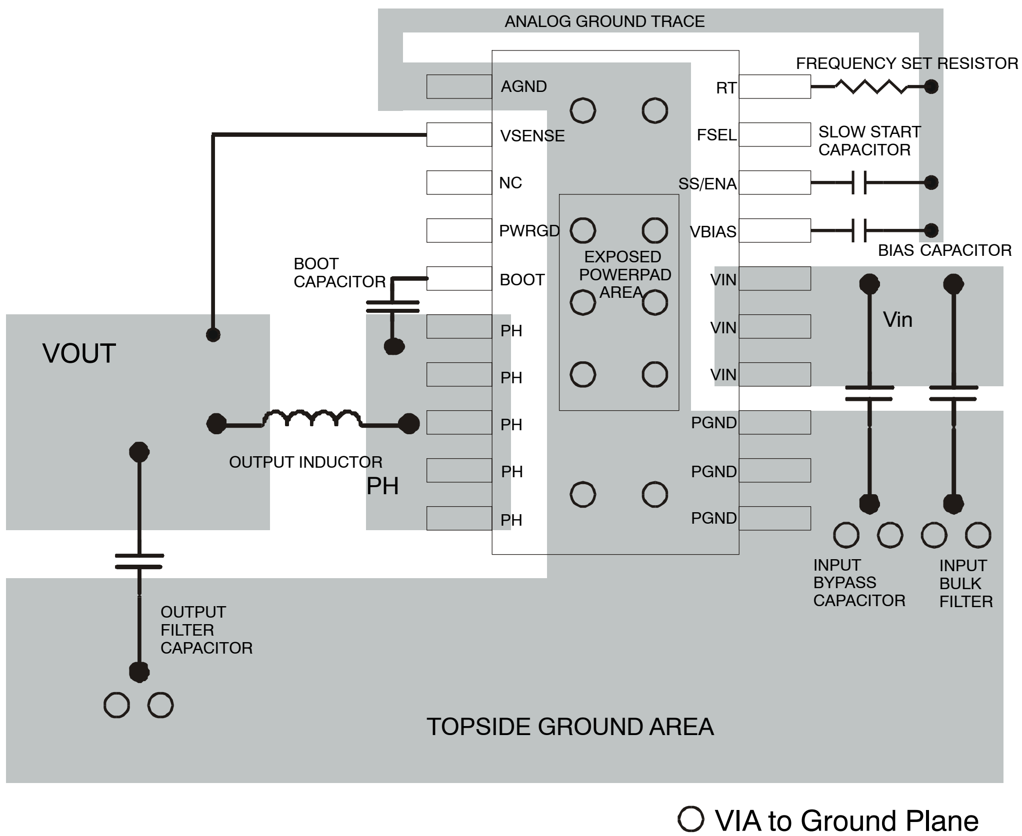


Figure 11. TPS54311 − 16 PCB Layout

LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

For operation at full rated load current, the analog ground plane must provide adequate heat dissipating area. A 3 inch by 3 inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD should be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available should be used when 3 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer should be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Six vias should be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the ten recommended that enhance thermal performance should be included in areas not under the device package.

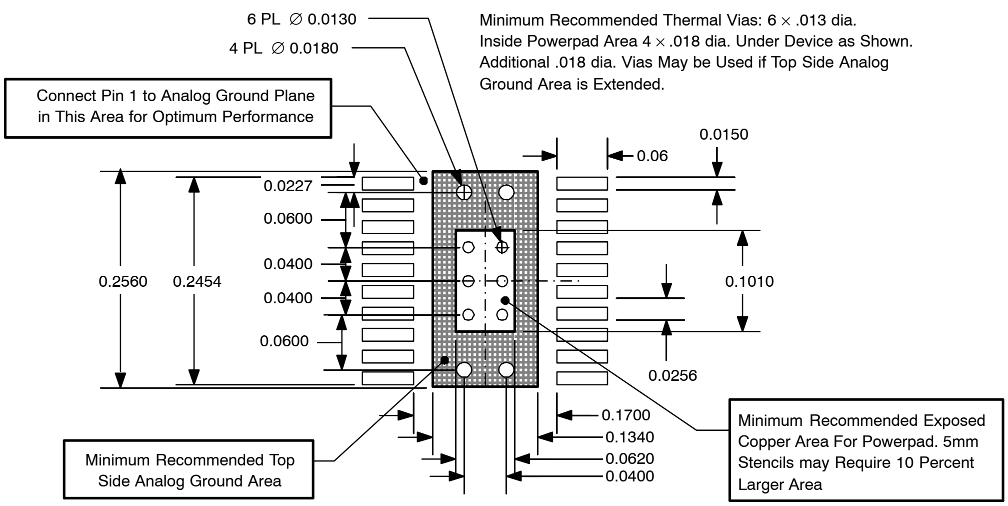


Figure 12. Recommended Land Pattern for 20-Pin PWP PowerPAD

PERFORMANCE GRAPHS

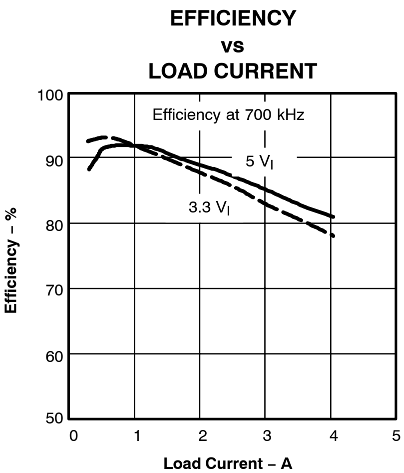


Figure 13

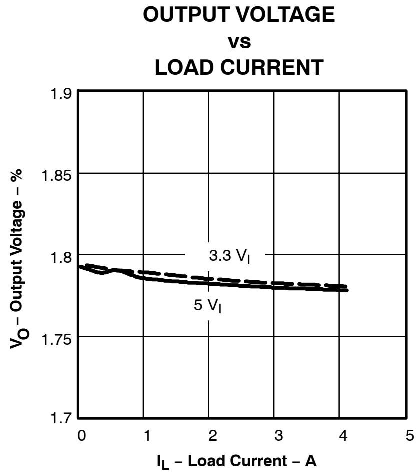


Figure 14

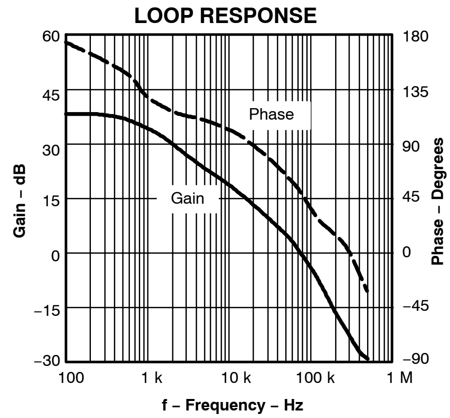


Figure 15

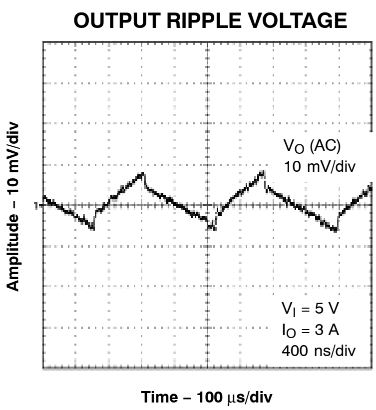


Figure 16

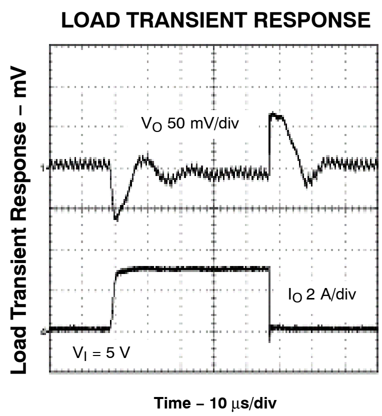


Figure 17

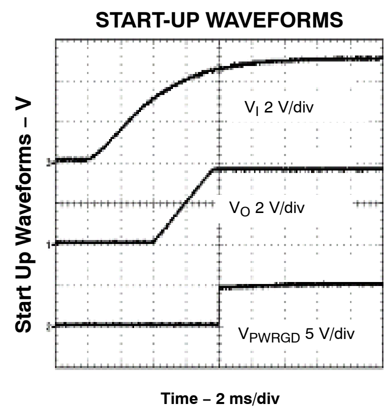


Figure 18

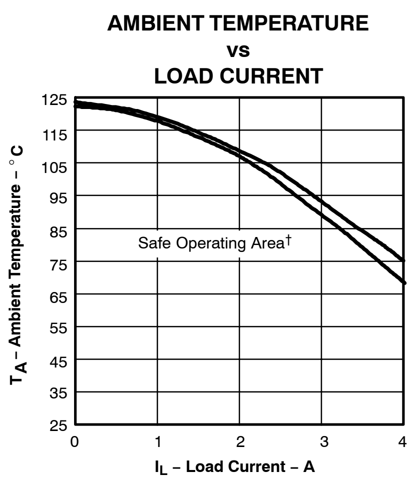


Figure 19

† Safe operating area is applicable to the test board conditions listed in the Dissipation Rating Table section of this data sheet.

DETAILED DESCRIPTION

Under Voltage Lock Out (UVLO)

The TPS54311 − 16 incorporates an under voltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-µs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

Slow-Start/Enable (SS/ENA)

The slow-start/enable pin provides two functions; first, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-µs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

DEVICE	OUTPUT VOLTAGE	SLOW-START
TPS54311	0.9 V	3.3 ms
TPS54312	1.2 V	4.5 ms
TPS54313	1.5 V	5.6 ms
TPS54314	1.8 V	3.3 ms
TPS54315	2.5 V	4.7 ms
TPS54316	3.3 V	6.1 ms

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND. Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\ \text{V}}{5\ \mu\text{A}} \qquad (2)$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ \text{V}}{5\ \mu\text{A}} \qquad (3)$$

The actual slow-start is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

VBIAS Regulator (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor should be placed close to the VBIAS pin and returned to AGND. External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.70 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

Voltage Reference

The voltage reference system produces a precise V_{ref} signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high precision regulation of the TPS54311 − 16, since it cancels offset errors in the scale and error amplifier circuits.

Oscillator and PWM Ramp

The oscillator frequency can be set to internally fixed values of 350 kHz or 550 kHz using the FSEL pin as a static digital input. If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 kHz to 700 kHz by connecting a resistor to the RT pin to ground and floating the FSEL pin. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{SWITCHING FREQUENCY} = \frac{100\ \text{k}\Omega}{R} \times 500\ \text{kHz} \qquad (4)$$

Table 1. Summary of the Frequency Selection Configurations

SWITCHING FREQUENCY	FSEL PIN	RT PIN
350 kHz, internally set	Float or AGND	Float
550 kHz, internally set	≥ 2.5 V	Float
Externally set 280 kHz to 700 kHz	Float	R = 68 k to 180 k

Error Amplifier

The high performance, wide bandwidth, voltage error amplifier is gain limited to provide internal compensation of the control loop. The user is given limited flexibility in choosing output L and C filter components. Inductance values of 4.7 µH to 10 µH are typical and available from several vendors. The resulting designs exhibit good noise and ripple characteristics, along with exceptional transient response. Transient recovery times are typically in the range of 10 to 20 µs.

PWM Control

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse duration. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as V_{ref}. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54311 − 16 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

Dead-Time Control and MOSFET Drivers

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turn-on times of the MOSFET drivers. The high-side driver does not turn on until the gate drive voltage to the low-side FET is below 2 V. The low-side driver does not turn on until the voltage at the gate of the high-side MOSFETs is below 2 V. The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

Overcurrent Protection

The cycle by cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and differential amplifier and comparing it to the preset overcurrent threshold. The high-side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents false tripping of the current limit. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

Thermal Shutdown

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown when the junction temperature decreases to 10°C below the thermal shutdown trip point and starts up under control of the slow-start circuit. Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the soft-start circuit, heating up due to the fault, and then shutting down upon reaching the thermal shutdown point.

Power Good (PWRGD)

The power good circuit monitors for under voltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold, or SS/ENA is low, or thermal shutdown is asserted. When VIN = UVLO threshold, SS/ENA = enable threshold, and VSENSE > 90% of V_{ref}, the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35-µs falling edge deglitch circuit prevent tripping of the power good comparator due to high frequency noise.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS54311PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54311PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54311PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54311PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54312PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54312PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54312PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54312PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54313PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54313PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54313PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54313PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54314PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54314PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54314PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54314PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54315PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54315PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54315PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54315PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54316PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54316PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54316PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54316PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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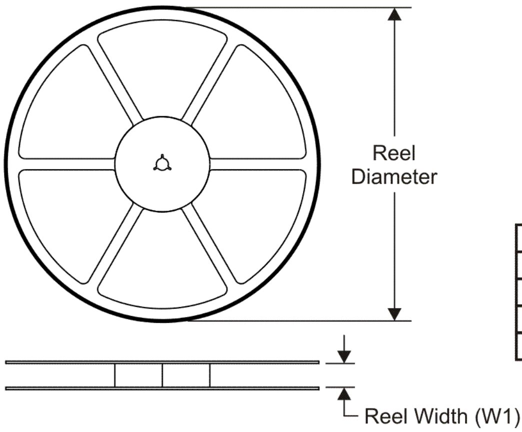
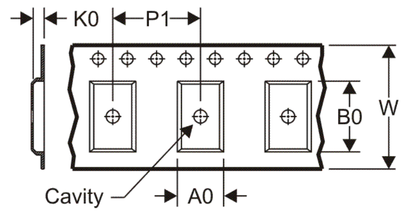
TAPE AND REEL INFORMATION

REEL DIMENSIONS

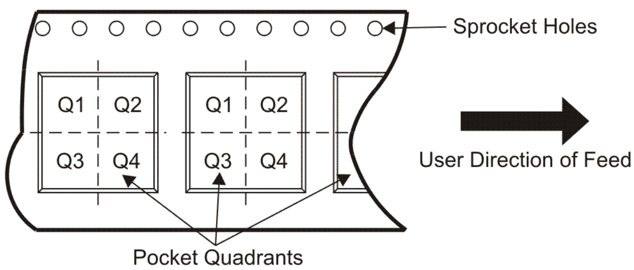


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

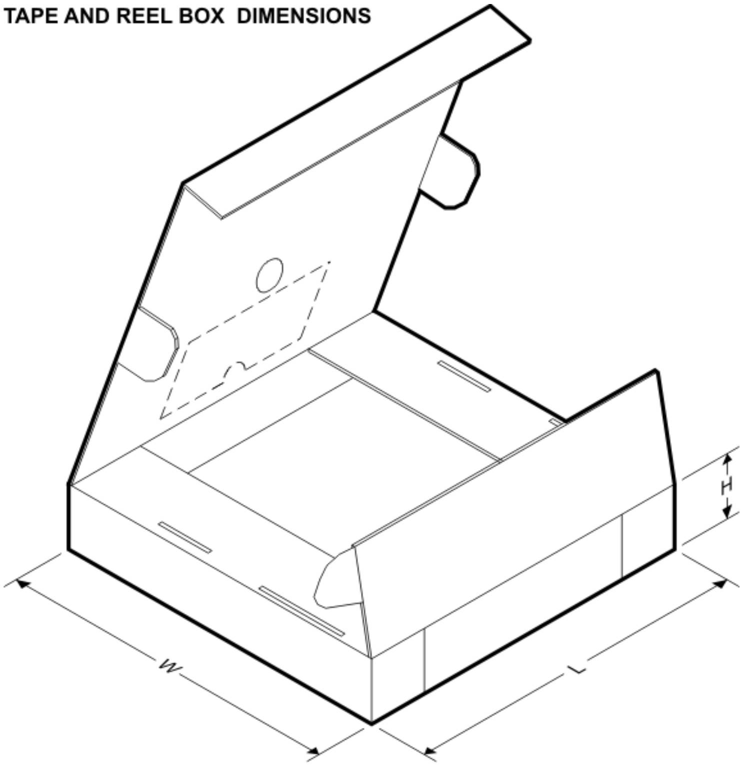
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54311PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS54312PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS54313PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS54314PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS54315PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS54316PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

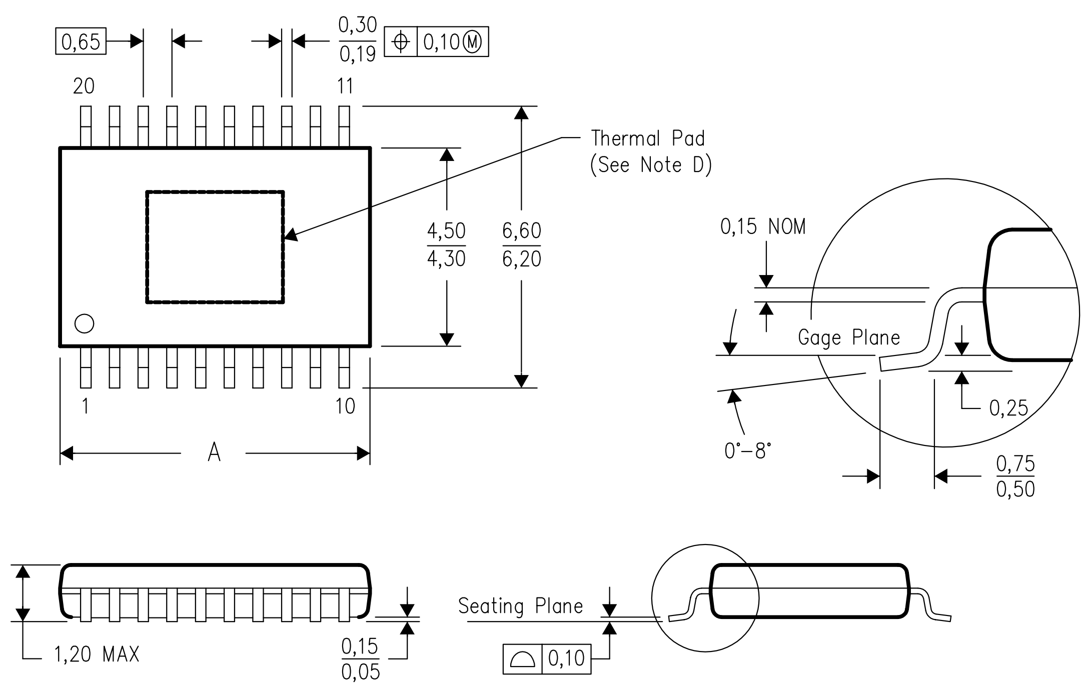


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54311PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS54312PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS54313PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS54314PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS54315PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS54316PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0

PWP (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20 PIN SHOWN



PINS ** / DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/H 12/05

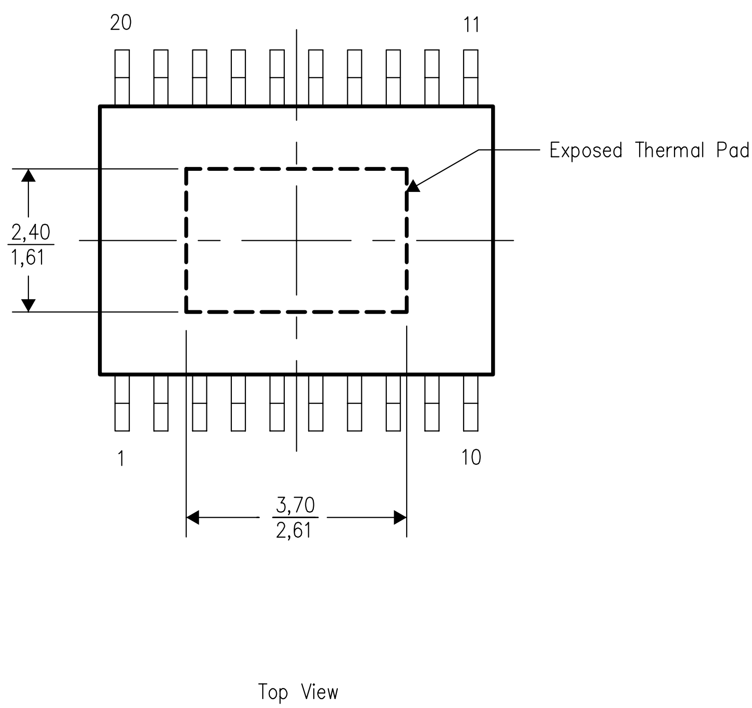
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. Falls within JEDEC MO–153

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

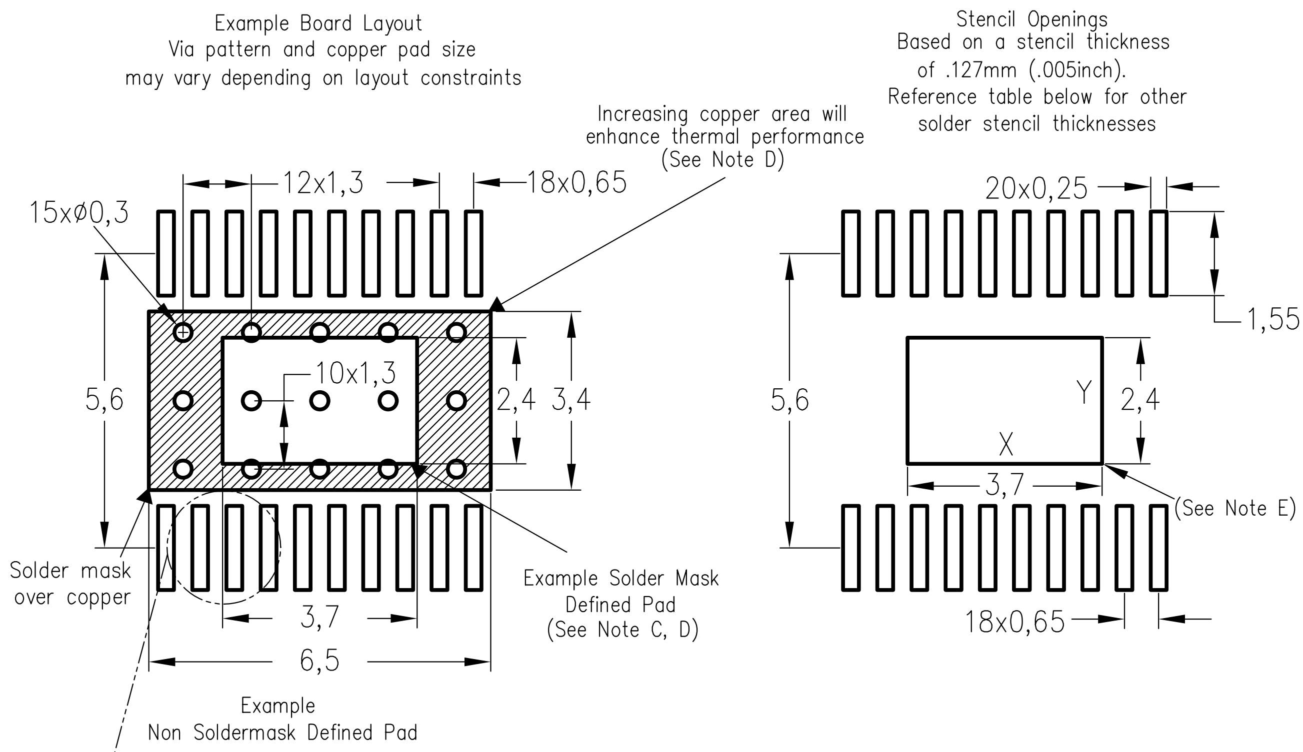
The exposed thermal pad dimensions for this package are shown in the following illustration.

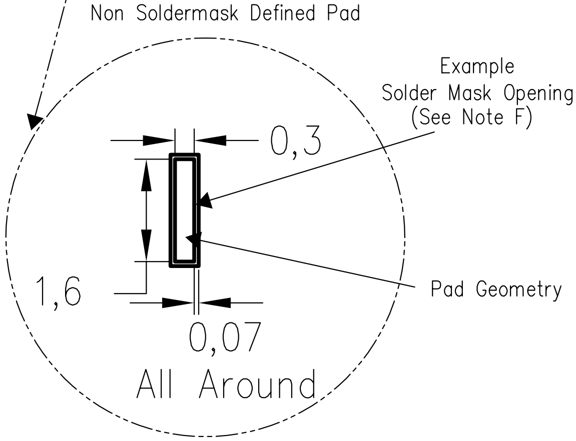


NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R-PDSO-G20) PowerPAD™





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609-7/E 10/07

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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