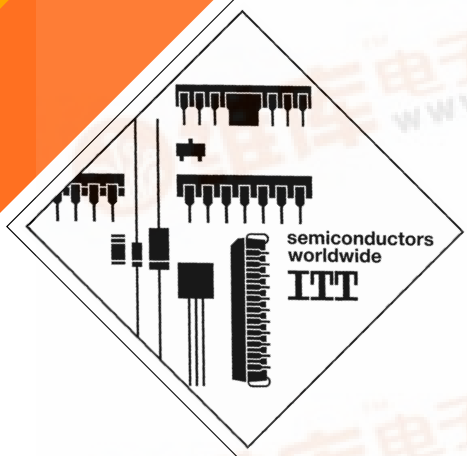


TPU 2735
Teletext Processor

Edition Jan. 13, 1993
6251-312-4E

ITT Semiconductors

TPU 2735

Contents

Contents, continued

TPU 2735

Teletext Processor for Level 1 Teletext

Note:
If not otherwise designated the pin numbers mentioned refer to the 40-pin DIL package.

1. Introduction

The TPU 2735 is specified to handle Level-1-Teletext information (in Germany: Videotext) as it is transmitted today by the TV broadcast stations in Great Britain, Germany and other European countries. The TPU 2735 is part of the DIGIT 2000 digital TV system and works in conjunction with the other VLSI circuits and processors of this system. This makes the Teletext adapter designed with the TPU 2735 very simple and economic (see Fig. 1–1).

The TPU 2735 is an N-channel VLSI MOS circuit, housed in a 40-pin Dil plastic package and contains on a single silicon chip the following functions:

– one-chip solution of the Teletext processing (except for external RAM)

– ghost compensation to eliminate the effects of ghost pictures due to reflections

– reduced access time is provided for the Teletext pages by receiving and storing up to eight pages in one go

– up to 32 stored pages

– automatic language-dependent character selection

– switchover facility PAL/NTSC/D2MAC

– full level one features (FLOF) support

– level 1.5 Spanish Teletext support

– largely compatible to the TPU 2732/33

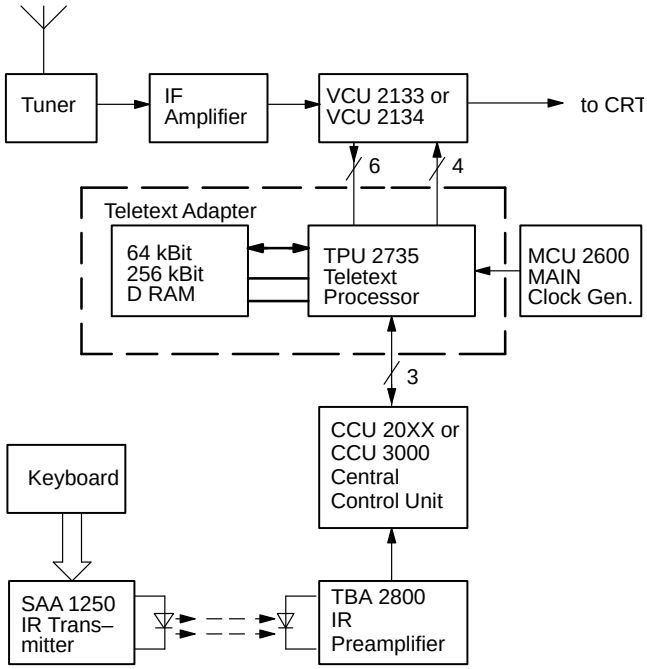


Fig. 1–1: Teletext application block diagram

2. Functional Description

The TPU 2735 whose block diagram is shown in Fig. 2–1, operates according to a rigid timing determined by the vertical cycle of the TV receiver. The data acquisition period starts at line 7 with PAL or line 10 with NTSC and ends at line 22 with PAL or line 21 with NTSC. During this period, the input data is processed by a ghost filter which is able to compensate reflections with short delay time of 0 to 0.8 µs for PAL or 0 to 1 µs for NTSC. In the D2MAC mode the acquisition is active from line 1 to 22 and line 313 to 334.

In the Data Acquisition Unit the Teletext information is synchronized and identified. A comparator preselects the pages with page numbers that are requested by the CCU 2000 or CCU 3000 Central Control Unit and loads them into the RAM. To eliminate speed problems of the external Dynamic RAM, the data is buffered in an internal RAM buffer (Fig. 2–1). The comparator contained in the data acquisition unit decides into which sector of the DRAM the data is stored.

The display period starts at line 48 with PAL or line 50 with NTSC and ends at line 286 with PAL or line 242 with NTSC. The display control unit selects one of the stored eight pages for display. The 8-bit character words are transformed into a 6 x 10 dot matrix with PAL or 6 x 8 dot matrix with NTSC by a character generator (ROM) of 96 programmed characters and are displayed in 24 rows of 40 characters each. Optionally, 25 rows can be displayed in PAL/D2MAC. Different character sets are available for eight languages under CCU or transmitter control, the required character set being selected automatically by the control bits C_{12} to C_{14} of row 0 of the Teletext page displayed. Every tenth line with PAL or every eighth line with NTSC a new Teletext row is loaded from the DRAM into the RAM buffer. When the RAM is not accessed by the TPU 2735, the memory control refreshes the memory and handles CCU requests for RAM access.

Via the IM bus the CCU can access all RAM locations and controls the TPU 2735 by loading the appropriate registers in the RAM, so that the TPU 2735 can be used to display text from other sources. The TPU 2735 can display a list of contents of the stored eight pages (menu) all by itself.The TPU 2735 can use either one 64 Kx1 bit Dynamic RAM or one 256 Kx1 bit Dynamic RAM. So, RAM capacity is flexible to store up to 32 pages. The DRAMs can be standard types (see section 3.).

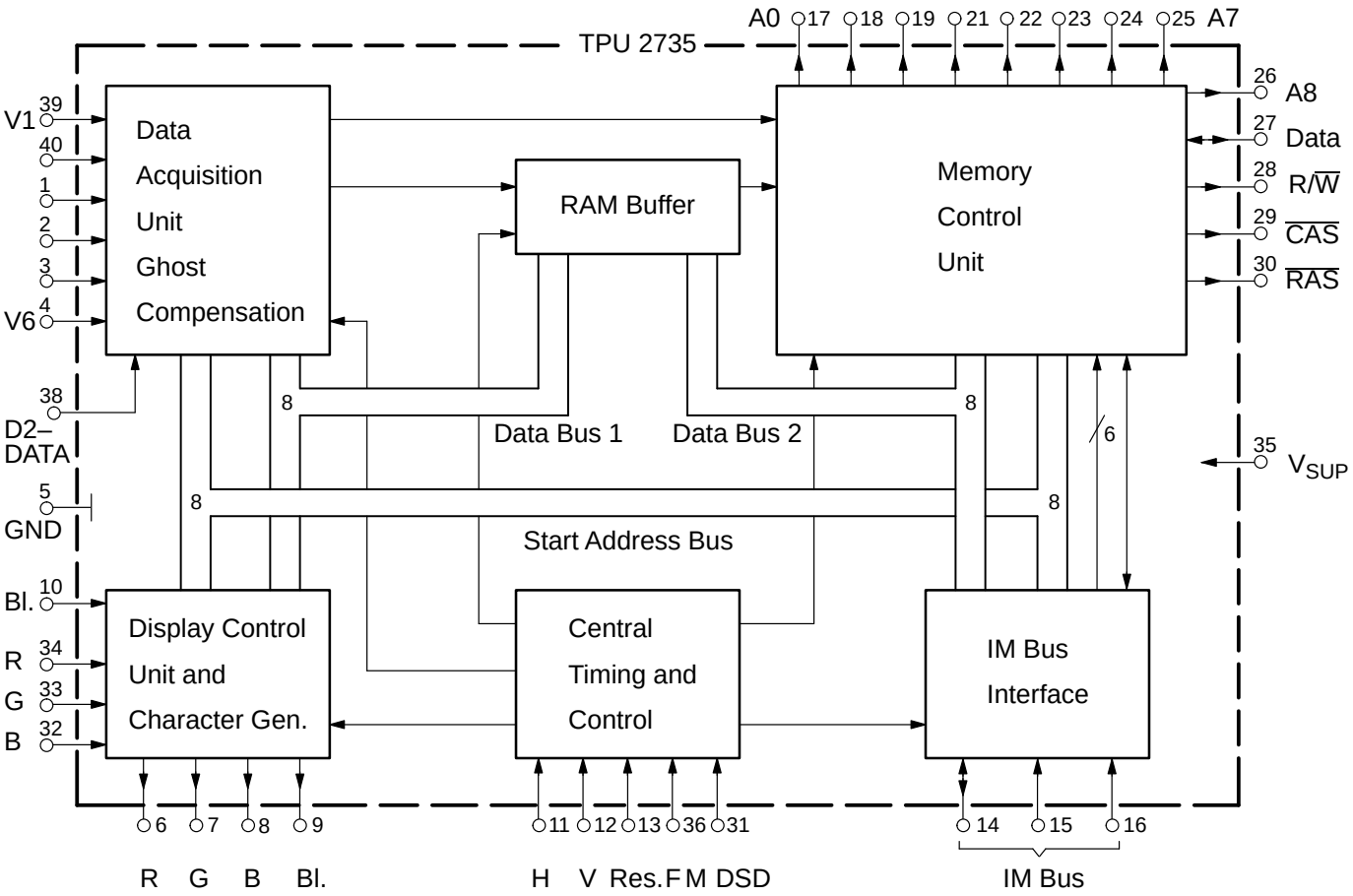


Fig. 2–1: Block diagram of the TPU 2735

3. Specifications

3.1. Outline Dimensions

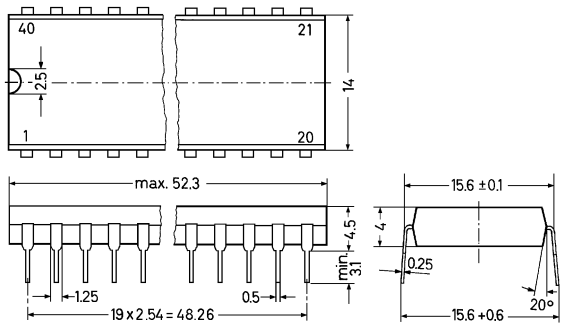


Fig. 3–1: TPU 2735 in 40-pin DIL package
Weight approx. 6 g, Dimensions in mm

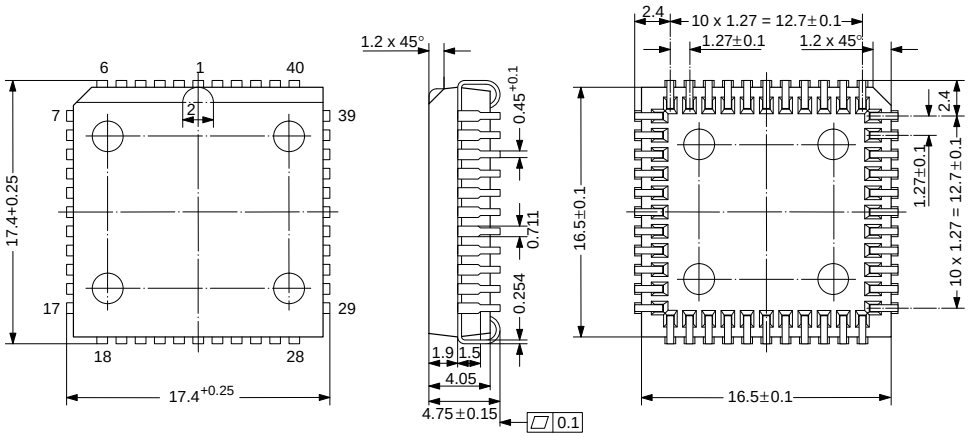


Fig. 3–2: TPU 2735 in 44-pin PLCC package,
Weight approx. 2.2 g, Dimensions in mm

3.2. Pin Connections

3.2.1. 40-Pin Dil Plastic Package

1. V3 Video Input
2 V4 Video Input
3 V5 Video Input
4 V6 Video Input (MSB)
5 GND
6 R Output
7 G Output
8 B Output
9 Fast Blanking Output
10 Fast Blanking Input
11 Horizontal Blanking Pulse Input/D2SYNC Input
12 Vertical Blanking Pulse Input
13 $\overline{\text{Reset}}$ Input
14 IM Bus Data Input/Output
15 IM Bus Ident Input
16 IM Bus Clock Input
17 A0 RAM Address Output
18 A1 RAM Address Output

19 A2 RAM Address Output
20 N.C.
21 A3 RAM Address Output
22 A4 RAM Address Output
23 A5 RAM Address Output
24 A6 RAM Address Output
25 A7 RAM Address Output
26 A8 RAM Address Output
27 Data Input/Output
28 Read/$\overline{\text{Write}}$ Output
29 $\overline{\text{CAS}}$ Output
30 $\overline{\text{RAS}}$ Output
31 Skew Data Input
32 B Input
33 G Input
34 R Input
35 V_{SUP}
36 ΦM Main Clock Input
37 N.C.
38 D2Data Input
39 V1 Video Input (LSB)
40 V2 Video Input

3.2.2. 44-Pin PLCC Package

1 V2 Video Input
2 Leave Vacant
3 V3 Video Input
4 V4 Video Input
5 V5 Video Input
6 V6 Video Input (MSB)
7 GND
8 R Output
9 G Output
10 B Output
11 Fast Blanking Output
12 Fast Blanking Input
13 Horizontal Blanking Pulse Input / D2SYNC Input
14 $\overline{\text{Reset}}$ Input
15 IM Bus Data Input/Output
16 IM Bus Ident Input
17 IM Bus Clock Input
18 A0 RAM Address Output
19 Leave Vacant
20 Leave Vacant
21 A1 RAM Address Output
22 A2 RAM Address Output
23 Vertical Blanking Pulse Input
24 A3 RAM Address Output
25 A4 RAM Address Output
26 A5 RAM Address Output
27 A6 RAM Address Output
28 A7 RAM Address Output
29 A8 RAM Address Output
30 Data Input/Output
31 Read/$\overline{\text{Write}}$ Output
32 $\overline{\text{CAS}}$ Output
33 $\overline{\text{RAS}}$ Output
34 Skew Data Input
35 B Input
36 G Input
37 R Input
38 GND
39 VSUP
40 ΦM Main Clock Input
41 Leave Vacant
42 D2 Data Input
43 Leave Vacant
44 V1 Video Input (LSB)

3.3. Pin Descriptions (for 40-pin DIL package)

Pin 1 to 4 and 39, 40 – Video Inputs V1 to V6 (Fig. 3–4)
Inputs for the digitized composite video signal from the VCU 213x or VAD 2150. The video signal uses a parallel Gray code, input V6 is the most significant bit (MSB).

Pin 5 – Ground, 0 V

Pins 6 to 9 – R, G, B and Fast Blanking Outputs (Fig. 3–6 and 3–7)
The R, G and B outputs deliver the Teletext RGB signal to the additional RGB inputs (pins 30 to 32) of the VCU 2133 or VCU 2134 in the case of Teletext operation. The fast blanking output serves for switching the video channel between normal TV and Teletext operation. It must be connected to the fast blanking input (pin 33) of the VCU.

Pin 10 – Fast Blanking Input (Fig. 3–10)
This pin is used to switch over to an external RGB source. The external RGB signal is connected to pins 32 to 34 of the TPU 2735. A low level at pin 10 switches the external RGB signal to the RGB outputs of the TPU 2735 and enables the Fast Blanking Output (pin 9 high). Pin 10 floats to a high level if not connected. The RGBE control bit sets the priority to the external RGB inputs if both, teletext and external RGB are active. Two bits in the IM Bus Hardware test/configuration register (see section 6.4.) allow to select the polarity of pin 10 and overwrite the fast blank signal.Boxes of TPU text can be cut into an external RGB signal. The RGB and blanking outputs are controlled according to the table below. The settings TTM=1 and RGBE=0 are recommended for normal Teletext. For on-screen display, TTM=1 and RGBE=1 are recommended. For clarification, the connections are shown in Fig. 3–2 and the TV display appearance in Fig. 3–3.

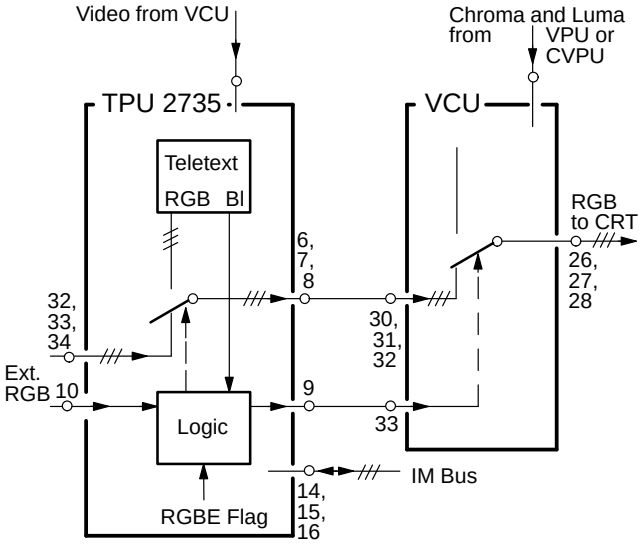


Fig. 3–3: Signal paths for RGB signals in TPU 2735 and VCU 2133 or VCU 2134

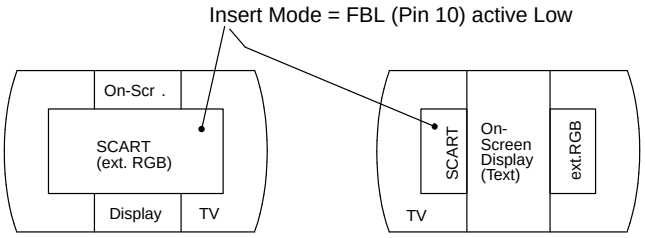


Fig. 3–4: Priorities on the screen, depending on TTM and RGBE

TTM	RGBE	Ext. Fast Blanking Pin 10	Internal TPU Text Blanking	Fast Blanking Output Pin 9	RGB Output Pins 6 to 8	Screen*
0	0	1	0	0	pins 32 to 34	Video
0	1	x	0	1	pins 32 to 34	SCART
0	0	0	0	1	pins 32 to 34	SCART
1	0	1	0	0	Text	Video
1	0	1	1	1	Text	Text
1	0	0	x	1	pins 32 to 34	SCART
1	1	x	1	1	Text	Text
1	1	1	0	0	pins 32 to 34	Video
1	1	0	0	1	pins 32 to 34	Scart

x = don't care
* = see Fig. 3–2 and 3–3

Pin 11 – Undelayed Horizontal Blanking Pulse/ D2SYNC Input (Fig. 3–8)
This pin is connected to the undelayed horizontal blanking output of the deflection processor DPU25xx. For D2MAC teletext mode this pin is also connected to the D2SYNC output of the D2MAC processor DMA2270. (Both pins are tristate outputs).

Pin 12 – Vertical Blanking Pulse (Fig. 3–8)
This pin is connected to the "combined delayed horizontal and vertical blanking pulse" output of the DPU25xx.

Pin 13 – $\overline{\text{Reset}}$ Input (Fig. 3–8)
Provided a clock is present at pin 36, a low level at pin 9 resets the internal circuitry of the TPU 2735. For normal operation high level is required.

Pins 14 to 16 – IM Bus Connections
By means of these pins, the TPU 2735 is linked with the CCU. Pins 15 (Ident Input) and 16 (Clock Input) are configured as shown in Fig. 3–8. Pin 14 (Data Input/Output) is shown in Fig. 3–9. The data transfer via the IM bus is explained in section 6.

Pin 17 to 19, 21 to 26 – DRAM Address Outputs (Fig. 3–7)

Pin 27 – DRAM Data Input/Output (Fig. 3–10)

Pin 28 – Read/Write Output (Fig. 3–7)
This output supplies the R/$\overline{\text{W}}$ control signal to the external DRAM.

Pin 29 – $\overline{\text{CAS}}$ Output (Fig. 3–7)
This output supplies the Column Address Select (CAS) signal for the external DRAM.

Pin 30 – $\overline{\text{RAS}}$ Output (Fig. 3–7)
This output supplies the Row Address Select (RAS) signal for the external DRAM.

Pin 31 – Deflection Skew Data Input (Fig. 3–11)
This pin can be connected to pin 7 of the DPU 25xx Deflection Processor. When DSEN = 1 (see R-DAC of register chain 2) this input controls the horizontal position of the Teletext RGB signal.

Pins 32 to 34 – RGB Inputs (Fig. 3–6)
These pins can be connected to an external RGB source. The specified level of these signals is 0 V to 0.7 V. For other DC levels, an AC coupling has to be used to pins 32 to 34, and a clamping circuit in the VCU has to adjust the DC level.

Pin 35 – V_{SUP}, 5V Supply Voltage

Pin 36 – ΦM Main Clock Input (Fig. 3–12)
Via this pin the TPU 2735 is supplied with the required main clock signal of 20.25, 17.7, 14.4 MHz produced by the MCU 2600 or MCU 2632 Clock Generator IC.

Pin 38 – D2Data Input (Fig. 3–8)
For D2MAC teletext acquisition this pin is connected to the D2Data Output of the DMA 2270.

3.4. Pin Circuits (pin numbers for 40-pin DIL package)

The following figures schematically show the circuitry at the various pins. The integrated protection structures are not shown. The letter “E” means enhancement, the letter “D” depletion.

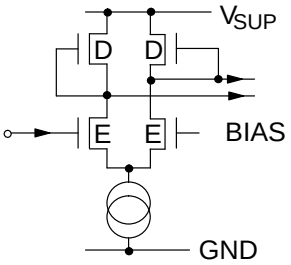


Fig. 3–5: Pins 1 to 4, 39, 40, Inputs

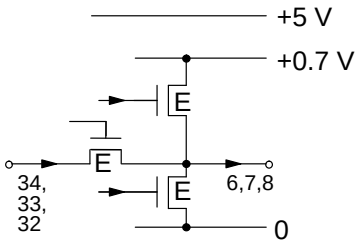


Fig. 3–6: Pins 6 to 8 and 32 to 34, RGB Inputs and Outputs

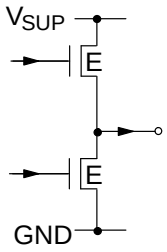


Fig. 3–7: Pins 9, 17, 18, 19, 21 to 26, 28, 29, 30, Outputs

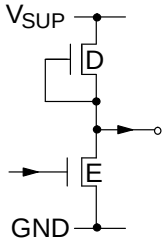


Fig. 3–8: Pins 11 to 13, 15, 16 and 38, Inputs

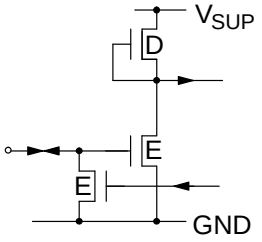


Fig. 3–9: Pin 14, Input/Output

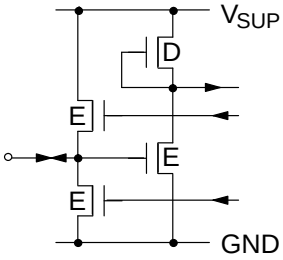


Fig. 3–10: Pin 27, Input/Output

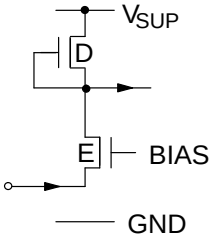


Fig. 3–11: Pin 10, 31, Inputs

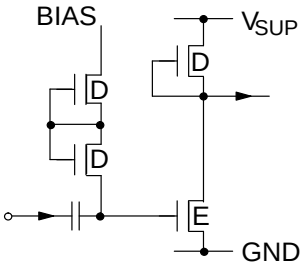


Fig. 3–12: Pin 36, Input

3.5. Electrical Characteristics

All voltages refer to pin 5, all pin numbers refer to DIL Package.

3.5.1. Absolute Maximum Ratings

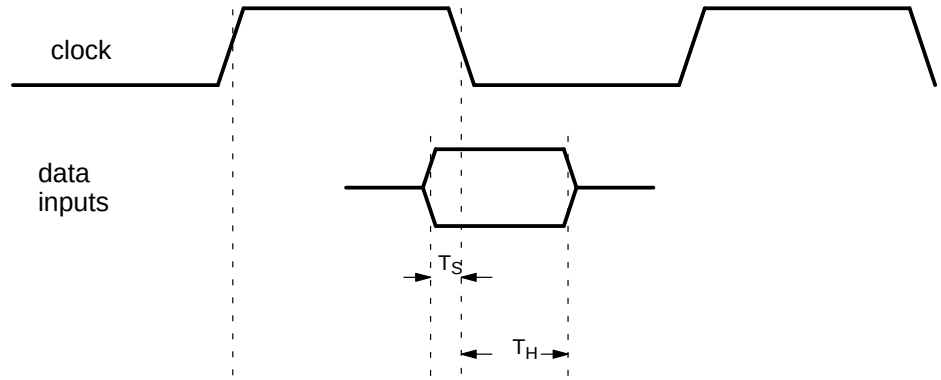
Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	–40	+125	°C
V_{SUP}	Supply Voltage	35	–	6	V
V_I	Input Voltage, all Inputs	–	–0.3V	V_{SUP}	–
V_O	Output Voltage, all Outputs	–	–0.3V	V_{SUP}	–
I_O	Output Voltage, all Outputs	–	The push-pull outputs are short-circuit-proof with respect to ground and supply.		–

3.5.2. Recommended Operating Conditions at T_A = 0 °C to 65 °C, f_c = 14.3 to 20.3 MHz

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{SUP}	Supply Voltage	35	4.75	5.0	5.25	V	
V_{IH}	Input Voltage High, Video Inputs	39, 40, 1 to 4	$V_{SUP}/2$ +0.3			V	
V_{IL}	Input Voltage Low, Video Inputs				$V_{SUP}/2$ –0.3	V	
V_{IH}	Input Voltage High, Fast Blank Input	10	0.9			V	
V_{IL}	Input Voltage Low, Fast Blank Input	10			0.5	V	
V_{IH}	Input Voltage High	11, 12, 14, 15, 16	2.4			V	
V_{IL}	Input Voltage Low	11, 12, 14, 15, 16			0.8	V	
V_{IH}	Input Voltage High, Reset Input	13	2.4			V	
V_{IL}	Input Voltage Low, Reset Input	13			1.2	V	
V_{IH}	Input Current High, Skew Data Input	31			–20	µA	
V_{IL}	Input Voltage Low, Skew Data Input	31			1.2	V	

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_I	Input Voltage, Analog RGB Inputs	32, 33, 34		0.7	1	V_{PP}	
V_{PP}	Input Voltage Swing, Clock Input	36	0.8		2.4	V_{PP}	
V_{DC}	Input Voltage DC Level, Clock Input	36	1.5		3.5	V	
V_{IH}	Input Voltage High, D2DATA Input	38	2.4			V	
V_{IL}	Input Voltage Low, D2DATA Input	38			0.8	V	
f_c	Clock Frequency, PAL	36		17.7		MHz	
f_c	Clock Frequency, NTSC	36		14.4		MHz	
f_c	Clock Frequency, D2MAC	36		20.25		MHz	
C_L	Load Capacitance, DRAM Interface	17, 18, 19 21 to 30			30	pF	
T_S	Input Setup Time, Video Inputs, PAL/NTSC	39, 40, 1 to 4	9			ns	ref. to neg. clock edge
T_H	Input Hold Time, Video Inputs PAL/NTSC		8			ns	ref. to neg. clock edge
T_S	Input Setup Time, H Input PAL/NTSC	11	0			ns	ref. to neg. clock edge
T_H	Input Hold Time, H Input PAL/NTSC	11	20			ns	ref. to neg. clock edge
T_S	Input Setup Time, H Input D2MAC	11	–10			ns	ref. to pos. clock edge
T_H	Input Hold Time, H input D2MAC	11	25			ns	ref. to pos. clock edge
T_V	Pulse Width, V Input	12			58	H (64 µs)	
T_S	Input Setup Time, D2Data Input	38	5			ns	ref. to pos. clock edge
T_H	Input Hold Time, D2Data Input	38	10			ns	ref. to pos. clock edge



Data inputs timing chart and symbols (ref to neg. clock edge)

3.5.3. Characteristics of the Digital Section, T_A = 0 °C to 65 °C

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{SUP}	Supply Current	35		200	240		at 0 °C
V_{OH}	Output Voltage, High Fast Blank Output	9	3.5			V	I_O = –0.1 mA
V_{OL}	Output Voltage, Low Fast Blank Output	9			0.6	V	I_O = 1.6 mA
V_{OL}	Output Voltage, Low IM Bus Data	14			0.4	V	I_O = 3.0 mA
V_{OH}	Output Voltage, High DRAM Interface	17, 18, 19, 21 to 30	3.5			V	I_O = –0.1 mA
V_{OL}	Output Voltage, Low DRAM Interface	17, 18, 19, 21 to 30			0.6	V	I_O = 1.6 mA
C_I	Input Capacitance	39, 40, 1 to 4, 11, 12, 13, 14, 15, 16, 31, 36		5		pF	

3.5.4. Characteristics, RGB Interface

RGB inputs terminated with 75 Ω, RGB outputs terminated with 1 MΩ || 20 pF

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
Internal RGB Outputs							
V_{OL}	RGB Output Voltage low	6, 7, 8		20	50	mV	
V_{OH}	RGB Output Voltage high	6, 7, 8		0.14		V_{SUP}	
V_{OH}	RGB Output Voltage high	6, 7, 8	630	700	770	mV	V_{SUP} = 5V

Characteristics, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
ΔV_{OH}	Differential RGB Output Voltage, High	6, 7, 8		20	50	mV	V_{SUP} = 5V
ΔV_{OL}	Differential RGB Output Voltage, Low	6, 7, 8		10		mV	V_{SUP}= 5V
V_N	Noise at RGB Outputs	6, 7, 8		10		mV RMS	Teletext Mode, B_w = 6 MHz
External RGB Interface							
C_I	Input Capacitance RGB Inputs	34, 33, 32			10	pF	
R_{ON}	Resistance from RGB Inputs to RGB Outputs	6, 7, 8 to 34, 33, 32		200	300	Ω	ext. inputs on
ΔR_{ON}	Differential Resistance	6, 7, 8 to 34, 33, 32			10	Ω	ext. inputs on
R_{OFF}	Resistance from RGB Inputs to RGB Outputs	6, 7, 8 to 34, 33, 32	1			MΩ	ext. inputs off
B_w	Bandwidth ext. RGB	6, 7, 8 to 34, 33, 32	6			MHz	ext. inputs on
α	Cross-Talk RGB Inputs to RGB Intern	6, 7, 8 to 34, 33, 32		50		dB	measured at RGB Outputs, ext. inputs off B_w = 6 MHz
α	Cross-Talk RGB Inputs to RGB Inputs	6, 7, 8 to 34, 33, 32		35		dB	measured at RGB Outputs, ext. inputs on B_w = 6 MHz
V_N	Noise at RGB Outputs	6, 7, 8		5		mV RMS	ext. inputs on B_w = 6 MHz

3.5.5. Characteristics of the External RAM

The TPU 2735 is designed to control one dynamic 64 kbit or 256 kbit RAM. The essential RAM characteristics are:

– page mode capability

– access time from $\overline{CAS}$ 100ns

– 256 cycle 4 ms refresh (A0 to A7)

– max. $\overline{RAS}$ pulsewidth 10 µs

– data in setup time 0ns

– address setup time 0ns

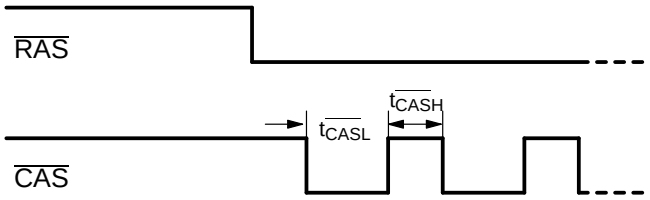


Fig. 3–13: $\overline{RAS}$ and $\overline{CAS}$ timing

	PAL	NTSC	D2MAC
$t_{\overline{CASH}}$	85 ns	104 ns	85 ns
$t_{\overline{CASL}}$	113 ns	104 ns	113 ns

4. Various Operation Modes of the TPU 2735

4.1. The Menu Mode

In the menu mode, on the screen of the TV set is displayed a list of contents of the RAM. This list is achieved by displaying row 0 of all sectors at the same time (Fig. 4–1). Each row 0 is supplemented by the sector number and the requested page number. These two informations are placed at the beginning of each row 0 in the same way as the status indicator. The menu is displayed immediately if MEN (R-DC1) is set to 1. The lower part of the menu cannot be displayed in double-height mode.

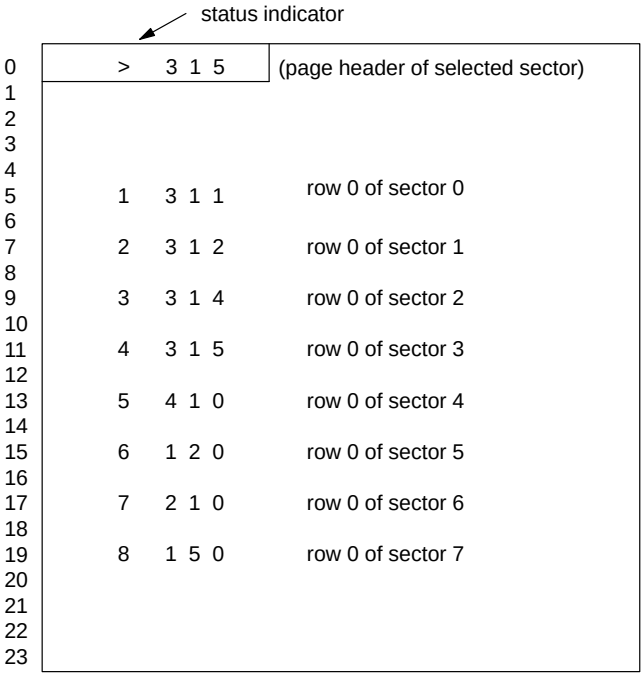


Fig. 4–1: Display of the menu on the screen (example)

4.2. Teletext Display without Interlaced Lines

In this operation mode, the flicker of the TV screen is reduced. For this, the TPU 2735 can distinguish between field 1 and field 2 of a TV frame. If the TPU 2735 is supplied by sync signals without interlace, the character rounding of normal height characters is switched off automatically thus enabling a balanced display of a Teletext page displayed without interlaced lines. The DPU 25.. Deflection Processor Unit can provide appropriate sync signals on request of the CCU.

When a subtitle or a newsflash page is displayed with both TV picture and Teletext characters on the screen, the TPU 2735 sets a flag (TVS = 1 in R-DC3) to indicate that a display with interlaced lines is referable.

4.3. The Effect of Errors in the Transmission of Teletext Data

4.3.1. Errors in the Hamming-Code Protected Data

Single errors are corrected and have no further effect. Rows with multiple errors are not loaded into the DRAM. The error flag of this page number is set and the TPU tries to read this page when it occurs again without clearing the previously acquired data.

4.3.2. Errors in Data with Parity Check

Data with parity errors is not written to the RAM. A parity error sets the error flag of the received page number. The TPU tries to read this page again without clearing the previously acquired data.

4.4. Multipage Conflict Situation

A conflict situation arises if the TPU 2735 receives a new page while the reception of another requested page has not been finished. This situation comes up if requested pages of different magazine numbers are transmitted with interleaved rows or if the last page of a block of pages from the same magazine is requested.

In a conflict situation only the first page is stored immediately. The others have to wait until they are transmitted again. A page which has a conflict with another page loses its priority over the following page when it is stored and regains priority when all pages involved in a conflict have been stored. The selected page does not loose its priority to guarantee the updating of the display.

5. RAM Organization

The external RAM is a 64 kbit or 256 kbit dynamic RAM. A RAM sector is defined as 8 kbit and is capable to store the information of one teletext page.

A 64 kbit RAM holds 8 sectors, a 256 kbit RAM is organized as 4 blocks of 8 sectors.

A RAM sector is organized in 25 rows of 40 bytes (row 0 to row 24) and one row of 24 bytes (row 25). The first 8 bytes of row 0 and the first 11 bytes of row 25 of each sector contain control and status information for the stored teletext page.

Row 24 of sector 0 in block 0 is used as a register for control information from the control microprocessor. When the TPU2735 is used in FLOF mode sector 0 of each block is used to store row 27 teletext information. In the extended character set (ECS) mode the TPU2735 stores row 26 information in the sector preceding the current acquisition sector. RAM organization is summarized in the following table:

Table 5–1: Memory Organization of Sector N Block M

Row Number		
row 0	row 26 des.code 0 of sector N+1	in ECS mode, N even only
row 1	row 26 des.code 1 of sector N+1	”
.	.	
.	.	
row 14	row 26 des.code 14 of sector N+1	”
row 15	row 8/30*	in sector 0, block 0 only
row 16	rolling header	FLOF, ECS mode, sector 0, block 0 only
row 17	row 27* of ttx page in sector 1	in sector 0, block 0 ... 3
row 18	row 27* of ttx page in sector 2	”
.	.	
.	.	
row 23	row 27* of ttx page in sector 7	”
row 24	register chain 2	in sector 0, block 0 only
row 24	rolling header	in sector 1, block 0 if FLOF, ECS are not selected

*) only designation code 000X is stored

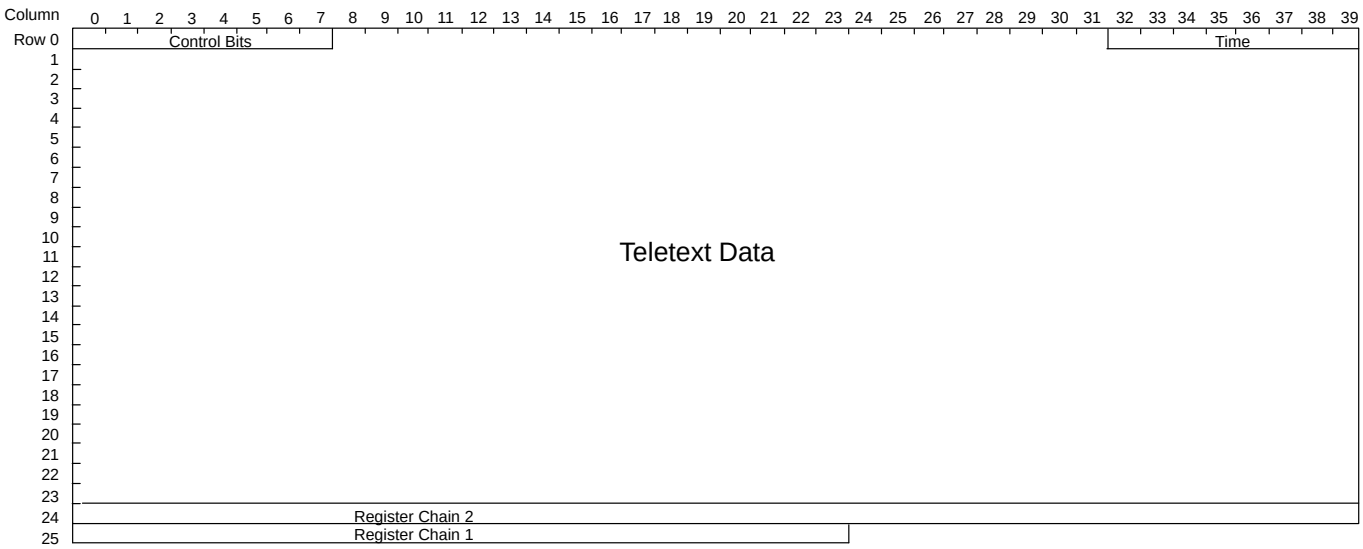


Fig. 5–1: Organization for 64 Kbit RAM, divided into 8 sectors, sector 0 shown

6. Controlling the TPU 2735 with the CCU 2030, CCU 2050 or CCU 2070

TPU and CCU communicate via the IM bus. The CCU can read from and write to all RAM locations of the TPU system and can test the status (ready/busy) of the control interface of the TPU. The CCU can control the TPU by addressing the control registers in the RAM.

The TPU 2735 distinguishes the following types of commands:

Command	IM Bus Address
read a 16-bit write address	7 A (Hex)
read a 16-bit read address	7 B (Hex)
8-bit data transfer (read or write)	7 C (Hex)
status test	7 D (Hex)
hardware test/configuration	7 E (Hex)

Each type of command has its own IM bus address. The TPU has accomplished a CCU command when the busy flags are 0.

Every data transfer starts with a TPU status check, i.e. a read status command with status equal to zero. Next the read or write address is transferred. After the address command another status check is required. The subsequent data is written to or read from the RAM according to the preceding address command. The RAM address is incremented after each data transfer.

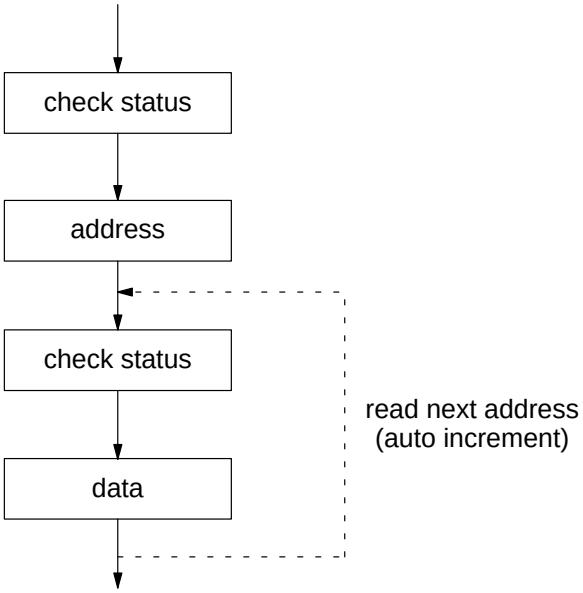


Fig. 6–1: Command sequence for reading data from TPU to CCU with optional auto increment

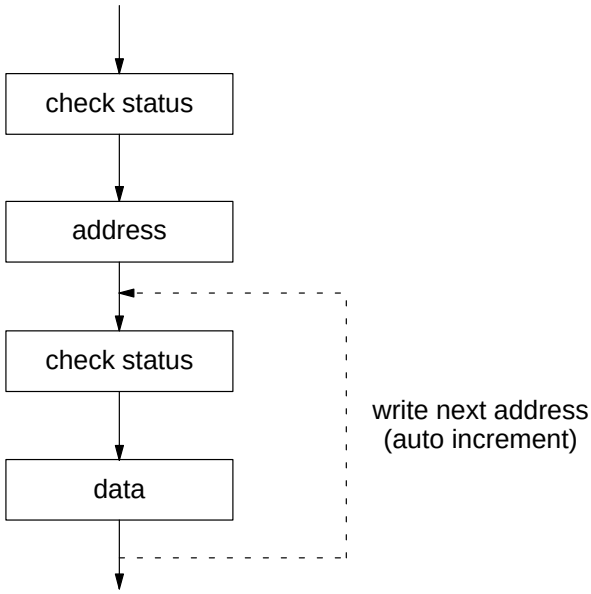


Fig. 6–2: Command sequence for writing data from TPU to CCU with optional auto increment

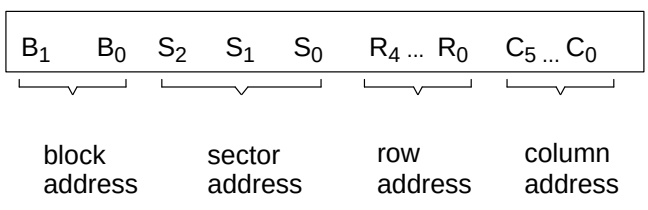
The maximum busy time is 2.5 ms. The test of the interface status can be followed immediately by another command if the busy flag was low or by a second test if the busy flag was high.

6.1. The Address Commands

The 16-bit address consists of four parts:

– block address (0 to 3)	2 bits
– sector address (0 to 7)	3 bits
– row address (0 to 25)	5 bits
– column address (0 to 39)	6 bits

Each sector defines the memory locations for a Teletext page and consists of 25 rows. The rows 0 to 24 can be used as display memory, row 24 and row 25 can be used as control registers. The row and column addresses correspond to the position of the character display on the screen. The data format of the address (C_0 being transmitted first) is:



6.2. The Data Transfer Command

A data command transfers 8 bits of data from the CCU to the TPU or vice versa. The transfer direction depends on the type of the last address command before the data transfer command. A data transfer command following a read address command makes the TPU answer with 8 bits of data. The LSB is transmitted first.

D7	D6	D5	D4	D3	D2	D1	D0

MSB LSB

The RAM address of subsequent data transfer commands is automatically incremented by 1. However, the sector address is not incremented on row address overflow.

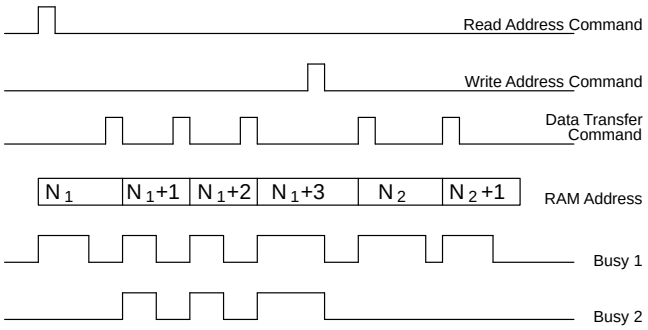


Fig. 6–3: Example of a Read/Write command sequence

6.3. The Status Test Command

The TPU answers to this command with an 8-bit status word:

0	0	0	0	0	0	BUI 2	BUI 1

MSB LSB

The busy flags indicate the status of the interface as follows:

BUI 1	BUI 2	Interface Status
0	0	ready for commands
1	0	not ready for commands
1	1	ready only for address commands

6.4. The IM Bus Hardware Test/Configuration Register

This register allows to control the polarity and the state of the fast blank input signal. The register is write only and is cleared with hardware reset. All unused bits must be set to zero.

D7	D6	D5	D4	D3	D2	D1	D0
0	FBP	FBO	0	0	0	0	0

FBP: Fast Blank Polarity:
0 active low (compatible with TPU 2732)
1 active high

FBO: Fast Blank Overwrite:
0 no action
1 set Fast Blank to 1 (internally) – in this state FBP allows to switch the FB signal under program control.

7. The Control Registers of Register Chain 2

The registers which are used by the CCU to control the TPU have the addresses 0/24/0 to 0/24/30 and are designated as register chain 2. The following pages define the function of the individual registers. An asterisk* marks those bits which can be modified by the TPU. In a write access, each undefined control bit must be set to zero to ensure future compatibility.

Register Chain 2

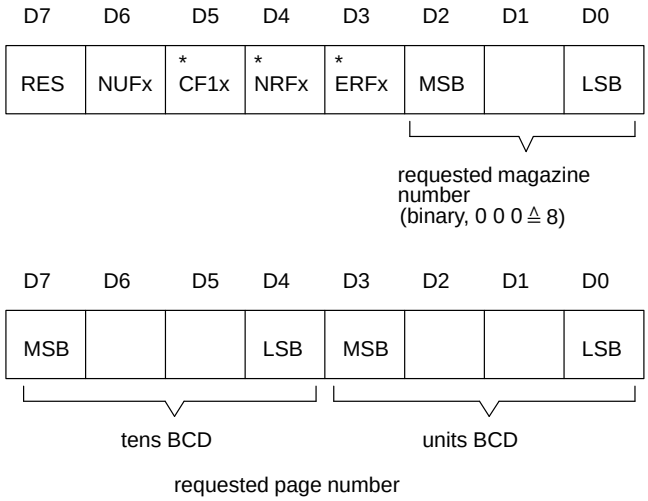
address	bytes	name	
0/24/0	2	R–PR0	page request
2	2	R–PR1	
4	2	R–PR2	
6	2	R–PR3	
8	2	R–PR4	
10	2	R–PR5	
12	2	R–PR6	
14	2	R–PR7	
0/24/16	2	R–PS	page selection
18	2	R–SC	subcode
20	1	R–DS	display selection
21	1	R–DAC	data acquistion control
22	2	R–SI	status indicator
0/24/24	1	R–DC1	display control
25	1	R–DC2	
26	1	R–DC3	
27	1	R–DC4	
28	1	R–DC5	
29	1	R–DC6	
0/24/30	1	R–MC	memory control

7.1. The Page Request Registers, R-PRx

Each sector of the acquisition block has its own page request register. Their structure can be seen below. They have to be loaded with the page numbers of the pages which shall be stored in the according sector when the TPU receives this page. If more than one register contains the same page number the register with the lowest sector number has the highest priority.

R-PRx Page Request Registers

address 0/24/2x, 2-byte register



x is the sector number where the page is to be stored.

RES: Bit is reserved, set to zero

NUFx: no updating flag
NUFx = 1 prevents the data acquisition unit of the TPU from writing to the RAM sector x. NUFx can be used in the HALT mode to protect a received page against modifications.

ERFx: error flag
The TPU sets ERFx = 1 if a bit error was detected during the reception of a Teletext page. The TPU will load a page with ERFx = 1 once again as soon as it is transmitted again. ERFx has to be reset when the page request register is loaded with a new page number.

NRFx: new request flag
NRFx has to be set to 1 if the CCU loads a new request into R-PRx. The TPU resets NRFx when the requested page has been received. NRFx influences the page header (rolling header and color) when sector x or the menu is displayed (see section 7.5. “Data Acquisition Register R-DAC 1”).

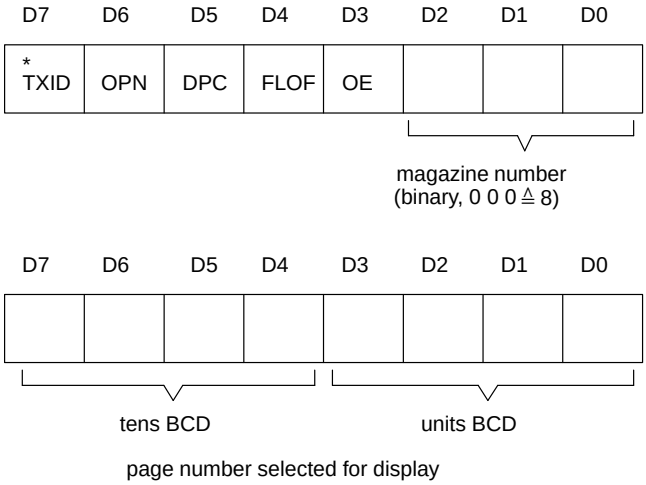
CF1x: conflict flag 1
CF1x: = 1 indicates a conflict situation where the requested page of sector x is involved. CF1x = 1 leads to a longer access time (see section 4.4. “Multipage Conflict Situation”). CF1x has to be reset when the page request register is loaded with a new page number.

7.2. The Page Selection Register, R-PS

The CCU can write a number of a page into R-PS when this page has been requested before and shall now be displayed. R-PS has only effect if SIC = 1. (see section 9., “Two Ways to Select a Page for Display”).

R-PS Page Selection Register

address 0/24/16, 2-byte register



TXID: Teletext transmission indicator
TXID = 1 if a Teletext line was detected in the vertical flyback interval.

OPN: open
OPN = 1 makes the TPU receive a requested page whenever it is transmitted. OPN = 0 makes the TPU receive a requested page only if NRF = 1, or errors have been detected (ERF = 1), or C_4 = 1 or C_8 = 1 (clear page or update page).

DPC: disable parity checking
DPC = 1 disables parity checking for the data bytes of all received TTX rows.

FLOF: enable FLOF mode
FLOF = 1 enables reception of rows 24, 27 and 8/30.

OE: odd/even data sampling
OE = 0 samples the odd data bits off the D2DATA signal, OE=1 samples the even data bits. This bit is used to select the TTX Data channel for DMAC VBI TTX Data.

7.3. The Subcode Register, R-SC

The subcode register can be used to make the TPU 2735 respond only to transmitted pages with the subcode specified in R-SC. The subcode is normally interpreted as a time code.

R-SC Subcode Register

address 0/24/18, 2-byte register

D7	D6	D5	D4	D3	D2	D1	D0
SSC0	SCT2	SCT1	SCT0	SCU3	SCU2	SCU1	SCU0

SCT: subcode tens (minutes tens)

SCU: subcode units (minutes units)

D7	D6	D5	D4	D3	D2	D1	D0
SSC2	SSC1	SCM1	SCM0	SCH3	SCH2	SCH1	SCH0

SC: subcode control

SCM: subcode thousands (hours tens)

SCH: subcode hundreds (hours units)

The subcode-control flags SCC 0 to SCC 2 determine for which sector the subcode is valid.

Subcode Control Flags

SSC2	SSC1	SSC0	Function
0	0	0	subcode ignored
0	0	1	subcode valid only for sector 1
0	1	0	subcode valid only for sector 2
0	1	1	subcode valid only for sector 3
1	0	0	subcode valid only for sector 4
1	0	1	subcode valid only for sector 5
1	1	0	subcode valid only for sector 6
1	1	1	subcode valid for all sectors

7.4. The Display Selection Register, R-DS

R-DS controls the selection of a RAM sector for display. The sector number of the displayed sector is either determined by the TPU using R-PS or by the CCU.

R-DS Display Selection Register

address 0/24/20, 1-byte register

D7	D6	D5	D4	D3	D2	D1	D0
* ERS	SIC	* NRS	* RPS	* RPSV	* MSB		* LSB

Sector number of displayed sector

ERS: error flag of the selected page
ERS = 1 means: the selected page has been received with errors. ERS is for internal use of the TPU 2735.

SIC: start internal comparison
The CCU has to set SIC = 1 when a new page number is loaded into R-PS. SIC is reset by the TPU when RPS is valid.

NRS: new request flag of the selected page
NRS = 1 means: the selected page has not yet been received. NRS is only for internal use of the TPU.

RPS: requested page is selected
The TPU sets RPS to 1 if a page number of one of the eight request registers is identical to the selected page number of R-PS (see section 9., “Two Ways to Select a Page for Display”). When RPS is set to one and Display (R-DC3) and Acquisition Block (R-MC) are different, the current magazine (in parallel magazine mode) is taken from R-PS.

RPSV: RPS flag valid
Only if RPSV = 1 the value of RPS is valid. When R-PS has been loaded with a new page number the TPU accomplishes a comparison within 20 ms. The result is written into R-DS. When a comparison is accomplished RPSV is set to 1. The CCU can reset RPSV after loading R-PS and then check if RPSV is set to 1 again.

7.5. The Data Acquisition Control Register, R-DAC

This register controls the slicer, the ghost compensation, the acquisition of the page header and the skew data.

R-DAC Data Acquisition Control Register

address 0/24/21, 1-byte register

D7	D6	D5	D4	D3	D2	D1	D0
TBD	DSEN	RHA	NRT	NRH	NDA	NGC	* $\overline{\text{RGC}}$

TBD: vertical blanking delay
Set to 1 if the delay between horizontal and vertical blanking pulse is more than 32 ms in field 1 of a TV frame. TBD is used to adapt the TPU 2735 to different sources of the blanking pulses required for synchronization of the TPU (see Fig. 7–1). TBD must be set to 0 in D2MAC mode.

DSEN: deflection skew data enable
DSEN = 0: the horizontal display start is controlled by pin 11. DSEN = 1: the horizontal display start is controlled by pin 31 (skew data).

The TPU 2735 is able to adjust the horizontal phase of the Teletext RGB signal under control of deflection skew data (DSD) at pin 31. The phase can be adjusted by steps of 1/16 of the main clock period, i. e. 3.5 ns for PAL and 4.4 ns for NTSC. DSD provides a Teletext picture without visible jitter even when there is no color burst in the video signal and the DPU is not in the locked mode. For more details refer to the description of the DPU 25.. Deflection Processor.

RHA: rolling header always
NRT: no rolling time
NRH: no rolling header

Refer to Table Rolling Header Options

NDA: no data acquisition;
Default value is NDA = 0. If NDA = 1, the Teletext data acquisition is switched off.

NGC: no ghost compensation
NGC = 1 switches off the ghost compensation

$\overline{\text{RGC}}$: reset ghost compensation;
Zero written to this bit resets the ghost compensation filter; returns automatically to 1 when the reset command is executed.

Rolling Header Options

RHA	NRT	NRH	Option
0	0	0	rolling header while searching the selected page, rolling time always
0	0	1	only time is rolling
0	1	0	only central header section is rolling while searching (recommended for NTSC mode)
0	1	1	header does not change
1	0	0	rolling header always
1	X	1	ignore parallel magazine control bit (C11 in 8.4.) for rolling header acquisition

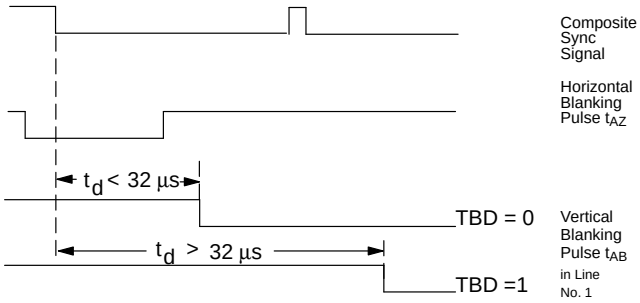


Fig. 7–1: Timing diagram for the horizontal and vertical blanking pulses t_{AZ} and t_{AB} for two cases

7.6. The Status Indicator Register, R-SI

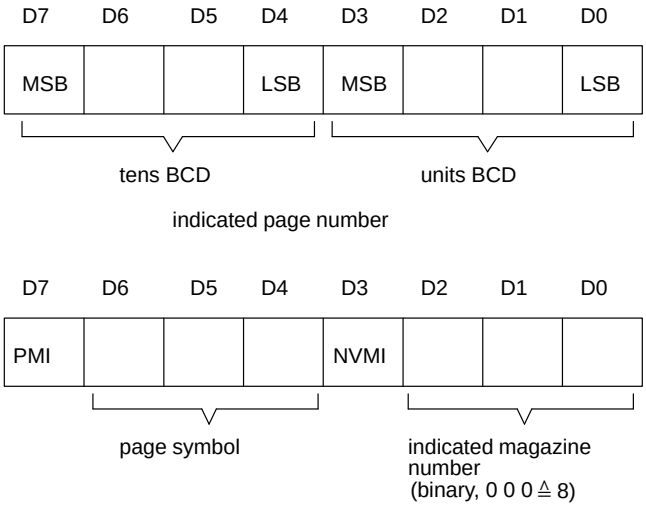
The contents of R-SI determine the eight characters of the status indicator in left corner of row 0. The status indicator displays three numerals which represent a page number. PMI and NVMI determine the mode of their display:

Page Symbol List

PMI	NVMI	Display Mode
0	0	white, steady
1	0	light-blue, steady
0	1	yellow, steady
1	1	red, flashing

R-SI Status Indicator Register

address 0/24/22, 2-byte register



PMI: programming mode indicator;
PMI = 1 changes the color of the indicated page number to blue. PMI can be used to indicate that a new page number is not complete or has not yet been accepted.

NVMI: non-volatile memory indicator;
NVMI = 1 changes the color of the indicator to yellow

Page Symbol List

D6	D5	D4	Page Symbols
0	0	0	“space”
0	0	1	R
0	1	0	S
0	1	1	T
1	0	0	=
1	0	1	>
1	1	0	?
1	1	1	P

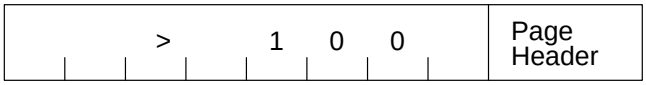


Fig. 7–2: Display of the status indicator in the left corner of row 0

7.7. The Display Control Registers, R-DC1 to R-DC6

The flags of R-DC1 determine the way the control information (page header, status indicator, time, menu) is displayed. The flags of R-DC2 and R-DC4 determine the way the Teletext page is displayed. The flags of R-DC5 determine which character set is used.

R-DC1 Display Control Register 1

address 0/24/24, 1-byte register

D7	D6	D5	D4	D3	D2	D1	D0
TOE	MEN	* TOF	* BXT	* PAH	* IND	* TIM	HLT

TOE: timeout enable
TOE = 1 enables the automatic reset of BXT, PAH, IND and TIM after 5 s for PAL or 4 s for NTSC.

MEN: display menu
MEN = 0 means normal display, and MEN = 1 means that the menu is displayed.

TOF: text off
TV picture is displayed (BL = 0)

BXT: display boxes (with time-out option) in a TV picture

PAH: display page header
If PAH is set to 1 by the CCU, a 5 second timer is started. During these 5 sec the row 0 of the selected sector is displayed. Thereafter, PAH is reset to 0. Time-out can be switched off by TOE = 0. If PAH, TOF and TTM are 1, the row 0 of the selected sector is boxed in the normal TV picture.

IND: display indicator (with time-out option)
similar to PAH, but the first eight characters of row 0 of the selected sector are displayed.

TIM: display time (with time-out option)
similar to PAH, but the last eight characters of row 0 of the selected sector are displayed in white.

HLT: indicate halt mode
If HLT = 1 the last eight characters of the displayed page header are replaced by a symbol which indicates that the page is not updated. TIM has priority over HLT.

PAH and BXT are influenced by the data acquisition control according to the following table:

Display Behaviour of Updated Pages

Requested Page of Sector N is received	Sector N is selected for display	Subtitle Page	Clear Page	Update Page	NRFx	Set PAH and BXT
0	x	x	x	x	x	0
1	0	x	x	x	x	0
1	1	x	x	x	1	1
1	1	0	1	x	x	1
1	1	0	x	1	x	1
1	1	1	x	x	0	0

x = don't care

R-DC2 Display Control Register 2

address 0/24/25, 1-byte register

D7	D6	D5	D4	D3	D2	D1	D0
TTM	DW	DR	MIX	* UPI	REV	DLB	DHT

TTM: Teletext mode
If TTM = 0, no Teletext data is displayed. The R, G, B inputs are connected to the R, G, B outputs. The state of the Fast Blanking output depends on the Fast Blanking input and the RGBE control bit (ref. section 7.8.).
If TTM = 1, Teletext data is displayed according to the status of the control registers.

DW,DR: double width
DW = 0 and DHT = 0 means normal display. DW = 1 and DR = 0 displays the left half of the Teletext page in double width characters. If DR = 1 and DW = 1, the right half of the screen is shown in double width; any attribute characters that are in the left half of the page will have no effect. DW = 1 and DHT = 1 means double size display. In this case DR and DLB select 1 of 4 possible display quadrants.

MIX: mixed display
If MIX = 1, characters may be displayed with TV background. The margin background is TV picture (see Table below).

UPI: update indicator
Default value is UPI = 0. UPI is set by the TPU whenever the page which is selected for display is updated. UPI is not reset by the TPU. The CCU may monitor UPI and reset UPI after an update has been detected.

REV: reveal
If REV = 1, the conceal control character 1/8 has no effect.

DLB: display large bottom
DLB has no effect if DHT = 0, see DHT.

DHT: double height
DHT = 0 and DW = 0 means normal display. DHT = 1 and DLB = 0 means large top. DHT = 1 and DLB = 1 means large bottom. In connection with control character 0/13 some characters may not be fourfold high – 0/13 has no effect.

R-DC3 Display Control Register 3

address 0/24/26, 1-byte register

D7	D6	D5	D4	D3	D2	D1	D0
* TVS	DB1	DB0	X	X	X	X	X

TVS: TV synchronization required (mixed mode)
The TPU sets TVS = 1 if the displayed Teletext page consists of mixed data TV/Teletext, e. g.
MIX = 1, C6 = 1 (subtitle), C5 = 1 (newsflash).

DB: Display Block
Address (0 to 3) of the current block (8 pages) to display.

X: for internal use only
Should not be modified via IM bus.

MIX	C_5 or C_6	BXT	TOF	PAH	IND	TIM	background				
							normal	box	indicator	header	time
0	0	x	0	x	x	x	TT	TT	TT	TT	TT
0	1	x		0	0	0	–	TT	–	–	–
0	0	0	1	0	0	0	–	–	–	–	–
0	0	1	1	0	0	0	–	TT	–	–	–
1	0	0	x	0	0	0	TV	TV	TV	TV	TV
1	1	x	0	0	0	0	TV	TT	TV	TV	TV
1	0	1	0	0	0	0	TV	TV	TV	TV	TV
1	1	0	1	0	0	0	TV	TV	TV	TV	TV
1	1	0	1	1	0	0	TV	TT	TT	TT	TT
1	1	0	1	0	1	0	TV	TT	TT	TV	TV
1	1	0	1	0	0	1	TV	TT	TV	TV	TT
1	1	1	1	0	0	0	TV	TT	TV	TV	TV
1	1	1	1	1	0	0	TV	TT	TT	TT	TT
1	1	1	1	0	1	0	TV	TT	TT	TV	TV
1	1	1	1	0	0	1	TV	TT	TV	TV	TT

TT = Teletext – = not displayed

R-DC4 Display Control Register 4

address 0/24/27, 1-byte register

D7	D6	D5	D4	D3	D2	D1	D0
INO	IBL	NTSC	D2 MAC	NTS	NHS	NFL	NCR

INO: inverted outputs (R, G, B and Fast Blanking)

IBL: inverse blanking
If IBL = 1, the Fast Blanking output is inverted.

NTSC: NTSC mode

D2MAC: D2MAC mode

NTS: no text suppression
NTS = 1 disables control bit C10.

NHS: no header suppression
NHS = 1 disables control bit C7.

NFL: no flash
NFL = 1 disables control character 0/8.

NCR: no character rounding
NCR = 0 means character rounding on, and NCR = 1 is character rounding off. If the TPU 2735 is supplied by a sync signal with non-interlaced lines, character rounding is turned off automatically for normal height characters. Double height characters are displayed with character rounding unless NCR = 1.

R-DC5 Display Control Register 5

address 0/24/28, 1-byte register

D7	D6	D5	D4	D3	D2	D1	D0
IISP	UKS	ECS	UPEN	ELS	LS 2	LS 1	LS 0

IISP: indicator insertion suppression
IISP = 1 suppresses the display of the status indicator and displays the memory locations x/0/0 to x/0/7 instead.

UKS: swap UK/US English character set
Default value is UKS = 0, (ref. to Table below).
UKS = 0:
The UK character set is displayed in PAL mode.
The US character set is displayed in NTSC mode.
UKS =1:
The US character set is displayed in PAL mode.
The UK character set is displayed in NTSC mode.

ECS: Extended character set mode
Reception of rows x/26 and additional (Spanish) character set are enabled. The memory organization is changed in order to store the row x/26 for each sector (please ref. to sect. 5 pg. 16). Two additional control characters ‘0x0: alpha black’ and ‘0x10: mosaic black’ are processed. Additional characters for the Spanish Teletext system are provided, these characters overlay the control characters with bit 7 (MSB) set.

UPEN: update enable
Default value is UPEN = 0.
UPEN = 1prevents BTX and PAH from being set when the displayed page is updated. Only the update indicator UPI will be set and the software may decide about the way an update is shown on the display.

ELS: external language selection
ELS = 1: The selection of the different character sets is under software control, using the display control register R-DC5 (LS2, LS1 and LS0).
ELS = 0: The selection of the different character sets is under transmitter control, using the control bits C12, C13 and C14 of the page header.

LSx: Language select code

C_{12} LS2	C_{13} LS1	C_{14} LS0	NTSC Mode	UKS	Character Set selected
0	0	0	0	0	English, UK Version
0	0	0	1	0	English, US Version
0	0	0	0	1	English, US Version
0	0	0	1	1	English, UK Version
0	0	1	x	x	German
0	1	0	x	x	Scandinavian
0	1	1	x	x	Italian
1	0	0	x	x	French/Belgian
1	0	1	x	x	Spanish
1	1	0	x	x	English, US Version
1	1	1	x	x	reserved

x = don’t care

R-DC6 Display Control Register 6

address 0/24/29, 1-byte register

D7	D6	D5	D4	D3	D2	D1	D0
DS	DLS	HDA	HDA	HDA	HDA	HDA	HDA

DS: double-scan mode
DS = 1 doubles the display frequencies. When DS = 1 and DSEN = 0, the RGB horizontal period is 567.5 main clock periods for PAL and 515 main clock periods for NTSC.

DLS: Display lines
DLS = 0 selects 24 display lines. DLS = 1 selects 25 display lines. DLS = 1 is only valid in PAL, D2MAC modes. Row flag RRO is used to control line 25, (see section 8.5.). DLS also effects the number of lines cleared with the CDS (Clear Display Sector) command (see section 7.8.).

HDA: horizontal display adjustment
A 6-bit binary number can be loaded into HDA to shift the Teletext picture from the left towards the right edge of the screen. The additional RGB delay generated by HDA is in steps of 1/4 character.

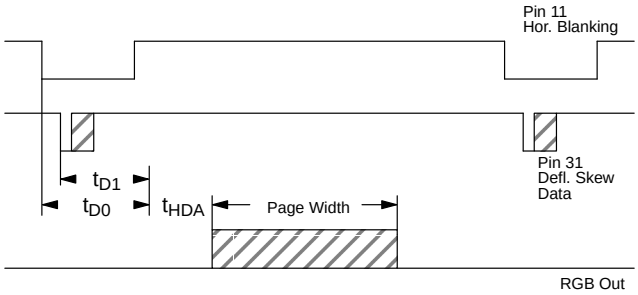


Fig. 7–3: Horizontal display start in normal scan mode
t_{D1} = minimum delay of the horizontal RGB start from DSD at pin 31 (DSEN = 1)
t_{D0} = minimum delay of the horizontal RGB start from horizontal blanking at pin 11 (DSEN = 0)
t_{D1} = 12.2 µs for PAL/D2MAC and 10.8 µs for NTSC
t_{D0} = 15.6 µs for PAL/D2MAC and 14.6 µs for NTSC

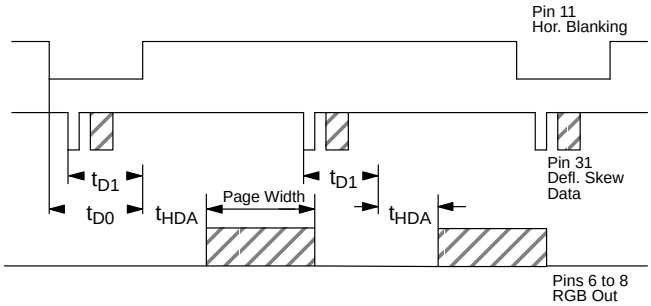


Fig. 7–4: Horizontal display start in double-scan mode
t_{D1} = minimum delay of the horizontal RGB start from DSD at pin 31 (DSEN = 1)
t_{D0} = minimum delay of the horizontal RGB start from horizontal blanking at pin 11 (DSEN = 0)
t_{D1} = 10.4 µs for PAL and 10.8 µs for NTSC
t_{D0} = 6.9 µs for PAL and 6.4 µs for NTSC

Display Timing

Main Clock Period T		Double Scan	Double Width	Pixel Width	Page Width (µs)
56.4/49.4 ns	PAL/D2MAC	0	0	169.2 ns = 3 · T	40.6
56.4/49.4 ns	PAL/D2MAC	1	0	84.6 ns = 1.5 · T	20.3
56.4/49.4 ns	PAL/D2MAC	0	1	338.3 ns = 6 · T	–
56.4/49.4 ns	PAL/D2MAC	1	1	169.2 ns = 3 · T	–
69.8 ns	NTSC	0	0	139.7 ns = 2 · T	33.5
69.8 ns	NTSC	1	0	69.8 ns = 1 · T	16.7
69.8 ns	NTSC	0	1	279.4 ns = 4 · T	–
69.8 ns	NTSC	1	1	139.7 ns = 2 · T	–

In NTSC mode the Teletext page is about 18% smaller than in PAL mode.

7.8. The Memory Control Register, R-MC

R-MC provides an easy way to clear parts of the selected RAM sector.

R-MC Memory Control Register

address 0/24/30, 1-byte register

D7	D6	D5	D4	D3	D2	D1	D0
RGBE	* RGBI	AB1	ABO	SST	* CDS	* CR1	* CR2

RGBE: switch external RGB signal to the RGB outputs (see section 3.3., pin 10).

RGBI: indicator for external blanking in line 6, i.e. constant external blanking

ABx: Address of current acquisition block

SST: is for testing purposes only
SST = stop on same page header. SST = 1 makes the TPU close a page whenever a new page header of the same magazine is received. Default value is SST = 0.

CDS: clear display sector;
CDS = 1 clears the data part of the selected display sector.

Depending on the DLS control bit in R_DC5 of RC2, 24 or 25 lines of the sector will be written. Also the “Display Header Options” (ref. to R_DAC in section 7.5) influence the write operation: if “Rolling Header” or “Rolling Time” is selected, the respective areas in the rolling header and/or rolling time fields are cleared and the contents of the current display page remains unchanged. If CDS is set to 1 the display period of the subsequent field is turned into an erase period: read is turned to write, and data is stuck to blank (0x20). The next field resets CDS to 0.

CR1: clear register chain 1 of the selected display sector

CR2: clear register chain 2

CR1(2) = 1 clears all bits of all registers of register chain 1(2). This is done in the field following the clear command in line 25, 26. CR1(2) is reset by the TPU when the clear command is executed. Power-up reset makes CR2 = 1.

8. The Control Registers of Register Chain 1

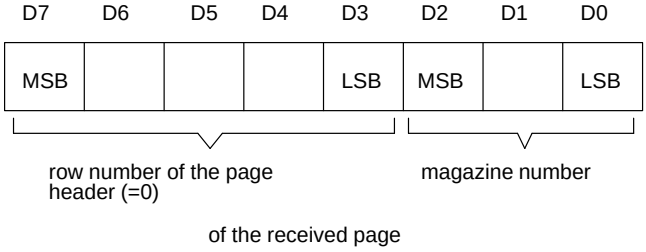
Each RAM sector has its own registers for internal control purposes. These registers are designated as register chain 1 (of sector x) and have the addresses x/25/0 to x/25/10. They are used for control information of the Teletext transmitter and information about the status of the data acquisition. In a normal Teletext mode the CCU does not read or modify these registers. The following pages define the function of the individual registers. In a write access, each undefined control bit must be set to zero to ensure future compatibility.

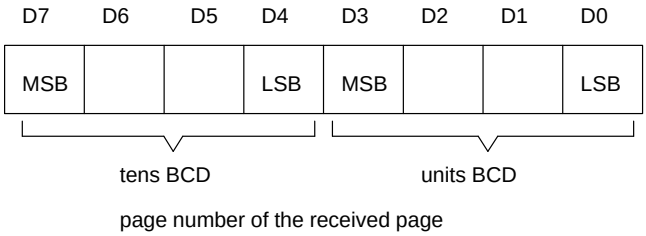
Register Chain 1 of Sector x

address	bytes	name	
x/25/0	2	R–PI	page identification
x/25/2	1	R–CB1	control bits
3	1	R–CB2	
4	1	R–CB3	
x/25/5	6	R–RF	row flags

8.1. The Page Identification Register, R-PI

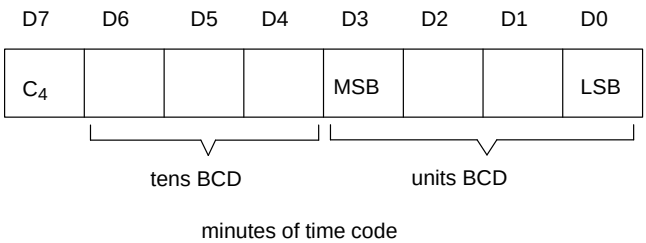
address x/25/0, 2-byte register





8.2. The Control Bit Register 1, R-CB1

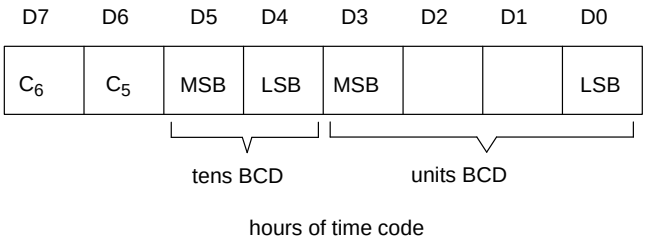
address x/25/2, 1-byte register



C_4 clear page: C_4 0→1 clears row flags and makes BXT=PAH=1

8.3. The Control Bit Register 2, R-CB2

address x/25/3, 1-byte register



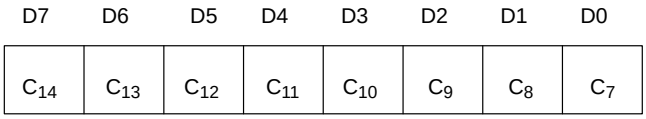
C_5: newsflash

C_6: subtitle

only boxed information is displayed and superimposed on a TV picture.

8.4. The Control Bit Register 3, R-CB3

address x/25/4, 1-byte register



C_{14}: language selection (see R-DC5)

C_{13}: language selection (see R-DC5)

C_{12}: language selection (see R-DC5)

C_{11}: serial magazine mode

C_{10}: inhibit Teletext: inhibits the display of page

C_9: out of sequence: this header is not used for the rolling-header display

C_8: update: C_8 0→1 makes BXT=PAH=1

C_7: suppress header: this header is not displayed
The function of C7 is influenced by the “No Header Suppression” (NHS) control bit in register R_DC4 of register chain 2. Also the “Display Page Header” (PAH) control bit in register R_DC1 of RC2 overwrites C7. Note that PAH is set every time the page is updated, and must be reset to enable the function of C7.

8.5. The Row Flag Register, R-RFx

address x/25/5, 6-byte register

D7	D6	D5	D4	D3	D2	D1	D0
R7	R6	R5	R4	R3	R2	R1	R0
R15	R14	R13	R12	R11	R10	R9	R8
R23	R22	R21	R20	R19	R18	R17	R16
RR7	RR6	RR5	RR4	RR3	RR2	RR1	RR0
RR15	RR14	RR13	RR12	RR11	RR10	RR9	RR8
RR23	RR22	RR21	RR20	RR19	RR18	RR17	RR16

A row flag is set to 1 by the TPU if the corresponding row has been received. When a new page is received, all row flags of the corresponding sector are cleared.
The display unit displays only those rows whose row flags are 1.

The registers x/25/8 to x/25/10 contain the right-hand-side row flags which are used in NTSC mode. They control the display of the last 8 character positions of each row which are transmitted in separate lines.

In PAL/D2MAC mode some of the right-hand side row flags are used when the FLOF or ECS bits are active:

rowflag RR0: controls display of row x/24. This flag is under software control

rowflag RR4: indicates reception of a row x/27 and is set/reset by TPU

rowflag RR8: indicates reception of one or more rows x/26, set/reset by TPU

8.6. The Timing of the Register Chains

The contents of the register chains 1 and 2 is updated in the TPU only once per field. This is important for a command sequence with commands which rely on the execution of preceding commands, e. g. “a clear display” command followed by new display data. In this example a pause of 2 fields is necessary before the new data is written into the RAM: one field for the TPU to recognize the clear command and another field to execute this command.

9. Two Ways to Select a Page for Display

First Way
Load the selected page number into R-PS and set SIC = 1; if the page number has already been requested, R-DS is loaded automatically with the according sector number and RPS is set to 1; if RPS remains 0, the CCU has to load one of the eight R-PR 0 to 7 with this page number.

Second Way
The CCU compares the selected page number with the contents of R-PR 0 to 7; if the page number is not found in R-PR 0 to 7, one register of R-PR 0 to 7 has to be loaded with the selected page number. The CCU loads the number of the selected sectors into R-DS.

The R-PS register and SIC control bit are kept for compatibility with TPU 2732. For new software the second way for page selection is recommended.

10. Reset of the TPU 2735 Teletext Processor

The power-up reset makes TTM = 0 (no Teletext mode) and CR 2 = 1 (clear register chain 2). A software reset is achieved by setting CR 2 = 1.

11. Application Notes

Problem: **Clamping of External RGB Signals**

The external RGB inputs are fed through the TPU to the VCU. Clamping of these signals is done by the VCU during the color key pulse. The RGB switches of the TPU are controlled by the external “Fast Blank” input to the TPU and by internal control bits (TTM, RGBE, please refer to sections 3.3., 6.4.). In some cases the external fast blank signal is switched off during the horizontal blanking interval (e.g. PIP insertion and OSD active). In these cases the external RGB inputs are not switched to the VCU during the blanking interval and the clamping fails. To force clamping of the RGB inputs in all modes the color key should be ‘ored’ to the external fast blank signal.

Problem: **Conflict flag**

The conflict flag in the page request register is set if the TPU273x has opened a page for acquisition and receives a header row for another page that is requested in some other request register. This usually happens when the last page of a magazine is requested. In the case of a conflict the internal logic of the TPU assigns the highest priority to the page selected for display. Setting the ‘no updating’ flag for this page will resolve the conflict. (In order to get an ‘open’ page into NUF mode one should set NUP and NRF.) Also the behavior of the acquisition circuit is influenced by the open (OPN) bit in the page selection register. This bit forces the acquisition circuit to keep pages open and thereby makes conflict situations worse. This bit should be zero for normal Teletext acquisition.

Continuous long updating times for the ‘time’ field are also influenced by the conflict.

The World System Teletext Specification reserves a Row0 of page 0x?FF (hexadecimal) for the function of magazine close row. Transmitting this row would solve all of these problems.

Problem: **Spanish Teletext**

As the decoding of the information transmitted in rows 26 is done by the CCU obviously the control program has to check for the reception of any row26. The actual row26 processing is only required for the page currently displayed. This should be done in the ‘idle loop’ of the control program. There is no other way than polling to see if a row26 was received.
The ‘Spanish Teletext Specification’ requires the extra characters to be transmitted with even parity. Therefore a true ‘Spanish Teletext Page’ cannot be received without errors and will be acquired again and again. (It is not recommended to use the NPC mode.) A way to detect the reception of a ‘new’ (i.e. different) page is to check the subcode information stored in register chain one. Usually a subcode of all zeros or all ones indicates a non-rolling page.

Problem: **Initialization**

Initialization of the TPU should always start with a clear of register chain 2 via the CR2 bit in the R_MC register. If the mode is switched to NTSC/D2MAC, setting the appropriate control bit in register R_DC4 should be the next action. Since internal clocks of the TPU are switched by these bits, the next thing should be a clear of all registers in register chain 2 (except the mode register R_DC4). In case of NTSC mode, it is recommended to set the NTSC bit, wait for two fields, check that the NTSC bit is still set, and then start the clearing of register chain 2. After this procedure the normal initialization of registers should follow.

Samples for TPU2735-E are available and are marked TPU2735-TC18. The logic of these samples is identical to TPU2735-TC15.

Data Sheet Update: **ECS**

In ECS mode the TPU acquires Teletext rows x/26. The memory organization is changed in order to store the row x/26 for each sector (ref. to section 5). Two additional control characters “0x0: alpha black” and “0x10: mosaic black” are processed. Additional characters for the Spanish Teletext system are provided (ref. Fig. 11–1). These characters overlay the control characters with bit 7 (MSB) set.

	0	1
0	ö	À
1	ï	.
2	â	ê
3	ô	ã
4	õ	Ü
5	Í	ä
6	ë	î
7	û	Á
8	Ñ	Õ
9	Ã	Ç
10	↑	È
11	É	→
12	a	o
13	Ó	#
14	Ò	Ï
15	Ú	ò

Fig. 11–1: Extended character set for Spanish Teletext system

TPU2735-E Character Set for Eastern Europe Application

TPU2735 will be available with a character set for Eastern European countries. This version of TPU2735 will be designated TPU2735-E. The only logic changes are for control of character sets via register R-DC5 in register chain 2. An NTSC character set will not be supported by TPU2735-E, the UKS bit in R-DC5 allows to select two different character set assignments.

Character Set Assignments Register R-DC5

LS	UKS=0	UKS=1
0	English	Polish
1	German	German
2	Swedish	Hungarian
3	Italian	Italian
4	French	French
5	Polish	Polish
6	Turkish	Turkish
7	Rumanian	Rumanian

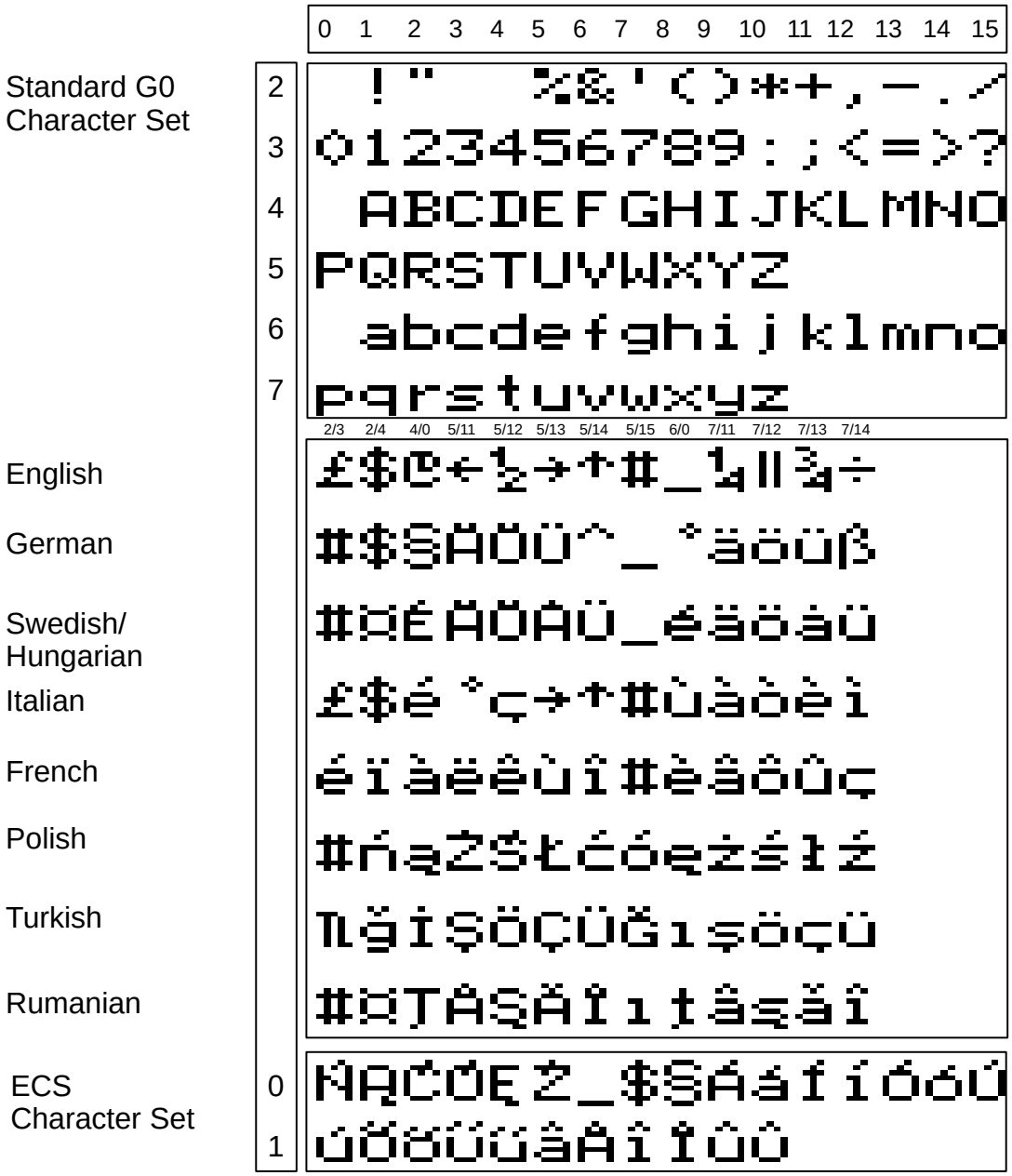


Fig. 11–2: TPU 2735-E character set for Eastern Europe Application

12. Description of the IM Bus

The INTERMETALL Bus (IM Bus for short) was designed to control the DIGIT 2000 ICs by the CCU Central Control Unit. Via this bus the CCU can write data to the ICs or read data from them. This means the CCU acts as a master whereas all controlled ICs are slaves.

The IM Bus consists of three lines for the signals Ident (ID), Clock (CL) and Data (D). The clock frequency range is 50Hz to 170 kHz. Ident and clock are unidirectional from the CCU to the slave ICs, Data is bidirectional. Bidirectionality is achieved by using open-drain outputs with on-resistances of 150 Ω maximum. The 2.5 kΩ pull-up resistor common to all outputs is incorporated in the CCU.

The timing of a complete IM Bus transaction is shown in Fig. 12–1 and Table 12–1. In the non-operative state the signals of all three bus lines are High. To start a transaction the CCU sets the ID signal to Low level, indicating an address transmission, and sets the CL signal to Low level as well to switch the first bit on the Data line. Thereafter eight address bits are transmitted beginning with the LSB. Data takeover in the slave ICs occurs at the positive edge of the clock signal. At the end of the address byte the ID signal goes High, initiating the address comparison in the slave circuits. In the addressed slave the IM bus interface switches over to Data read or write, because these functions are correlated to the address.

Also controlled by the address the CCU now transmits eight or sixteen clock pulses, and accordingly one or two bytes of data are written into the addressed IC or read out from it, beginning with the LSB.

The completion of the bus transaction is signalled by a short low-state pulse of the ID signal. This initiates the storing of the transferred data.

It is permissible to interrupt a bus transaction for up to 10 ms.

Table 12–1: Timing of the IM bus signals

Time	t_{IM1}	t_{IM2}	t_{IM3}	t_{IM4}	t_{IM5}	t_{IM6}	t_{IM7}	t_{IM8}	t_{IM9}	t_{IM10}
Min. µs	0	3.0	3.0	0	1.5	6.0	0	0	0	3.0

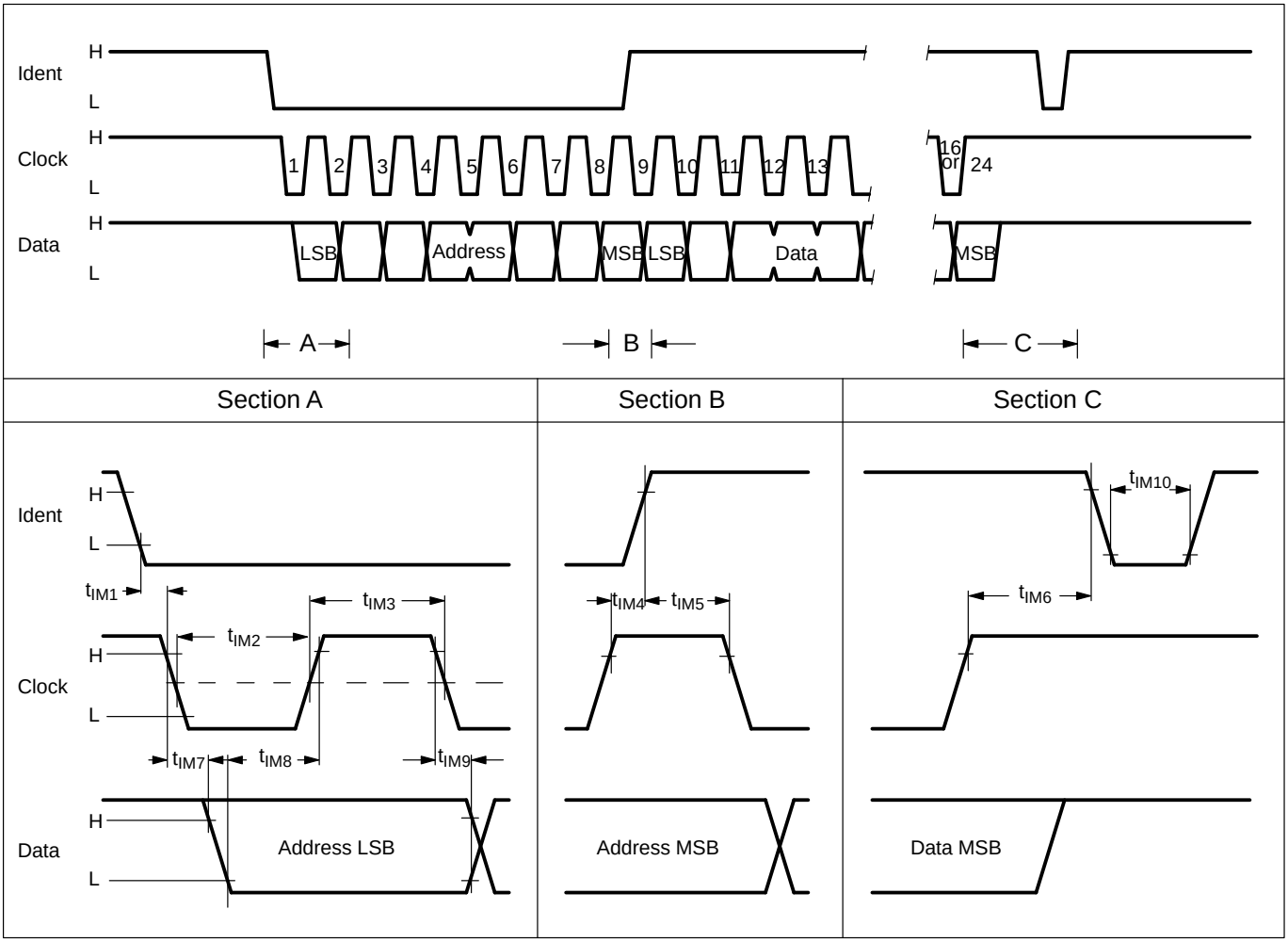


Fig. 12–1: IM bus waveforms

TPU 2735

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End of Data Sheet

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