# TRF5901
# SINGLE-CHIP RF TRANSCEIVER
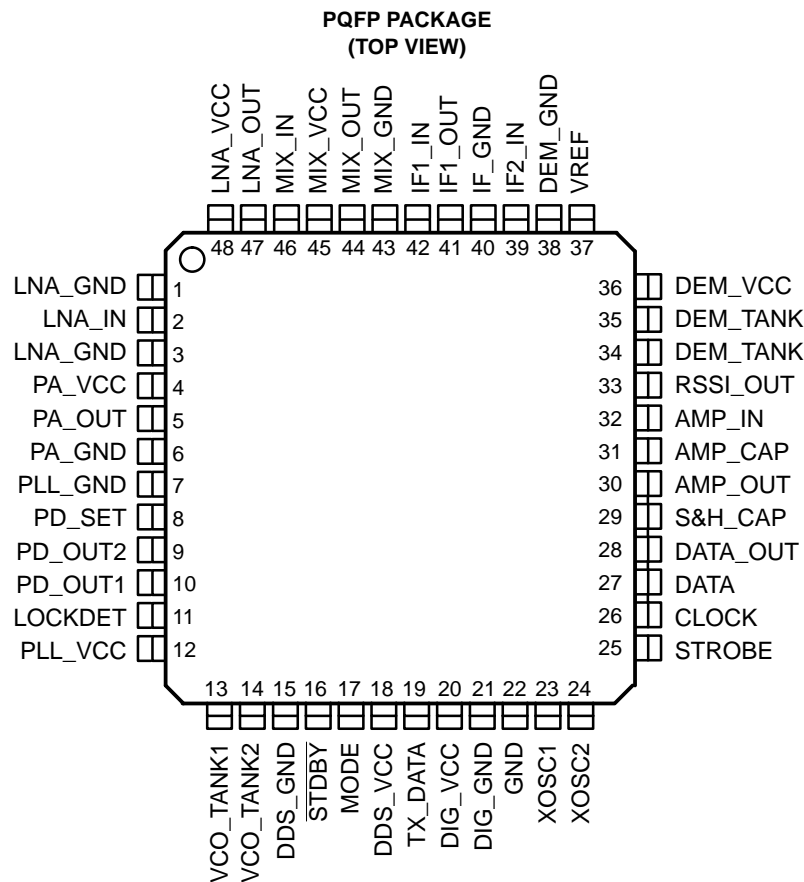
SWRS014 – DECEMBER 2002

- Single-Chip RF Transceiver for 915-MHz ISM Band
- 902-MHz to 928-MHz Operation
- FM/FSK Operation for Transmit and Receive
- 24-Bit Direct Digital Synthesizer (DDS) With 11-Bit DAC
- On-Chip VCO and PLL
- On-Chip Reference Oscillator
- Minimal External Components Required
- Low Power Consumption
- Typical Output Power of 4.5 dBm

- Typical Output Frequency Resolution of 230 Hz
- Ultrafast Lock Times From DDS Implementation
- Two Fully Programmable Operational Modes
- 3-V to 3.6-V Operation
- Fast Radio Strength Signal Indicator (RSSI)
- Flexible Serial Interface to TI MSP430 Microcontroller
- 48-Pin Low-Profile Plastic Quad Flat Package (PQFP)

**PQFP PACKAGE**
**(TOP VIEW)**

| Left pins | | Right pins |
|---|---|---|
| 1 LNA_GND | | 36 DEM_VCC |
| 2 LNA_IN | | 35 DEM_TANK |
| 3 LNA_GND | | 34 DEM_TANK |
| 4 PA_VCC | | 33 RSSI_OUT |
| 5 PA_OUT | | 32 AMP_IN |
| 6 PA_GND | | 31 AMP_CAP |
| 7 PLL_GND | | 30 AMP_OUT |
| 8 PD_SET | | 29 S&H_CAP |
| 9 PD_OUT2 | | 28 DATA_OUT |
| 10 PD_OUT1 | | 27 DATA |
| 11 LOCKDET | | 26 CLOCK |
| 12 PLL_VCC | | 25 STROBE |

Top pins (48–37): LNA_VCC, LNA_OUT, MIX_IN, MIX_VCC, MIX_OUT, MIX_GND, IF1_IN, IF1_OUT, IF_GND, IF2_IN, DEM_GND, VREF

Bottom pins (13–24): VCO_TANK1, VCO_TANK2, DDS_GND, STDBY, MODE, DDS_VCC, TX_DATA, DIG_VCC, DIG_GND, GND, XOSC1, XOSC2

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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**TEXAS INSTRUMENTS**

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## description

The TRF5901 single-chip solution is a low cost FSK transceiver to establish a frequency-agile, half-duplex, bidirectional RF link. The device is available in a 48-lead TQFP package and is designed to provide a fully functional multichannel FM transceiver. The single-chip transceiver operates down to 3 V and is expressly designed for low power consumption. The synthesizer has a typical channel spacing of approximately 230 Hz to allow narrow-band as well as wide-band application. Due to the narrow channel spacing of the direct digital synthesizer (DDS), the DDS can be used to adjust the TX/RX frequency and allows the use of inexpensive reference crystals.

Two fully-programmable operation modes, Mode0 and Mode1, allow fast switching between two preprogrammed settings (e.g., TX(RX)_frequency_0, RX(TX)_frequency_1) without reprogramming the device. Each functional block of the transceiver can be specifically enabled or disabled via the serial interface.

## transmitter

The transmitter consists of an integrated VCO, a complete fully programmable direct digital synthesizer, and a power amplifier. The internal VCO can be used with an external tank circuit or an external VCO. The divider, prescaler, and reference oscillator require only the addition of an external crystal and a loop filter to provide a complete DDS with a typical frequency resolution of 230 Hz.

The 8-bit FSK frequency deviation register determines the frequency deviation in FSK mode. The modulation itself is done in the direct digital synthesizer, hence no additional external components are necessary.

Since the typical RF output power is approximately 4.5 dBm, no additional external RF power amplifier is necessary in most applications.

## receiver

The integrated receiver is intended to be used as a single-conversion FSK receiver. It consists of an integrated VCO, a complete fully programmable direct digital synthesizer, a low-noise amplifier, mixer, IF amplifier, limiter, FM/FSK demodulator with an external LC tank circuit, and a data slicer. The receive strength signal indicator ( RSSI ) can be used for fast carrier sense detection or as an on/off keying, or amplitude shift keying, (OOK/ASK) demodulator. In the *learning mode*, during a learning sequence (0,1,0,1,0,....), the initial tolerances of the LC demodulator tank circuit are compensated and an external capacitor is charged to a dc voltage that is proportional to the average demodulation dc level. This level is the zero reference for the data slicer to generate the logical levels of the data sequence that follow the learning sequence. Using the internal data switch, the demodulated OOK and FSK signals are available at the same DATA_OUT terminal.

## baseband interface

The TRF5901 can easily be interfaced to a baseband processor such as the Texas Instruments MSP430 ultralow-power microcontroller (see Figure 1). The TRF5901 serial control registers are programmed by the MSP430 and the MSP430 performs baseband operations in software.

**TEXAS INSTRUMENTS**
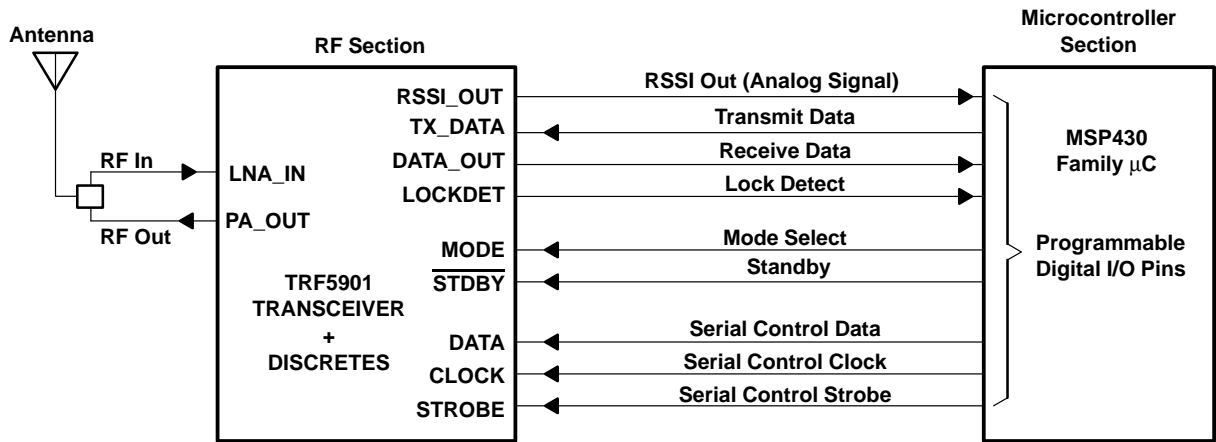
**Figure 1. System Block Diagram for Interfacing to the MSP430 Microcontroller**

## functional block diagram
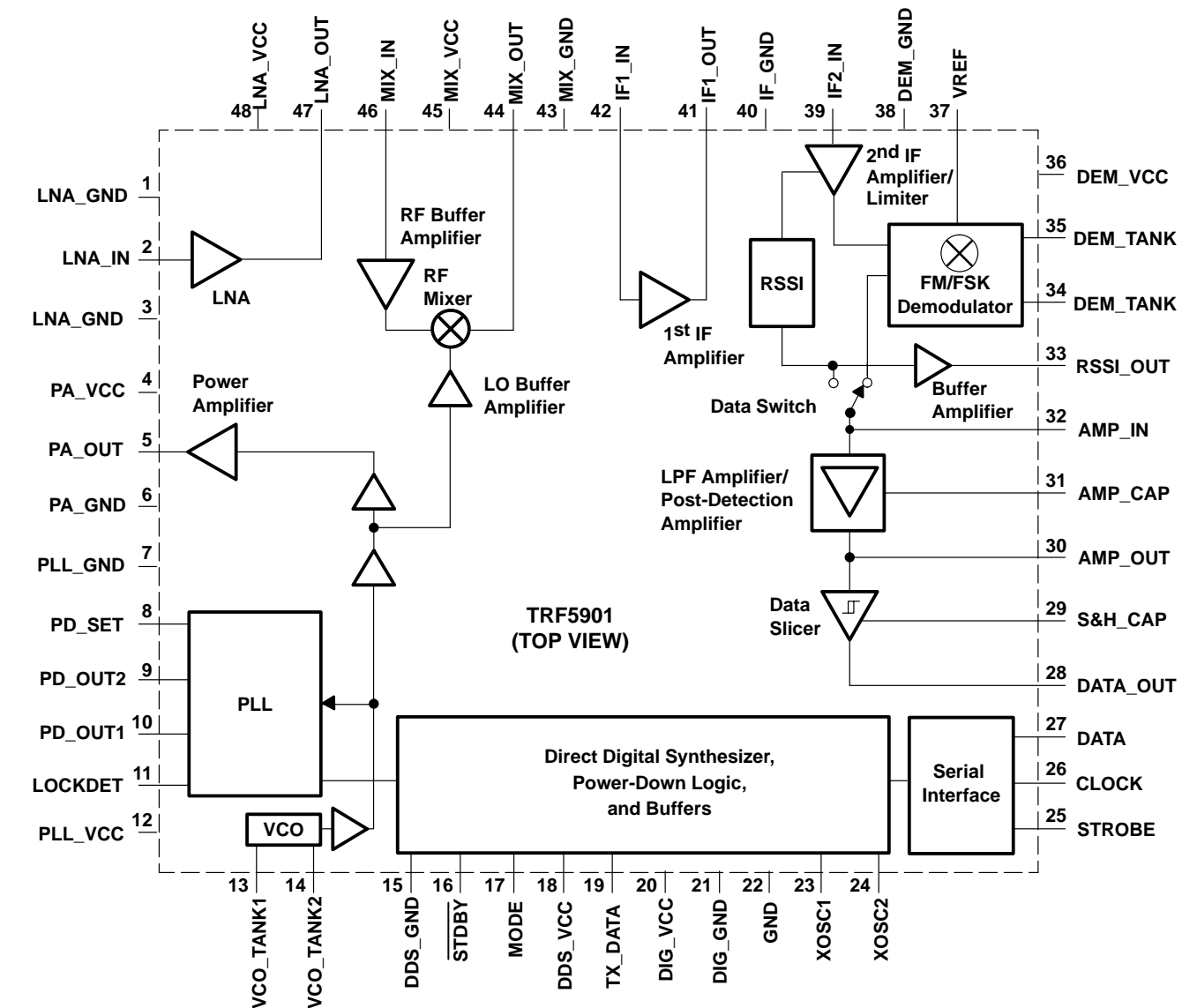


## Terminal Functions

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AMP_CAP | 31 | I/O | Connection for LPF amplifier/post-detection amplifier capacitor/resistor used to reduce the internal low-pass filter frequency and to adjust the post-detection gain. |
| AMP_IN | 32 | I | Analog post-detection amplifier input |
| AMP_OUT | 30 | O | Analog post-detection amplifier output |
| CLOCK | 26 | I | Serial interface clock signal |
| DATA | 27 | I | Serial interface data signal |
| DATA_OUT | 28 | O | Digital output of the data slicer, active high |
| DDS_GND | 15 | | Direct digital synthesizer ground |

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**Terminal Functions (Continued)**

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| DDS_VCC | 18 | | Direct digital synthesizer supply voltage |
| DEM_GND | 38 | | Quadrature demodulator ground |
| DEM_TANK | 34, 35 | I/O | Quadrature demodulator tank connection |
| DEM_VCC | 36 | | Quadrature demodulator supply voltage |
| DIG_GND | 21 | | Digital ground |
| DIG_VCC | 20 | | Digital supply voltage |
| IF_GND | 40 | | Intermediate frequency (IF) section ground |
| IF1_IN | 42 | I | Single-ended input for the 1st intermediate frequency (IF) amplifier |
| IF1_OUT | 41 | O | Single-ended output for the 1st intermediate frequency (IF) amplifier |
| IF2_IN | 39 | I | Single-ended input for the 2nd IF amplifier/limiter |
| LNA_GND | 1, 3 | | Low-noise amplifier ground |
| LNA_IN | 2 | I | Low-noise amplifier input |
| LNA_OUT | 47 | O | Low-noise amplifier output, open collector |
| LNA_VCC | 48 | | Low-noise amplifier supply voltage |
| LOCKDET | 11 | O | PLL lock detect output, active high. PLL locked when LOCKDET = 1. |
| MIX_GND | 43 | | Mixer ground |
| MIX_IN | 46 | I | Single-ended RF mixer input |
| MIX_OUT | 44 | O | Single-ended RF mixer output |
| MIX_VCC | 45 | | Mixer supply voltage |
| MODE | 17 | I | Mode select input. The functionality of the device in Mode0 or Mode1 can be programmed via the A-, B-, C-, and D-word of the serial control interface. |
| GND | 22 | | Ground |
| PA_GND | 6 | | Power amplifier ground |
| PA_OUT | 5 | O | Power amplifier output, open collector |
| PA_VCC | 4 | | Power amplifier supply voltage |
| PD_OUT1 | 10 | O | Charge pump output – PLL in locked condition |
| PD_OUT2 | 9 | O | Charge pump output – PLL in unlocked condition |
| PD_SET | 8 | | Charge pump current setting terminal. An external resistor ($R_{PD}$) is connected to this terminal to set the nominal charge pump current. |
| PLL_GND | 7 | | PLL ground |
| PLL_VCC | 12 | | PLL supply voltage |
| RSSI_OUT | 33 | O | Receive strength signal indicator, analog output |
| S&H_CAP | 29 | I/O | Connection for sample and hold capacitor for the data slicer. This capacitor determines the integration time constant of the integrator while in the learning mode. |
| $\overline{STDBY}$ | 16 | I | Standby control for the TRF5901, active low. While $\overline{STDBY}$ = 0, the contents of the control registers are still valid and can be programmed via the serial control interface. |
| STROBE | 25 | I | Serial interface strobe signal |
| TX_DATA | 19 | I | Digital modulation buffered input for FSK/FM modulation of the carrier, active high |
| VCO_TANK1 | 13 | I | VCO tank circuit connection. Should be left open if an external VCO is used. |
| VCO_TANK2 | 14 | I | VCO tank circuit connection. May also be used to input an external VCO signal. |
| VREF | 37 | I | Reference voltage for the quadrature demodulator |
| XOSC1 | 23 | O | Reference crystal oscillator connection |
| XOSC2 | 24 | I | Reference crystal oscillator connection. May be used as a single-ended clock input if an external crystal is not used. |

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, PLL_VCC, DDS_VCC, DIG_VCC, PA_VCC,
DEM_VCC, MIX_VCC, LNA_VCC (see Note 1) . . . . . . . . . . . . . . . . . . –0.6 to 4.5 Vdc
Input voltage, logic signals . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –0.6 to 4.5 Vdc
Storage temperature range . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All GND and VCC terminals must be connected to either ground or supply, respectively, even if the function block is not used.
ESD NOTE: Terminal 5 is not protected against ESD; other terminals have limited ESD protection to 1 kV HBM.

## recommended operating conditions

|  | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, PA_VCC, PLL_VCC, DIG_VCC, DDS_VCC, DEM_VCC, MIX_VCC, LNA_VCC | 3 | | 3.6 | V |
| Operating temperature | –40 | | 85 | °C |
| High-level input voltage, $V_{IH}$ (DATA, CLOCK, STROBE, TX_DATA, MODE, $\overline{STDBY}$) | $V_{CC}$–0.5 | | | V |
| Low-level input voltage, $V_{IL}$ (DATA, CLOCK, STROBE, TX_DATA, MODE, $\overline{STDBY}$) | | | 0.5 | V |
| High-level output voltage, $V_{OH}$ (LOCKDET, DATA_OUT); $I_{OH}$ = 0.5 mA | $V_{CC}$–0.5 | | | V |
| Low-level output voltage, $V_{OL}$ (LOCKDET, DATA_OUT); $I_{OL}$ = 0.5 mA | | | 0.5 | V |

## electrical characteristics over full range of operating conditions, (typical values are at PLL_VCC, DDS_VCC, DIG_VCC, DEM_VCC, MIX_VCC, LNA_VCC, PA_VCC = 3 V, $T_A$ = 25°C) (unless otherwise noted)

### supply current consumption in each mode

| MODE | | ACTIVE STAGES | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Power down (standby mode) | | None | | 0.5 | 5 | µA |
| RX – FSK (narrow band) or carrier sense | | DDS, PLL, VCO, LNA (normal mode), mixer, first IF amplifier, limiter, (demodulator, LPF amplifier, data slicer or RSSI) | | 28 | 35 | mA |
| TX | **PA STATE** | DDS, PLL, VCO, PA | | | | mA |
| | 0-dB attenuation | | | 37 | 53 | |
| | 10-dB attenuation | | | 26 | 35 | |
| | 20-dB attenuation | | | 21 | 27 | |
| | PA disabled | | | 9.5 | 13 | |

**electrical characteristics over full range of operating conditions, (typical values are at PLL_VCC, DDS_VCC, DIG_VCC, DEM_VCC, MIX_VCC, LNA_VCC, PA_VCC = 3 V, $T_A$ = 25°C) (unless otherwise noted) (continued)**

**LNA/RF mixer**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| RF frequency range | | 902 | | 928 | MHz |
| LNA gain | LNA in normal mode | 7.5 | 12 | | dB |
| | LNA in low-gain mode | | 4 | | dB |
| LNA noise figure | LNA in normal mode | | 4 | 5.8 | dB |
| LNA input 1-dB compression | LNA in normal mode | −20 | −15 | | dBm |
| | LNA in low-gain mode | −18 | −13 | | dBm |
| LNA input IP3 | LNA in normal mode | −12 | −5 | | dBm |
| | LNA in low-gain mode | −6 | 1 | | dBm |
| LNA input impedance | | | See Figure 3 | | Ω |
| LNA output impedance | | | See Figure 4 | | Ω |
| LO frequency range | | 891 | | 939 | MHz |
| IF frequency range | | | 10.7 | | MHz |
| Mixer conversion gain | | 3 | 7.5 | | dB |
| Mixer SSB noise figure | IF frequency = 10.7 MHz | | 17.5 | | dB |
| Mixer input impedance | | | See Figure 5 | | Ω |
| Mixer input IP3 | | −8 | 1 | | dBm |
| Mixer input 1-dB compression | | | −9 | | dBm |
| LO level at mixer input | | | | −35 | dBm |
| Mixer output impedance | IF frequency = 10.7 MHz, See Figure 6 | | 330 | | Ω |

**VCO**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Frequency range | | 891 | | 939 | MHz |
| Tuning range | | | 60 | | MHz |
| Phase noise | 50-kHz offset | | −86 | | dBc/Hz |
| Tuning voltage | | 0.5 | | $V_{CC}$−0.4 | V |

**first IF amplifier**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| IF amplifier frequency range | | | 10.7 | | MHz |
| IF amplifier gain | | 5.5 | 7 | | dB |
| IF amplifier noise figure | | | 12 | 14 | dB |
| IF amplifier input 1-dB compression | | −12 | −3 | | dBm |
| IF amplifier input IP3 | | −3.5 | 4 | | dBm |
| IF amplifier input impedance | IF frequency = 10.7 MHz, See Figure 8 | | 330 | | Ω |
| IF amplifier output impedance | IF frequency = 10.7 MHz, See Figure 9 | | 330 | | Ω |

**electrical characteristics over full range of operating conditions, (typical values are at PLL_VCC, DDS_VCC, DIG_VCC, DEM_VCC, MIX_VCC, LNA_VCC, PA_VCC = 3 V, $T_A$ = 25°C) (unless otherwise noted) (continued)**

### second IF amplifier/limiter

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| IF amplifier/limiter frequency range | | | 10.7 | | MHz |
| IF amplifier/limiter gain† | | | 80 | | dB |
| IF amplifier/limiter noise figure† | | | 9 | | dB |
| IF amplifier/limiter input impedance | IF frequency = 10.7 MHz, See Figure 10 | | 330 | | Ω |

† Not directly accessible, specified by design

### RSSI

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| RSSI range at limiter input | | −80 | | −10 | dBm |
| RSSI output voltage range | | 0.44 | | 2.6 | V |
| Nominal slope | | | 19 | | mV/dB |
| Response time step from power off to −20 dBm at limiter input | | | 1 | 5 | µs |

### low-pass filter amplifier [second order]

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Internal low-pass filter frequency | | | 0.75 | | MHz |

### demodulator

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Demodulation output bandwidth‡ | IF frequency = 10.7 MHz | | 0.3 | | MHz |
| Acquisition range‡ | IF frequency = 10.7 MHz | | 300 | | kHz |
| Slew rate‡ | | | 2 | | V/µs |

‡ Dependent upon external LC tank circuit.

### data slicer

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Output current | $R_{(load)}$ = 3.3 kΩ, $C_{(load)}$ = 10 pF | | 1 | | mA |
| Rise time | $R_{(load)}$ = 3.3 kΩ, $C_{(load)}$ = 10 pF | | 0.1 | | µs |

### direct digital synthesizer (DDS)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Reference oscillator input frequency, $f_{ref}$ | as oscillator | | 15 | | 26 | MHz |
| | as buffer | | 15 | | 26 | |
| Programmable DDS divider ratio | | 22 bits | 0 | | 4194303 | |
| DDS divider resolution, $\Delta f$ | | | $N \times f_{ref} \div 2^{24}$ | | | |
| FSK – modulation register ratio | | 8 bits | 0 | | 1020 | |
| FSK – modulation resolution | | | $N \times f_{ref} \div 2^{22}$ | | | |

**electrical characteristics over full range of operating conditions, (typical values are at PLL_VCC, DDS_VCC, DIG_VCC, DEM_VCC, MIX_VCC, LNA_VCC, PA_VCC = 3 V, T$_A$ = 25°C) (unless otherwise noted) (continued)**

**PLL**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| RF input frequency | | 891 | | 939 | MHz |
| RF input power | Internal VCO bypassed; external input applied to VCO_TANK2 | | −10 | | dBm |
| RF input divider ratio, N | | 256 | | 512 | |
| RF output frequency resolution | | | $N \times f_{ref} \div 2^{24}$ | | |
| Charge pump current | Programmable with external resistor, 100 kΩ nominal, APLL = 0 | | 70 | | µA |

**power amplifier**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Frequency range | | 902 | | 928 | MHz |
| Amplifier output power | 0-dB attenuation | −1 | 4.5 | | dBm |
| | 10-dB attenuation | −5 | −0.5 | | |
| | 20-dB attenuation | −14 | −8 | | |
| | Amplifier off | | | −56 | |
| Optimal load impedance | | | See Figure 22 | | |
| 2$^{nd}$-order harmonic | V$_{CC}$ = 3 V, 0-dB attenuation | | −13 | | dBc |
| 3$^{rd}$-order harmonic | V$_{CC}$ = 3 V, 0-dB attenuation | | −27 | | dBc |

**typical mode switching and lock times**

| OPERATION | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Frequency hop time between adjacent channels, during receive† | From transition of MODE to DATA_OUT valid, channel spacing = 500 kHz, APLL = 111b (maximum) | | 30 | | µs |
| Receive-to-transmit turnaround time† | From transition of MODE to valid RF signal at PA_OUT, PLL locked, 10.7 MHz RX to TX separation | | 200 | | µs |
| Transmit-to-receive turnaround time† | From transition of MODE to valid data at DATA_OUT, PLL locked, 10.7 MHz RX to TX separation | | 200 | | µs |
| Standby to receive time† | From rising edge of STDBY to valid data at DATA_OUT, APLL = 111b (maximum) | | 600 | | µs |
| Standby to transmit time† | From rising edge of STDBY to valid RF signal at PA_OUT, APLL = 111b (maximum) | | 500 | | µs |

† Highly dependent upon loop filter topology.

**timing data for serial interface (see Figure 2)**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| f$_{(CLOCK)}$ | CLOCK frequency | | 20 | MHz |
| t$_{w(CLKHI)}$ | CLOCK high time pulse width, CLOCK high | 25 | | ns |
| t$_{w(CLKLO)}$ | CLOCK low time pulse width, CLOCK low | 25 | | ns |
| t$_{su(DATA)}$ | Setup time, data valid before CLOCK high | 25 | | ns |
| t$_{h(DATA)}$ | Hold time, data valid after CLOCK high | 25 | | ns |
| t$_{w(STROBEHI)}$ | Strobe high time pulse width, STROBE high (see Note 2) | 25 | | ns |
| t$_{w(STROBELO)}$ | Strobe low time pulse width, STROBE low | 25 | | ns |

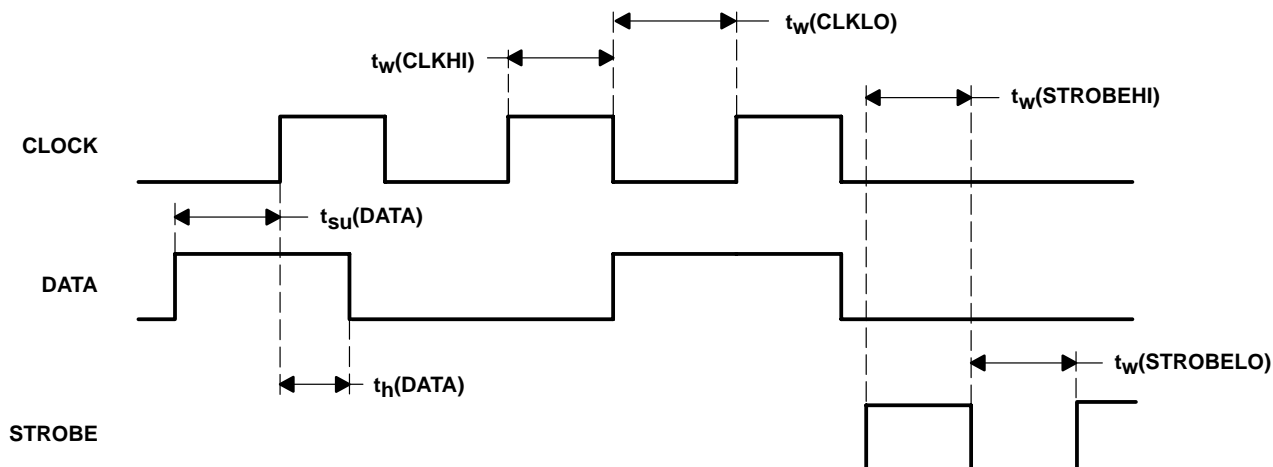NOTE 2: CLOCK and DATA must both be low when STROBE is asserted (STROBE = 1).

**Figure 2. Serial Data Interface Timing**

## detailed description

### low-noise amplifier

The low-noise amplifier (LNA) provides a typical gain of 13 dB and a typical noise figure of 3.3 dB.

Two operating modes, normal and low-gain mode, can be selected. The normal operation mode is selected when maximum sensitivity at low input levels is required. If high RF input levels are applied to the TRF5901, the LNA should be operated in the low-gain mode. This ensures a minimum of nonlinear distortions in the overall receiver chain.
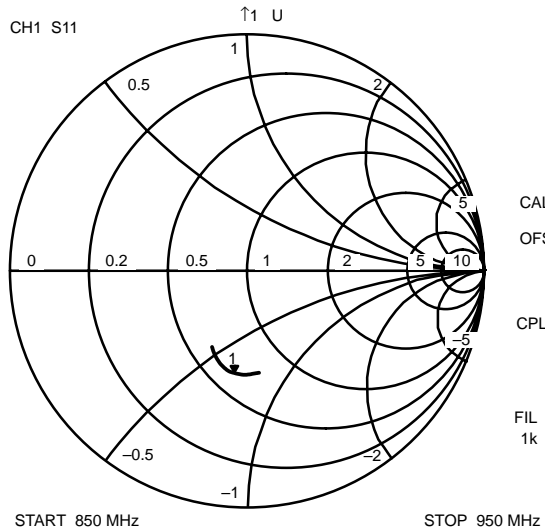


**Figure 3. Typical LNA Input Impedance (S11) at Device Terminal LNA_IN**
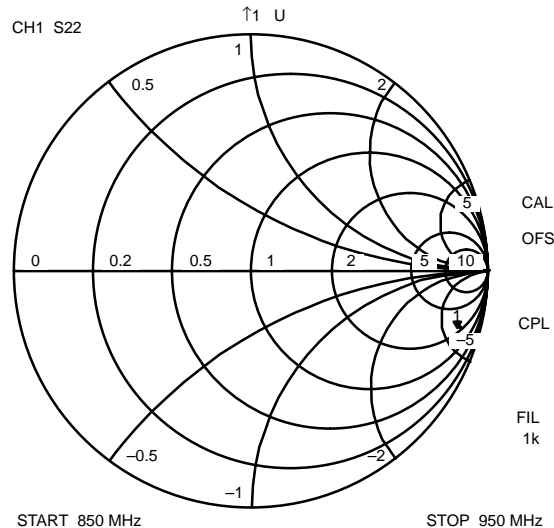


**Figure 4. Typical LNA Output Impedance (S22) at Device Terminal LNA_OUT**

The low impedance of the LNA input can be easily matched to 50 Ω to interface with a filter or an RF switch. At the LNA open collector output, a filter network can be used for image suppression as well as impedance matching.

**RF mixer**

The RF mixer is designed to operate with the on-chip VCO. If an external LO is used, a typical drive level of –10 dBm should be applied at the VCO input terminal. The mixer is a conventional double-balanced Gilbert cell mixer designed to provide a high IP3, typically 1 dBm.

Since the mixer output's push-pull amplifier has a 330-Ω output impedance, a conventional 330-Ω ceramic filter can be directly connected to the output without additional matching. The mixer output can also be directly connected to the second IF amplifier/limiter input terminal, IF2_IN, through a single conventional 330-Ω ceramic filter, thus bypassing the first IF amplifier.

Figure 5 and Figure 6 show the RF mixer input and output impedances, respectively.
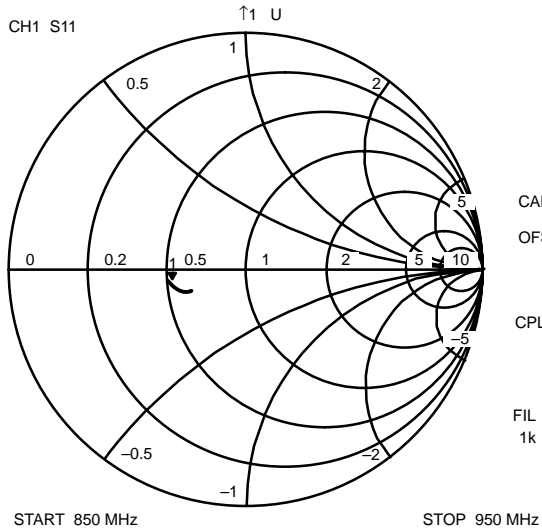


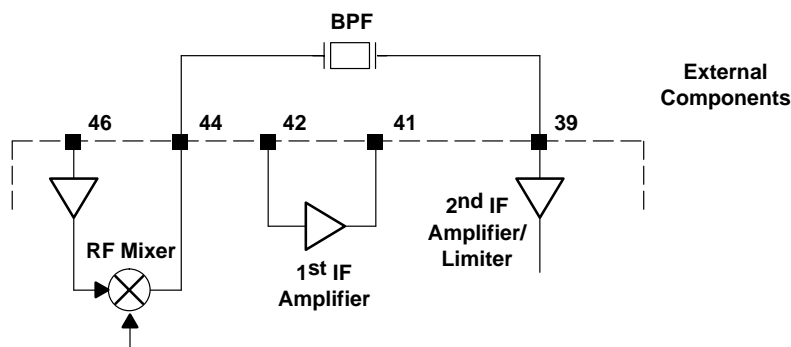**Figure 5. Typical RF Mixer Input Impedance (S11) at Device Terminal MIX_IN**
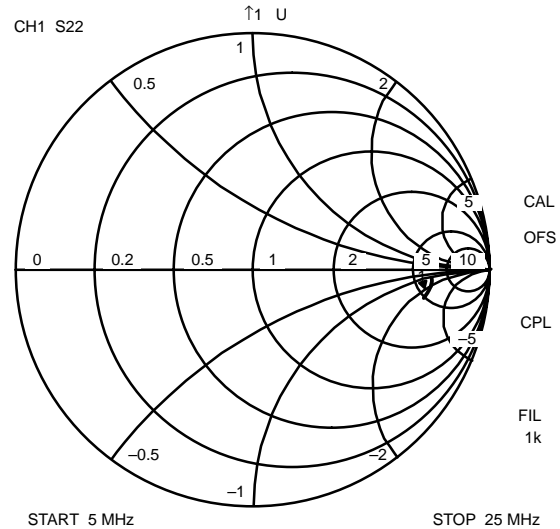


**Figure 6. Typical RF Mixer Output Impedance (S22) at Device Terminal MIX_OUT**

**first IF amplifier**

The first IF amplifier provides a typical gain of 7 dB to compensate for losses caused by a ceramic filter. The input and output of the first IF amplifier is matched internally to 330 Ω, permitting direct connections to 330-Ω ceramic filters. If filters with different impedances are used, an impedance matching network is required.

A second filter can be connected between the first IF amplifier and the second IF amplifier/limiter to increase the receiver selectivity. Alternately, the RF mixer output can be directly connected to the second IF amplifier as shown in Figure 7. A single ceramic filter can also be used to connect terminal 41 to terminal 39. In this case, a 0.1-μF dc-blocking capacitor should be used to connect terminal 44 to 42 to maximize receiver sensitivity.

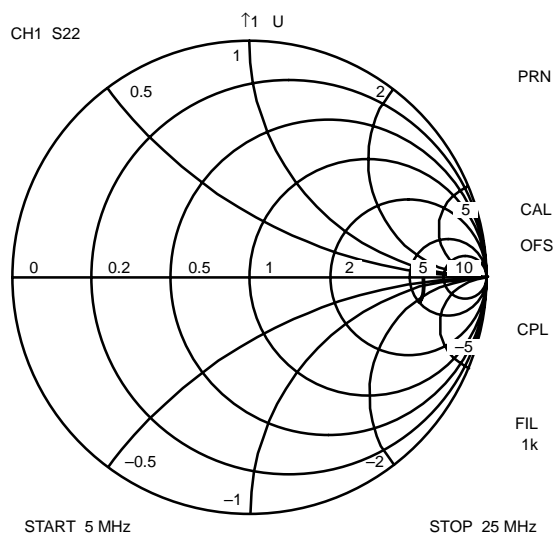## first IF amplifier (continued)



**Figure 7. Bypassing the First IF Amplifier**

Figure 8 and Figure 9 show the first IF amplifier input and output impedances, respectively.
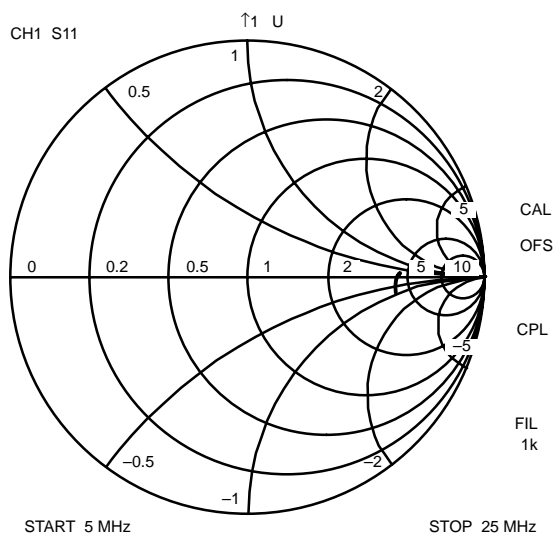


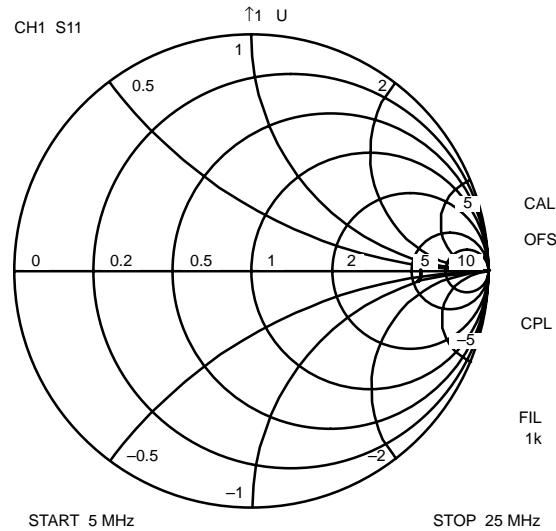**Figure 8. Typical First IF Amplifier Input Impedance (S11) at Device Terminal IF1_IN**



**Figure 9. Typical FIrst IF Amplifier Output Impedance (S22) at Device Terminal IF1_OUT**

## second IF amplifier/limiter

The second IF amplifier/limiter consists of several differential amplifier stages with an overall gain of approximately 80 dB. At the IF2_IN 330-$\Omega$ input, a minimum signal level of approximately 32 $\mu$V is required to generate a limited signal at the limiter output. The limiter output is directly fed to the FM/FSK demodulator.

Figure 10 shows the second IF amplifier/limiter input impedance.

**second IF amplifier/limiter (continued)**



**Figure 10. Typical Second IF Amplifier/Limiter Input Impedance (S11) at Device Terminal IF2_IN**

**received signal strength indicator (RSSI)**

The received signal strength indicator provides a voltage at terminal 33, RSSI_OUT, that is proportional to the RF limiter input level. The slope of the RSSI circuit is typically 19 mV/dB over a frequency range of 10 MHz to 21.4 MHz. Because of its ultrafast response time (typically 1 µs per –20 dBm to off step), the RSSI can easily be used as an amplitude-shift keying (ASK) or on/off keying (OOK) demodulator for data rates up to 100K bit/sec.

**FM/FSK demodulator**

The demodulator is intended for analog (FM) and digital (FSK) frequency demodulation. It consists of a quadrature demodulator with an external LC tank circuit. A variable inductor, internal to the TRF5901, operates in parallel with the external tank circuit (see Figure 13), and is used to adjust the external tank circuit's resonant frequency. If the tolerances of the external demodulator tank circuit components can provide a maximum frequency error of less than 5%, then no additional adjustments are required. As long as the device is in the *learning mode*, the internal reactance automatically fine-adjusts the resonant frequency of the external LC tank circuit. Depending on the supply voltage, the tank circuit tuning range is approximately four times the discriminator 3-dB bandwidth.

While in the *learning mode* i.e., during a dc-free learning sequence of 0,1,0,1,0,...., the initial tolerances of the LC demodulator tank circuit are compensated and an external capacitor (connected to terminal 29, S&H_CAP) is charged to a dc voltage that is proportional to the average demodulation dc level. This level establishes the decision threshold voltage and consequently sets the zero reference for the data slicer to generate the logical levels of the data sequence that follow the learning sequence. Therefore, the user can use a non-dc-free data signal.

The demodulator is automatically activated if the limiter (x_LIM) and low-pass filter amplifier (x_LPF) are activated and the data switch is set to FSK/FM reception (x_SW = 0).

**data switch**

The TRF5901 incorporates an internal data switch used to select the input signal for the low-pass filter amplifier/post detection amplifier. Depending on the settings in the Mode0 or Mode1 enable registers (C-word, D-word), the user can select between OOK/ASK or FSK baseband processing without having to change external components.

**low-pass filter amplifier/post-detection amplifier**

The low-pass filter amplifier/post-detection amplifier is configured to operate as a current-to-voltage amplifier and may be used to realize a low-pass filter for post detection. The low-pass amplifier bandwidth may be adjusted according to noise and signal bandwidth requirements. An internal 10-pF capacitor sets the maximum –3-dB corner frequency to approximately 0.75 MHz (see Figure 11 and Figure 12).
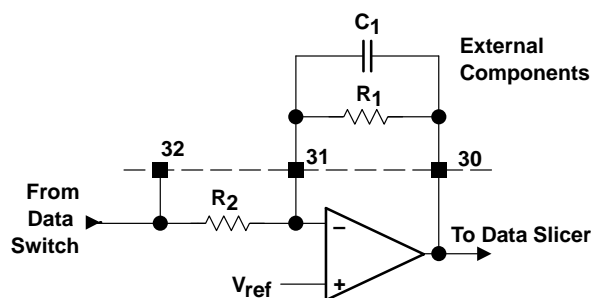


**Figure 11. First-Order Low-Pass Filter Example**
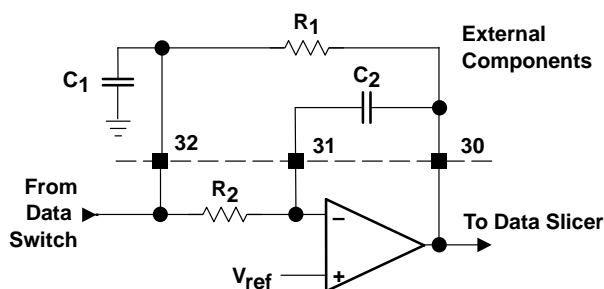


**Figure 12. Second-Order Low-Pass Filter Example**

The amplifier can be configured as a first- or second-order low-pass filter with bandwidths that are determined by external components. The internal resistor $R_2$ is set to 10 k$\Omega$, hence the –3-dB corner frequency for a second-order low pass filter (as shown in Figure 12) can be derived from the following formula:

$$f_g \cong \frac{1}{2 \times \pi \times \sqrt{10 \text{ k}\Omega \times R_1 \times C_1 \times C_2}}, \text{ where } \quad C_1 \approx 3 \times C_2$$

**data slicer**

The data slicer is fundamentally a comparator. The data slicer provides binary logic level signals, derived from the demodulated and low-pass filtered IF signal, that are able to drive external CMOS compatible inputs. The noninverting input is directly connected to the internal reference voltage, $V_{ref}$, and the inverting input is driven by the output of the low-pass filter amplifier/post-detection amplifier. The decision threshold of the data slicer is determined by the internal reference voltage, $V_{ref}$. The automatic frequency control (AFC) loop scheme for the TRF5901 is shown in Figure 13.

**data slicer (continued)**



**Figure 13. AFC Loop to Control the Data Slicer Decision Threshold**

The integrator, acting as an error amplifier, takes the low-pass filtered output signal and generates a control voltage proportional to the frequency error of the external tank circuit as compared to the limiter output signal. By adjusting the value of the internal variable inductor, this control voltage is used to fine-tune the external tank to its nominal value.

The acquisition time of the AFC loop can be adjusted by an external capacitor connected to terminal 29, S&H_CAP. This capacitor determines the integration time constant of the integrator *while in learning mode*. As a rule of thumb, the time constant of the AFC loop should be at least five times greater than the baseband signal fundamental period.

The time constant of the entire AFC control loop can be calculated as follows:

$$\tau_{AFC} \approx 22 \text{ k}\Omega \times C_{\text{terminal 29}}$$

The automatic frequency control loop controls the resonant frequency of the external LC tank without any additional external adjustments as long as *learning mode* operation is selected. If *hold mode* is selected, the AFC loop is open and an external dc voltage can be applied at terminal 29 to set the threshold of the data slicer. During *learning mode*, a precharged capacitor (connected to terminal 29, S&H_CAP) can be used to set the dc threshold voltage of the data slicer in *hold mode*.

In other words, the data slicer constantly integrates the incoming signal during the learning sequence (0,1,0,1. . .) and charges the external capacitor connected to terminal 29, S&H_CAP to a dc voltage level, $V_{ref}$, that is proportional to the average demodulation dc level. After a predefined time (dependent upon the application), the data slicer is switched to *hold mode*. The data slicer stops integrating and uses the voltage stored on the external capacitor as the decision threshold between a logic 0 or a logic 1 on the DATA_OUT terminal 28.

## reference oscillator

The reference oscillator provides the DDS system clock. It allows operation, with a suitable external crystal, between 15 MHz and 26 MHz.

An external oscillator may be used to supply clock frequencies between 15 MHz and 26 MHz. The external oscillator should be directly connected to XOSC2, terminal 24. The other oscillator terminal (XOSC1, terminal 23) should be left open or can be used as a buffered version of the signal applied at terminal 24 (see Figure 14). The same crystal or externally supplied oscillator signal is used to derive the transmit and receive frequencies.
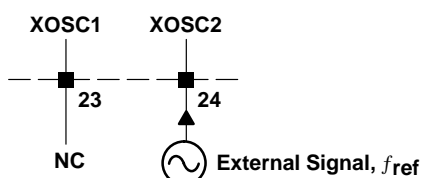


**Figure 14. Applying an External Oscillator Signal**

## direct digital synthesizer (DDS)

### general principles of DDS operation

In general, a direct digital synthesizer (DDS) is based on the principle of generating a sinewave signal in the digital domain. Benefits include high precision, wide frequency range, a high degree of software programmability, and extremely fast lock times.

A block diagram of a typical DDS is shown in Figure 15. It generally consists of an accumulator, sine lookup table, a digital-to-analog converter, and a low-pass filter. All digital blocks are clocked by the reference oscillator.
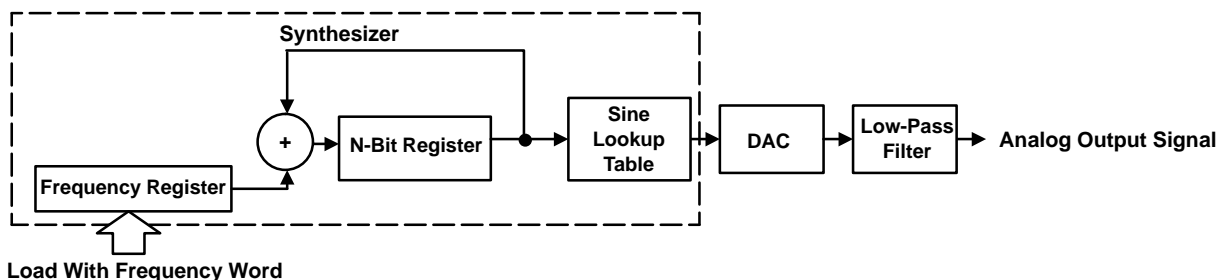


**Figure 15. Typical DDS Block Diagram**

The DDS constructs an analog sine waveform using an N-bit adder counting up from 0 to $2^N$ in steps of the frequency register, whereby generating a digital ramp waveform. Each number in the N-bit output register is used to select the corresponding sine wave value out of the sine lookup table. After the digital-to-analog conversion, a low-pass filter is necessary to suppress unwanted spurious responses.

The analog output signal can be used as a reference input signal for a phase locked loop. The PLL circuit then multiplies the reference frequency by a predefined factor.

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### TRF5901 direct digital synthesizer implementation

A block diagram of the DDS implemented in the TRF5901 is shown in Figure 16. It consists of a 24-bit accumulator clocked by the reference oscillator along with control logic settings.
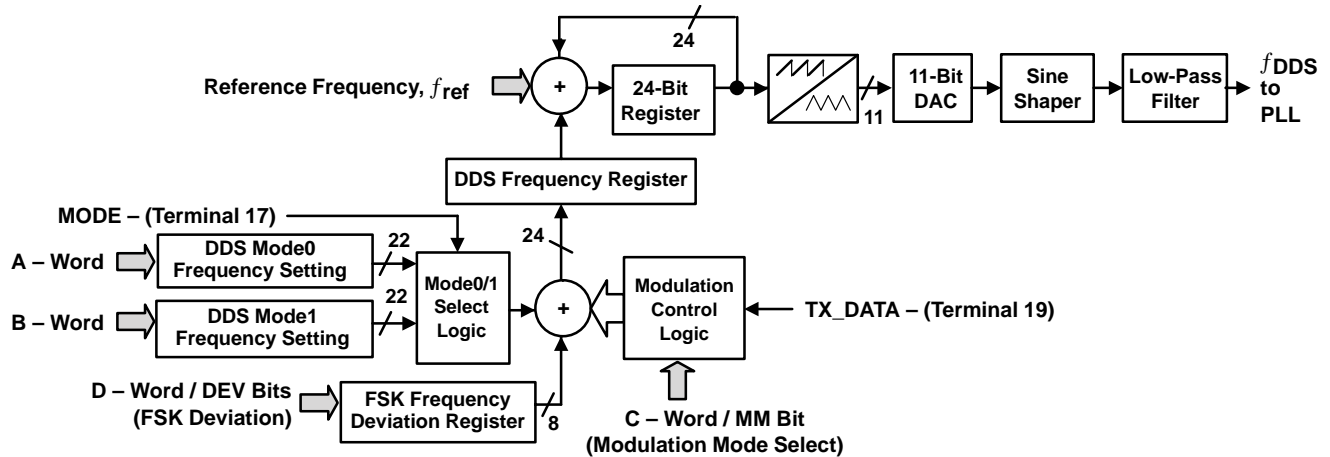


**Figure 16. DDS Block Diagram as Implemented in the TRF5901**

The frequency of the reference oscillator, $f_{ref}$, is the DDS sample frequency, which also determines the maximum DDS output frequency. Together with the accumulator width (in bits), the frequency resolution of the DDS can be calculated. Multiplied by the divider ratio (prescaler) of the PLL, N, the minimum frequency step size of the TRF5901 is calculated as follows:

$$\Delta f = N \times \frac{f_{ref}}{2^{24}}$$

The 24-bit accumulator can be programmed via two 22-bit frequency setting registers (the A-word determines the mode0 frequency, the B-word determines the mode1 frequency) with the two MSB bits set to zero. Consequently, the maximum bit weight of the DDS system is reduced to 1/8 (see Figure 17). This bit weight corresponds to a VCO output frequency of $(f_{ref}/8) \times N$. Depending on the MODE terminal's (terminal 17) logic level, the internal mode select logic loads the frequency register with either the DDS_0 or DDS_1 frequency (see Figure 16 and Figure 17).
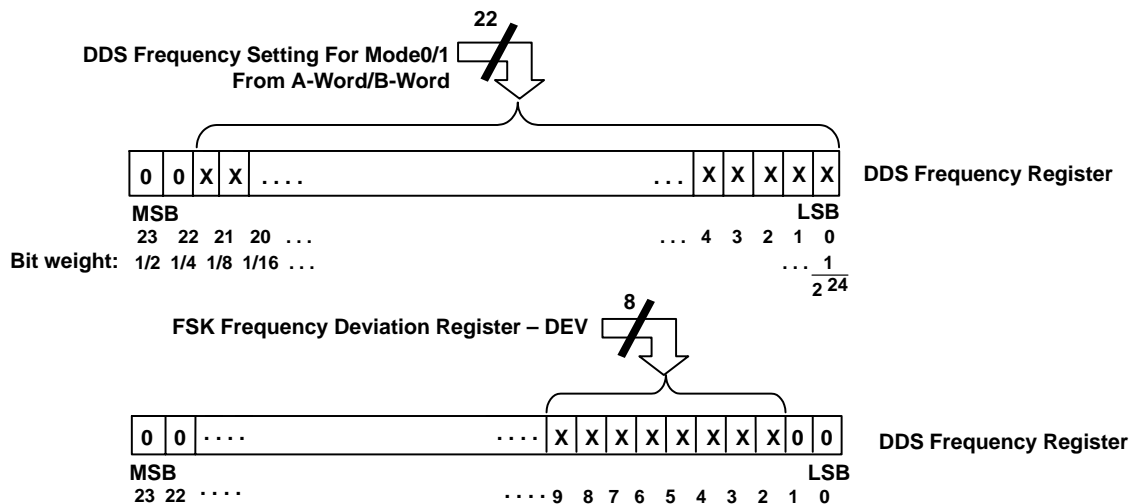


**Figure 17. Implementation of the DDS Frequency and FSK Frequency
Deviation in the DDS Frequency Register**

### TRF5901 direct digital synthesizer implementation (continued)

The VCO output frequency, $f_{out}$, which is dependent on the DDS_x frequency settings ( DDS_0 in the A-word or DDS_1 in the B-word ), can be calculated as follows:

$$f_{out} = DDS\_x \times N \times \frac{f_{ref}}{2^{24}} = N \times \frac{f_{ref} \times DDS\_x}{2^{24}}$$

If FSK modulation is selected (MM=0; C-Word, bit 16) the 8-bit FSK deviation register can be used to program the frequency deviation of the 2-FSK modulation. Figure 17 illustrates where the 8 bits of the FSK deviation register map into the 24-bit DDS frequency register. Since the two LSBs are set to zero, the total FSK deviation can be determined as follows:

$$\Delta f_{2-FSK} = N \times \frac{DEV \times f_{ref}}{2^{22}}$$

Hence, the 2-FSK frequency, set by the level of TX_DATA, is calculated as follows:

$$f_{out1:TX\_DATA=Low} = N \times \frac{f_{ref} \times DDS\_x}{2^{24}} \qquad f_{out2:TX\_DATA=High} = N \times \frac{f_{ref} \times (DDS\_x + 4 \times DEV)}{2^{24}}$$

This frequency modulated output signal is used as a reference input signal for the PLL circuit.

Note that the frequencies $f_{out1}$ and $f_{out2}$ are centered about the frequency $f_{center} = (f_{out1} + f_{out2})/2$. When transmitting FSK, $f_{center}$ is considered to be the effective carrier frequency and any receiver local oscillator (LO) should be set to the same $f_{center}$ frequency $\pm$ the receiver's IF frequency ($f_{IF}$) for proper reception and demodulation.

For the case of low-side injection, the receiver LO would be set to $f_{LO} = f_{center} - f_{IF}$. Using low-side injection, the received data at terminal 28, DATA_OUT, would be inverted from the transmitted data applied at terminal 19, TX_DATA. Conversely, for high-side injection, the receiver LO would be set to $f_{LO} = f_{center} + f_{IF}$. Using high-side injection, the received data would be the same as the transmitted data.

In addition, when the TRF5901 is placed in receive mode, it is recommended that the TX_DATA terminal be kept low. In this manner, the actual LO frequency injected into the mixer is $f_{out1} = f_{LO}$. If TX_DATA is set high, the contents of the deviation register would offset the receiver LO resulting in poor receiver sensitivity.

Channel width (frequency deviation) for 2-FSK modulation and channel spacing are software programmable. The minimum channel width and minimum channel spacing depend on the RF system frequency plan.

Since the DDS registers are static, preprogrammed values are retained during standby mode. This feature greatly reduces turnon time, reduces current consumption when coming out of standby mode, and enables very fast lock-times. The PLL lock-times ultimately determine when data can be transmitted or received.

### phase-locked loop

The phase-locked loop (PLL) of the TRF5901 consists of a phase detector (PD) and a frequency acquisiton aid (FD), two charge pumps, an external loop filter, a voltage controlled oscillator (VCO), and a programmable fixed prescaler (N-divider) in the feedback loop (see Figure 18).

The PLL as implemented in the TRF5901 multiplies the DDS output frequency and further suppresses the unwanted spurious signals produced by the direct digital synthesizer.

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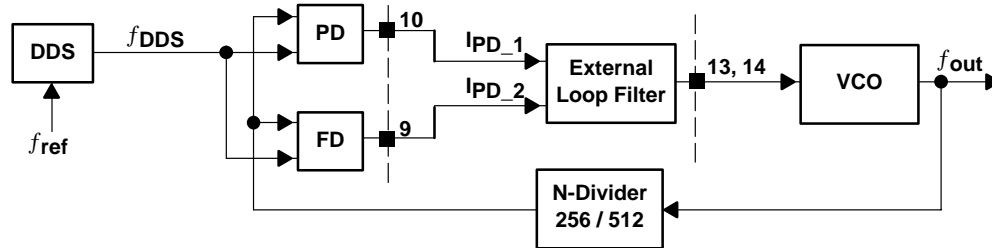
**phase-locked loop (continued)**



**Figure 18. Basic PLL Structure**

**VCO**

A modified Colpitts oscillator architecture with an external resonant circuit is used for the TRF5901. The internal bias current network adjusts the signal amplitude of the VCO. This allows a wide range of Q-factors (30….60) for the external tank circuit.

The VCO can be bypassed by applying an external RF signal at VCO_TANK2, terminal 14. To drive the internal PLL, a typical level of −10 dBm should be applied. When an external VCO is used, the x_VCO bit should be set to 0.

**phase detector and charge pumps**

The TRF5901 contains two charge pumps for locking to the desired frequency: one for coarse tuning of the frequency differences (called the frequency acquisition aid), and one for fine tuning of the phase differences (used in conjunction with the phase detector).

The XOR phase detector and charge pumps produce a mean output current that is proportional to the phase difference between the reference frequency and the VCO frequency divided by N; N=256 or 512. The TRF5901 generates the current pulses $I_{PD\_1}$ during normal operation (PLL locked).

An additional slip detector and acquisition aid charge pump generates current pulses at terminal PD_OUT2 during the lock-in of the PLL. This charge pump is turned off when the PLL locks in order to reduce current consumption. The multiplication factor of the acquisition aid current $I_{PD\_2}$ can be programmed by three bits (APLL) in the C-word.

The slip detector output, PD_OUT2, at terminal 9 should be connected directly to the loop filter capacitor $C_1$, as in Figure 21. The nominal charge pump current $I_0$ is determined by the external resistor $R_{PD}$, connected to terminal 8, and can be calculated as follows:

$$I_0 = \frac{7\ V}{R_{PD}}$$

During normal operation (PLL locked), the acquisition aid charge pump is disabled and the maximum charge pump current $I_{PD\_1}$ is determined by the nominal value $I_0$ (see Figure 19).



**Figure 19. Normal Operation Charge Pump Current, $I_{PD\_1}$**

Each time the PLL is in an unlocked condition, the acquisition aid charge pump generates current pulses $I_{PD\_2}$. The $I_{PD\_2}$ current pulses are APLL times larger than $I_0$ (see Figure 20).

**phase detector and charge pumps (continued)**
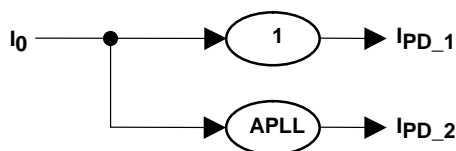


**Figure 20. Acquisition Aid ($I_{PD\_2}$) and Normal Operation ($I_{PD\_1}$) Charge Pump Currents**

**programmable divider**

The internal divider ratio, N, can be set to 256 or 512 via the C-word. Since a higher divider ratio adds additional noise within the multiplication loop, the lowest divider ratio possible for the target application should be used.

**loop filter**

Loop filter designs are a balance between lock-time, noise, and spurious suppression. For the TRF5901, common loop filter design rules can be used to determine an appropriate low-pass filter. Standard formulas can be used as a first approach to calculate a basic loop filter. Figure 21 illustrates a basic third-order loop filter.
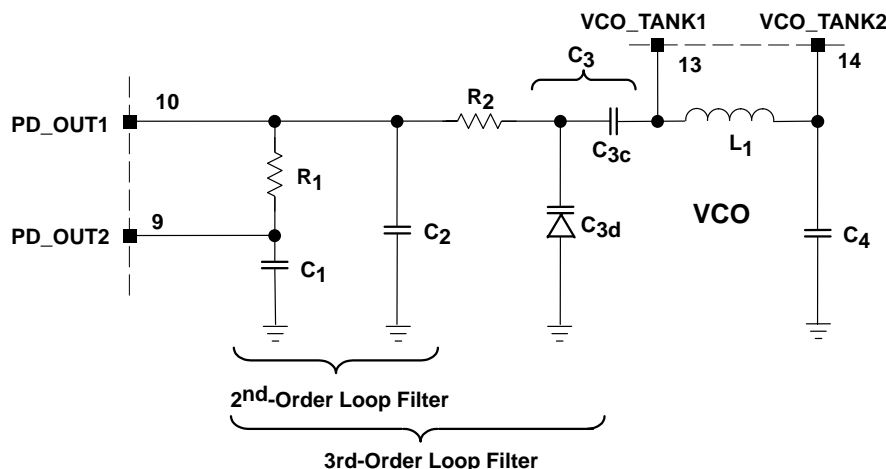


**Figure 21. Basic Third-Order Loop Filter Structure**

For maximum suppression of the unwanted frequency components, the loop filter bandwidth should generally be made as narrow as possible. At the same time, the filter bandwidth has to be wide enough to allow for the 2-FSK modulation and appropriate lock-time. A detailed simulation of the phase-locked loop should be performed and later verified on PCB implementations.

**power amplifier**

The power amplifier (PA) can be programmed via two bits (P0 and P1 in the D-word) to provide varying output power levels. Several control loops are implemented internally to set the output power and to minimize the sensitivity of the power amplifier to temperature, load impedance, and power supply variations. The output stage of the PA usually operates in Class-C and enables easy impedance matching. PA_OUT, terminal 5, is an open collector output terminal.
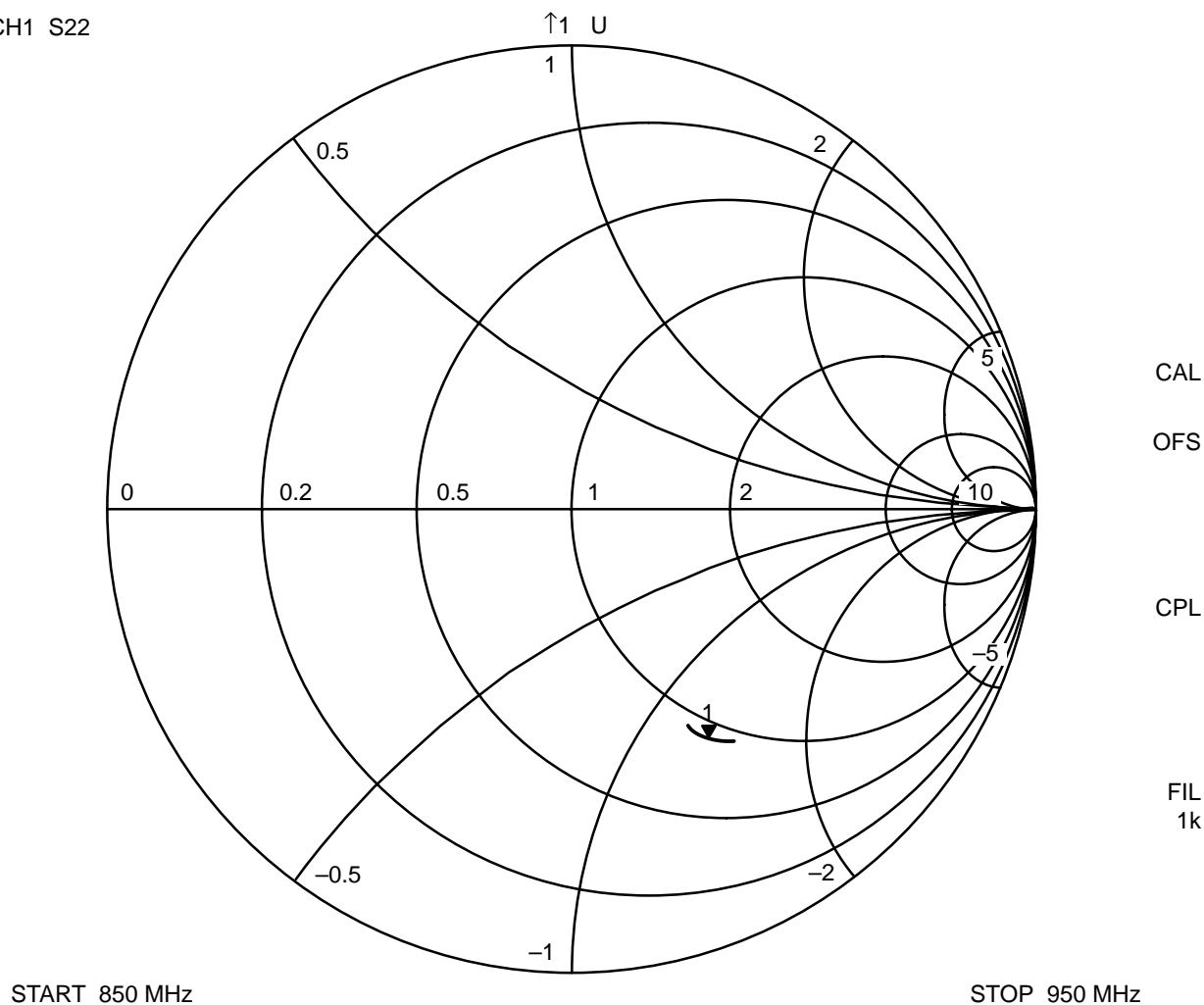
**power amplifier (continued)**



**Figure 22. Power Amplifier Output Impedance (S22) at Device Terminal 5**

# PRINCIPLES OF OPERATION

## serial control interface

A 3-wire unidirectional serial bus (CLOCK, DATA, STROBE) is used to program the TRF5901 (see Figure 23). The internal registers contain all user programmable variables including the DDS frequency setting registers as well as all control registers.

At each rising edge of the CLOCK signal, the logic value on the DATA terminal is written into a 24-bit shift register. Setting the STROBE terminal high loads the programmed information into the selected latch. While the STROBE signal is high, the DATA and CLOCK lines must be low (see Figure 2). Since the CLOCK and STROBE signals are asynchronous, care should be taken to ensure these signals remain free of glitches and noise.

As additional leading bits are ignored, only the least significant 24 bits are serial-clocked into the shift register. Due to the static CMOS design, the serial interface consumes virtually no current and it can be programmed in active as well as in standby mode.

The control words are 24 bits in length. The first incoming bit functions as the most significant bit ( MSB ).

To fully program the TRF5901, four 24-bit words must be sent: the A-, B-, C-, and D-word. If individual bits within a word are to be changed, then it is sufficient to program only the appropriate 24-bit word.

The definition of the control words are illustrated in Figure 24. Tables 1, 2, and 3 describe the function of each parameter.
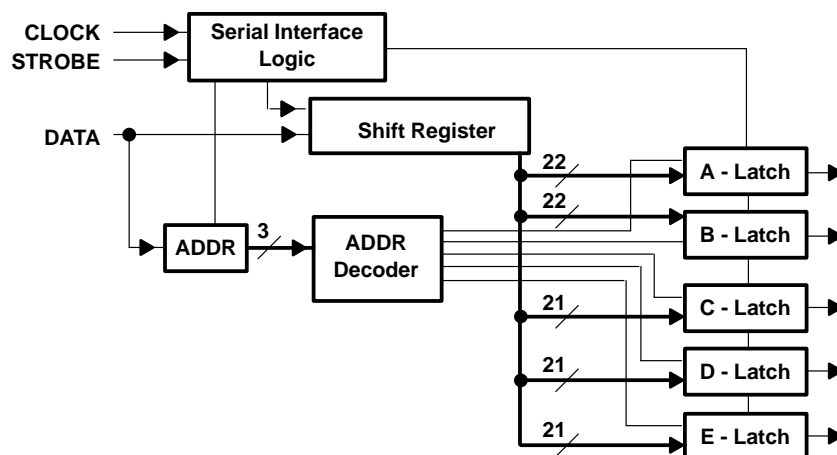


**Figure 23.  Serial Interface Block Diagram**

The E-latch, addressed by an ADDR equal to 111, is reserved for test purposes and should not be used. Inadvertently addressing the E-latch activates the test modes of the TRF5901.

If the test mode has been inadvertently activated, it can only be exited by switching $V_{CC}$ on and off or by clearing the E-latch. The E-latch can be cleared by addressing it and resetting its entire contents by programming 1110 0000 0000 0000 0000 0000.

As part of a proper power-up sequence, it is recommended to clear the E-latch each time $V_{CC}$ is applied before starting further operations with the TRF5901.

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## PRINCIPLES OF OPERATION

**A-Word (Programming of DDS_0)**

MSB                                                                                          LSB

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | ├———————— DDS Frequency Setting for Mode0 (DDS_0 [21:0]) ——————————┤ |

ADDR

**B-Word (Programming of DDS_1)**

MSB                                                                                          LSB

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | ├———————— DDS Frequency Setting for Mode1 (DDS_1 [21:0]) ——————————┤ |

ADDR
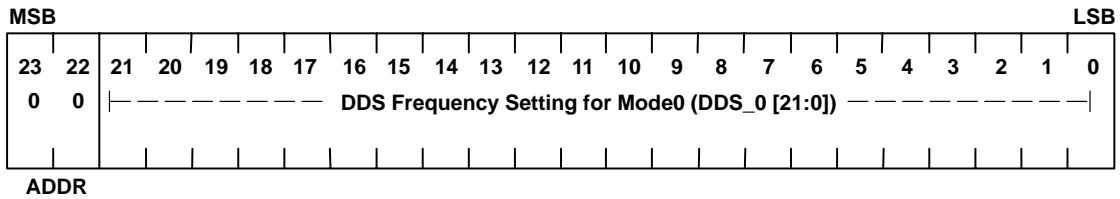
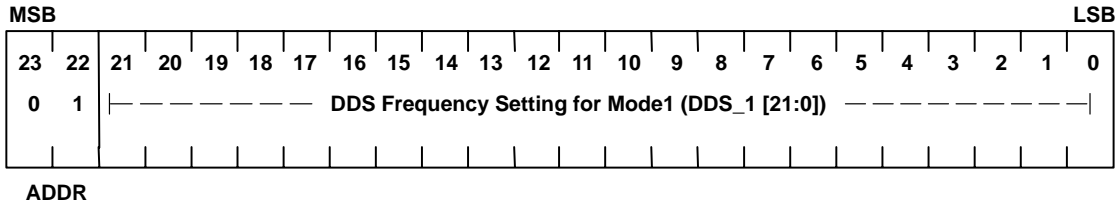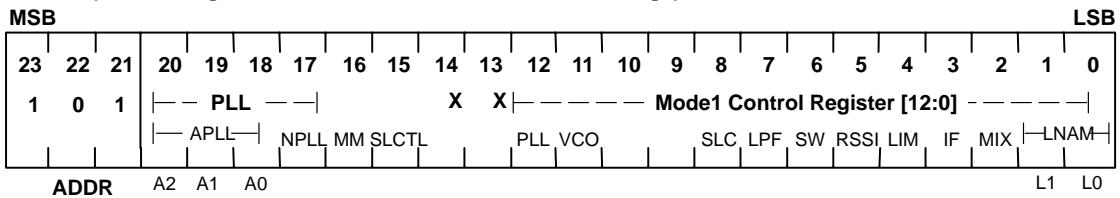**C-Word (Control Register for PLL, Data Slicer and Mode1 Settings)**

MSB                                                                                          LSB

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | ├—— PLL ——┤ | | | X | X | ├————— Mode1 Control Register [12:0] —————┤ |

|  |  |  | ├— APLL —┤ | NPLL | MM | SLCTL | | | PLL | VCO | | | SLC | LPF | SW | RSSI | LIM | IF | MIX | ├—LNAM—┤ |

ADDR   A2  A1  A0                                                                          L1   L0

**D-Word (Control Register for Mode0 Settings)**

MSB                                                                                          LSB

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ├——— Mode0 Control Register [12:0] ———┤ |

|  |  |  | | | | | | | | | PLL | VCO | | | SLC | LPF | SW | RSSI | LIM | IF | MIX | ├—LNAM—┤ |

ADDR                                                                                       L1   L0
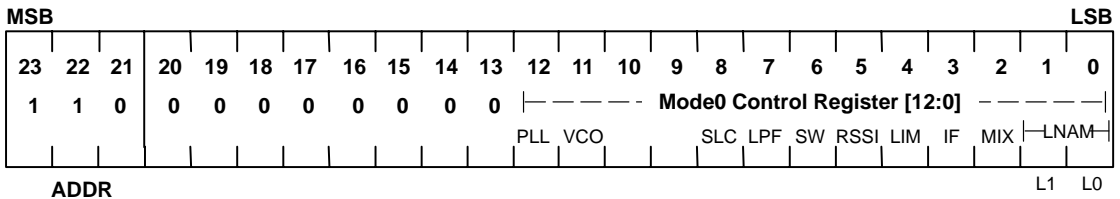
NOTE: Start programming with MSB and ensure that the CLOCK and DATA lines are low during the rising edge of the strobe signal.

**Figure 24. Serial Control Word Format**

## PRINCIPLES OF OPERATION

### Table 1. Mode0 Control Register Description (D-Word)

| SYMBOL | BIT LOCATION | NUMBER OF BITS | DESCRIPTION | INITIAL SETTINGS AFTER POWER UP | |
|---|---|---|---|---|---|
| | | | | DEFAULT STATE | DEFAULT VALUE |
| 0_LNAM | [1:0] | 2 | Low-noise amplifier operation mode<br><br>**L1**    **L0**<br>0      0    : LNA disabled<br>0      1    : LNA enable – low-gain mode<br>1      0    : LNA disabled<br>1      1    : LNA enable – normal operation mode | Disabled | 00b |
| 0_MIX | [2] | 1 | Enable mixer        1: enabled     0: disabled | Disabled | 0b |
| 0_IF | [3] | 1 | Enable 1st IF amplifier    1: enabled     0: disabled | Disabled | 0b |
| 0_LIM | [4] | 1 | Enable limiter        1: enabled     0: disabled | Disabled | 0b |
| 0_RSSI | [5] | 1 | Enable RSSI        1: enabled     0: disabled | Disabled | 0b |
| 0_SW | [6] | 1 | Data switch<br><br>0 : LPF amplifier input routed to demodulator (FSK/FM)<br>1 : LPF amplifier input routed to RSSI (OOK/ASK) | Routed to Demodulator | 0b |
| 0_LPF | [7] | 1 | Enable LPF amplifier    1: enabled     0: disabled | Disabled | 0b |
| 0_SLC | [8] | 1 | Enable data slicer      1: enabled     0: disabled | Disabled | 0b |
| 0_PA | [10:9] | 2 | Power amplifier mode<br><br>**P1**    **P0**<br>0      0    : disabled<br>0      1    : 10-dB attenuation, enable modulation via TX_DATA<br>1      0    : 20-dB attenuation, enable modulation via TX_DATA<br>1      1    : 0-dB attenuation, enable modulation via TX_DATA | Disabled | 00b |
| 0_VCO | [11] | 1 | During operation, this bit should always be enabled (1: enabled), unless an external VCO is used. | Disabled | 0b |
| 0_PLL | [12] | 1 | Enable PLL (DDS system, RF, VCO, divider, phase comparator and charge pump)<br>            1: enabled     0: disabled | Disabled | 0b |

NOTE: The FM/FSK demodulator is automatically enabled if the limiter and low-pass amplifier are enabled and the data switch is set to FSK reception.

## PRINCIPLES OF OPERATION

**Table 2. Mode1 Control Register Description (C-Word)**

| SYMBOL | BIT LOCATION | NUMBER OF BITS | DESCRIPTION | INITIAL SETTINGS AFTER POWER UP | |
|---|---|---|---|---|---|
| | | | | DEFAULT STATE | DEFAULT VALUE |
| 1_LNAM | [1:0] | 2 | Low-noise amplifier operation mode<br><br>**L1**　　**L0**<br>0　　　0　 : LNA disabled<br>0　　　1　 : LNA enable – low-gain mode<br>1　　　0　 : LNA disabled<br>1　　　1　 : LNA enable – normal operation mode | Disabled | 00b |
| 1_MIX | [2] | 1 | Enable mixer　　　　　　1: enabled　　0: disabled | Disabled | 0b |
| 1_IF | [3] | 1 | Enable 1$^{st}$ IF amplifier　　1: enabled　　0: disabled | Disabled | 0b |
| 1_LIM | [4] | 1 | Enable limiter　　　　　1: enabled　　0: disabled | Disabled | 0b |
| 1_RSSI | [5] | 1 | Enable RSSI　　　　　　1: enabled　　0: disabled | Disabled | 0b |
| 1_SW | [6] | 1 | Data switch<br><br>0 : LPF amplifier input routed to demodulator (FSK/FM)<br>1 : LPF amplifier input routed to RSSI (OOK/ASK) | Routed to Demodulator | 0b |
| 1_LPF | [7] | 1 | Enable LPF amplifier　　1: enabled　　0: disabled | Disabled | 0b |
| 1_SLC | [8] | 1 | Enable data slicer　　　1: enabled　　0: disabled | Disabled | 0b |
| 1_PA | [10:9] | 2 | Power amplifier mode<br><br>**P1**　　**P0**<br>0　　　0　 : disabled<br>0　　　1　 : 10-dB attenuation, enable modulation via TX_DATA<br>1　　　0　 : 20-dB attenuation, enable modulation via TX_DATA<br>1　　　1　 : 0-dB attenuation, enable modulation via TX_DATA | Disabled | 00b |
| 1_VCO | [11] | 1 | During operation, this bit should always be enabled (1: enabled), unless an external VCO is used. | Disabled | 0b |
| 1_PLL | [12] | 1 | Enable PLL (DDS system, VCO, RF divider, phase comparator and charge pump)<br>　　　　　　　　　1: enabled　　　0: disabled | Disabled | 0b |

NOTE: The FM/FSK demodulator is automatically enabled if the limiter and low-pass amplifier are enabled and the data switch is set to FSK reception.

## PRINCIPLES OF OPERATION

### Table 3. Miscellaneous Control Register Description

| SYMBOL | WORD | BIT LOCATION | NUMBER OF BITS | DESCRIPTION | INITIAL SETTINGS AFTER POWER UP | |
|---|---|---|---|---|---|---|
| | | | | | DEFAULT STATE | DEFAULT VALUE |
| DDS_0 | A-word | [21:0] | 22 | DDS frequency setting in Mode0 | Zero | All zeroes |
| DDS_1 | B-word | [21:0] | 22 | DDS frequency setting in Mode1 | Zero | All zeroes |
| DEV | D-word | [20:13] | 8 | FSK frequency deviation register | Zero | All zeroes |
| SLCTL | C-word | [15] | 1 | Slicer mode select bit<br>0 : hold mode<br>1 : learning mode | Hold mode | 0b |
| APLL | C-word | [20:18] | 3 | Acceleration factor for the frequency acquisition aid charge pump<br>**A2   A1   A0**<br>0    0    0    : 1<br>0    0    1    : 20<br>0    1    0    : 40<br>0    1    1    : 60<br>       :<br>1    1    1    : 140 | Zero | 000b |
| NPLL | C-word | [17] | 1 | PLL divider ratio<br>0 : 256<br>1 : 512 | 256 | 0b |
| MM | C-word | [16] | 1 | Modulation mode select. Sets the behavior of pin TX_DATA to FSK data input.<br>0 : FSK/FM<br>1 : Do not use | FSK mode | 0b |

### operating modes

Table 4 and Table 5 illustrate operating modes and transmit frequencies as set by the $\overline{\text{STDBY}}$, MODE and TX_DATA terminals used in conjunction with the DDS frequency settings.

### Table 4. Transmitting Data in FSK Mode (MM bit set to 0)

| TERMINAL | | | TRANSMIT FREQUENCY |
|---|---|---|---|
| $\overline{\text{STDBY}}$ | MODE | TX_DATA | |
| 1 | 0 | 0 | $f_{\text{out}} = f_{\text{ref}} \times N \times (\text{DDS\_0})/2^{24}$ |
| 1 | 0 | 1 | $f_{\text{out}} = f_{\text{ref}} \times N \times (\text{DDS\_0} + 4 \times \text{DEV})/2^{24}$ |
| 1 | 1 | 0 | $f_{\text{out}} = f_{\text{ref}} \times N \times (\text{DDS\_1})/2^{24}$ |
| 1 | 1 | 1 | $f_{\text{out}} = f_{\text{ref}} \times N \times (\text{DDS\_1} + 4 \times \text{dev})/2^{24}$ |

### Table 5. Operating Mode Per $\overline{\text{STDBY}}$ Terminal

| $\overline{\text{STDBY}}$ | OPERATING MODE |
|---|---|
| 0 | Standby/programming mode – power down of all blocks |
| 1 | Operating mode and programming mode |

Two independent operating modes, Mode0 and Mode1, allow extremely fast switching between two preprogrammed settings by toggling the MODE terminal. Each mode can be viewed as a bank of configuration registers which store the frequency settings and the enable/disable settings for each functional block of the TRF5901. The MODE terminal is then used to asynchronously switch between Mode0 and Mode1 as shown in Figure 25. Several examples of operating sequences are shown in Table 6.

## PRINCIPLES OF OPERATION
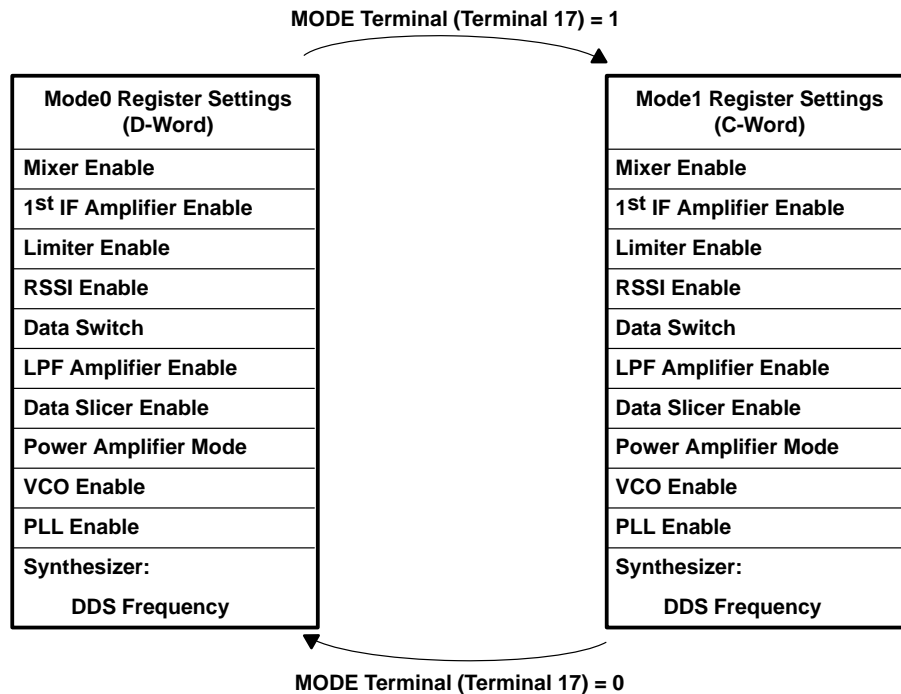
### operating modes (continued)

**MODE Terminal (Terminal 17) = 1**

| Mode0 Register Settings (D-Word) |
|---|
| Mixer Enable |
| 1st IF Amplifier Enable |
| Limiter Enable |
| RSSI Enable |
| Data Switch |
| LPF Amplifier Enable |
| Data Slicer Enable |
| Power Amplifier Mode |
| VCO Enable |
| PLL Enable |
| Synthesizer: DDS Frequency |

| Mode1 Register Settings (C-Word) |
|---|
| Mixer Enable |
| 1st IF Amplifier Enable |
| Limiter Enable |
| RSSI Enable |
| Data Switch |
| LPF Amplifier Enable |
| Data Slicer Enable |
| Power Amplifier Mode |
| VCO Enable |
| PLL Enable |
| Synthesizer: DDS Frequency |

**MODE Terminal (Terminal 17) = 0**

**Figure 25. Interaction Between MODE Terminal and Preprogrammed Mode0 and Mode1 Control Registers**

**Table 6. Operating Mode Examples**

| FUNCTION/DESCRIPTION | MODE0 | MODE1 |
|---|---|---|
| Receive polling with frequency hopping, or scan band | Receive on frequency 0 | Receive on frequency 1 |
| Transmit and receive on different frequencies | Transmit on frequency 0 | Receive on frequency 1 |
| Broadcast on one frequency and receive on another | Transmit on frequency 0 (broadcast channel) | Receive on frequency 1 |
| Rapid switch between receive and power saving mode (keep DDS/VCO running) | Receive on frequency 0 | All blocks off except DDS, VCO, and PLL |
| Emulate FSK transmit operation using the MODE terminal for wideband FSK | Transmit on frequency 0 | Transmit on frequency 0 + deviation |

# PRINCIPLES OF OPERATION

## operating modes (continued)

Figure 26 illustrates how the user of the TRF5901 can preload the serial control words while in standby/programming mode and then receive baseband data while in operating mode.
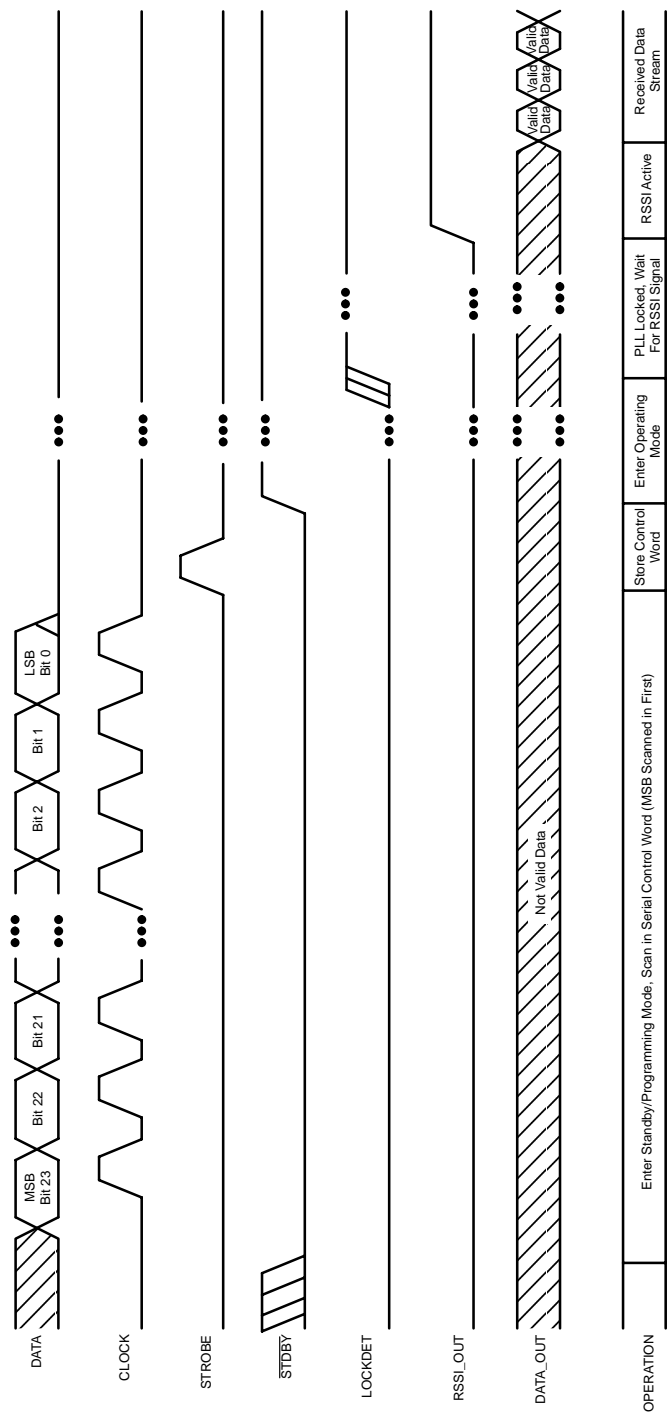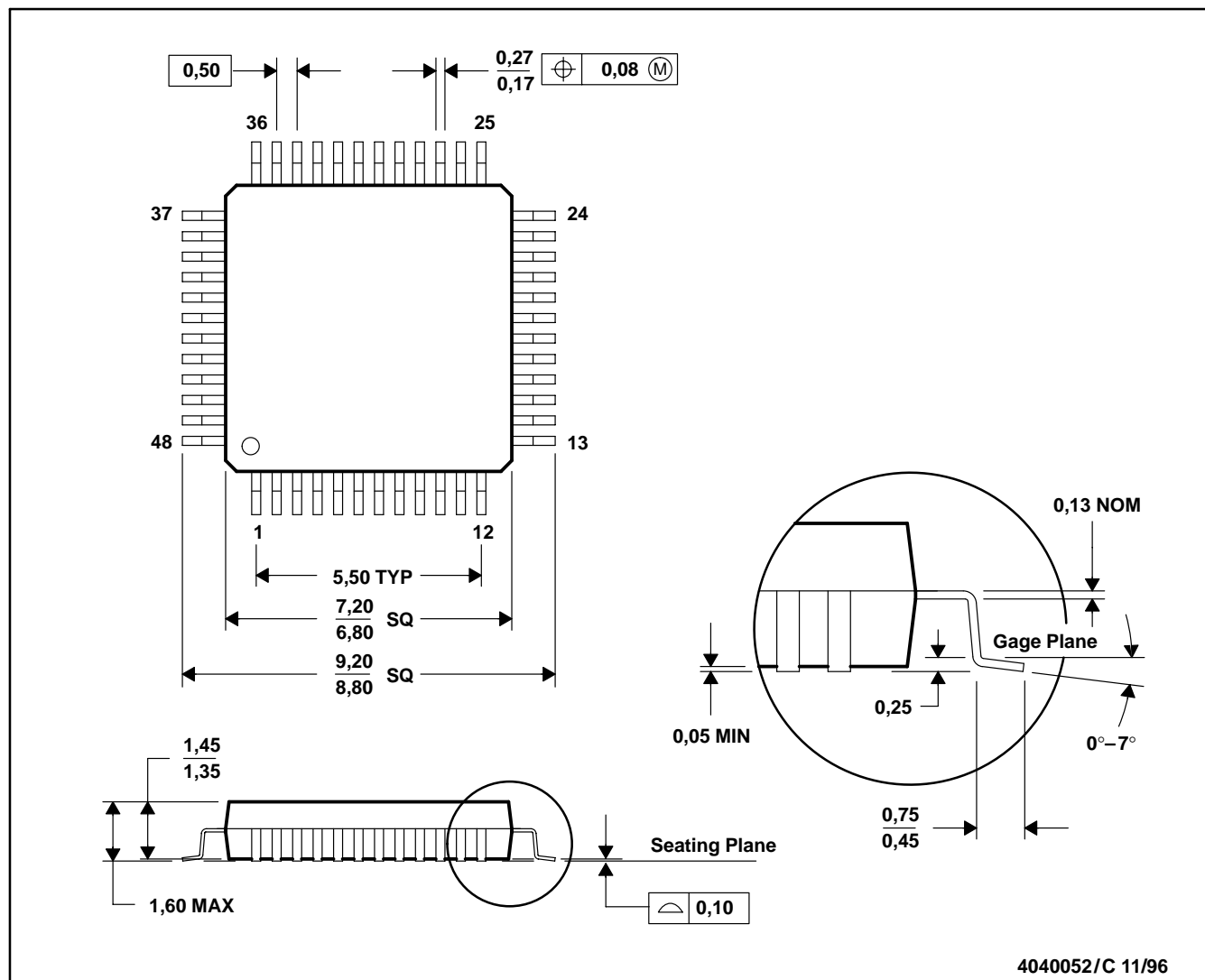


**Figure 26. Preloading Serial Control Word and Receiving Baseband Data**

## MECHANICAL DATA

**PT (S-PQFP-G48)**                                                    **PLASTIC QUAD FLATPACK**



4040052 / C 11/96

NOTES:  A.  All linear dimensions are in millimeters.
        B.  This drawing is subject to change without notice.
        C.  Falls within JEDEC MS-026
        D.  This may also be a thermally enhanced plastic package with leads connected to the die pads.

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

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