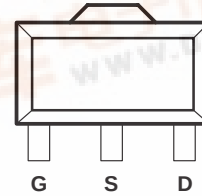


- **Wide Operating Frequency Range up to 1000 MHz**
- **High Output Power:**
 - Typical Value of 32 dBm at 4.8 V and 900 MHz
 - Typical Value of 29 dBm at 3.6 V and 900 MHz
- **High Gain:**
 - Typical Value of 9 dB at 4.8 V and 900 MHz at 32-dBm Output Power
- **High Power-Added Efficiency (PAE):**
 - Typical Value of 50% at 32-dBm Output Power
- **Low Cost**
- **Extremely Rugged:**
 - Sustains 20:1 Load Mismatch
- **Suitable for Various Wireless Applications**
- **Low Leakage Current <1 μ A**
- **SOT-89 Plastic Power Package**
- **1000 V Human Body Model ESD Protection on Gate and Drain**

PK PACKAGE
(TOP VIEW)



description

The TRF7003 power amplifier is a silicon, metal-oxide semiconductor, field-effect transistor (MOSFET) manufactured using the Texas Instruments RFMOS™ process. It is housed in a SOT-89 (PK) plastic power package. The TRF7003, suitable for a variety of wireless applications, has been characterized for global systems for mobile communications (GSM) power amplifier applications. The TRF7003, a rugged, low-cost device, operates from a single-polarity positive power supply and has low leakage current. Typical power output at 900 MHz is 32 dBm, with an associated power gain of 9 dB and 50-percent power-added efficiency (PAE).



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TRF7003

MOSFET POWER AMPLIFIER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Drain-source voltage, V_{DS}	15 V
Gate-source voltage, V_{GS}	7 V
Continuous drain current, I_D	2 A
Junction temperature, $T_{J\max}$	150°C
Thermal resistance, junction to case, $R_{\theta JC}$ (See Note 1)	10°C/W
Total device power dissipation at $T_C = 25^\circ\text{C}$	12.5 W
Derate above 25°C	100 mW/°C
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 100°C
ESD protection, gate and drain, human body model	1000 V

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: With infinite heatsink and no air flow

electrical characteristics over operating free-air temperature range (unless otherwise noted)

dc characteristics

PARAMETER	TEST CONDITIONS [‡]	LIMITS			UNITS
		MIN	TYP	MAX	
I_D Saturated drain current	$V_{DS} = 4.8\text{ V}$, $V_{GS} = 1.7\text{ V}$		0.7		A
g_m Transconductance	$V_{DS} = 4.8\text{ V}$, $V_{GS} = 1.7\text{ V}$		1000		mS
$V_{(TO)}$ Threshold voltage	$V_{DS} = 100\text{ mV}$, $I_{DS} = 1.5\text{ mA}$		1.0		V
$V_{(BR)sd}$ Source-drain breakdown voltage	$I_{ds} = 40\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$ Source is grounded		16		V
Leakage current	$V_{DS} = 4.8\text{ V}$, $V_{GS} = 0\text{ V}$		<1		μA

[‡] $T_A = 25^\circ\text{C}$

RF characteristics, $V_{DS} = 4.8\text{ V}$, $V_{GS} = 1.7\text{ V}$

PARAMETER	TEST CONDITIONS [§]	LIMITS			UNITS
		MIN	TYP	MAX	
Output power	Frequency = 900 MHz, $P_I = 23\text{ dBm}$	31	32		dBm
Power gain	Frequency = 900 MHz, $P_I = 23\text{ dBm}$		9		dB
η_{add} Power added efficiency	Frequency = 900 MHz, $P_I = 23\text{ dBm}$	45%	50%		
Ruggedness test	Frequency = 900 MHz, $P_I = 23\text{ dBm}$, Load VSWR = 20:1, All phase angles		¶		

[§] $T_A = 25^\circ\text{C}$, fixed matching circuit

¶ No degradation in output power after test.

TYPICAL CHARACTERISTICS

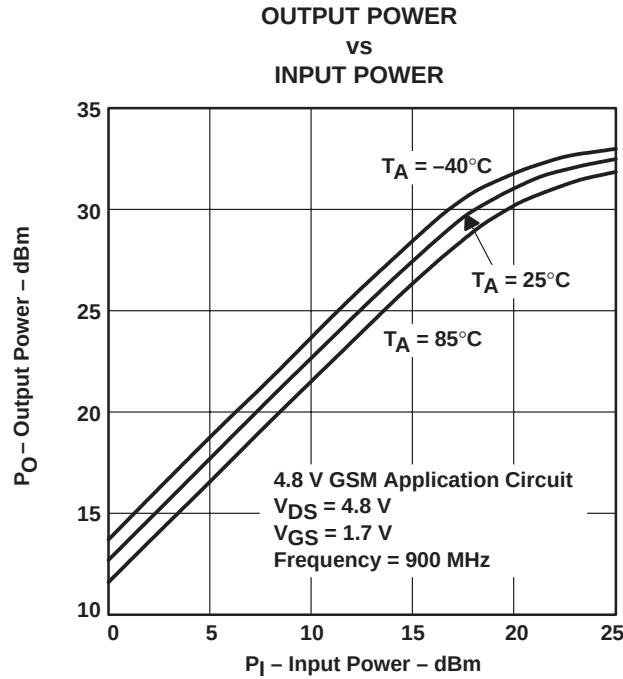


Figure 1

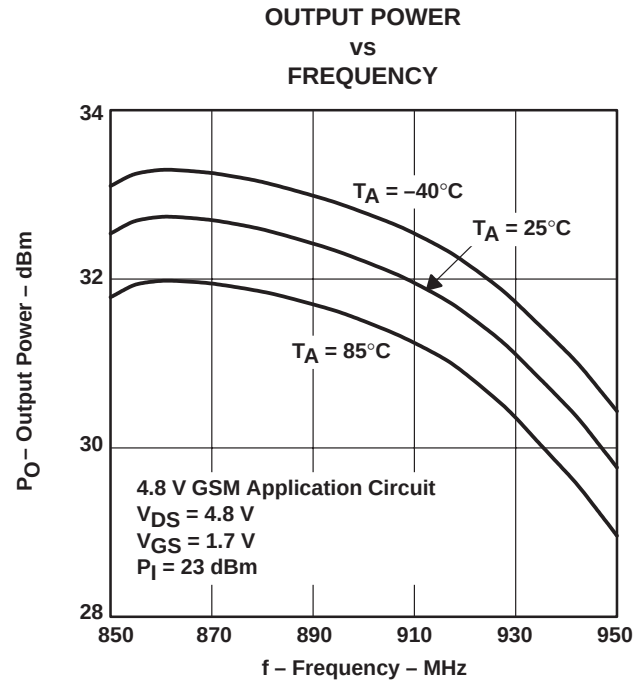


Figure 2

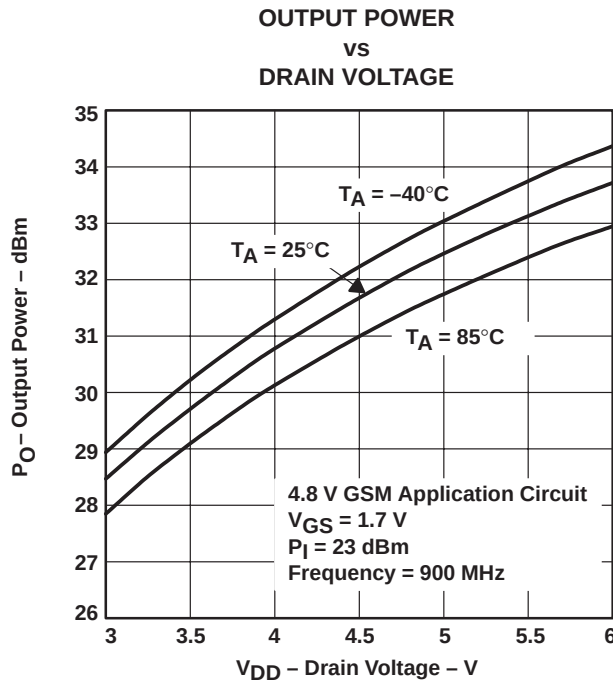


Figure 3

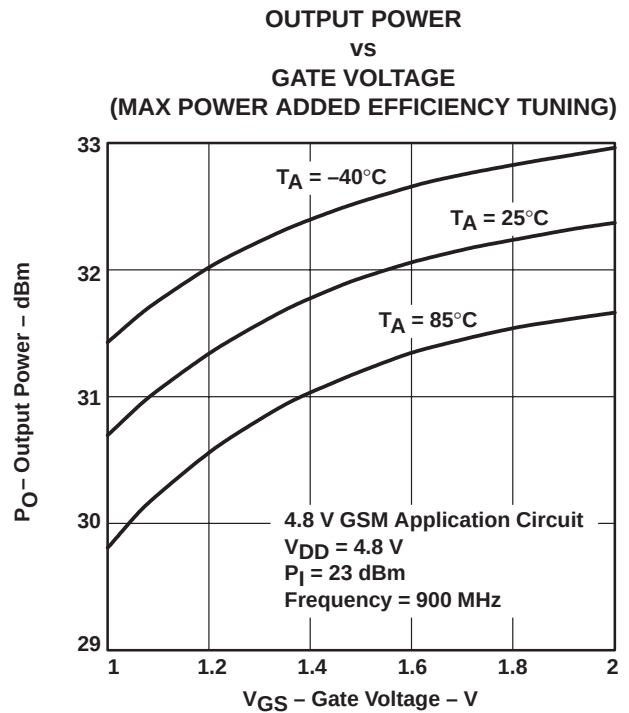


Figure 4

TRF7003
MOSFET POWER AMPLIFIER

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TYPICAL CHARACTERISTICS

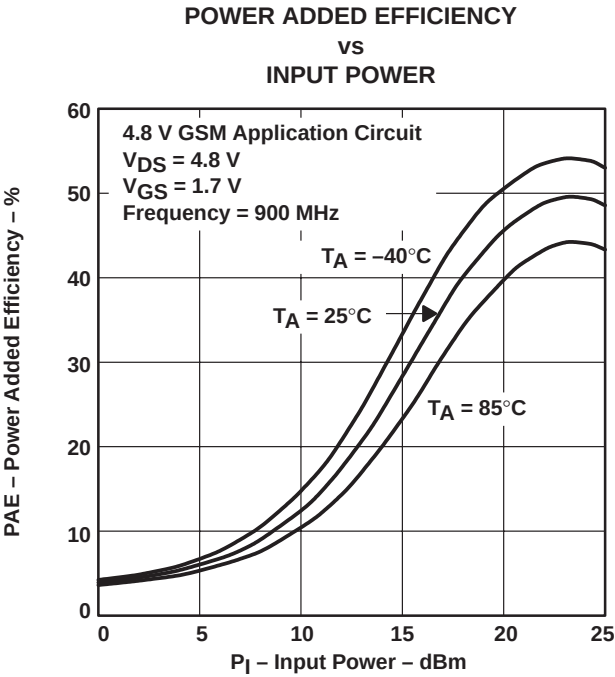


Figure 5

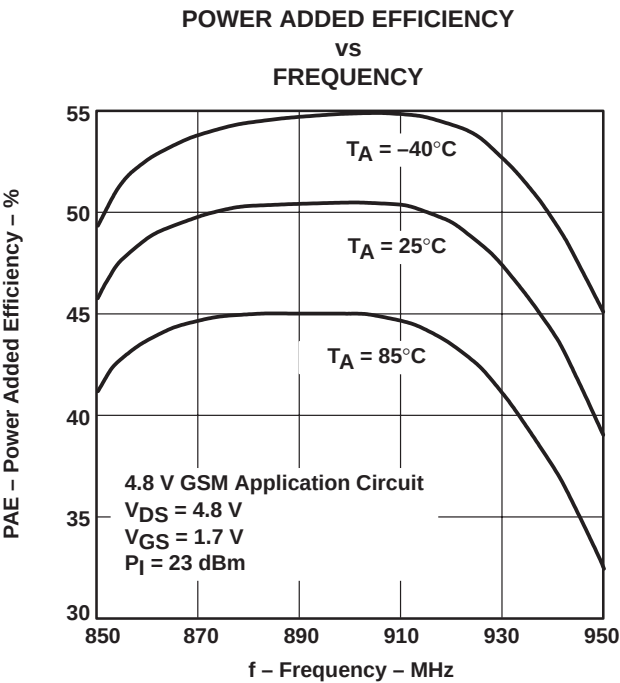


Figure 6

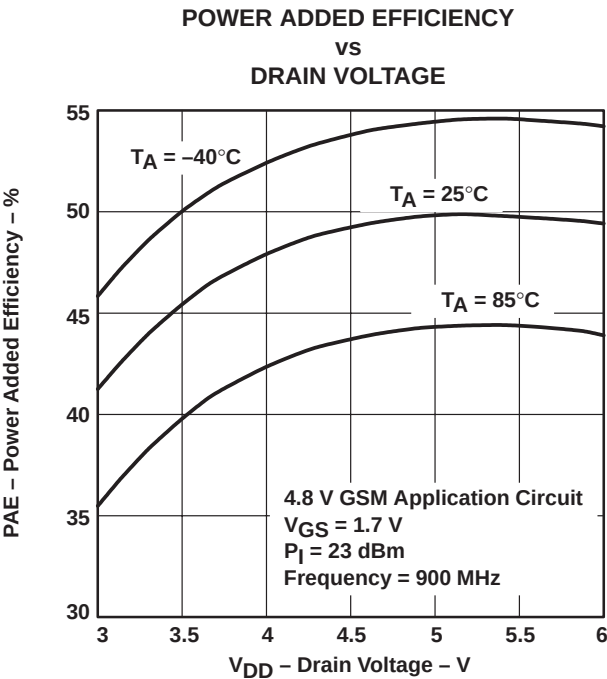


Figure 7

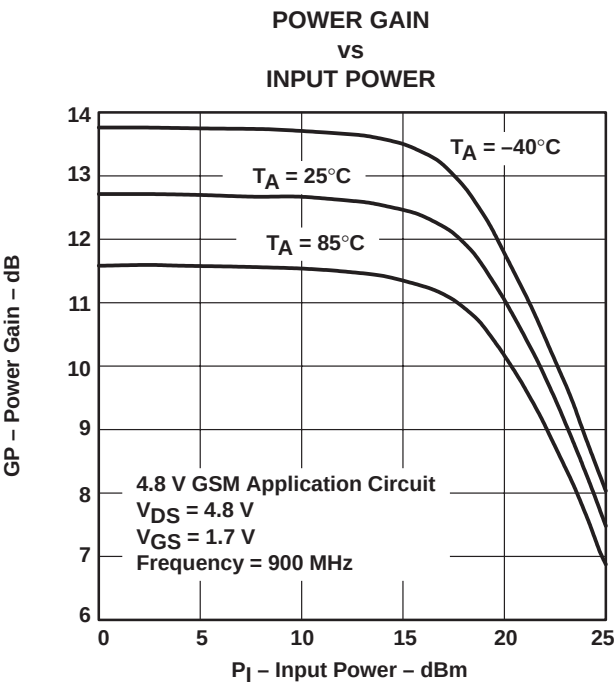


Figure 8

TYPICAL CHARACTERISTICS

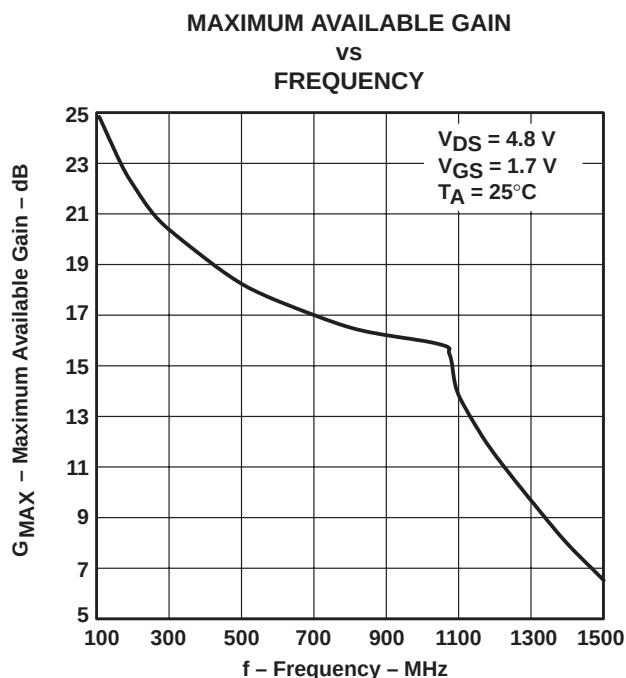


Figure 9

Table 1 lists the small signal scattering parameters of the TRF7003.

Table 1. Small Signal Scattering Parameters, $V_{DS} = 4.8\text{ V}$, $V_{GS} = 1.7\text{ V}$

FREQ MHz	S11 (MAG)	S11 (ANG)	S21 (MAG)	S21 (ANG)	S12 (MAG)	S12 (ANG)	S22 (MAG)	S22 (ANG)
100	0.87	-150.14	9.30	96.71	0.03	8.65	0.77	-166.79
200	0.87	-165.55	4.68	82.07	0.03	-4.19	0.79	-173.48
300	0.87	-171.34	3.06	71.95	0.03	-12.23	0.80	-175.44
400	0.88	-174.68	2.24	63.69	0.03	-18.69	0.82	-177.12
500	0.88	-177.12	1.74	56.64	0.03	-23.87	0.83	-178.14
600	0.89	179.25	1.40	49.46	0.02	-28.83	0.84	-179.71
700	0.89	178.67	1.15	43.07	0.02	-32.53	0.85	179.05
800	0.90	176.99	0.97	37.34	0.02	-36.07	0.86	177.34
900	0.91	175.01	0.83	32.10	0.02	-38.84	0.86	175.88
1000	0.91	173.15	0.71	26.71	0.02	-40.84	0.88	174.07
1100	0.91	171.29	0.62	21.52	0.02	-43.07	0.88	172
1200	0.91	169.46	0.55	16.99	0.02	-44.22	0.88	170.33
1300	0.91	167.47	0.48	12.40	0.01	-45.28	0.88	168.38
1400	0.91	165.25	0.43	7.64	0.01	-45	0.88	165.99
1500	0.90	163.33	0.39	3.76	0.01	-45	0.88	164.11

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The schematic diagram illustrates a 1.5-GHz CMOS differential amplifier designed for a 50-ohm input and output match. The circuit is centered around a differential pair of NMOS transistors, specifically the TRF7003 model. The gates of these transistors are connected to a common-mode gate voltage V_{GS} through a coupling capacitor $C6$. The drains are connected to a common-mode drain voltage V_{DS} through a coupling capacitor $C7$. A resistor $R1$ is connected between V_{DS} and the output node, and a capacitor $C8$ is connected from V_{DS} to ground. The source of the differential pair is connected to ground through an inductor $L1$. The input matching network consists of a series capacitor $C1$, followed by a 50-ohm transmission line segment with width $w = 22$ mils and length $l = 950$ mils, and then a shunt capacitor $C2$ to ground. The output matching network includes a series capacitor $C5$ followed by a 50-ohm transmission line segment with width $w = 22$ mils and length $l = 430$ mils, and then a shunt capacitor $C4$ to ground. The output is taken from the node after $C4$. The differential pair is biased by V_{GS} and V_{DS} sources, which are connected to the gates and drains respectively. The gates are also connected to ground through a capacitor $C6$, and the drains are connected to ground through a capacitor $C7$. The output is taken from the node after the final 50-ohm line segment and capacitor $C4$.

Figure 10. Recommended Application Circuit for 4.8-V GSM

Table 2. Component List

DESIGNATORS	DESCRIPTION	VALUE	MANUFACTURER [†]	MANUFACTURER P/N
C1	Capacitor	22 pF	ATC™	ATC100A220JP150X
C2	Capacitor	18 pF	ATC	ATC100A180JP150X
C3	Capacitor	16 pF	ATC	ATC100A160JP150X
C4	Capacitor	2.7 pF	ATC	ATC100A2R7CP150X
C5	Capacitor	100 pF	ATC	ATC100A101JP150X
C6	Capacitor	1 μF	MURATA	GRM220Y5V105Z010
C7	Capacitor	100 pF	ATC	ATC100A101JP150X
C8	Capacitor	1 μF	MURATA	GRM220Y5V105Z010
R1	Resistor	30 Ω	International Manufacturing Services	RCI-0402-30ROJ
L1	Inductor	15 nH	TOKO	LL2012-F15NK

ATC is a trademark of American Technical Ceramics Corporation

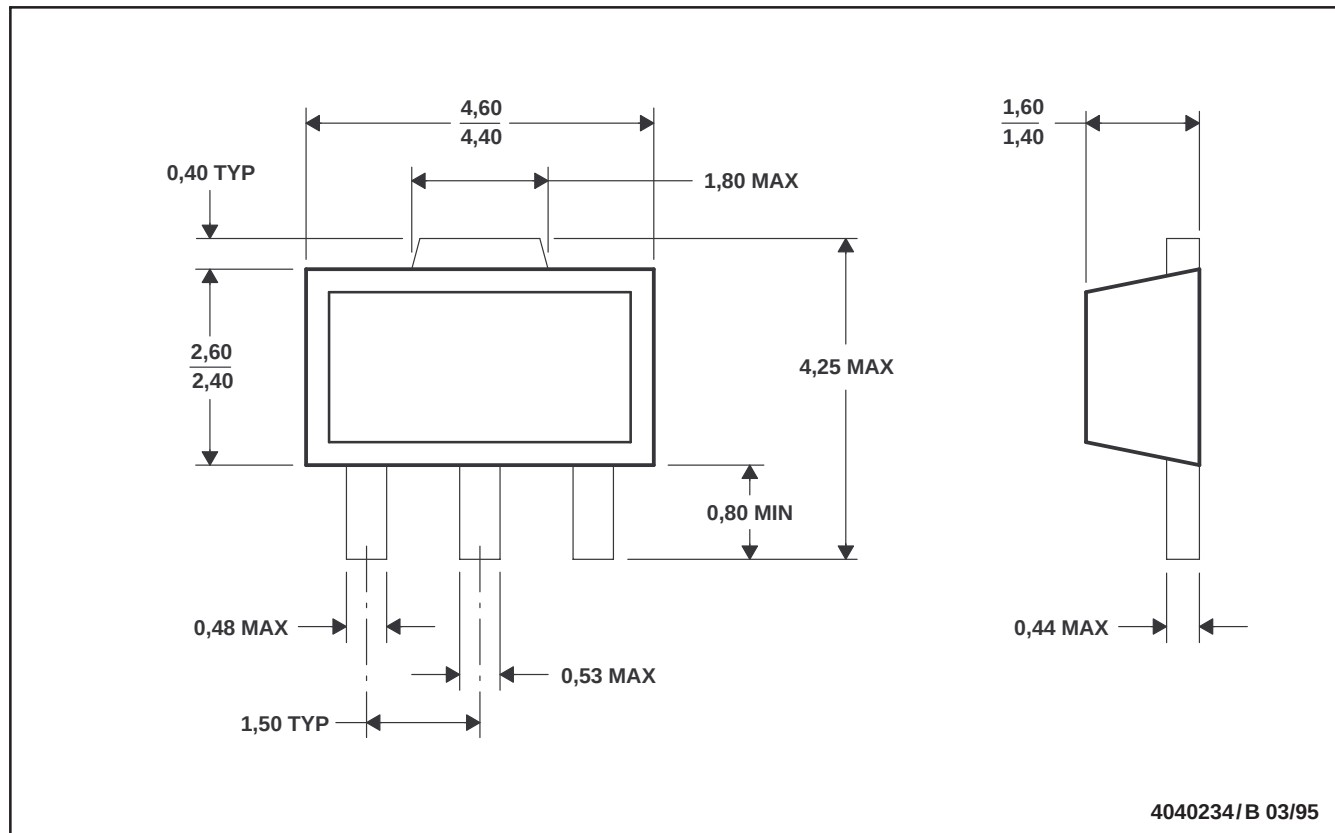
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MECHANICAL DATA

PK (R-PSSO-F3)

PLASTIC SINGLE-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.

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