

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288 WORDS × 8 BIT STATIC RAM

DESCRIPTION

The TC554001AFI/AFTI/ATRI is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5V ± 10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 10mA/MHz(typ) and minimum cycle time of 70 ns. It is automatically placed in low-power mode at 2 μA standby current (typ) when chip enable (CE) is asserted high. There are two control inputs. CE is used to select the device and for data retention control, and output enable (OE) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of -40° to 85°C, the TC554001AFI/AFTI/ATRI can be used in environments exhibiting extreme temperature conditions. The TC554001AFI/AFTI/ATRI is available in a standard plastic 32-pin small-outline package(SOP) and normal and reverse pinout plastic 32-pin thin-small-outline package(TSOP).

FEATURES

- Low-power dissipation
Operating: 55 mW/MHz (typical)
- Single power supply voltage of 5 V ± 10 %
- Power down features using CE
- Data retention supply voltage of 2.0 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of -40° to 85°C
- Standby Current (maximum) :

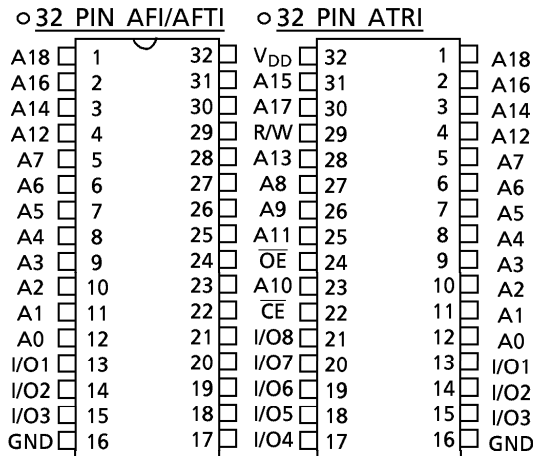
	TC554001AFI/AFTI/ATRI	
	-70, -85, -10	-75L, -85L, -10L
5.5V	200 μA	100 μA
3.0V	100 μA	50 μA

- Access Time (maximum)

	TC554001AFI/AFTI/ATRI		
	-70, -70L	-85, -85L	-10, -10L
Access Time	70 ns	85 ns	100 ns
CE Access Time	70 ns	85 ns	100 ns
OE Access Time	35 ns	45 ns	50 ns

- Package:
SOP32-P-525-1.27 (AFI) (Weight: g typ)
TSOP II 32-P-400-1.27 (AFTI) (Weight: g typ)
TSOP II 32-P-400-1.27A (ATRI) (Weight: g typ)

PIN ASSIGNMENT (TOP VIEW)



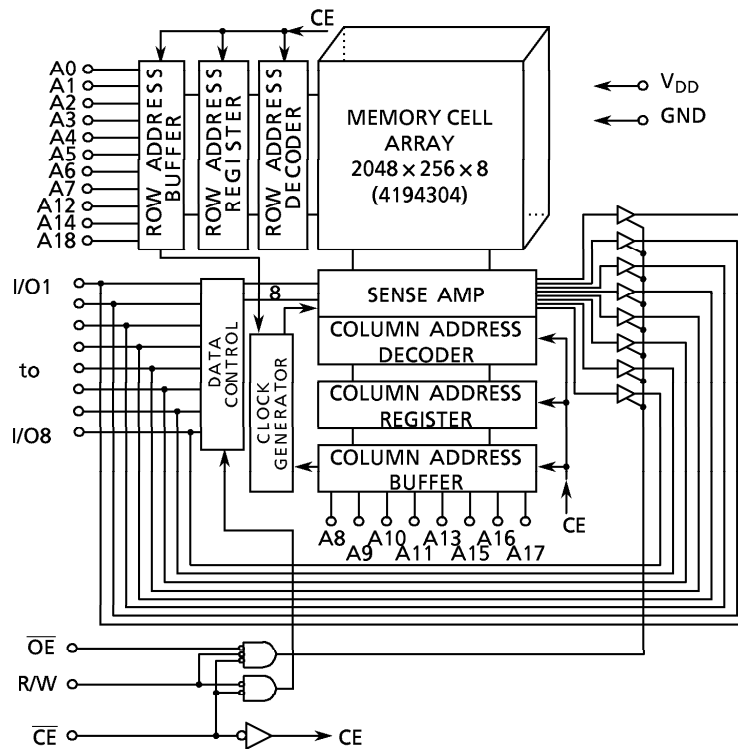
PIN NAMES

A0 to A18	Address Inputs
R/W	Read/Write Control
OE	Output Enable
CE	Chip Enable
I/O1 to I/O8	Data Input/Output
V _{DD}	Power (+ 5 V)
GND	Ground

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BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	CE	OE	R/W	I/O1 to I/O8	POWER
Read	L	L	H	D _{OUT}	I _{DDO}
Write	L	x	L	D _{IN}	I _{DDO}
Output Disabled	L	H	H	High-Z	I _{DDO}
Standby	H	x	x	High-Z	I _{DDs}

Note: X = don't care. H = logic high. L = logic low.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	- 0.3 to 7.0	V
V _{IN}	Input Voltage	- 0.3* to 7.0	V
V _{I/O}	Input and Output Voltage	- 0.5 to V _{DD} + 0.5	V
P _D	Power Dissipation	0.6	W
T _{solder}	Soldering Temperature (10 s)	260	°C
T _{strg.}	Storage Temperature	- 55 to 150	°C
T _{opr.}	Operating Temperature	- 40 to 85	°C

* - 3.0 V when measured at a pulse width of 50 ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = -40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.4	-	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	- 0.3*	-	0.6	V
V _{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

* - 3.0 V when measured at a pulse width of 50 ns

DC CHARACTERISTICS (Ta = -40° to 85°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT	
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}		-	-	± 1.0	μA	
I _{OH}	Output High Current	V _{OH} = 2.4 V		- 1.0	-	-	mA	
I _{OL}	Output Low Current	V _{OL} = 0.4 V		2.1	-	-	mA	
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V _{IL} or $\overline{OE} = V_{IH}$ V _{OUT} = 0 V to V _{DD}		-	-	± 1.0	μA	
I _{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ and R/W = V _{IH} I _{OUT} = 0 mA Other Inputs = V _{IH} /V _{IL}	Tcycle	min	-	-	70	mA
				1 μs	-	15	-	
I _{DDO2}	Operating Current	$\overline{CE} = 0.2$ V and R/W = V _{DD} - 0.2 V I _{OUT} = 0 mA Other Inputs = V _{DD} - 0.2 V/0.2 V	Tcycle	min	-	-	60	mA
				1 μs	-	10	-	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$		-	-	3	mA	
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2$ V V _{DD} = 2.0 to 5.5 V	-70, -85, -10	Ta = 25°C	-	2		-
				Ta = -40° to 85°C	-	-		200
		-70L, -85L, -10L	Ta = 25°C	-	2	5		
			Ta = -40° to 85°C	-	-	100	μA	

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 5\text{V} \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC554001AFI/AFTI/ATRI						UNIT
		-70, -70L		-85, -85L		-10, -10L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	70	-	85	-	100	-	ns
t_{ACC}	Address Access Time	-	70	-	85	-	100	
t_{CO}	Chip Enable Access Time	-	70	-	85	-	100	
t_{OE}	Output Enable Access Time	-	35	-	45	-	50	
t_{COE}	Chip Enable Low to Output Active	5	-	5	-	5	-	
t_{OEE}	Output Enable Low to Output Active	0	-	0	-	0	-	
t_{OD}	Chip Enable High to Output High-Z	-	30	-	35	-	40	
t_{ODO}	Output Enable High to Output High-Z	-	30	-	35	-	40	
t_{OH}	Output Data Hold Time	10	-	10	-	10	-	

WRITE CYCLE

SYMBOL	PARAMETER	TC554001AFI/AFTI/ATRI						UNIT
		-70, -70L		-85, -85L		-10, -10L		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	70	-	85	-	100	-	ns
t_{WP}	Write Pulse Width	50	-	55	-	60	-	
t_{CW}	Chip Enable to End of Write	60	-	70	-	80	-	
t_{AS}	Address Setup Time	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{ODW}	R/W Low to Output High-Z	-	30	-	35	-	40	
t_{OEW}	R/W Hige to Output Active	0	-	0	-	0	-	
t_{DS}	Data Setup Time	30	-	35	-	40	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

AC TEST CONDITIONS

Output Load: 100 pF + one TTL gate

Input Pulse Level: 0.4 V, 2.6 V

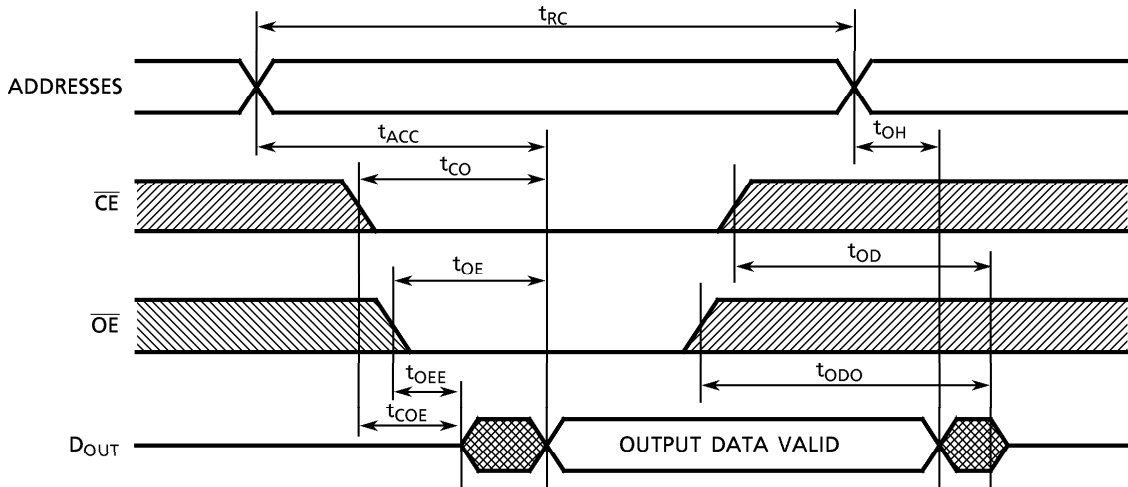
Timing Measurements: 1.5 V

Reference Level: 1.5 V

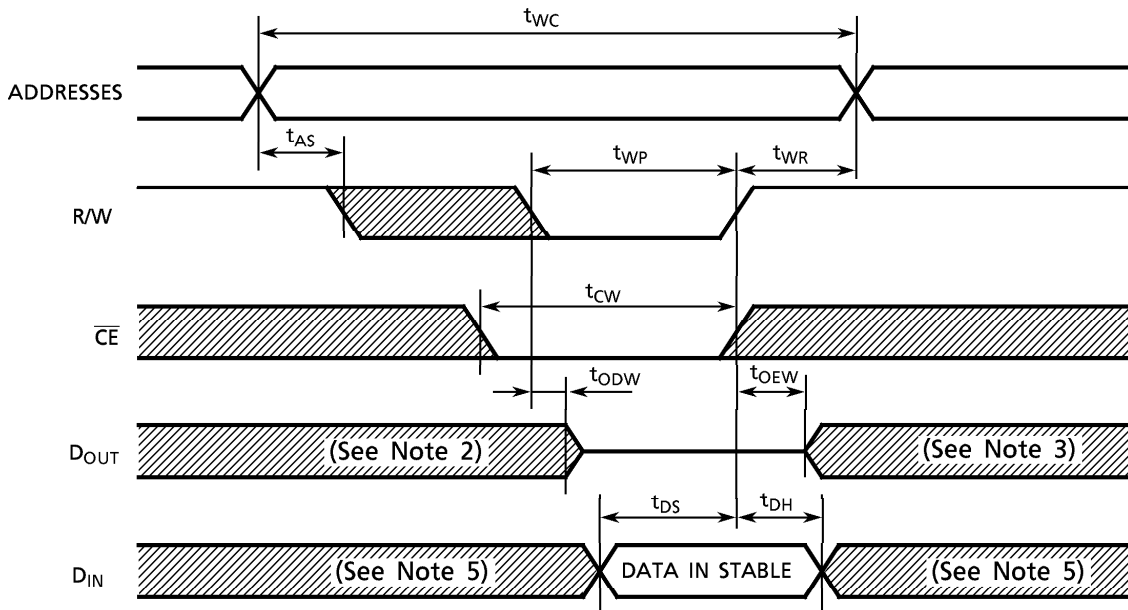
t_r, t_f : 5 ns

TIMING WAVEFORMS

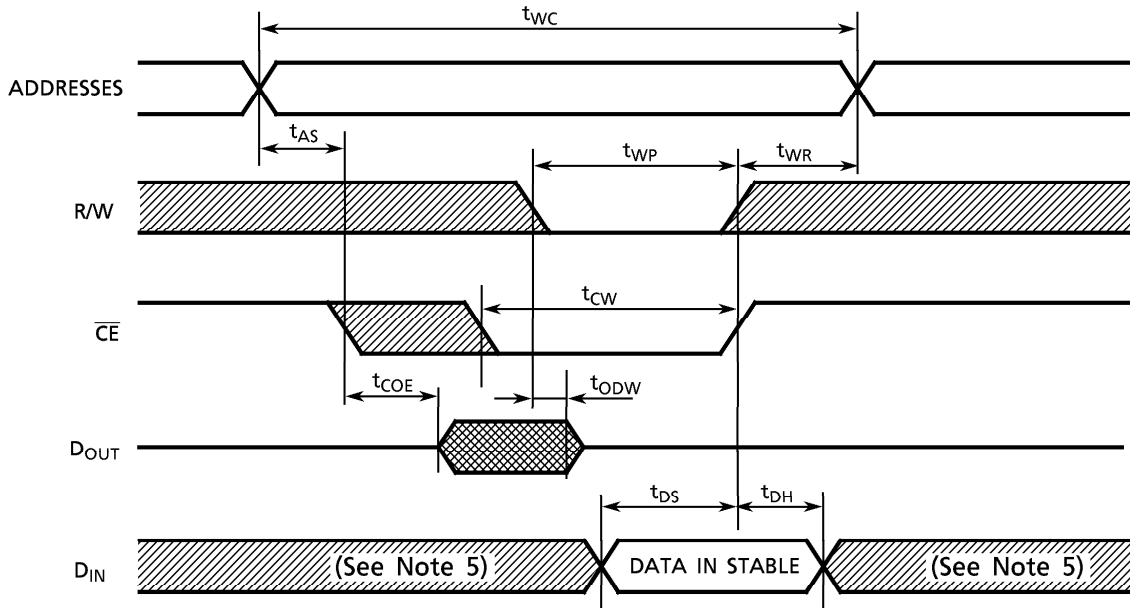
READ CYCLE (See Note 1)



WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 (\overline{CE} CONTROLLED) (See Note 4)



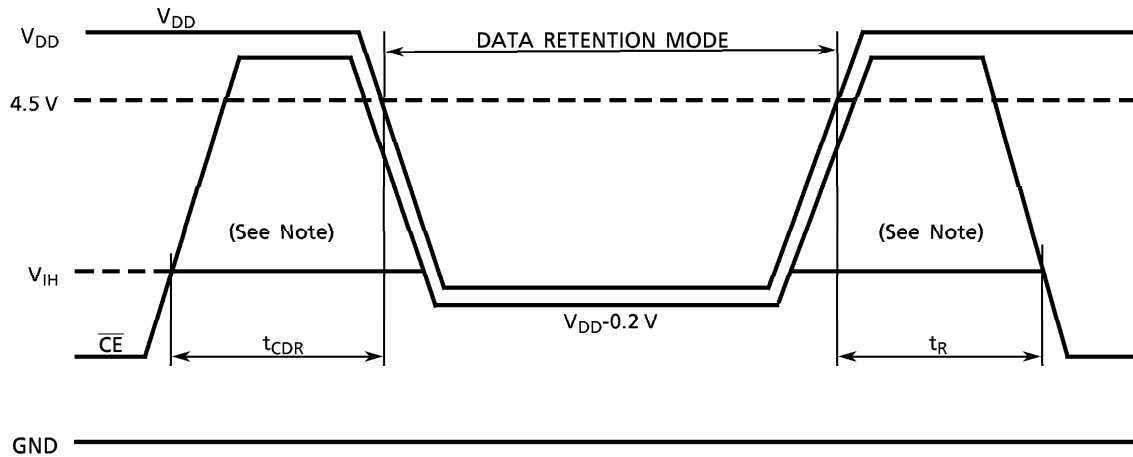
- (1) R/W remains High for Read Cycle.
- (2) If \overline{CE} goes coincident with or after R/W goes LOW, the output will remain at high impedance.
- (3) If \overline{CE} goes HIGH coincident with or before R/W goes HIGH, the output will remain at high impedance.
- (4) IF \overline{CE} is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	
V _{DH}	Data Retention Supply Voltage		2.0	-	5.5	V	
I _{DD52}	Standby Current	-70, -85, -10	V _{DH} = 3.0 V	-	-	100	μA
			V _{DH} = 5.5 V	-	-	200	
		-70L, -85L, -10L	V _{DH} = 3.0 V	-	-	50*	
			V _{DH} = 5.5 V	-	-	100	
t _{CDR}	Chip Deselect to Data Retention Mode Time		0	-	-	nS	
t _R	Recovery Time		5	-	-	mS	

* 5 μA (max) at Ta = -40° to 40°C

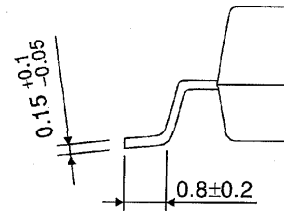
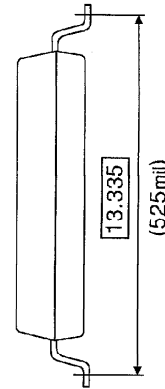
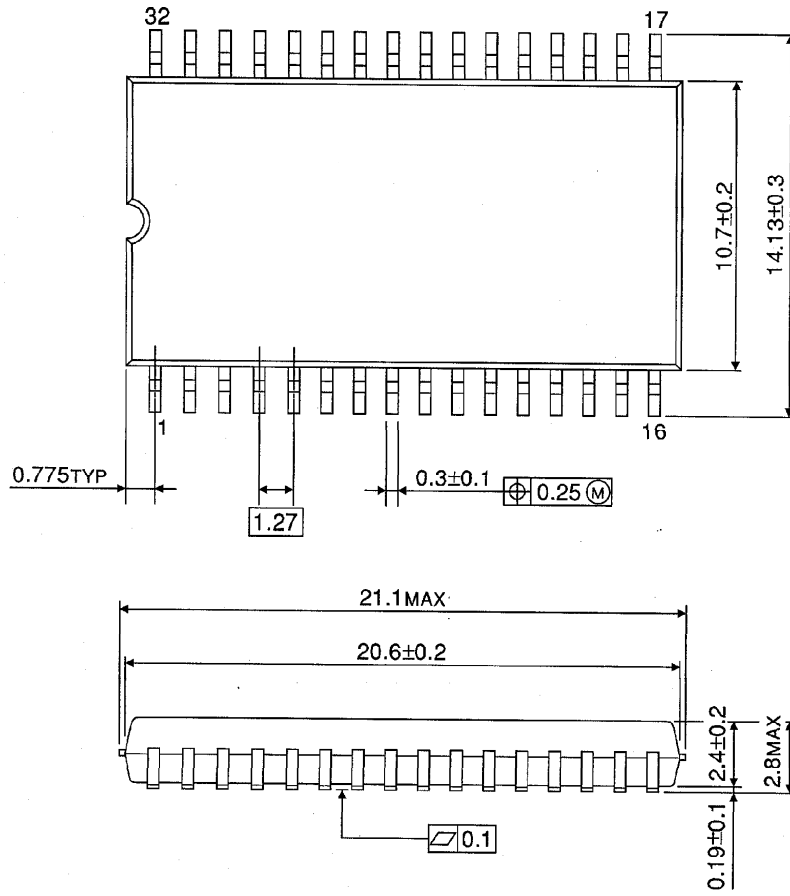
CE Controlled Data Retention Mode



Note: When \overline{CE} is operating at the V_{IH} level (2.4V), the standby current is given by I_{DD51} during the transition of V_{DD} from 4.5 to 2.6V.

PACKAGE DIMENSIONS (SOP32-P-525-1.27)

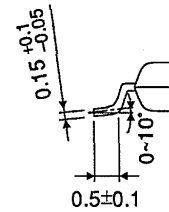
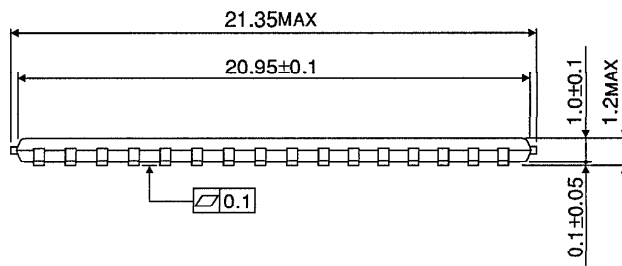
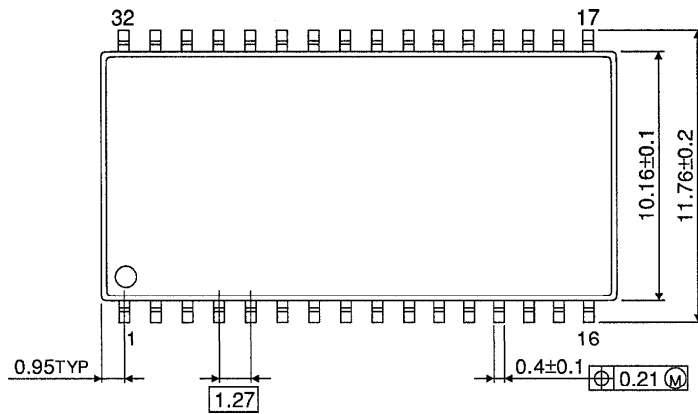
Unit in mm



Weight: g (typ)

PACKAGE DIMENSIONS (TSOPII 32-P-400-1.27)

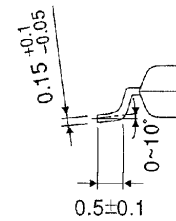
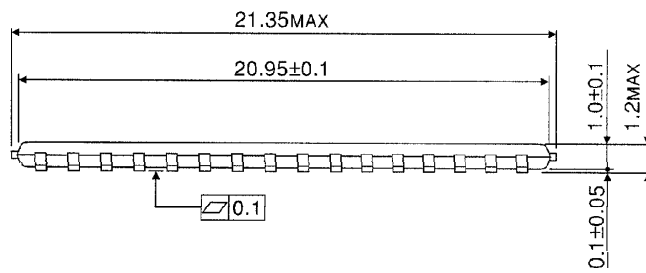
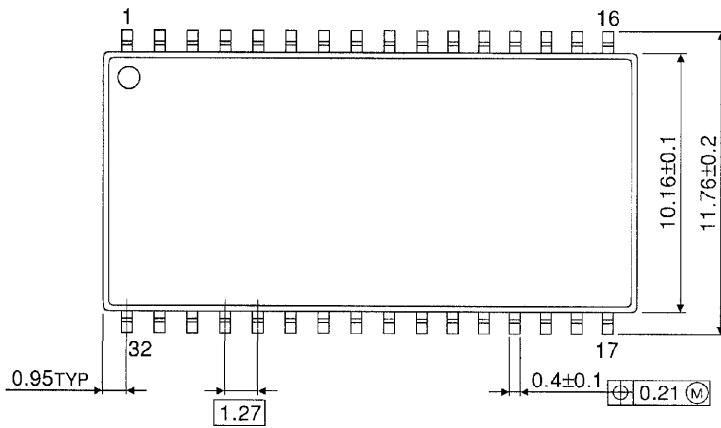
Unit in mm



Weight: g (typ)

PACKAGE DIMENSIONS (TSOPII 32-P-400-1.27A)

Unit in mm



Weight: g (typ)

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