TS3A5017
14-Ω DUAL SP4T ANALOG SWITCH
3.3-V/2.5-V DUAL 4:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

SCDS188 – JANUARY 2005

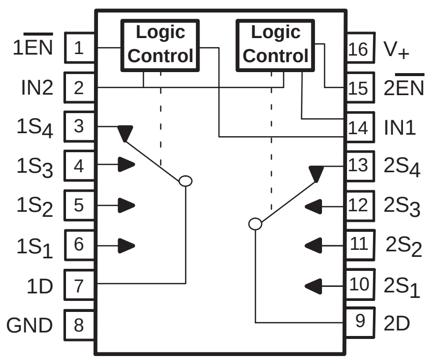
Description

The TS3A5017 is a dual single-pole quadruple-throw (4:1) analog switch that is designed to operate from 2.3 V to 3.6 V. This device can handle both digital and analog signals, and signals up to V_+ can be transmitted in either direction.

Applications

- **Sample-and-Hold Circuit**
- **Battery-Powered Equipment**
- **Audio and Video Signal Routing**
- **Communication Circuits**

SOIC, SSOP, TSSOP, OR TVSOP PACKAGE (TOP VIEW)



FUNCTION TABLE

$\overline{EN}$	IN2	IN1	D TO S S TO D
L	L	L	D = S_1
L	L	H	D = S_2
L	H	L	D = S_3
L	H	H	D = S_4
H	X	X	OFF

Features

- **Isolation in the Powered-Down Mode, $V_+ = 0$**
- **Low ON-State Resistance (10 Ω)**
- **Low Charge Injection**
- **Excellent ON-State Resistance Matching**
- **Low Total Harmonic Distortion (THD)**
- **2.3-V to 3.6-V Single-Supply Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

Summary of Characteristics

$V_+ = 3.3$ V, $T_A = 25°C$

Configuration	Dual Analog MUX/DEMUX (4:1 MUX/DEMUX)
Number of channels	2
ON-state resistance (r_{on})	11 Ω
ON-state resistance match (Δr_{on})	1 Ω
ON-state resistance flatness ($r_{on(flat)}$)	7 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	5 ns/1.5 ns
Charge injection (Q_C)	5 pC
Bandwidth (BW)	165 MHz
OFF isolation (O_{ISO})	−48 dB at 10 MHz
Crosstalk (X_{TALK})	−49 dB at 10 MHz
Total harmonic distortion (THD)	0.21%
Leakage current ($I_{D(OFF)}/I_{S(OFF)}$)	±0.1 μA
Power-supply current (I_+)	2.5 μA
Package option	16-pin SOIC, SSOP, TSSOP, or TVSOP

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	TS3A5017RGYR	YA017
	SOIC − D	Tube	TS3A5017D	TS3A5017
		Tape and reel	TS3A5017DR	
	SSOP (QSOP) − DBQ	Tape and reel	TS3A5017DBQR	YA017
	TSSOP − PW	Tube	TS3A5017PW	YA017
		Tape and reel	TS3A5017PWR	
	TVSOP − DGV	Tape and reel	TS3A5017DGVR	YA017

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Absolute Minimum and Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		−0.5	4.6	V
V_S, V_D	Analog voltage range(3)(4)		−0.5	4.6	V
I_K	Analog port diode current	V_S, V_D < 0	−50		mA
I_S, I_D	On-state switch current	V_S, V_D = 0 to 7 V	−128	128	mA
V_I	Digital input voltage range(3)(4)		−0.5	4.6	V
I_{IK}	Digital input clamp current	V_I < 0	−50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		−100		mA
θ_{JA}	Package thermal impedance(5)	D package		73	°C/W
		DB package		82	
		DGV package		120	
		DW package		108	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 3.3-V Supply(1)

V_+ = 3 V to 3.6 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_D, V_S					0		V_+	V
ON-state resistance	r_{on}	$0 \le V_S \le V_+$, I_D = −32 mA,	Switch ON, See Figure 13	25°C	3 V		11	12	Ω
				Full				14	
ON-state resistance match between channels	Δr_{on}	V_S = 2.1 V, I_D = −32 mA,	Switch ON, See Figure 13	25°C	3 V		1	2	Ω
				Full				3	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_S \le V_+$, I_D = −32 mA,	Switch ON, See Figure 13	25°C	3 V		7	9	Ω
				Full				10	
S OFF leakage current	$I_{S(OFF)}$	V_S = 1 V, V_D = 3 V, or V_S = 3 V, V_D = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	−0.1	0.05	0.1	μA
				Full		−0.2		0.2	
	$I_{SPWR(OFF)}$	V_S = 0 to 3.6 V, V_D = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	−1	0.5	1	
				Full		−5		5	
D OFF leakage current	$I_{D(OFF)}$	V_D = 1 V, V_S = 3 V, or V_D = 3 V, V_S = 3 V,	Switch OFF, See Figure 14	25°C	3.6 V	−0.1	0.05	0.1	μA
				Full		−0.2		0.2	
	$I_{DPWR(OFF)}$	V_D = 0 to 3.6 V, V_S = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	−1	0.5	1	
				Full		−5		5	
S ON leakage current	$I_{S(ON)}$	V_S = 1 V, V_D = Open, or V_S = 3 V, V_D = Open,	Switch ON, See Figure 15	25°C	3.6 V	−0.1	0.05	0.1	μA
				Full		−0.2		0.2	
D ON leakage current	$I_{D(ON)}$	V_D = 1 V, V_S = Open, or V_D = 3 V, V_S = Open,	Switch ON, See Figure 15	25°C	3.6 V	−0.1	0.05	0.1	μA
				Full		−0.2		0.2	
Digital Control Inputs (IN1, IN2, $\overline{EN}$)(2)									
Input logic high	V_{IH}			Full		2		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	−1	0.05	1	μA
				Full		−1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 3.3-V Supply(1) (continued)

V_+ = 3 V to 3.6 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_D = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	1	5	9.5	ns
				Full	3 V to 3.6 V	1		10.5	
Turn-off time	t_{OFF}	V_D = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	0.5	1.5	3.5	ns
				Full	3 V to 3.6 V	0.5		4.5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0 C_L = 0.1 nF,	See Figure 22	25°C	3.3 V		5		pC
S OFF capacitance	$C_{S(OFF)}$	V_S = V_+ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		19		pF
D OFF capacitance	$C_{D(OFF)}$	V_D = V_+ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		4.5		pF
S ON capacitance	$C_{S(ON)}$	V_S = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		25		pF
D ON capacitance	$C_{D(ON)}$	V_D = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		25		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	3.3 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	3.3 V		165		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	3.3 V		−48		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	3.3 V		−49		dB
Crosstalk Adjacent	$X_{TALK(ADJ)}$	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 21	25°C	3.3 V		−74		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 23	25°C	3.3 V		0.21		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		2.5	7	µA
				Full				10	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 2.5-V Supply(1)

V_+ = 2.3 V to 2.7 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_D, V_S					0		V_+	V
ON-state resistance	r_{on}	$0 \le V_S \le V_+$, I_D = −24 mA,	Switch ON, See Figure 13	25°C	2.3 V		20.5	22	Ω
				Full				24	
ON-state resistance match between channels	Δr_{on}	V_S = 1.6 V, I_D = −24 mA,	Switch ON, See Figure 13	25°C	2.3 V		1	2	Ω
				Full				3	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_S \le V_+$, I_D = −24 mA,	Switch ON, See Figure 13	25°C	2.3 V		16	18	Ω
				Full				20	
S OFF leakage current	$I_{S(OFF)}$	V_S = 0.5 V, V_D = 2.2 V, or V_S = 2.2 V, V_D = 0.5 V,	Switch OFF, See Figure 14	25°C	2.7 V	−0.1	0.05	0.1	µA
				Full		−0.2		0.2	
	$I_{SPWR(OFF)}$	V_S = 0 to 3.6 V, V_D = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	−1	0.5	1	
				Full		−5		5	
D OFF leakage current	$I_{D(OFF)}$	V_D = 0.5 V, V_S = 2.2 V, or V_D = 2.2 V, V_S = 0.5 V,	Switch OFF, See Figure 14	25°C	2.7 V	−0.1	0.05	0.1	µA
				Full		−0.2		0.2	
	$I_{DPWR(OFF)}$	V_D = 0 to 5.5 V, V_S = 5.5 V to 0,	Switch OFF, See Figure 14	25°C	0 V	−1	0.5	1	
				Full		−5		5	
S ON leakage current	$I_{S(ON)}$	V_S = 0.5 V, V_D = Open, or V_S = 2.2 V, V_D = Open,	Switch ON, See Figure 15	25°C	2.7 V	−0.1	0.05	0.1	µA
				Full		−0.2		0.2	
D ON leakage current	$I_{D(ON)}$	V_D = 0.5 V, V_S = Open, or V_D = 2.2 V, V_S = Open,	Switch ON, See Figure 15	25°C	2.7 V	−0.1	0.05	0.1	µA
				Full		−0.2		0.2	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1.7		5.5	V
Input logic low	V_{IL}			Full		0		0.7	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V	−1	0.05	1	µA
				Full		−1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 2.5-V Supply[1] (continued)

V_+ = 2.3 V to 2.7 V, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_D = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	1.5	5	8	ns
				Full	2.3 V to 2.7 V	1		10	
Turn-off time	t_{OFF}	V_D = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	0.3	2	4.5	ns
				Full	2.3 V to 2.7 V	0.3		6	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0 C_L = 0.1 nF,	See Figure 22	25°C	2.5 V				pC
S OFF capacitance	$C_{S(OFF)}$	V_S = V_+ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		18.5		pF
D OFF capacitance	$C_{D(OFF)}$	V_D = V_+ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		45		pF
S ON capacitance	$C_{NC(ON)}$	V_S = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		24		pF
D ON capacitance	$C_{D(ON)}$	V_D = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		24		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	2.5 V		2		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	2.5 V		165		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	2.5 V		−48		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	2.5 V		−49		dB
Crosstalk Adjacent	$X_{TALK(ADJ)}$	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 21	25°C	3.3 V		−74		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 23	25°C	2.5 V		0.29		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		2.5	7	µA
				Full				10	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

TYPICAL PERFORMANCE

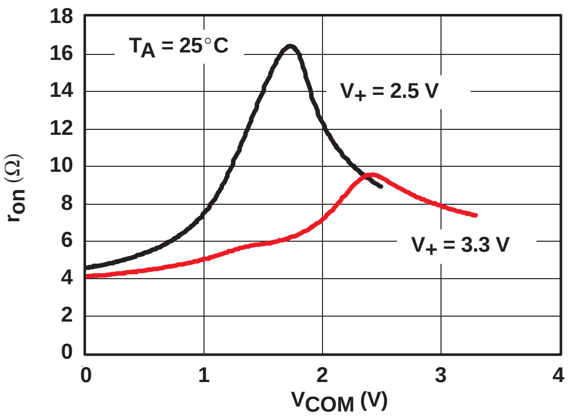


Figure 1. r_{on} vs V_{COM}

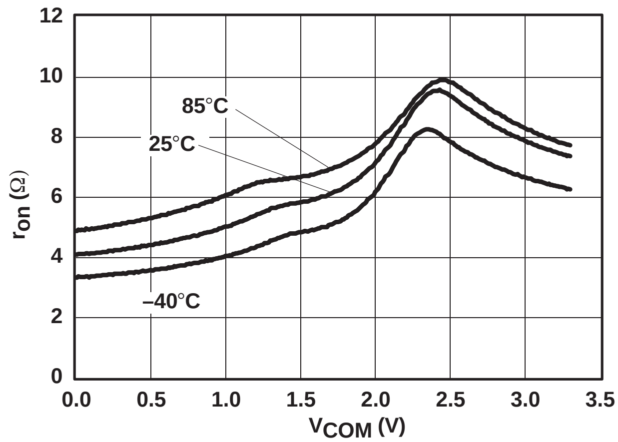


Figure 2. r_{on} vs V_{COM} (V_+ = 3.3 V)

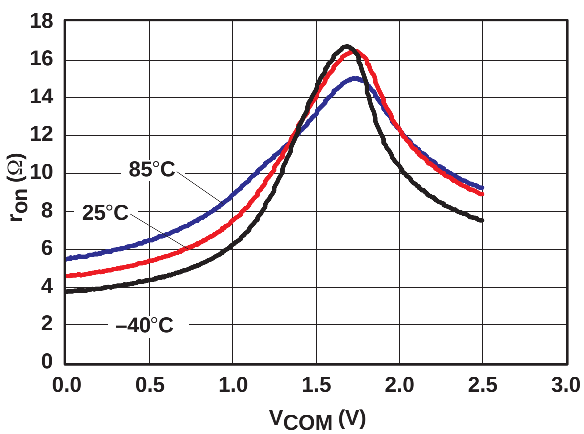


Figure 3. r_{on} vs V_{COM} (V_+ = 5 V)

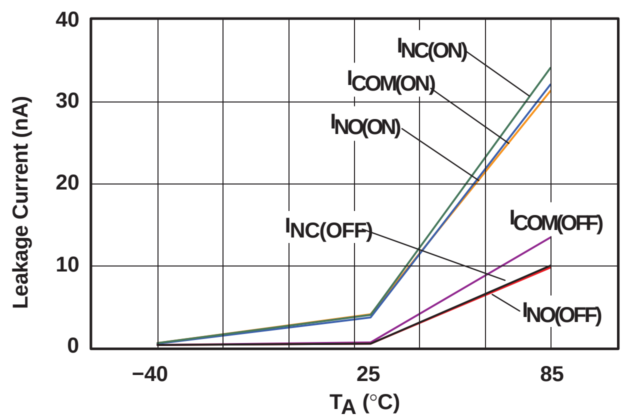


Figure 4. Leakage Current vs Temperature (V_+ = 5.5 V)

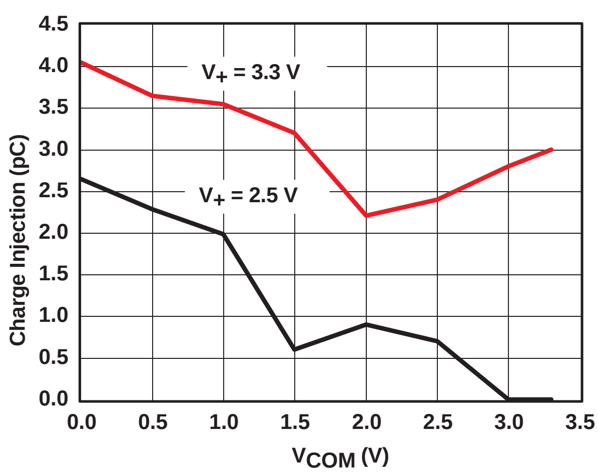


Figure 5. Charge-Injection (Q_C) vs V_{COM}

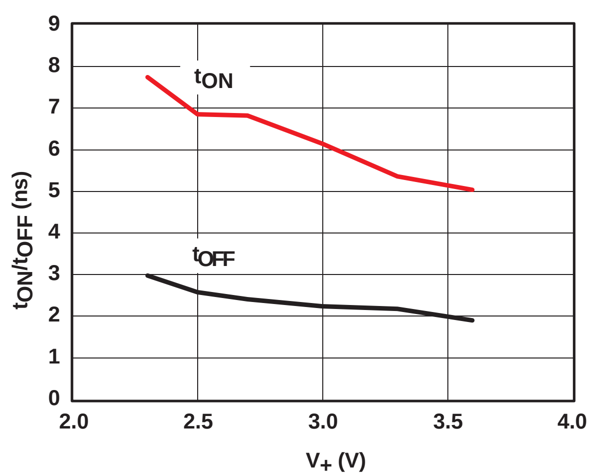


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

TYPICAL PERFORMANCE

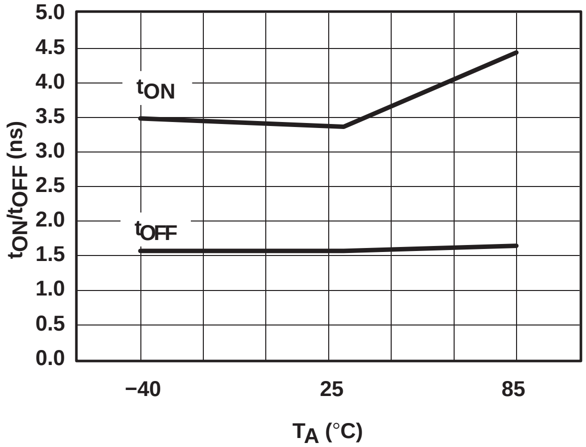


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

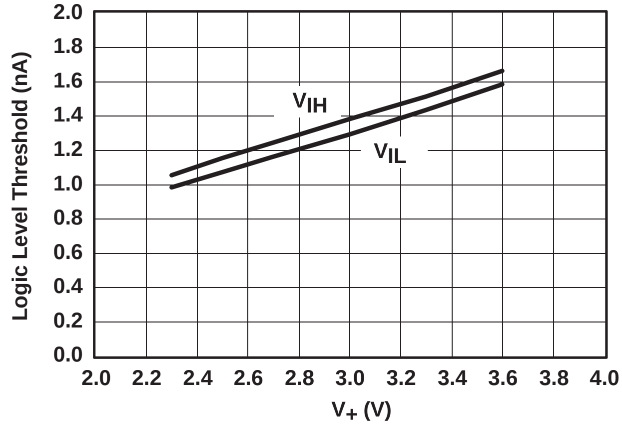


Figure 8. Logic-Level Threshold vs V_+

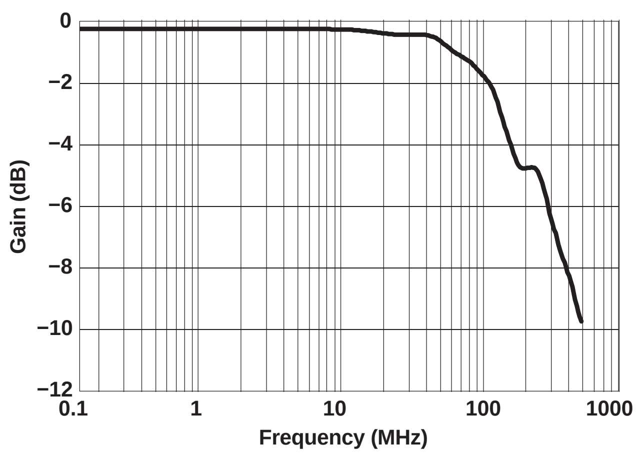


Figure 9. Bandwidth (Gain vs Frequency) (V_+ = 5 V)

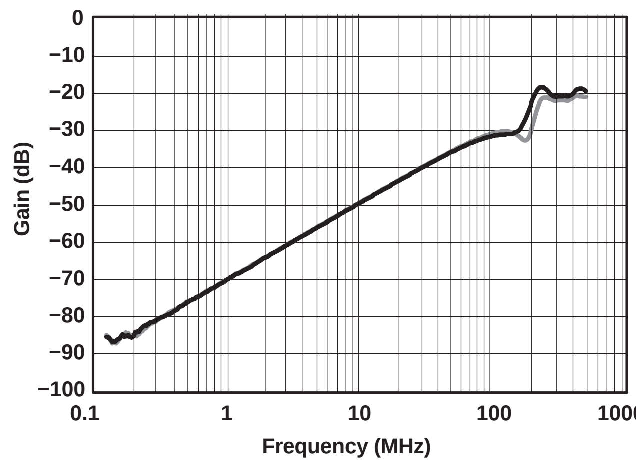


Figure 10. OFF Isolation and Crosstalk vs Frequency (V_+ = 5 V)

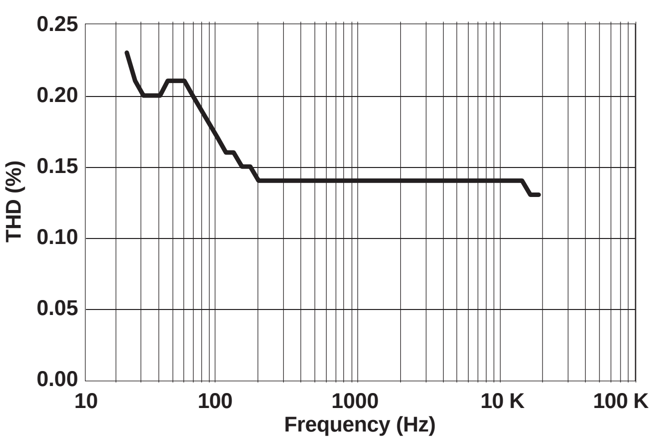


Figure 11. Total Harmonic Distortion vs Frequency

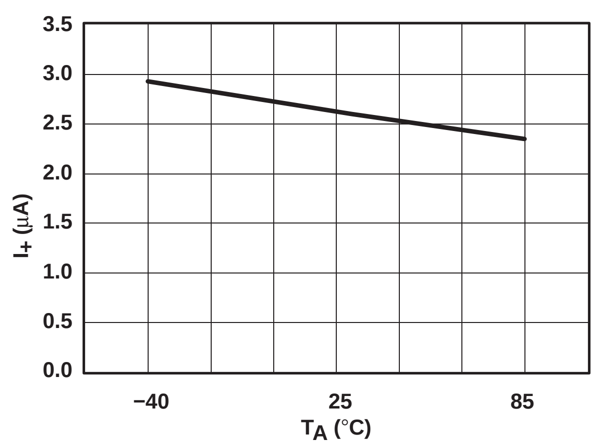


Figure 12. Power-Supply Current vs Temperature (V_+ = 3.6 V)

PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	$1\overline{EN}$	Enable (active low)
2	IN2	Digital control pin to connect D to S
3	$1S_4$	Analog I/O
4	$1S_3$	Analog I/O
5	$1S_2$	Analog I/O
6	$1S_1$	Analog I/O
7	1D	Common
8	GND	Ground
9	2D	Common
10	$2S_1$	Analog I/O
11	$2S_2$	Analog /O
12	$2S_3$	Analog I/O
13	$2S_4$	Analog I/O
14	IN1	Digital control pin to connect D to S
15	$2\overline{EN}$	Enable (active low)
16	V_+	Power supply

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_D	Voltage at D
V_S	Voltage at S
r_{on}	Resistance between D and S ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{S(OFF)}$	Leakage current measured at the S port, with the corresponding channel (S to D) in the OFF state
$I_{SPWR(OFF)}$	Leakage current measured at the S port, under powered down mode, $V_+ = 0$
$I_{S(ON)}$	Leakage current measured at the S port, with the corresponding channel (S to D) in the ON state and the output (D) open
$I_{D(OFF)}$	Leakage current measured at the D port, with the corresponding channel (D to S) in the OFF state
$I_{DPWR(OFF)}$	Leakage current measured at the D port, under powered down mode, $V_+ = 0$
$I_{D(ON)}$	Leakage current measured at the D port, with the corresponding channel (D to S) in the ON state and the output (S) open
V_{IH}	Minimum input voltage for logic high for the control input (IN, $\overline{EN}$)
V_{IL}	Maximum input voltage for logic low for the control input (IN, $\overline{EN}$)
V_I	Voltage at the control input (IN, $\overline{EN}$)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN, $\overline{EN}$)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (D or S) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (D or S) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (S or D) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_D$, C_L is the load capacitance, and ΔV_D is the change in analog output voltage.
$C_{S(OFF)}$	Capacitance at the S port when the corresponding channel (S to D) is OFF
$C_{S(ON)}$	Capacitance at the S port when the corresponding channel (S to D) is ON
$C_{D(OFF)}$	Capacitance at the D port when the corresponding channel (D to S) is OFF
$C_{D(ON)}$	Capacitance at the D port when the corresponding channel (D to S) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (S to D) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an adjacent ON channel ($1S_1$ to $2S_1$). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is −3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

PARAMETER MEASUREMENT INFORMATION

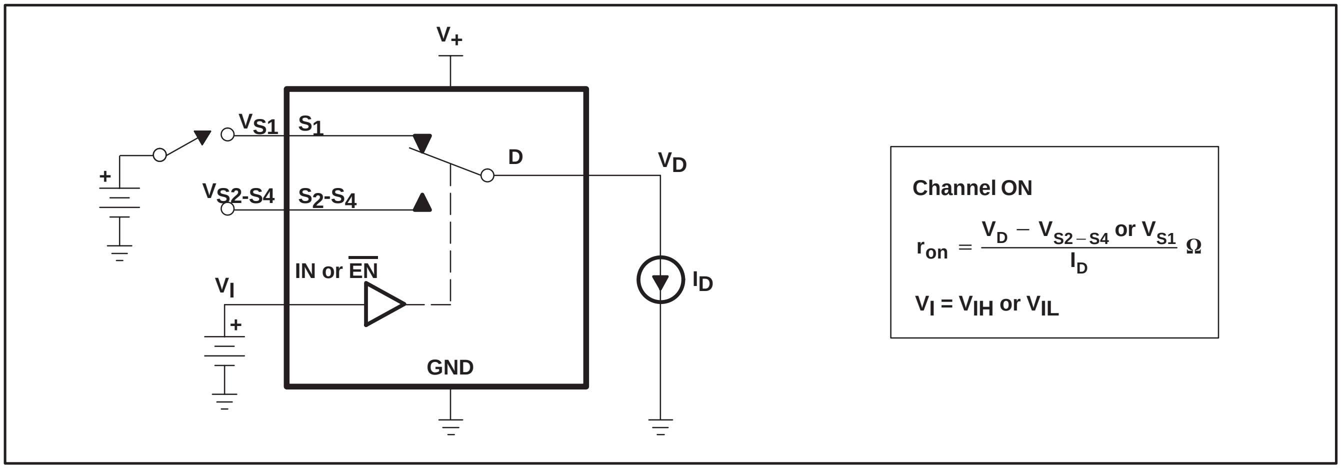


Figure 13. ON-State Resistance (r_{on})

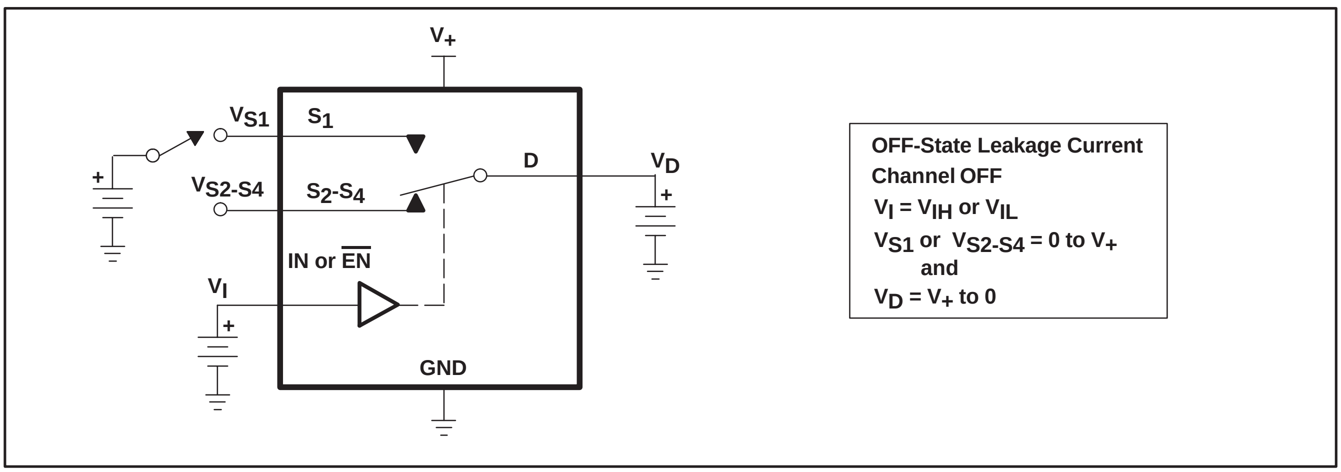


Figure 14. OFF-State Leakage Current ($I_{D(OFF)}$, $I_{S(OFF)}$, $I_{NO(OFF)}$)

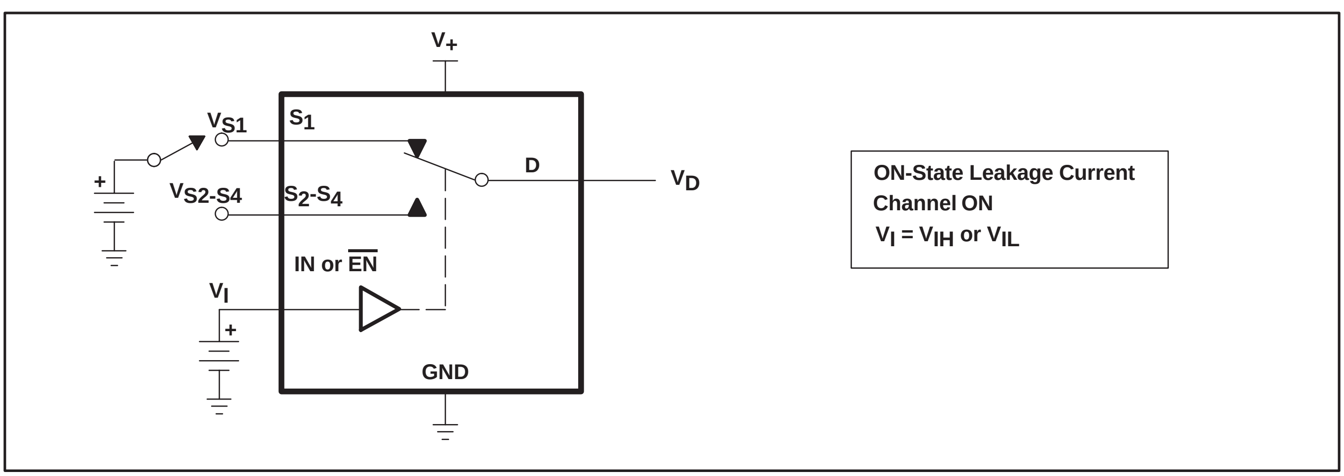


Figure 15. ON-State Leakage Current ($I_{D(ON)}$, $I_{S(ON)}$)

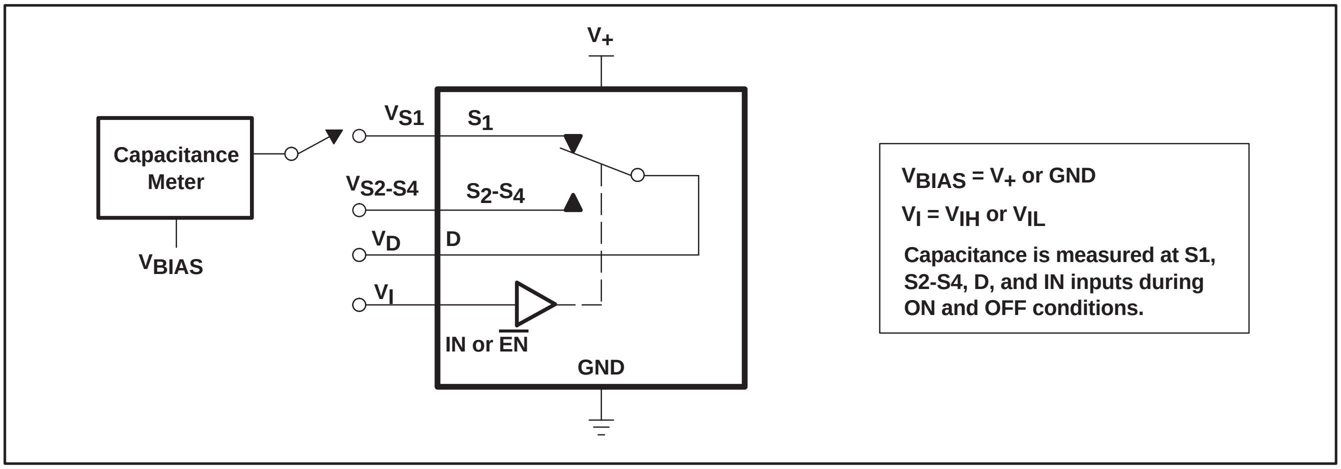
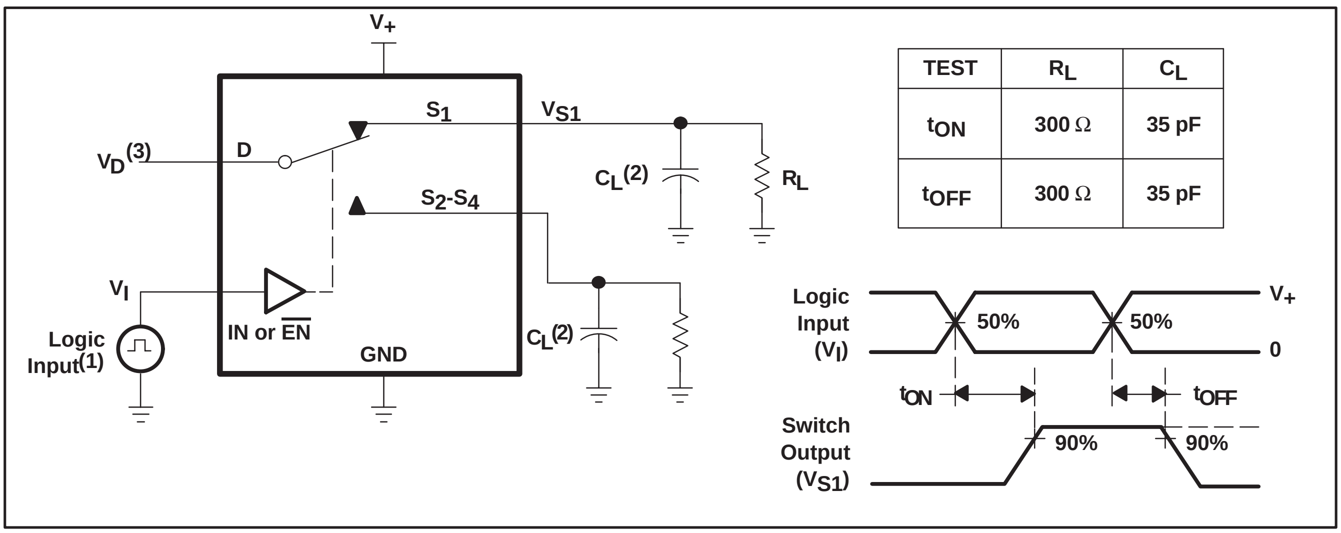


Figure 16. Capacitance (C_I, $C_{D(OFF)}$, $C_{D(ON)}$, $C_{S(OFF)}$, $C_{S(ON)}$)



TEST	R_L	C_L
t_{ON}	300 Ω	35 pF
t_{OFF}	300 Ω	35 pF

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.
(3) See Electrical Characteristics for V_D.

Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

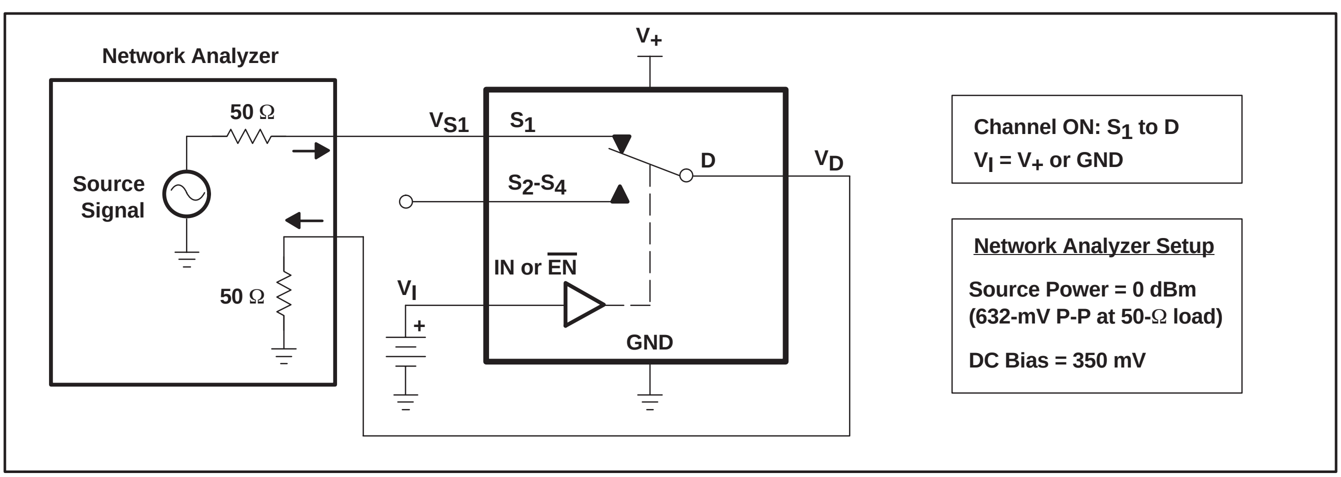


Figure 18. Bandwidth (BW)

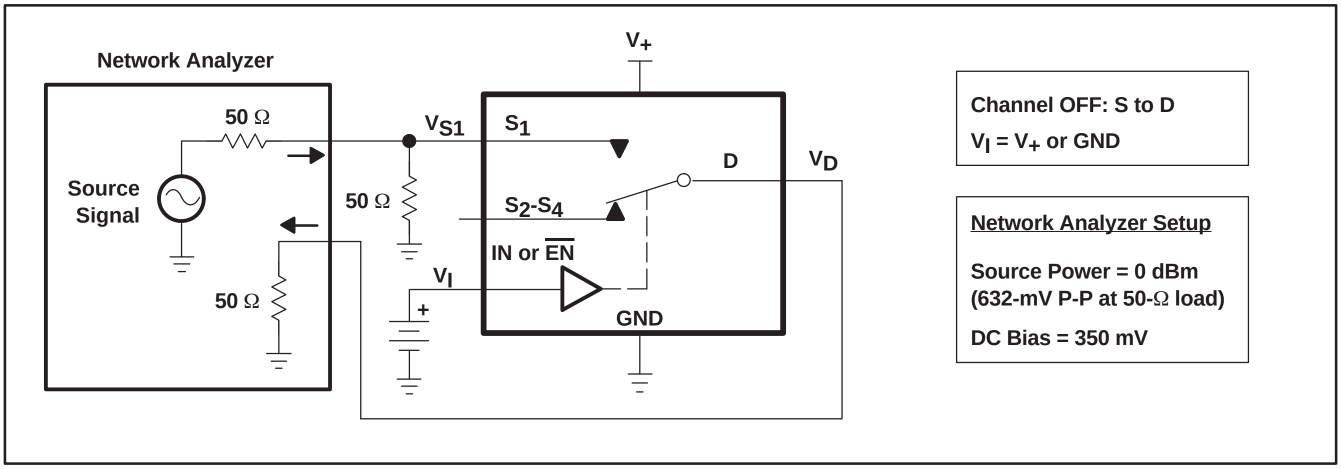


Figure 19. OFF Isolation (O_{ISO})

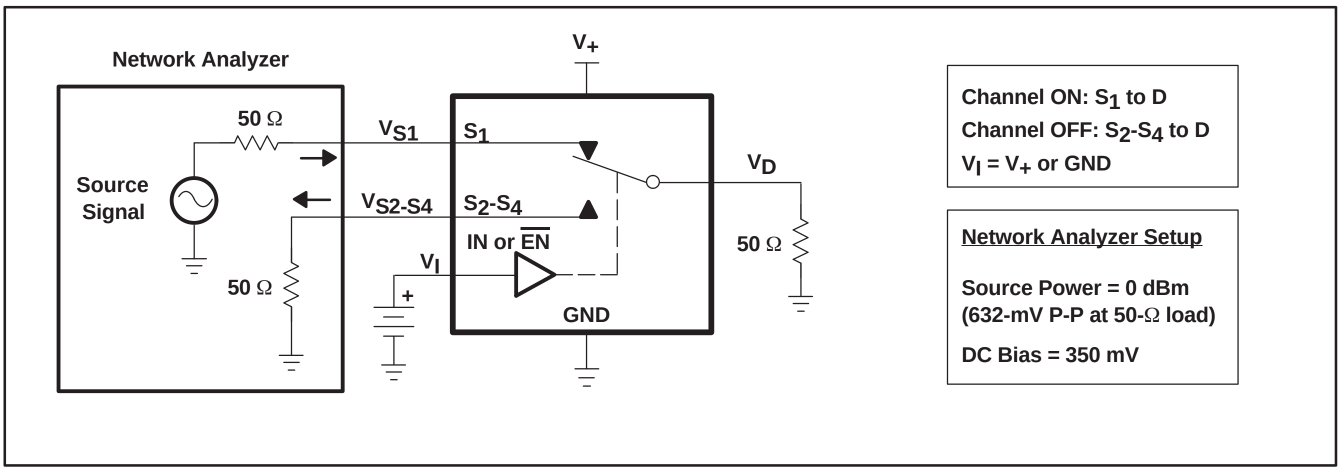


Figure 20. Crosstalk (X_{TALK})

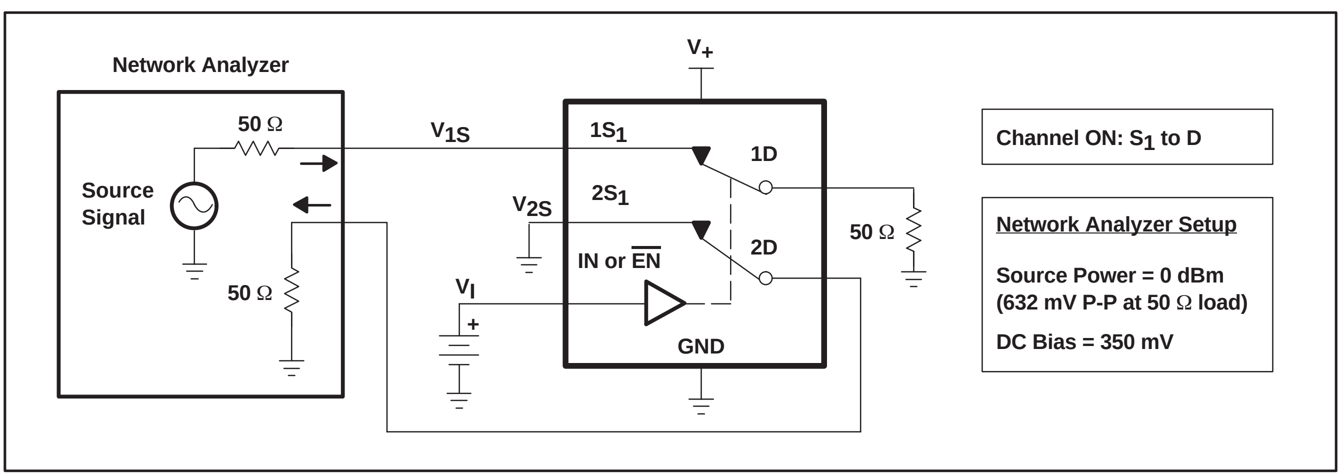
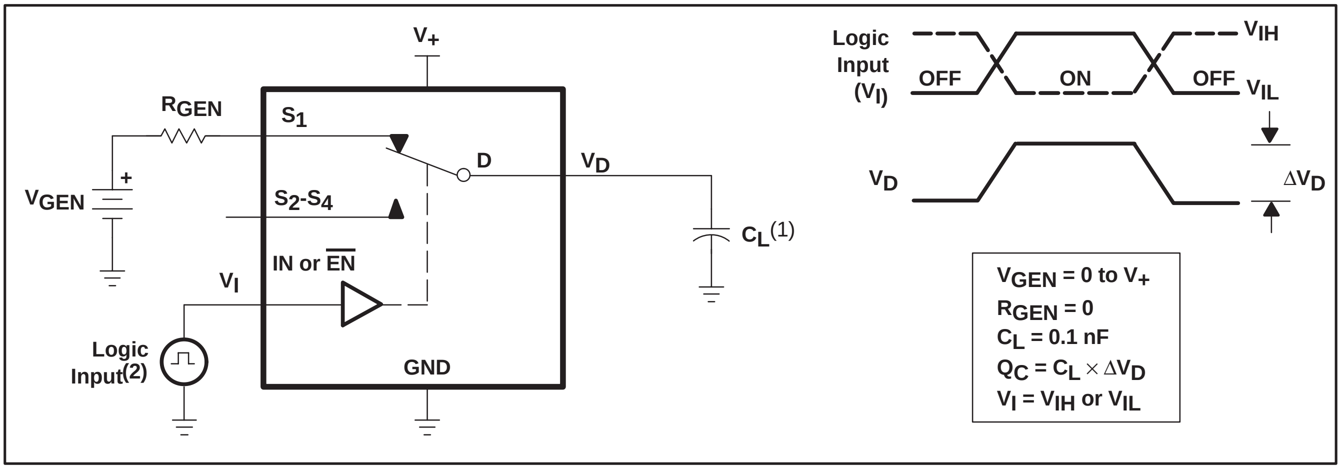
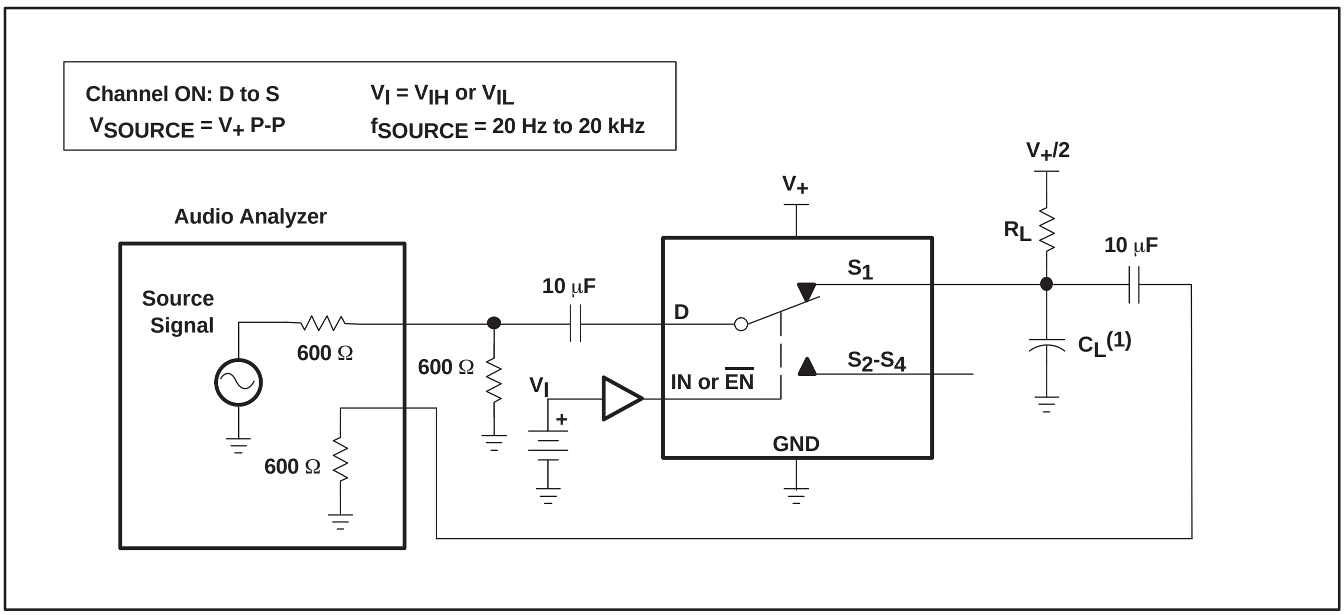


Figure 21. Adjacent Crosstalk



(1) C_L includes probe and jig capacitance.
(2) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 22. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 23. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
TS3A5017D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5017DBQR	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TS3A5017DBQRE4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TS3A5017DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5017DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5017DGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5017DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5017DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5017PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5017PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5017PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3A5017PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[(3)] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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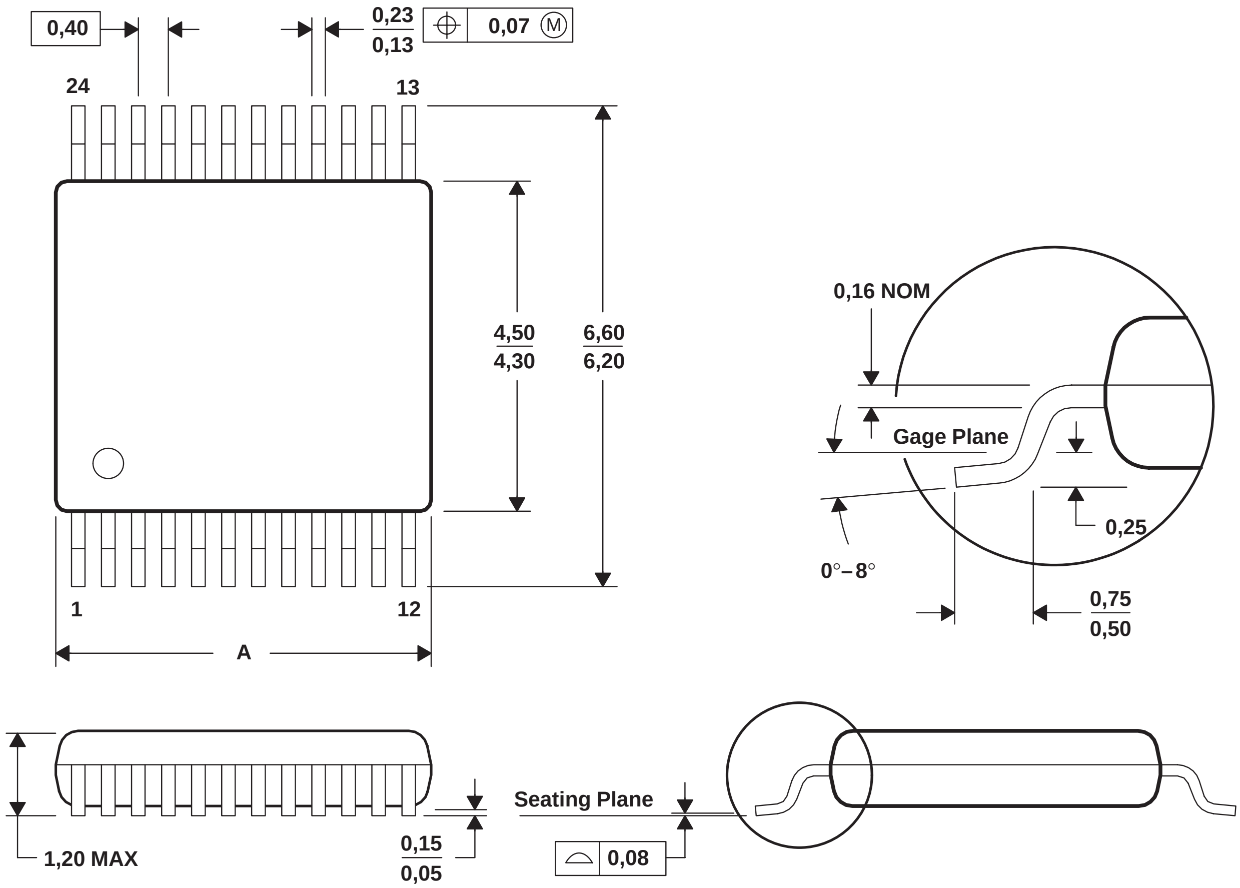
DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

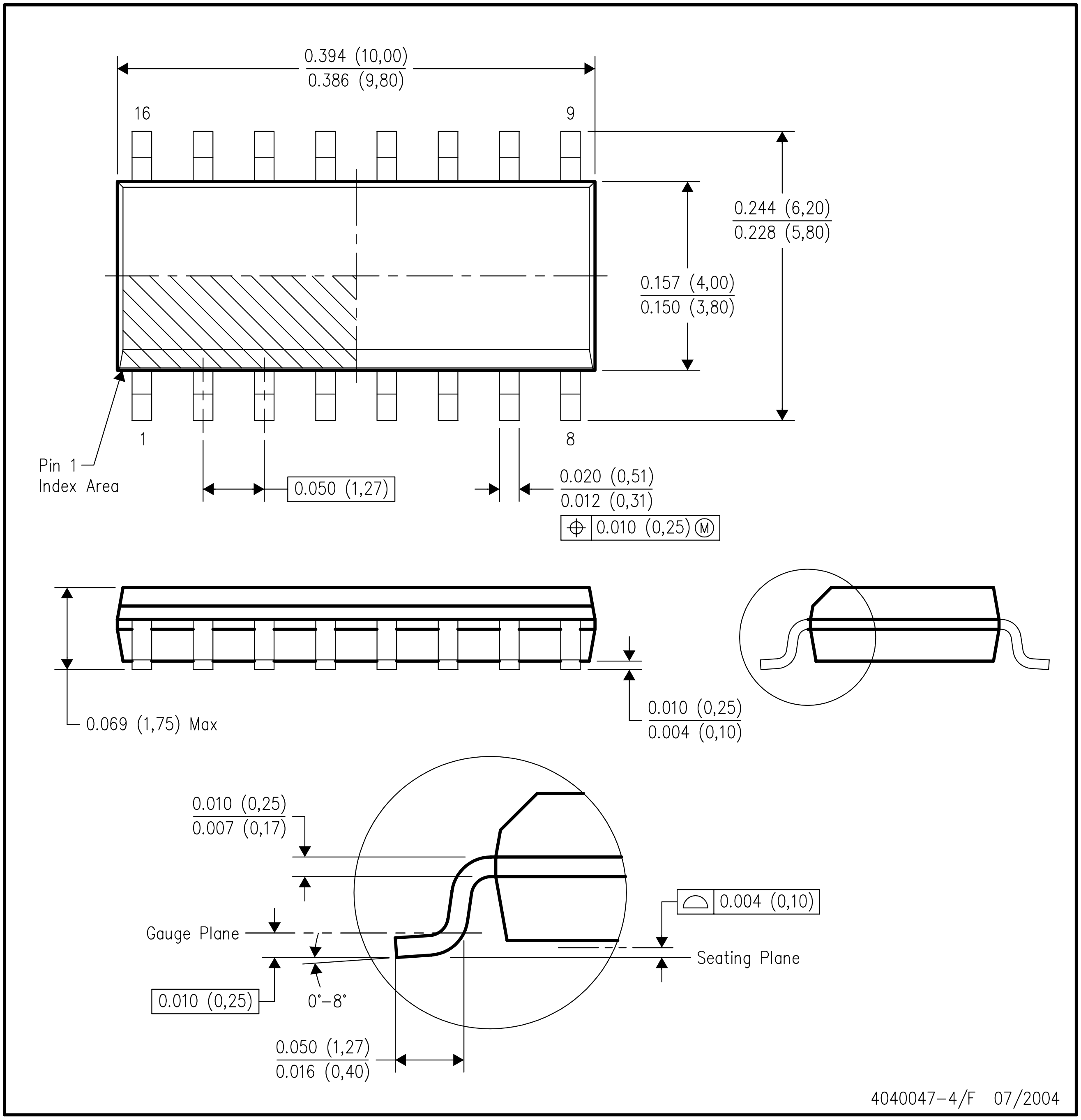


PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

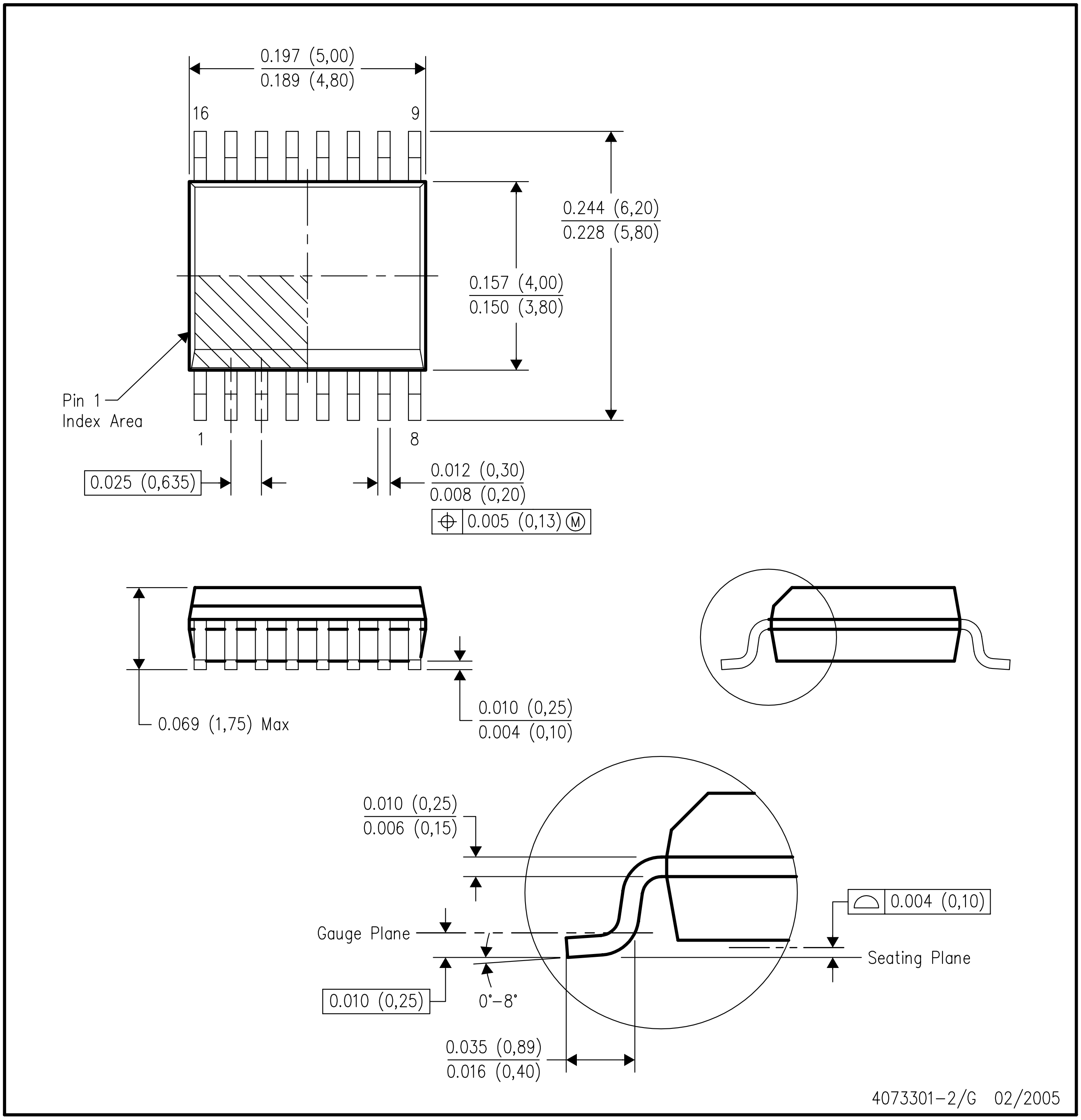
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins – MO-153
  14/16/20/56 Pins – MO-194

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AC.

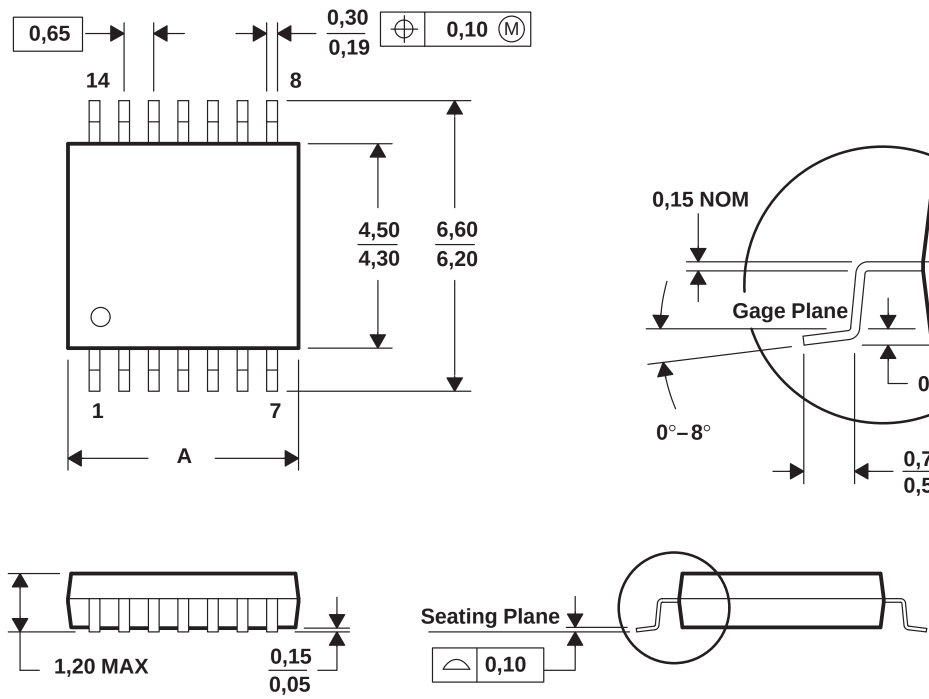
DBQ (R-PDSO-G16) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AB.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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