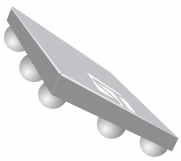
TS4975

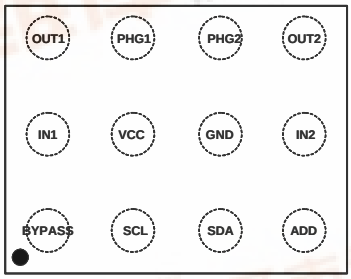
Stereo Headphone Drive Amplifier with Digital Volume Control via I²C Bus

- Operating from V_{CC} = 2.5V to 5.5V
- I²C bus control interface
- 40mW output power @ Vcc=3.3V, THD=1%, F=1kHz, with 16Ω load
- Ultra-low consumption in stdby mode: 0.6 µA
- Digital volume control range from 18dB to -34dB
- 14-step digital volume control
- 9 different output mode selections
- Pop & click noise reduction circuitry
- Flip-chip package 12 x 300µm bumps (lead-free)

TS4975EIJT - Flip Chip



Pin Out (top view)



Description

The TS4975 is a stereo audio headphone driver capable of delivering up to 102mW per channel of continuous average power into a 16Ω single-ended load with 1% THD+N from a 5V power supply. The overall gain of these headphone drivers is controlled digitally by volume control registers programmed via the I²C interface, minimizing the number of external components needed. This device can also easily be driven by an MCU to select the output modes, through the I²C bus interface.

A phantom ground configuration allows one to avoid using bulky capacitors on the outputs of the headphone amplifiers.

The TS4975 is packaged into a 1.8mm X 2.3mm Flip Chip package, ideally suited for space-conscious portable applications.

It has also an internal thermal shutdown protection mechanism.

Applications

- Mobile phones (cellular / cordless)
- PDAs
- Laptop/notebook computers
- Portable audio devices

Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
TS4975EIJT	-40, +85°C	Flip-chip	Tape & Reel	A75

1 Absolute Maximum Ratings

Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	Supply voltage (1)	6	V
V_i	Input Voltage (2)	G_{ND} to V_{cc}	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient (3)	200	°C/W
Pd	Power Dissipation	Internally Limited(4)	
ESD	Susceptibility - Human Body Model(5)	2	kV
ESD	Susceptibility - Machine Model (min. Value)	200	V
Latch-up	Latch-up Immunity	200	mA
	Lead Temperature (soldering, 10sec)	260	°C

1. All voltages values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V
3. Device is protected in case of over temperature by a thermal shutdown active @ 150°C.
4. Exceeding the power derating curves during a long period, may involve abnormal operating condition.
5. Human body model, 100pF discharged through a 1.5kOhm resistor, into pin to Vcc device.

Table 2. Operating conditions

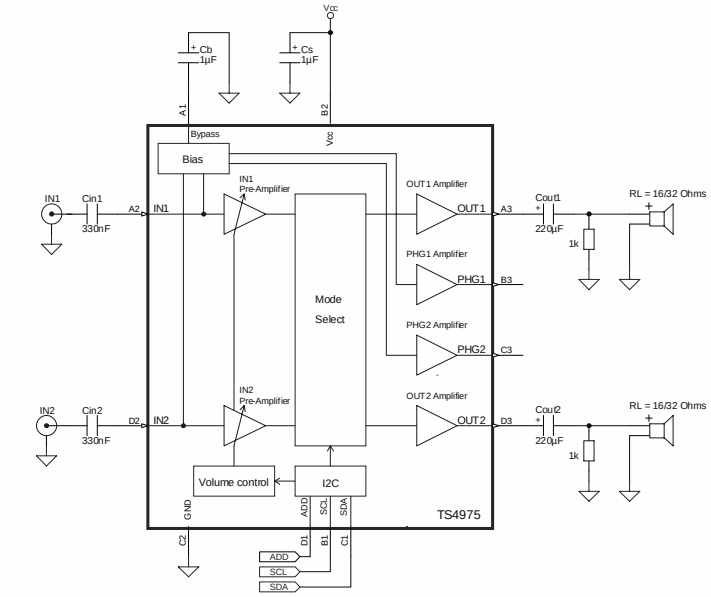
Symbol	Parameter	Value	Unit
VCC	Supply Voltage	2.5 to 5.5v	V
RL	Load Resistor	>16	Ω
CL	Load Capacitor RL = 16 to 100Ω, RL > 100Ω,	 400 100	pF
TOP	Operating Free Air Temperature Range	-40 to +85	°C
RTHJA	Flip Chip Thermal resistance Junction to Ambient	90	°C/W

2 Typical Application Schematics

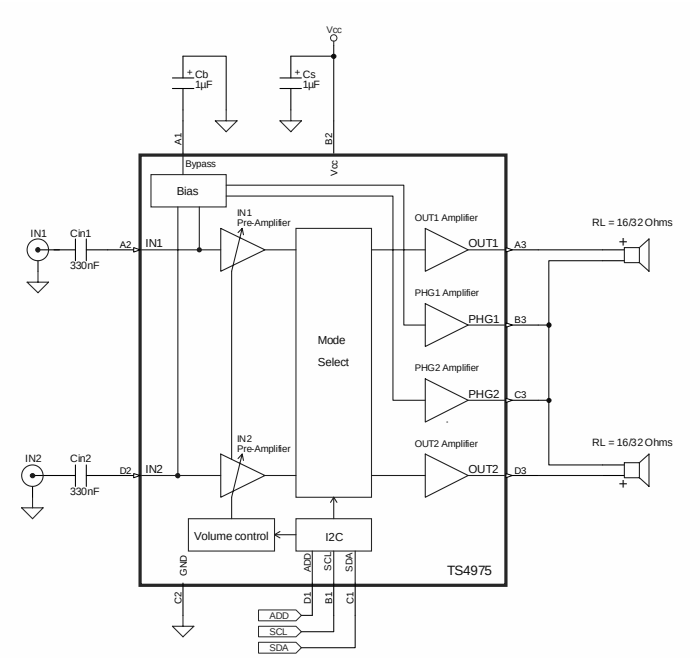
Figure 1 shows typical application schematics for the TS4975 in single-ended output configuration and in phantom ground output configuration.

Figure 1. Typical application schematics for two possible configurations

Single-ended output configuration



Phantom ground output configuration



3 Electrical Characteristics

Table 3. Electrical characteristics for the I²C interface

Symbol	Parameter	Value	Unit
VIL	Maximum Low level Input Voltage on pin SDA, SCL, VADD	0.3 V_{CC}	V
VIH	Minimum High Level Input Voltage on pin SDA, SCL, VADD	0.7 V_{CC}	V
FSCL	SCL Maximum clock Frequency	400	kHz
Vol	Max Low Level Output Voltage, SDA pin, Isink = 3mA	0.4	V
Ii	Input current on SDA, SCL. From 0.1Vcc to 0.9Vcc	10	µA

Table 4. Output noise (all inputs grounded)

	Unweighted Filter from Vcc=2.5V to 5V	Weighted Filter (A) from Vcc=2.5V to 5V
SE, G=+2dB	34µVrms	23µVrms
SE, G=+18dB	67µVrms	45µVrms
PHG, G=+2dB	34µVrms	23µVrms
PHG, G=+18dB	67µVrms	45µVrms

Table 5. V_{CC} = +2.5 V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load, Single Ended, Mode 1-4 No input signal, no load, Single Ended, Mode 5-8 No input signal, no load, Phantom Ground, Mode 1-4 No input signal, no load, Phantom Ground, Mode 5-8		 3 2 4.6 3.6	 4.2 2.8 6.5 5.3	mA
$I_{STANDBY}$	Standby Current (SCL and SDA at VCC level) No input signal		0.6	2	µA
Voo	Output Offset Voltage No input signal, RL = 32Ω, Phantom Ground		5	50	mV
Po	Output Power THD+N = 1% Max, f = 1kHz, RL = 16Ω, Single Ended THD+N = 1% Max, f = 1kHz, RL = 32Ω, Single Ended THD+N = 1% Max, f = 1kHz, RL = 16Ω, Phantom Ground THD+N = 1% Max, f = 1kHz, RL = 32Ω, Phantom Ground	 15 11 15 11	 21 13 21 13		mW
THD + N	Total Harmonic Distortion + Noise, Av = 2dB RL=32Ω, Po=10 mW, 20Hz < F < 20kHz, Single Ended RL=16Ω, Po=15 mW, 20Hz < F < 20kHz, Single Ended RL=32Ω, Po=10 mW, 20Hz < F < 20kHz, Phantom Ground RL=16Ω, Po=15 mW, 20Hz < F < 20kHz, Phantom Ground		 0.3 0.3 0.3 0.3		%
PSRR	Power Supply Rejection Ratio(1) F = 217Hz, RL = 16Ω, Av = 2 dB Vripple = 200mVpp, Input Grounded, Cb = 1µF, **Single Ended Output referenced to Phantom Ground** F = 217Hz, RL = 16Ω, Av = 2 dB Vripple = 200mVpp, Input Grounded, Cb = 1µF, **Single Ended Output referenced to Ground**		 60 60		dB
Crosstalk	Channel Separation, RL = 32Ω, Av = 2 dB with Single Ended F = 1kHZ, Po=10mW F = 20Hz to 20kHz, Po=10mW Channel Separation, RL = 32Ω, Av = 2 dB with Phantom Ground F = 1kHZ, Po=10mW F = 20Hz to 20kHz, Po=10mW		 103 75 69 69		dB
SNR	Signal To Noise Ratio, A-Weighted, Av=2dB, RL=32Ω, Po=12mW Single Ended Phantom Ground		 88 88		dB
ONoise	Output Noise voltage, A-Weighted, Av=2dB Single Ended Phantom Ground		 23 23		µVrms
G	Digital Gain Range In1 & In2 to Out1 & Out2	-34		+18	dB
	Digital Gain Stepsize		4		dB
	Gain error tolerance	-1		+1	dB
Zin	In1 & In2 Input Impedance, All Gain setting	25.5	30	34.5	kΩ
Twu	Wake up time, Cb=1µF		110	180	ms
Tws	Standby time		1		µs

1. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is an added sinus signal to Vcc @ F = 217Hz

Table 6. V_{CC} = +3.3V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load, Single Ended, Mode 1-4 No input signal, no load, Single Ended, Mode 5-8 No input signal, no load, Phantom Ground, Mode 1-4 No input signal, no load, Phantom Ground, Mode 5-8		 3 2 4.6 3.6	 4.2 2.8 6.5 5.3	mA
$I_{STANDBY}$	Standby Current (SCL and SDA at VCC level) No input signal		0.6	2	µA
Voo	Output Offset Voltage No input signal, RL = 32Ω, Phantom Ground		5	50	mV
Po	Output Power THD+N = 1% Max, f = 1kHz, RL = 16Ω, Single Ended THD+N = 1% Max, f = 1kHz, RL = 32Ω, Single Ended THD+N = 1% Max, f = 1kHz, RL = 16Ω, Phantom Ground THD+N = 1% Max, f = 1kHz, RL = 32Ω, Phantom Ground	 34 24 34 24	 40 26 40 26		mW
THD + N	Total Harmonic Distortion + Noise, Av = 2dB RL=32Ω, Po=20 mW, 20Hz < F < 20kHz, Single Ended RL=16Ω, Po=30 mW, 20Hz < F < 20kHz, Single Ended RL=32Ω, Po=20 mW, 20Hz < F < 20kHz, Phantom Ground RL=16Ω, Po=30 mW, 20Hz < F < 20kHz, Phantom Ground		 0.3 0.3 0.3 0.3		%
PSRR	Power Supply Rejection Ratio(1) F = 217Hz, RL = 16Ω, Av = 2 dB Vripple = 200mVpp, Input Grounded, Cb = 1µF, **Single Ended** **Output referenced to Phantom Ground** F = 217Hz, RL = 16Ω, Av = 2 dB Vripple = 200mVpp, Input Grounded, Cb = 1µF, **Single Ended** **Output referenced to Ground**		 61 61		dB
Crosstalk	Channel Separation, RL = 32Ω, Av = 2 dB with Single Ended F = 1kHZ, Po=20mW F = 20Hz to 20kHz, Po=20mW Channel Separation, RL = 32Ω, Av = 2 dB with Phantom Ground F = 1kHZ, Po=20mW F = 20Hz to 20kHz, Po=20mW		 103 75 69 69		dB
SNR	Signal To Noise Ratio, A-Weighted, Av=2dB, RL=32Ω, Po=25mW Single Ended Phantom Ground		 90 90		dB
Noise	Output Noise voltage, A-Weighted, Av=2dB Single Ended Phantom Ground		 23 23		µVrms
G	Digital Gain Range In1 & In2 to Out1 & Out2	-34		+18	dB
	Digital Gain Stepsize		4		dB
	Gain error tolerance	-1		+1	dB
Zin	In1 & In2 Input Impedance, All Gain setting	25.5	30	34.5	kΩ
Twu	Wake up time, Cb=1µF		90	156	ms
Tws	Standby time		1		µs

1. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is an added sinus signal to Vcc @ F = 217Hz

Table 7. V_{CC} = +5V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load, Single Ended, Mode 1-4 No input signal, no load, Single Ended, Mode 5-8 No input signal, no load, Phantom Ground, Mode 1-4 No input signal, no load, Phantom Ground, Mode 5-8		 3 2 4.6 3.6	 4.2 2.8 6.5 5.3	mA
$I_{STANDBY}$	Standby Current (SCL and SDA at VCC level) No input signal		0.6	2	µA
Voo	Output Offset Voltage No input signal, RL = 32Ω, Phantom Ground		5	50	mV
Po	Output Power THD+N = 1% Max, f = 1kHz, RL = 16Ω, Single Ended THD+N = 1% Max, f = 1kHz, RL = 32Ω, Single Ended THD+N = 1% Max, f = 1kHz, RL = 16Ω, Phantom Ground THD+N = 1% Max, f = 1kHz, RL = 32Ω, Phantom Ground	 92 59 92 59	 102 64 98 63		mW
THD + N	Total Harmonic Distortion + Noise, Av = 2dB RL=32Ω, Po=50 mW, 20Hz < F < 20kHz, Single Ended RL=16Ω, Po=80 mW, 20Hz < F < 20kHz, Single Ended RL=32Ω, Po=50 mW, 20Hz < F < 20kHz, Phantom Ground RL=16Ω, Po=80 mW, 20Hz < F < 20kHz, Phantom Ground		 0.3 0.3 0.3 0.3		%
PSRR	Power Supply Rejection Ratio(1) F = 217Hz, RL = 16Ω, Av = 2 dB Vripple = 200mVpp, Input Grounded, Cb = 1µF, **Single Ended Output referenced to Phantom Ground** F = 217Hz, RL = 16Ω, Av = 2 dB Vripple = 200mVpp, Input Grounded, Cb = 1µF, **Single Ended Output referenced to Ground**		 63 63		dB
Crosstalk	Channel Separation, RL = 32Ω, Av = 2 dB with Single Ended F = 1kHZ, Po=50mW F = 20Hz to 20kHz, Po=50mW Channel Separation, RL = 32Ω, Av = 2 dB with Phantom Ground F = 1kHZ, Po=50mW F = 20Hz to 20kHz, Po=50mW		 103 75 69 69		dB
SNR	Signal To Noise Ratio, A-Weighted, Av=2dB, RL=32Ω, Po=62mW Single Ended Phantom Ground		 95 95		dB
ONoise	Output Noise voltage, A-Weighted, Av=2dB Single Ended Phantom Ground		 23 23		µVrms
G	Digital Gain Range In1 & In2 to Out1 & Out2	-34		+18	dB
	Digital Gain Stepsize		4		dB
	Gain error tolerance	-1		+1	dB
Zin	In1 & In2 Input Impedance, All Gain setting	25.5	30	34.5	kΩ
Twu	Wake up time, Cb=1µF		80	144	ms
Tws	Standby time		1		µs

1. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is an added sinus signal to Vcc @ F = 217Hz

Figure 2. THD+N versus output power

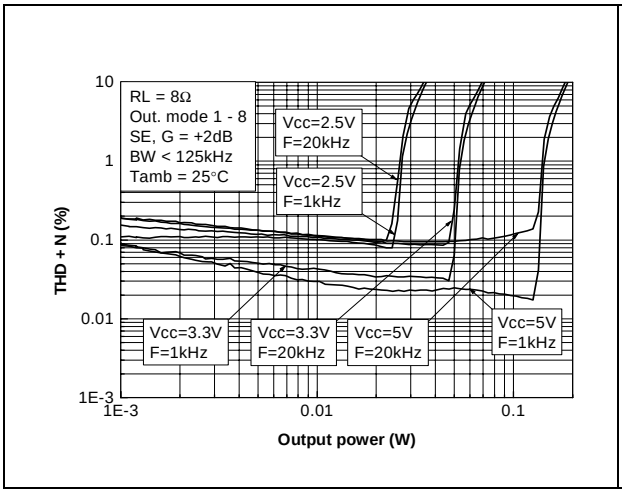


Figure 3. THD+N versus output power

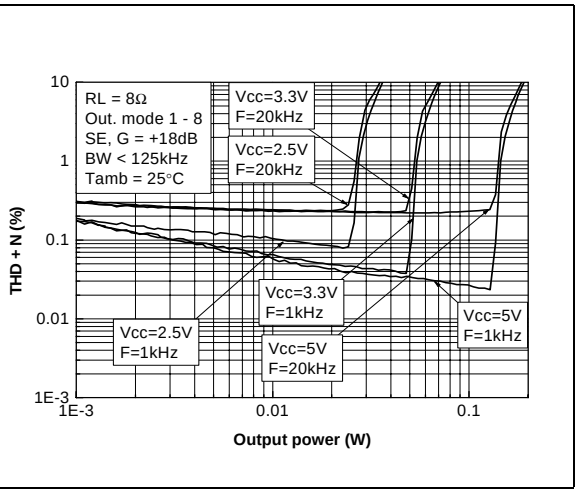


Figure 4. THD+N versus output power

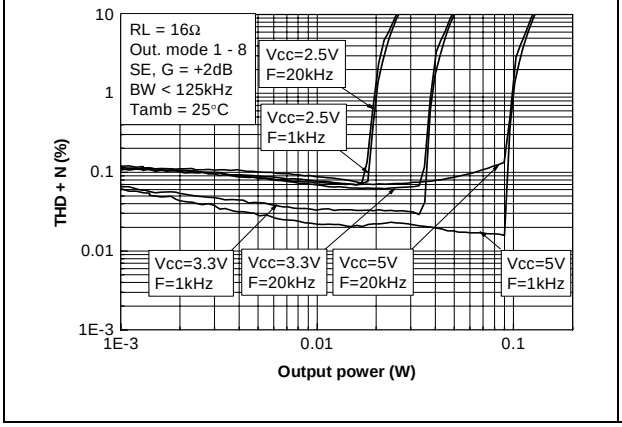


Figure 5. THD+N versus output power

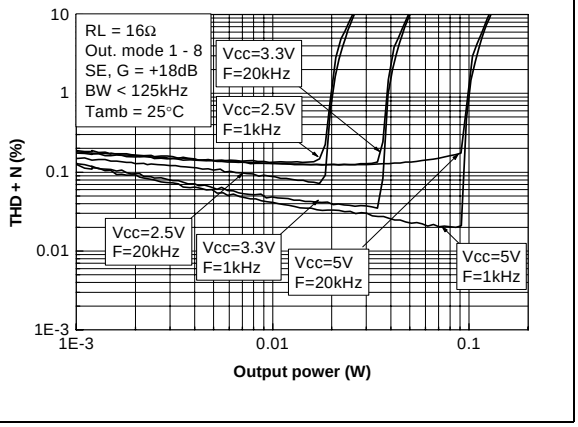


Figure 6. THD+N versus output power

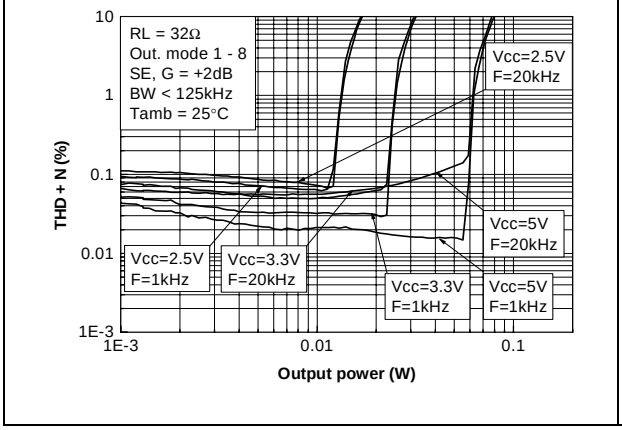


Figure 7. THD+N versus output power

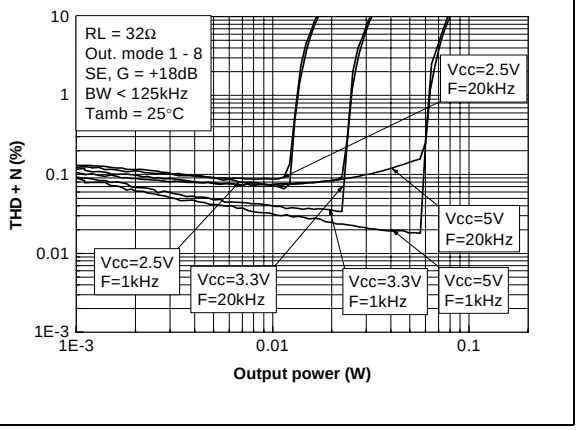


Figure 8. THD+N versus output power

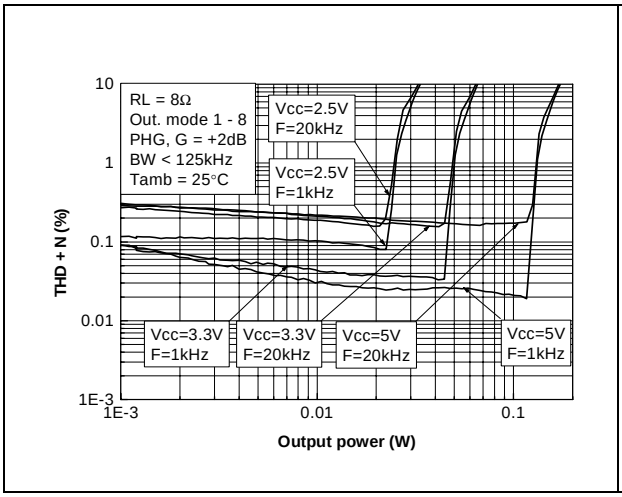


Figure 9. THD+N versus output power

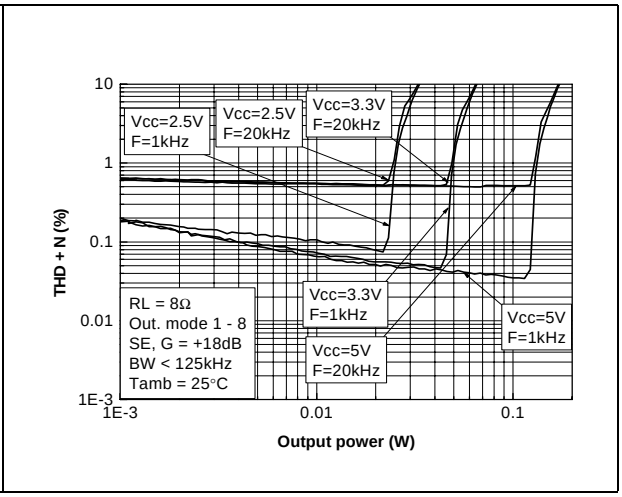


Figure 10. THD+N versus output power

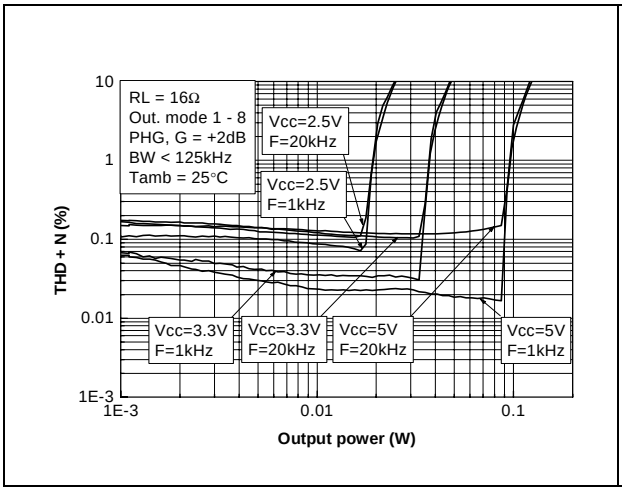


Figure 11. THD+N versus output power

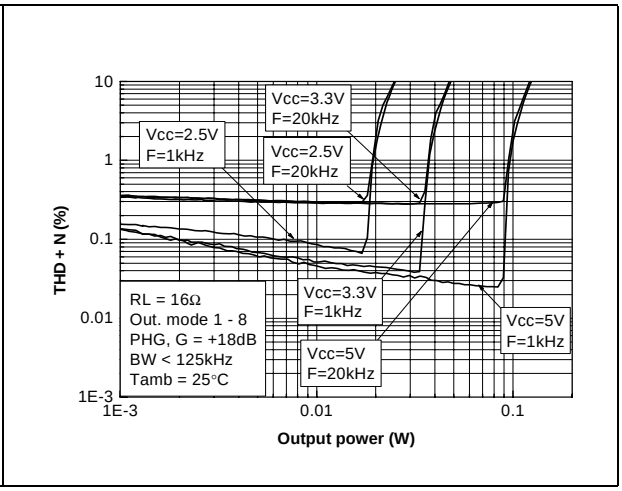


Figure 12. THD+N versus output power

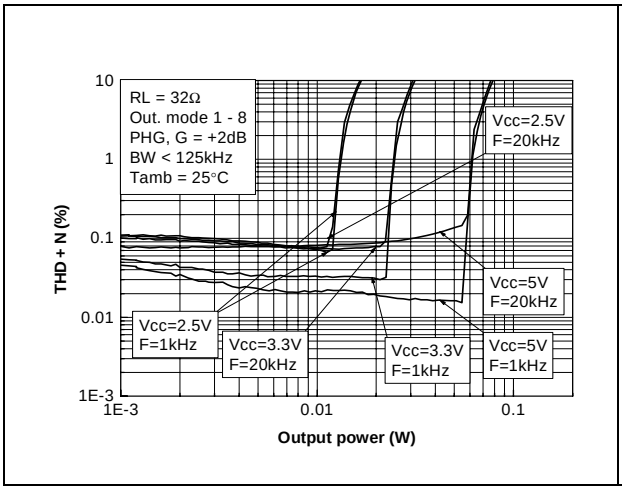


Figure 13. THD+N versus output power

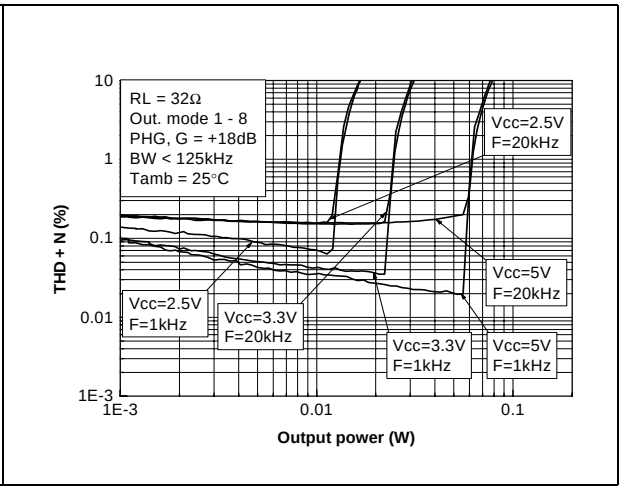


Figure 14. THD+N versus frequency

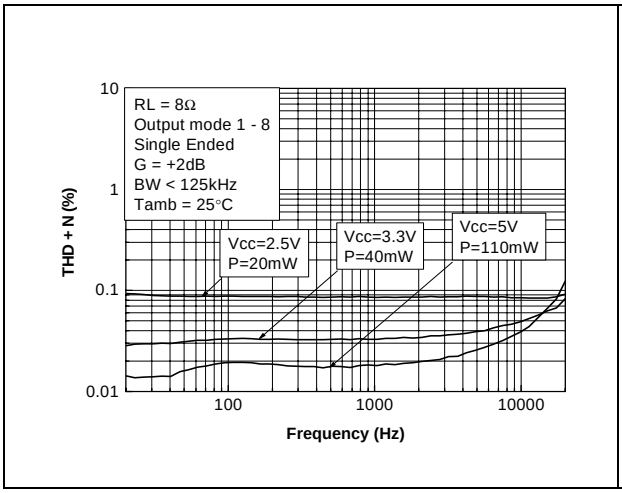


Figure 15. THD+N versus frequency

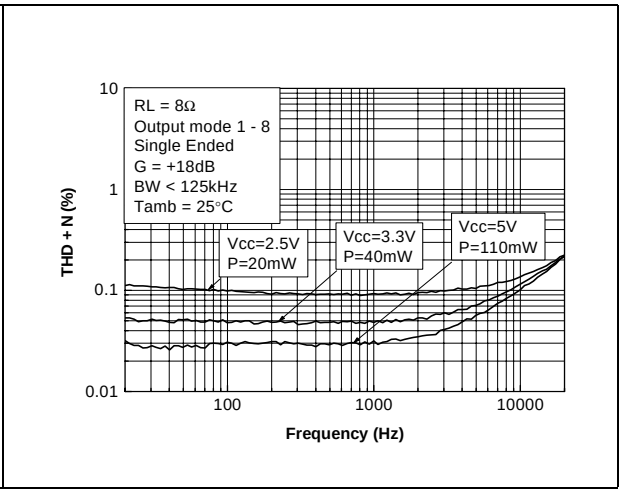


Figure 16. THD+N versus frequency

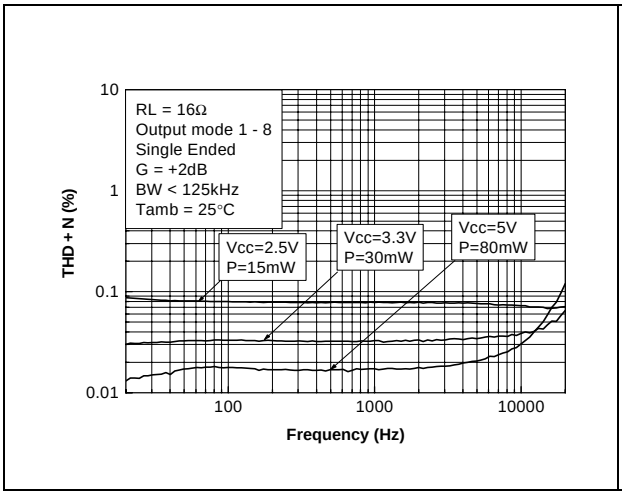


Figure 17. THD+N versus frequency

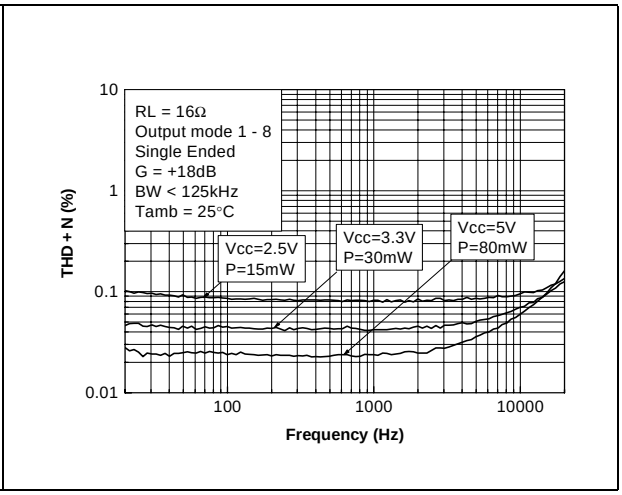


Figure 18. THD+N versus frequency

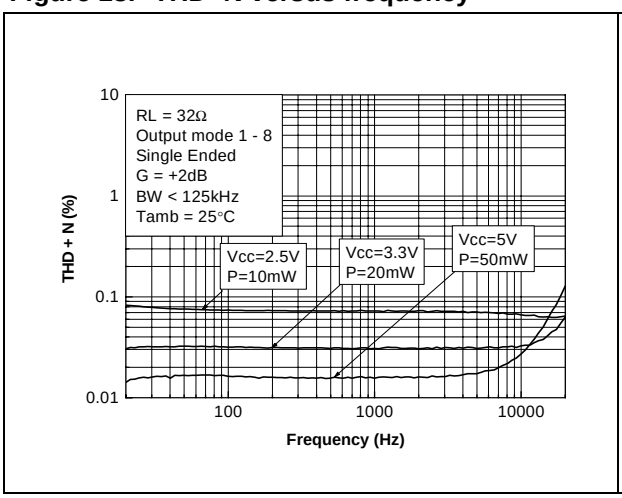


Figure 19. THD+N versus frequency

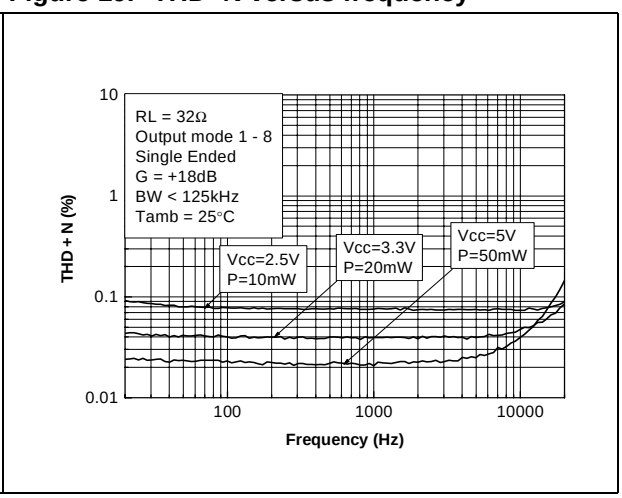


Figure 20. THD+N versus frequency

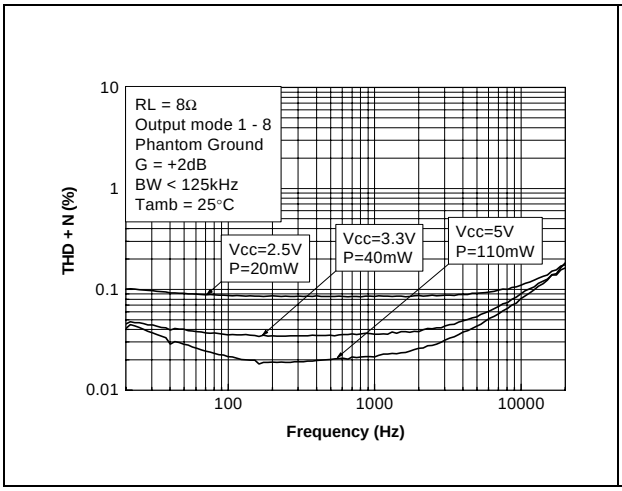


Figure 21. THD+N versus frequency

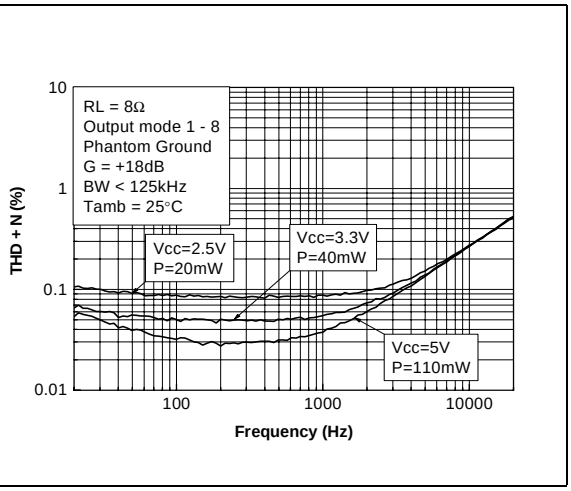


Figure 22. THD+N versus frequency

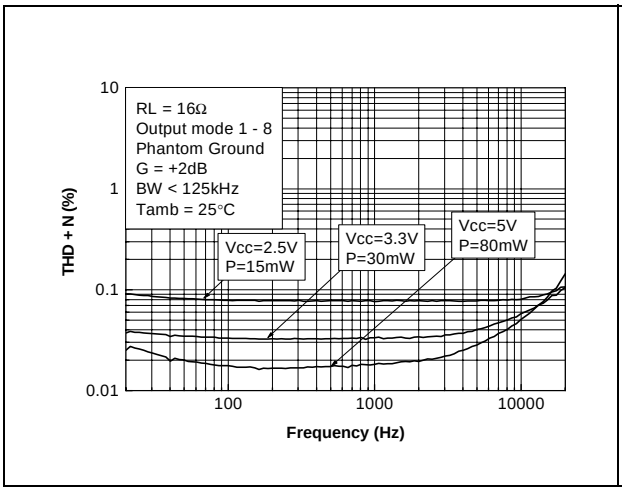


Figure 23. THD+N versus frequency

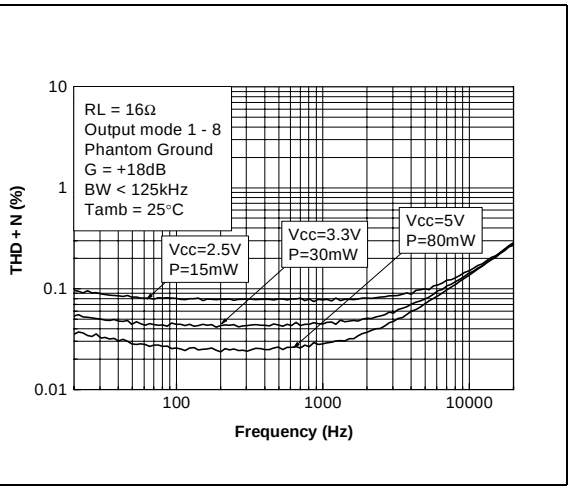


Figure 24. THD+N versus frequency

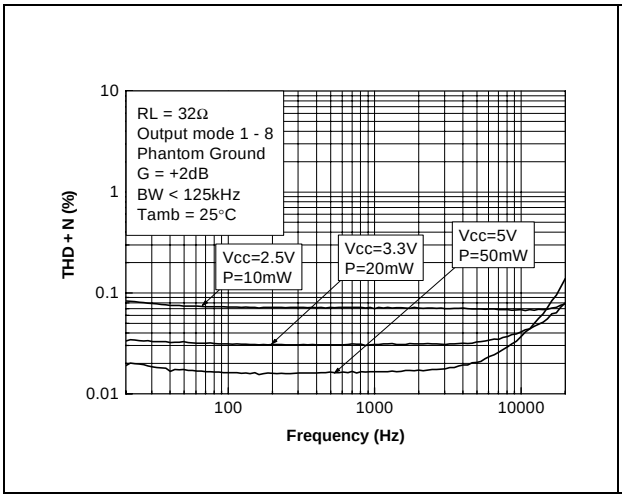


Figure 25. THD+N versus frequency

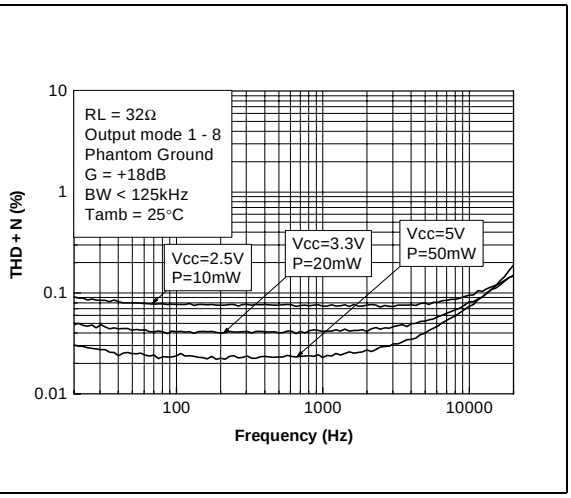


Figure 26. Output power versus power supply voltage

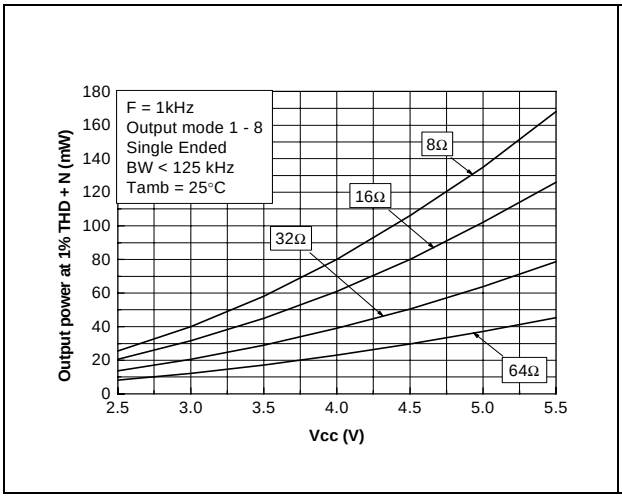


Figure 27. Output power versus power supply voltage

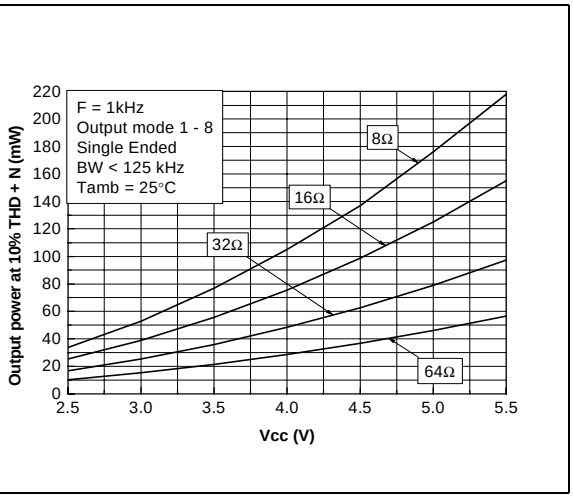


Figure 28. Output power versus power supply voltage

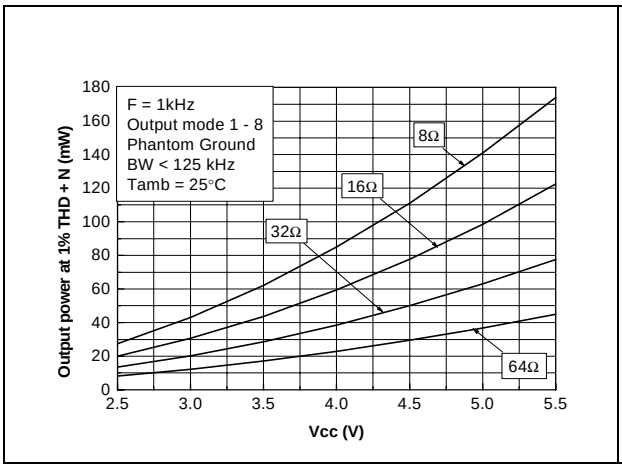


Figure 29. Output power versus power supply voltage

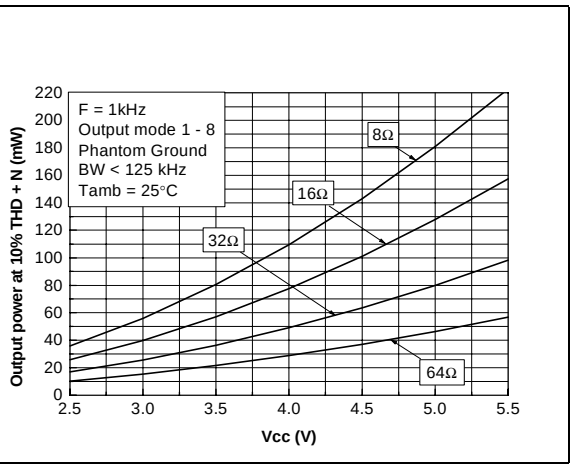


Figure 30. PSSR versus frequency

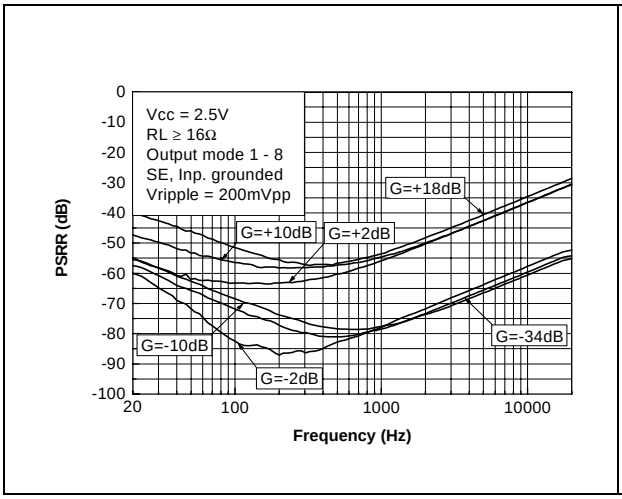


Figure 31. PSSR versus frequency

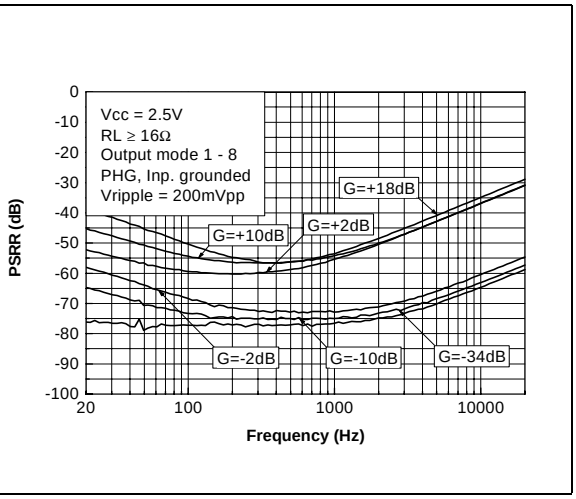


Figure 32. PSSR versus frequency

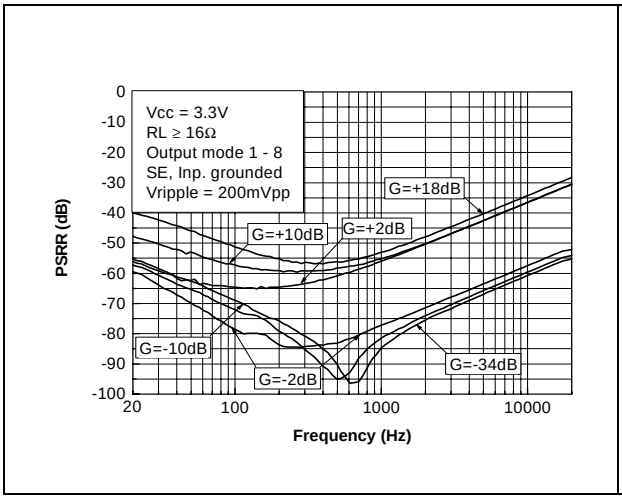


Figure 33. PSSR versus frequency

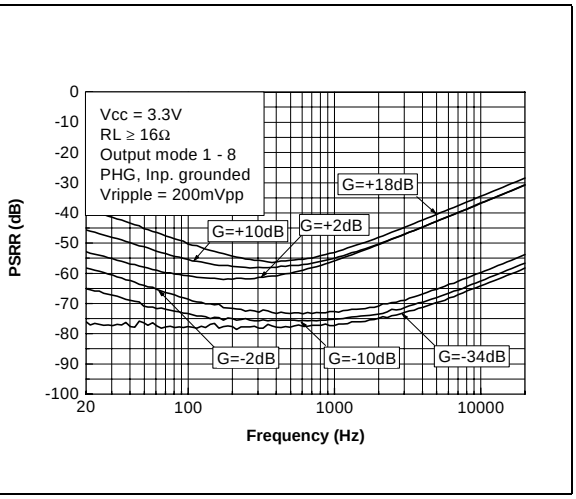


Figure 34. PSSR versus frequency

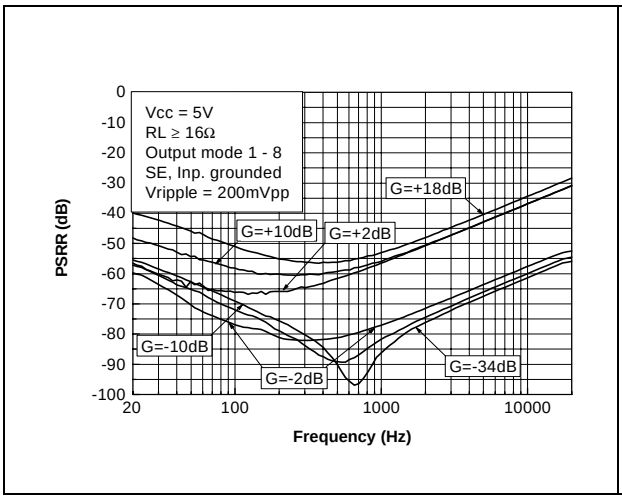


Figure 35. PSSR versus frequency

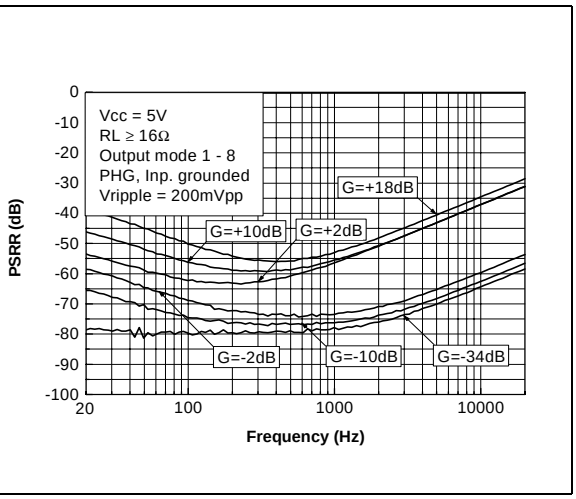


Figure 36. Crosstalk versus frequency

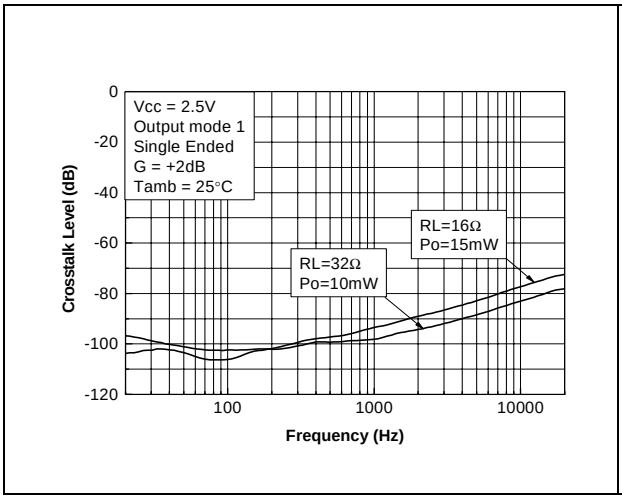


Figure 37. Crosstalk versus frequency

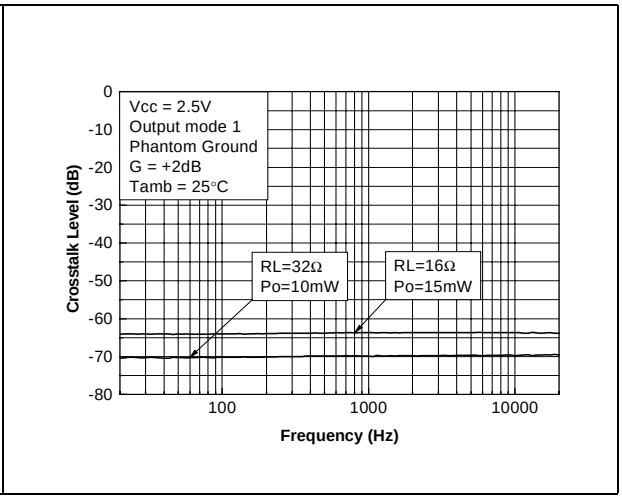


Figure 38. Crosstalk versus frequency

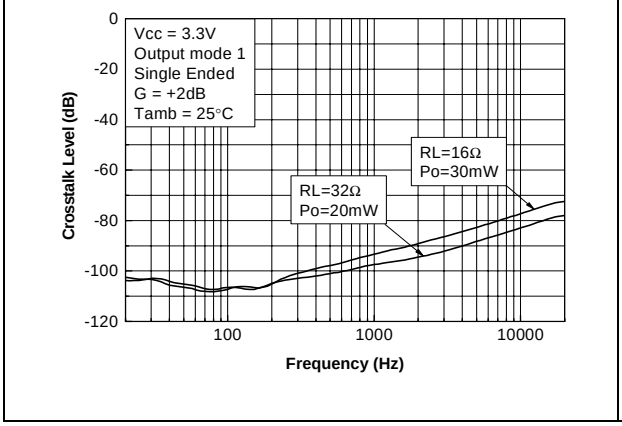


Figure 39. Crosstalk versus frequency

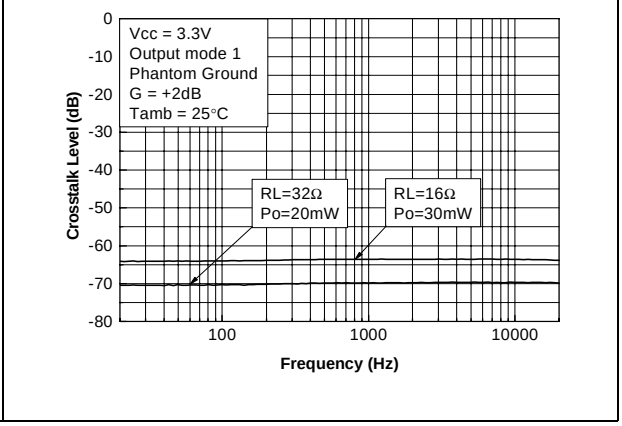


Figure 40. Crosstalk versus frequency

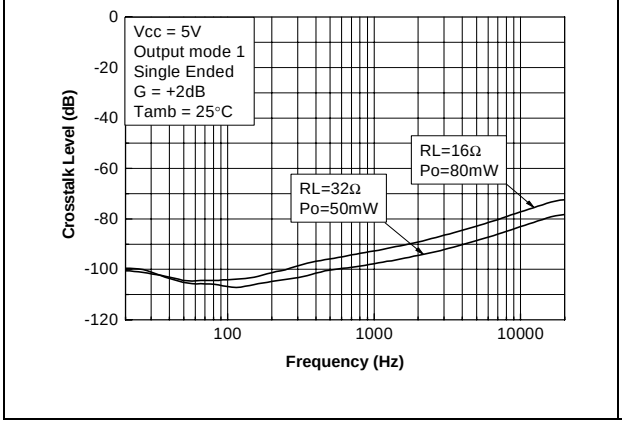


Figure 41. Crosstalk versus frequency

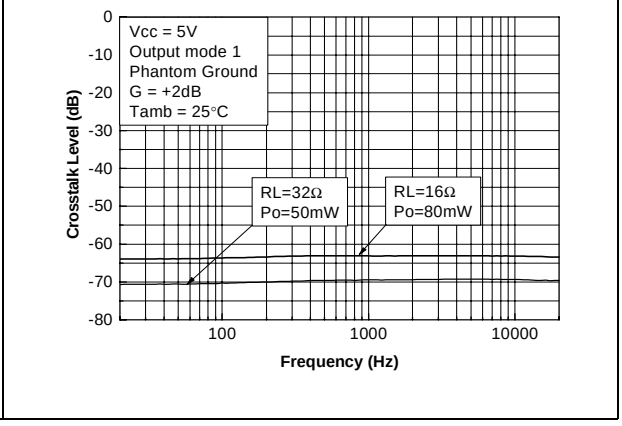


Figure 42. SNR versus power supply voltage

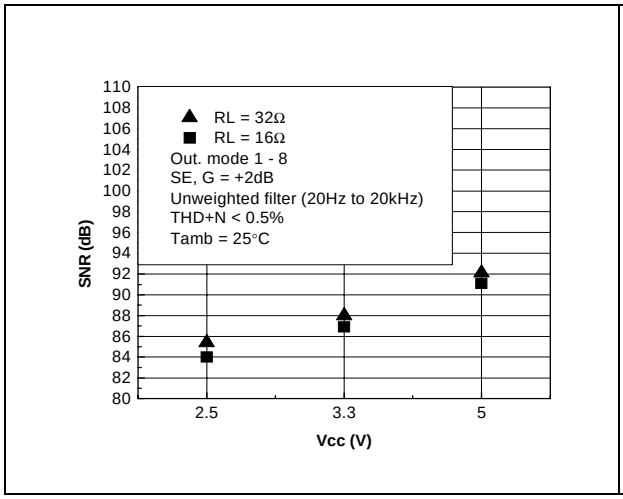


Figure 43. SNR versus power supply voltage

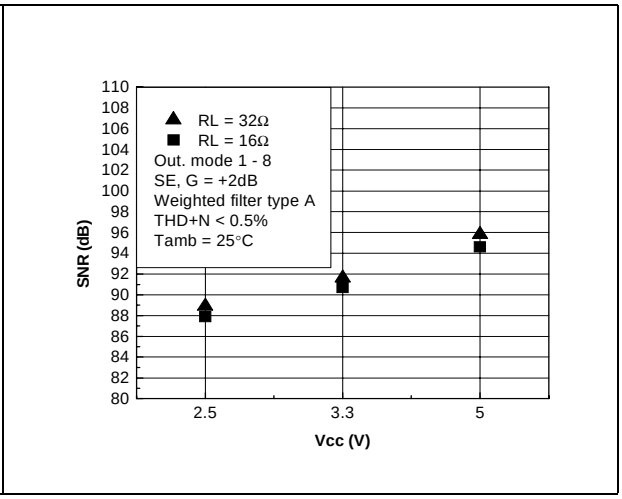


Figure 44. SNR versus power supply voltage

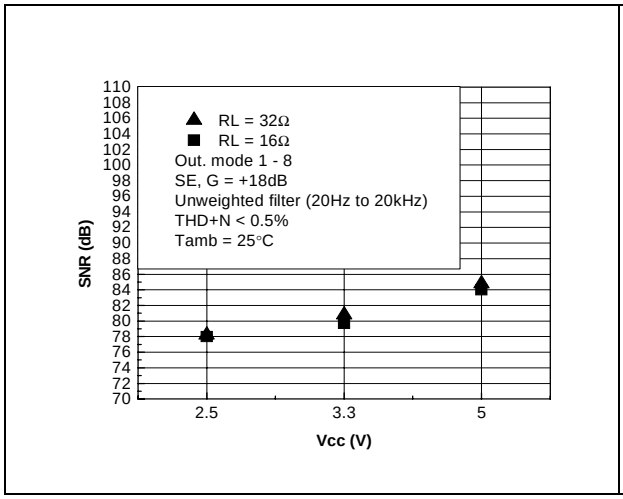


Figure 45. SNR versus power supply voltage

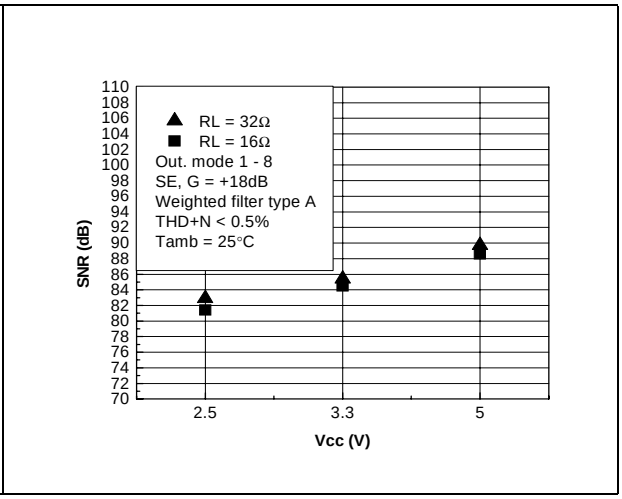


Figure 46. SNR versus power supply voltage

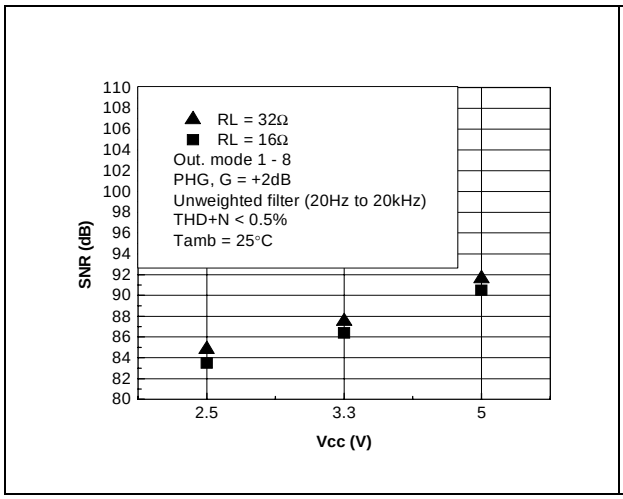


Figure 47. SNR versus power supply voltage

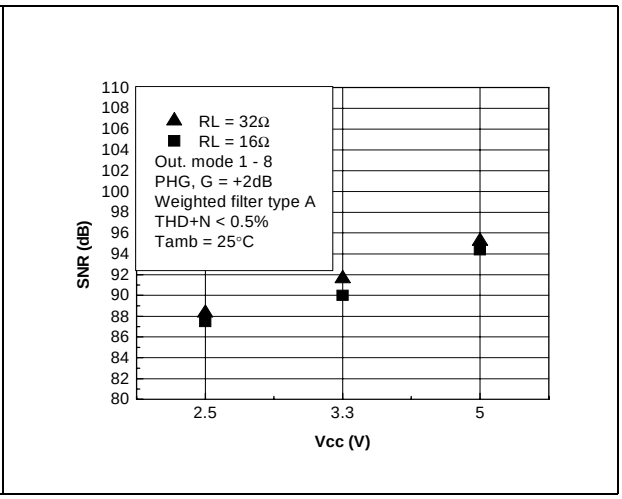


Figure 48. SNR versus power supply voltage

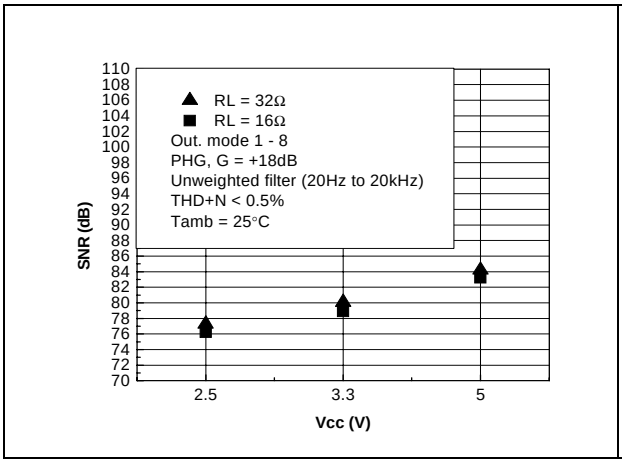


Figure 49. SNR versus power supply voltage

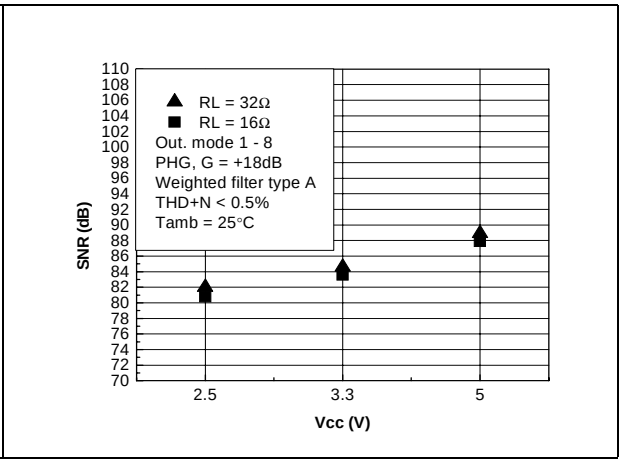


Figure 50. Frequency response

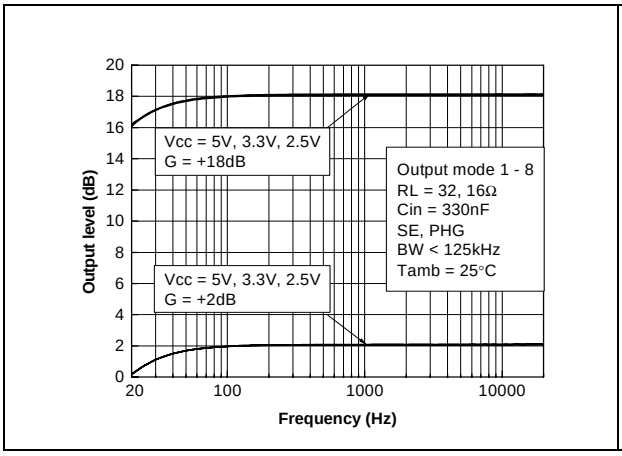


Figure 51. Current consumption versus power supply voltage

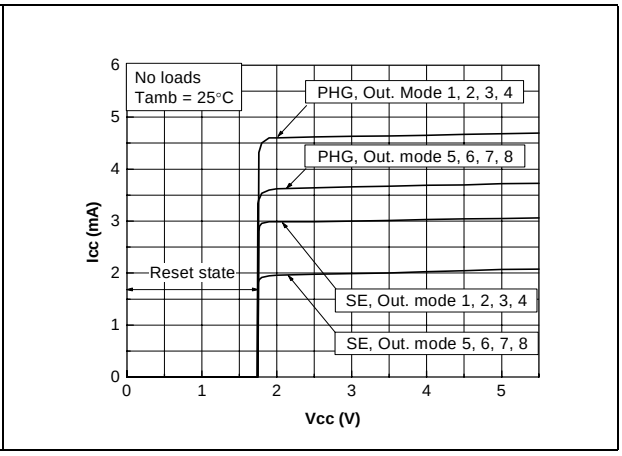


Figure 52. 3dB lower cut off frequency versus input capacitance

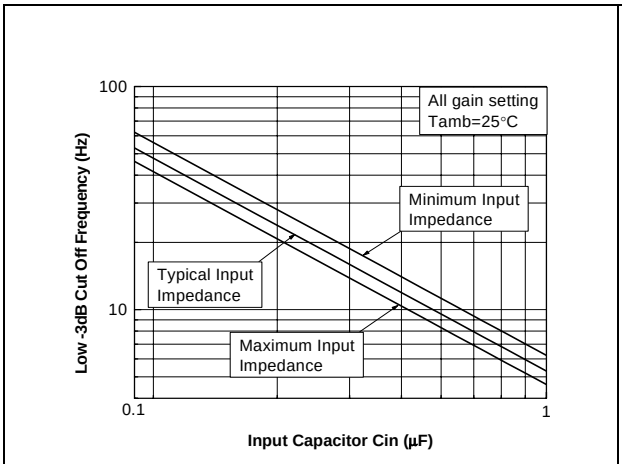


Figure 53. 3dB lower cut off frequency versus output capacitance

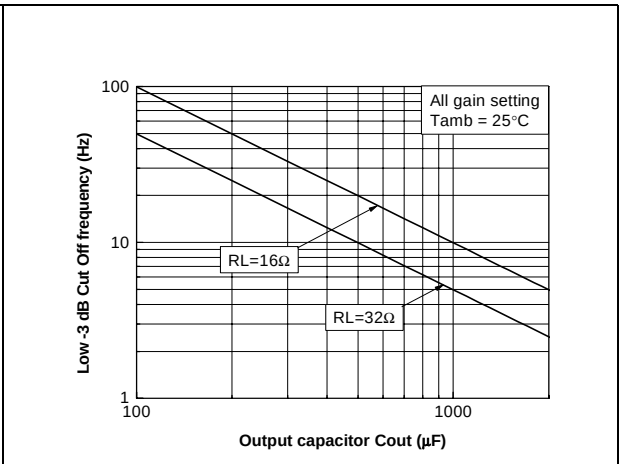


Figure 54. Power dissipation versus output power (one channel

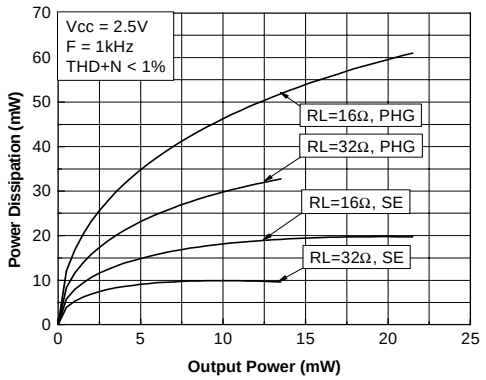


Figure 55. Power dissipation versus output power (one channel

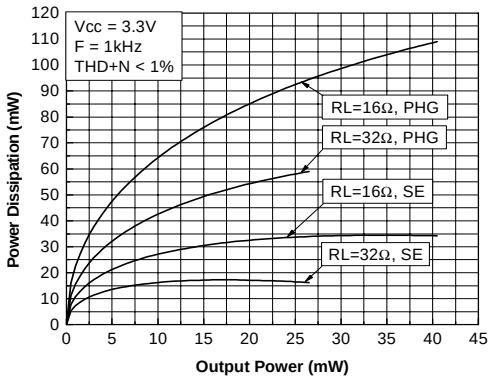


Figure 56. Power dissipation versus output power (one channel

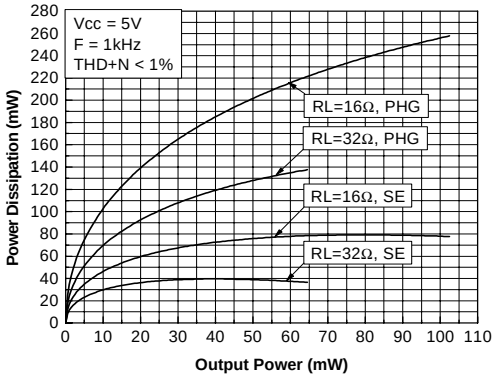
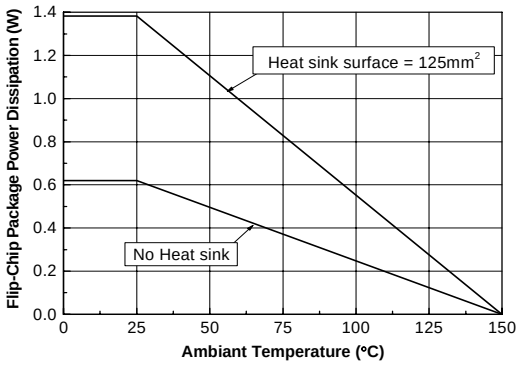


Figure 57. Power derating curves



4 Application Information

The TS4975 integrates 2 monolithic power amplifiers. The amplifier output can be configured as either SE (single-ended) capacitively-coupled output or PHG (phantom ground) output. *Figure 1 on page 3* shows schemas of these two configurations.

In a SE configuration an output capacitor, Cout, on each output is needed. This output coupling capacitor blocks the Vcc/2 voltage (to which the output amplifier is biased) and couples the audio signal to the load.

In a PHG configuration, internal buffers are connected to PHG1 and PHG2 pins biased to the Vcc/2 voltage, and output amplifiers are also biased to the Vcc/2 voltage. Therefore, no output capacitors are needed. The advantage of the PHG configuration is fewer external components compared with a SE configuration. However, note that the device has higher power dissipation (see Power dissipation and efficiency on page 22).

This chapter gives information on how to configure the TS4975 in application.

4.1 I²C bus interface

Table 8 summarizes the pin descriptions for the I²C bus interface.

Table 8. I²C bus interface pin descriptions

Pin	Functional Description
SDA	This is the serial data input pin
SCL	This is the clock input pin
ADD	User-setable portion of device's I2C address

4.1.1 I²C bus operation

The TS4975 uses a serial bus, which conforms to the I²C protocol, to control the chip's functions with two wires: Clock and Data. The Clock line is uni-directional. The Data line is bi-directional (open-collector) with an external chip pull-up resistor (typically 10 kOhm). The maximum clock frequency specified by the I²C standard is 400kHz.

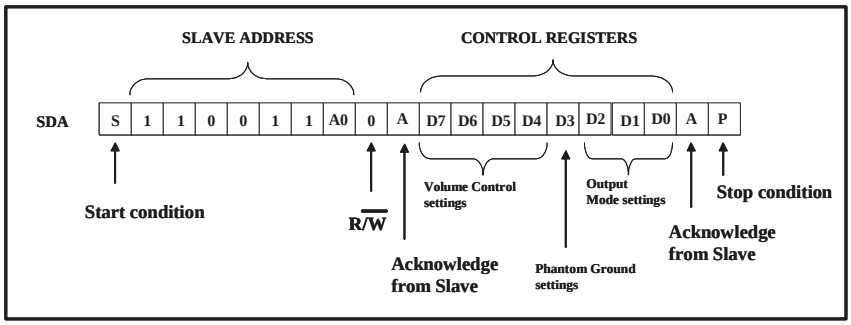
Table 9. Device slave address

A6	A5	A4	A3	A2	A1	A0	Rw
1	1	0	0	1	1	A0	X

The host MCU can write into the TS4975 control registers and read from the control registers. The slave address of the TS4975 for writing is CC or CE hex. In order to write data into the TS4975, after the "start" message, the MCU must send the following data:

- send the I²C address slave byte with a low level for the R/W bit
- send the data

Figure 58. I²C write operation



All bytes are sent with MSB bit first. The transfer of written data ends with a “stop” message. When transmitting several data, the data can be written with no need to repeat the “start” message and slave address.

The slave address of the TS4975 for reading is CD or CF hex. In order to read data from the TS4975, after the “start” message, the MCU must send and receive the following data:

- send the I²C address slave byte with a high level for the R/W bit
- receive the data (control register value)

All bytes are read with MSB bit first. The transfer of read data is ended with “stop” message. When transmitting several data, the data can be read with no need to repeat the “start” message and slave address. In this case the value of control register is read repeatedly.

When thermo shutdown or pop and click reduction is active, specific value is read from the TS4975 (See *4: Application Information on page 18*).

Table 10. Ouput mode selection: G from -34 dB to + 18dB (by steps of 4dB)(1)

Output Mode #	Headphone Output 1	Headphone Output 2
0	SD	SD
1	G x In1	G x In2
2	G x In2	G x In1
3	G x In1	G x In1
4	G x In2	G x In2
5	SD	G x In1
6	SD	G x In2
7	G x In1	SD
8	G x In2	SD

1. SD = Shutdown Mode
In1 = Audio Input 1
In2= Audio Input2
G = Gain from Audio Input 1and Input 2 to Output1 and Output2

4.1.2 Gain Register Operation

The gain of the TS4975 ranges from -34dB to +18 dB. At Power-up, both the right and left channels are set in Stand-by mode.

Table 11. Gain settings truth table

G: Gain (dB) #	D7 (MSB)	D6	D5	D4
-34	0	0	0	1
-30	0	0	1	0
-26	0	0	1	1
-22	0	1	0	0
-18	0	1	0	1
-14	0	1	1	0
-10	0	1	1	1
-6	1	0	0	0
-2	1	0	0	1
+2	1	0	1	0
+6	1	0	1	1
+10	1	1	0	0
+14	1	1	0	1
+18	1	1	1	0

Table 12. Output mode settings truth table

D3: PHG on / off	D2	D1	D0	COMMENTS
0	X	X	X	PHG **off**
1	x	x	x	PHG **on**
x	0	0	0	MODE 1
X	0	0	1	MODE 2
X	0	1	0	MODE 3
X	0	1	1	MODE4
X	1	0	0	MODE 5
X	1	0	1	MODE 6
X	1	1	0	MODE 7
X	1	1	1	MODE 8

Table 13. Stand-by mode I²C condition

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	X	X	X	X

Table 14. I²C control byte states

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	x	X	X	X	Undefined State

4.1.3 Acknowledge

The number of data bytes transferred between the start and the stop conditions from the CPU master to the TS4975 slave is not limited. Each byte of eight bits is followed by one acknowledge bit.

The TS4975 which is addressed, generates an acknowledge after the reception of each byte that has been clocked out.

4.2 Power dissipation and efficiency

Hypotheses:

- Voltage and current in the load are sinusoidal (Vout and Iout).
- Supply voltage is a pure DC source (Vcc).

Regarding the load we have:

$$V_{OUT} = V_{PEAK}\sin\omega t(V)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L}(A)$$

and

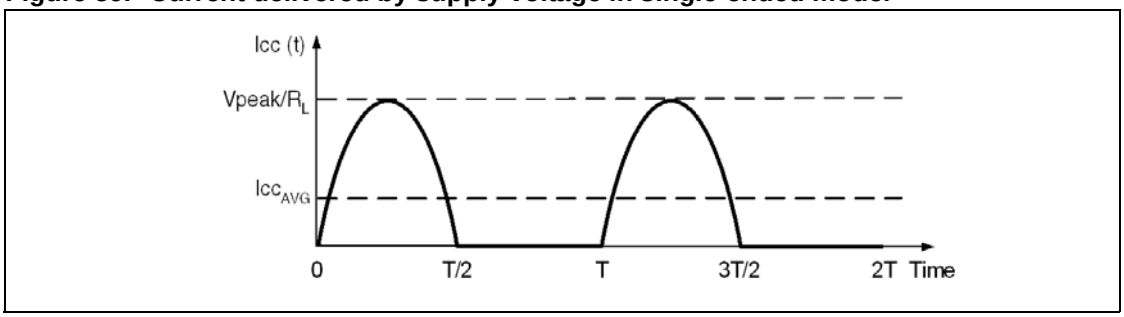
$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L}(A)$$

Single-ended configuration:

The average current delivered by the supply voltage is:

$$Icc_{AVG} = \frac{1}{2\pi}\int_0^{\pi}\frac{V_{PEAK}}{R_L}\sin(t)dt = \frac{V_{PEAK}}{\pi R_L}(A)$$

Figure 59. Current delivered by supply voltage in single-ended model



The power delivered by supply voltage is:

$$P_{supply} = V_{CC}I_{CC_{AVG}}(W)$$

So, the **power dissipation by each amplifier** is

$$P_{diss} = P_{supply} - P_{OUT}(W)$$

$$P_{diss} = \frac{\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - P_{OUT}(W)$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{OUT}} = 0$$

and its value is:

$$P_{diss_{MAX}} = \frac{V_{CC}^2}{\pi^2 R_L}(W)$$

Note: This maximum value depends only on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

$$\eta = \frac{P_{OUT}}{P_{supply}} = \frac{\pi V_{PEAK}}{2V_{CC}}$$

The maximum theoretical value is reached when Vpeak = Vcc/2, so

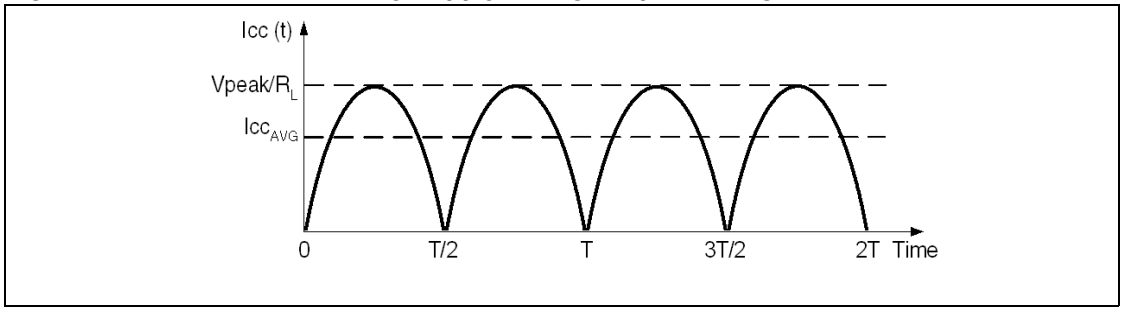
$$\eta = \frac{\pi}{4} = 78.5\%$$

Phantom ground configuration:

The average current delivered by the supply voltage is:

$$Icc_{AVG} = \frac{1}{\pi}\int_0^{\pi}\frac{V_{PEAK}}{R_L}\sin(t)dt = \frac{2V_{PEAK}}{\pi R_L}(A)$$

Figure 60. Current delivered by supply voltage in phantom ground mode



The power delivered by supply voltage is:

$$P_{supply} = V_{CC}I_{CC_{AVG}}(W)$$

Then, the power dissipation by each amplifier is

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - P_{OUT}(W)$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{OUT}} = 0$$

and its value is:

$$P_{diss_{MAX}} = \frac{2V_{CC}^2}{\pi^2 R_L}(W)$$

Note: This maximum value depends only on power supply voltage and load values.

The efficiency is the ratio between the output power and the power supply:

$$\eta = \frac{P_{OUT}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when Vpeak = Vcc/2, so

$$\eta = \frac{\pi}{8} = 39.25\%$$

The TS4975 is stereo amplifier so it has two independent power amplifiers. Each amplifier produces heat due to its power dissipation. Therefore the maximum die temperature is the sum of each amplifier's maximum power dissipation. It is calculated as follows:

- $P_{diss\ 1}$ = Power dissipation due to the first channel power amplifier.
- $P_{diss\ 2}$ = Power dissipation due to the second channel power amplifier.
- *Total* $P_{diss} = P_{diss\ 1} + P_{diss\ 2}$ (W)

In most cases, $P_{diss\ 1} = P_{diss\ 2}$, giving:

$$TotalP_{diss} = 2P_{diss1}$$

Single ended configuration:

$$TotalP_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - 2P_{OUT}(W)$$

Phantom ground configuration:

$$TotalP_{diss} = \frac{4\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - 2P_{OUT}(W)$$

4.3 Low frequency response

Input capacitor Cin

The input coupling capacitor blocks the DC part of the input signal at the amplifier input. In the low-frequency region, Cin starts to have an effect. Cin with Zin forms a first-order, high-pass filter with -3 dB cut-off frequency.

$$F_{CL} = \frac{1}{2\pi Z_{in} C_{in}}(Hz)$$

Zin is the input impedance of the corresponding input (30 kΩ for In1 & In2).

Note: For all inputs, the impedance value remains for all gain settings. This means that the lower cut-off frequency doesn't change with gain setting. Note also that 30 kΩ is a typical value and there is tolerance around this value (see 3: Electrical Characteristics on page 4).

In *Figure 50* you could easily establish the Cin value for a -3dB cut-off frequency required.

Output capacitor Cout

In single-ended mode the external output coupling capacitors Cout are needed. This coupling capacitor Cout with the output load RL also forms a first-order high-pass filter with -3 dB cut off frequency.

$$F_{CL} = \frac{1}{2\pi R_L C_{out}} (Hz)$$

See *Figure 51* to establish the Cout value for a -3dB cut-off frequency required.

These two first-order filters form a second-order high-pass filter. The -3 dB cut-off frequency of these two filters should be the same, so the following formula should be respected:

$$\frac{1}{2\pi Z_{in} C_{in}} \cong \frac{1}{2\pi R_L C_{out}}$$

4.4 Decoupling of the circuit

Two capacitors are needed to properly bypass the TS4975 — a power supply capacitor Cs and a bias voltage bypass capacitor Cb.

Cs has a strong influence on the THD+N in high frequency (above 7kHz) and indirectly on the power supply disturbances.

With 1 µF, you could expect similar THD+N performances like shown in the datasheet.

If Cs is lower than 1 µF, THD+N increases in high frequency and disturbances on power supply rail are less filtered.

To the contrary, if Cs is higher than 1 µF, those disturbances an the power supply rail are more filtered.

Cb has an influence on THD+N in lower frequency, but its value is critical on the final result of PSRR with input grounded in lower frequency:

- If Cb is lower than 1 µF, THD+N increases at lower frequencies and the PSRR worsens upwards.
- If Cb is higher than 1 µF, the benefit on THD+N and PSRR in the lower frequency range is small.

The value of Cb also has an influence on startup time.

4.5 Power-on reset

When power is applied to Vdd, an internal Power On Reset holds the TS4975 in a reset state until the supply voltage reaches its nominal value.

The Power On Reset has a typical threshold of 1.75V.

4.6 Notes on PSRR measurement

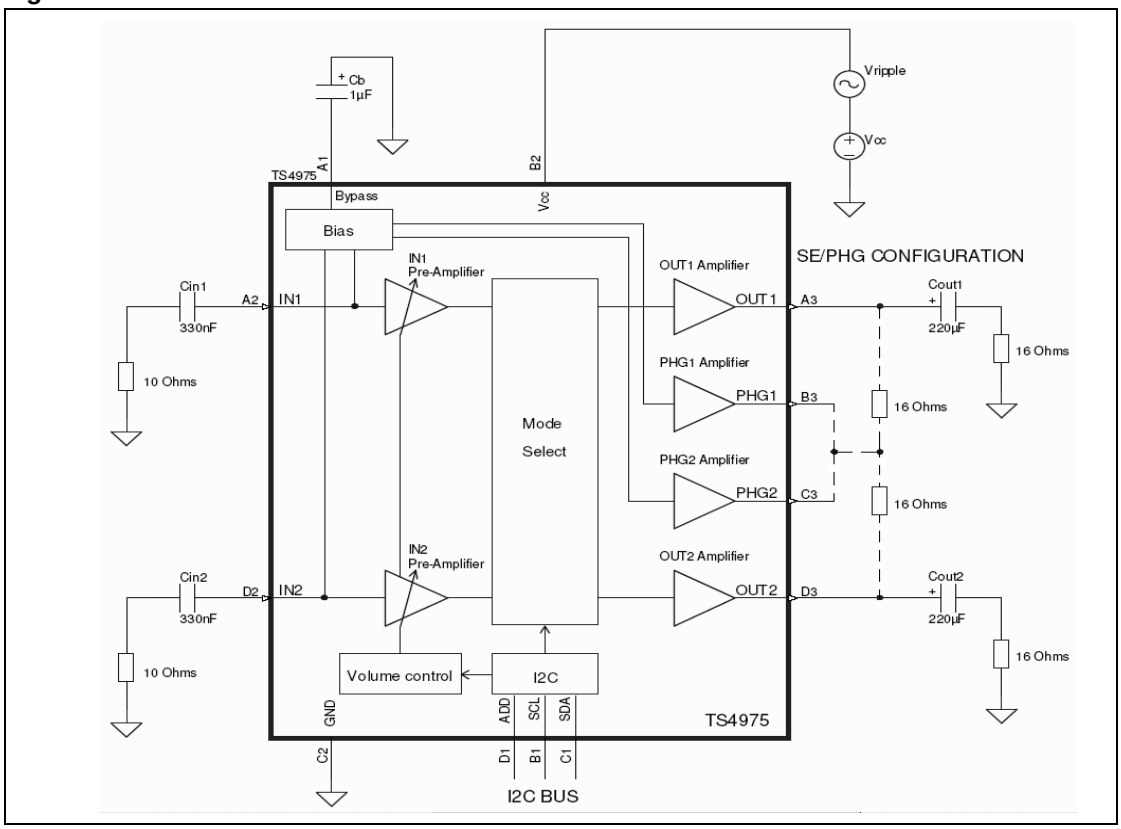
What is PSRR?

The PSRR is the Power Supply Rejection Ratio. The PSRR of a device is the ratio between a power supply disturbance and the result on the output. In other words, the PSRR is the ability of a device to minimize the impact of power supply disturbance to the output.

How we measure the PSRR?

The PSRR was measured according to the schematic shown in *Figure 61*.

Figure 61. PSRR measurement schematic



Principles of operation

- The DC voltage supply (Vcc) is fixed
- The AC sinusoidal ripple voltage (Vripple) is fixed
- No bypasss capacitor Cs is used

The PSRR value for each frequency is calculated as:

$$PSRR = 20Log\left[\frac{RMS_{(Output)}}{RMS_{(Vripple)}}\right](dB)$$

RMS is a rms selective measurement.

4.7 Startup time

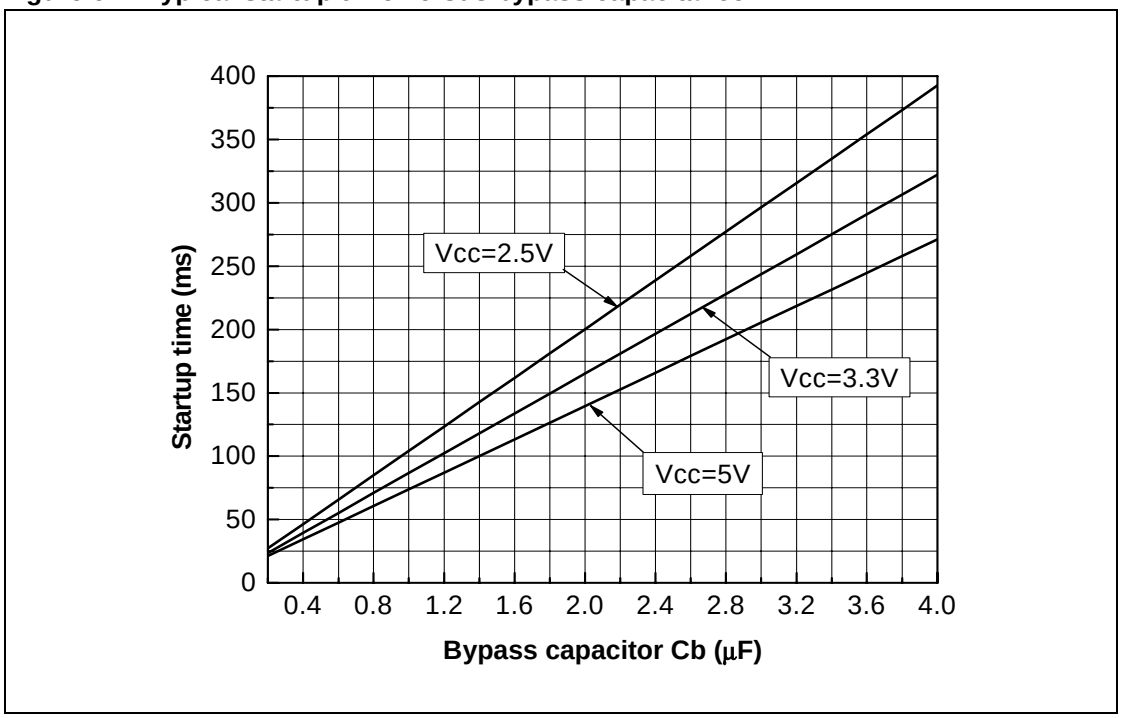
When the TS4975 is controlled to switch to full standby (output mode 0) to another output mode, a delay is necessary to stabilize the DC bias.This length of this delay depends on the Cb and Vcc values. A typical value can be calculated by following formula:

$$t_{wu} = C_b \times \frac{V_{CC}}{V_{CC} - 1.2} \times 50000 + 0.008(s)$$

This formula assumes that Cb voltage is equal to 0 V. If the Cb voltage is not equal 0 V, the startup time will be always lower.

In *Figure 50* you could easily establish typical startup time for given supply voltage and bypass capacitor Cb.

Figure 62. Typical startup time versus bypass capacitance



4.8 Pop and click performance

The TS4975 has internal pop and click reduction circuitry which eliminates the output transients, for example during switch-on or switch-off phases, during a switch from an output mode to another or during change in volume. The performance of this circuitry is closely linked to the values of the input capacitor Cin, the output capacitor Cout (for Single-Ended configuration) and the bias voltage bypass capacitor Cb.

The value of Cin and Cout is determined by the the lower cut-off frequency value requested. The value of Cb will affect the THD+N and PSRR values in lower frequencies.

The TS4975 is optimized to have a low pop and click in the typical schematic configuration (see *Figure 1 on page 3* SE and PHG configurations).

During the device start-up period when the pop and click reduction is active, the value FX hex (1111xxxx bin) can be read from the internal device registry.

Once the device is fully operational and the pop and click is inactive, the last value of control register can be read.

4.9 Thermo shutdown

The TS4975 device has internal protection in case of over temperature by thermal shutdown. Thermal shutdown is active when the device reaches temperature 150°C.

When thermo shutdown protection is active, value FX hex (1111xxxx bin) can be read from the internal device registry.

When thermo shutdown protection state disappears, the last value of control register can be read.

4.10 Demoboard

A demoboard for the TS4975 is available.

For more information about this demoboard, please refer to **Application Note AN2151**, which can be found on **www.st.com.**

Figure 60 shows the schematic of the demoboard. *Figure 61*, *Figure 62* and *Figure 64* show the component locations, top layer and bottom layer respectively.

Figure 63. Demoboard schematic

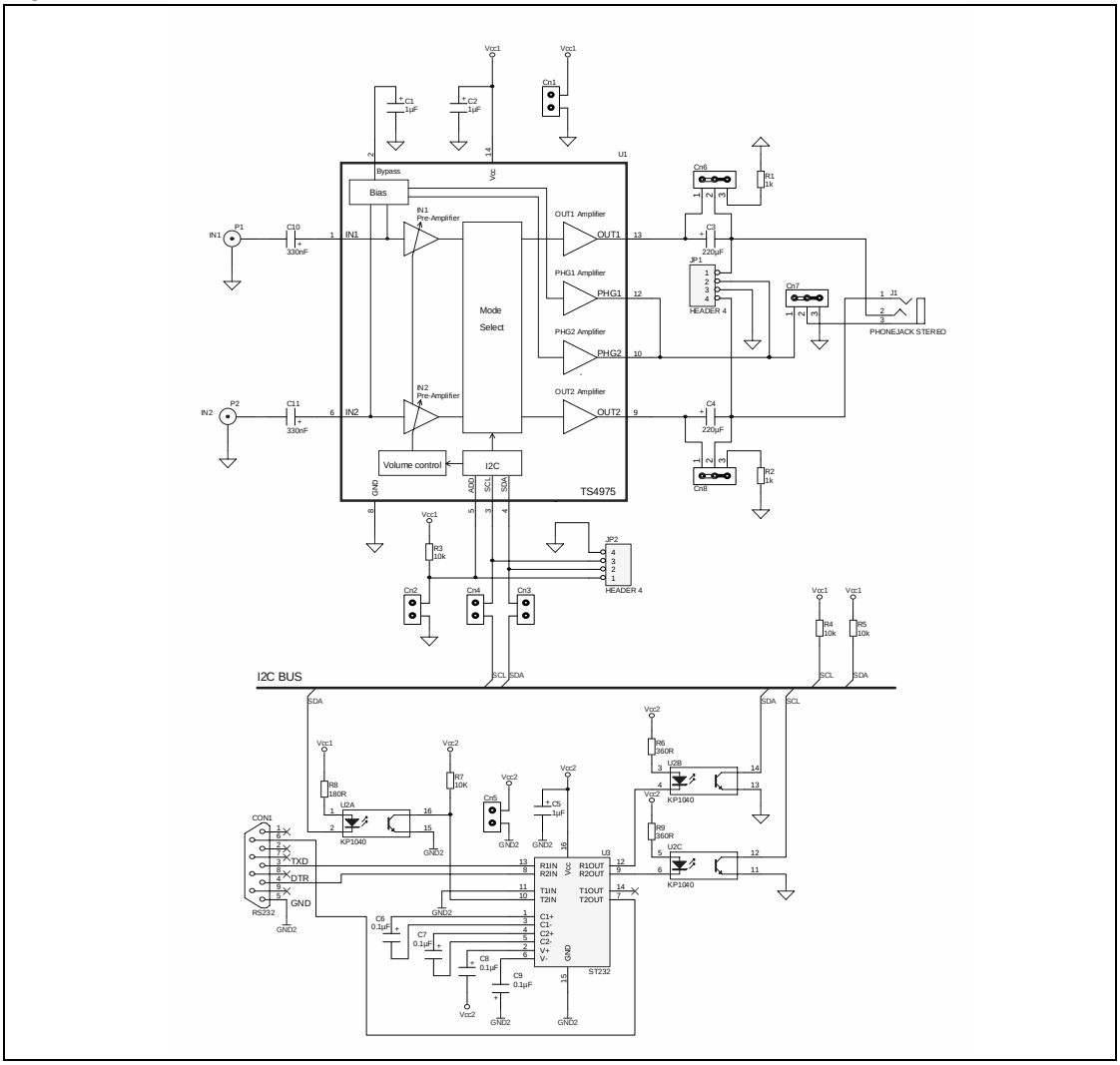


Figure 64. Bottom layer

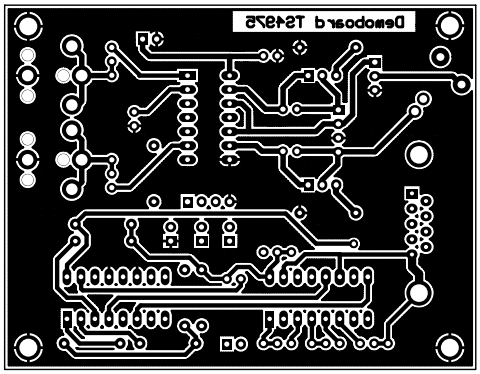


Figure 65. Top layer

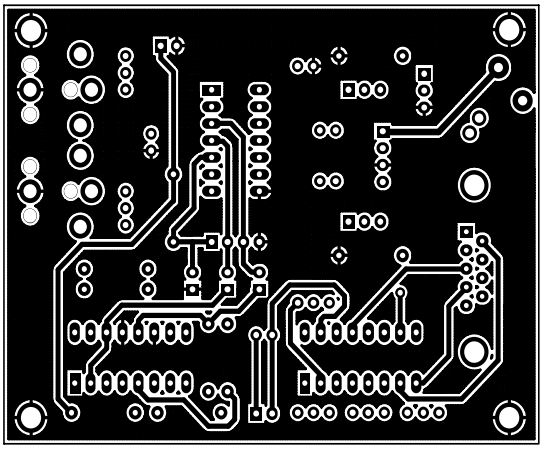
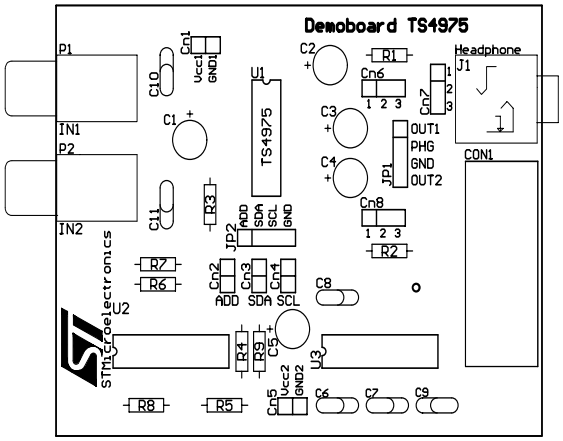


Figure 66. Componens location



5 Package Mechanical Data

Figure 67. TS4975 Footprint Recommendation

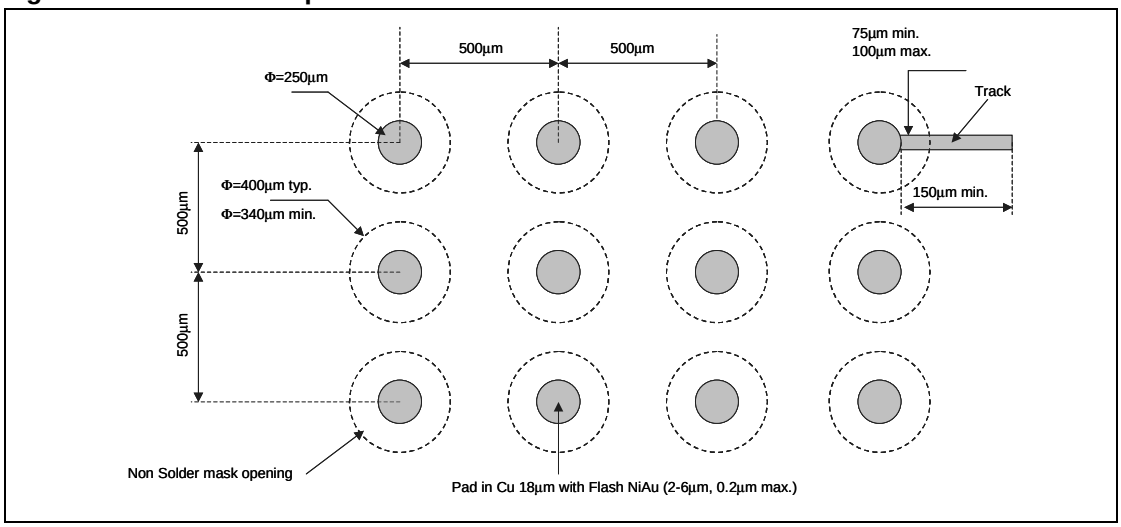


Figure 68. Pin out (top view)

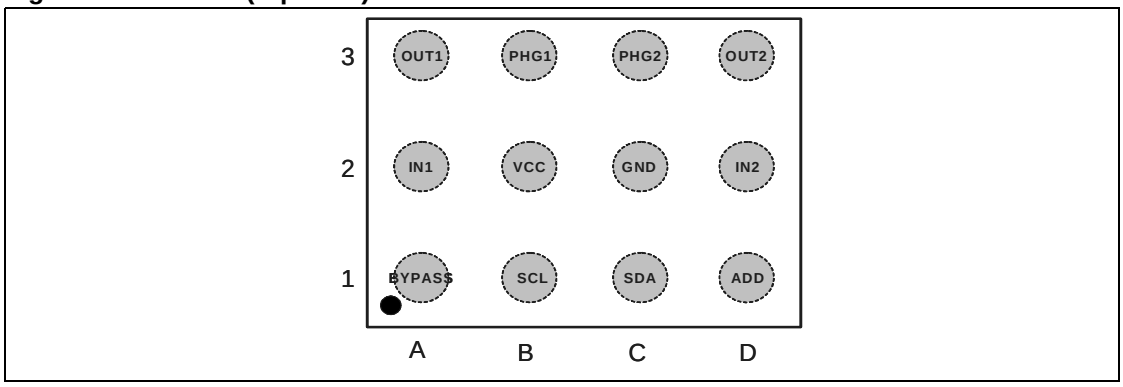


Figure 69. Marking (top view)

- Logo: ST
- Part Number: A75
- Date Code: YWW
- The Dot is for marking pin A1
  - E Lead Free symbol

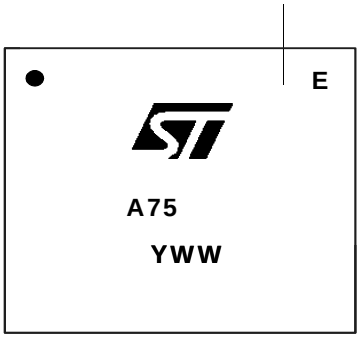
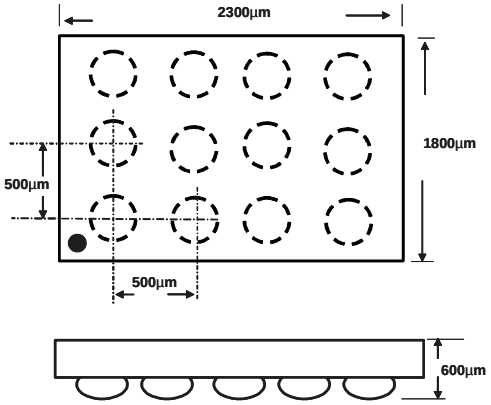
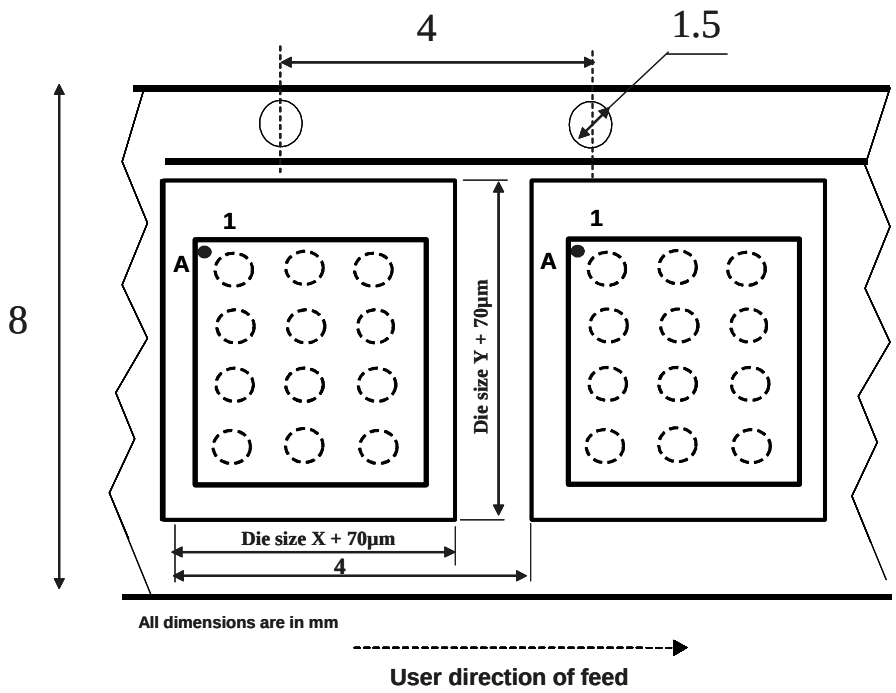


Figure 70. Flip-chip - 12 bumps



- Die size: 2.3mm x 1.8mm ± 30µm
- Die height (including bumps): 600µm
- Bumps diameter: 315µm ±50µm
- Bump diameter before reflew: 300µm ±10µm
- Bumps height: 250µm ±40µm
- Die height: 350µm ±20µm

Figure 71. Tape & reel specification (top view)



6 Revision History

Date	Revision	Changes
November-2004	1	Initial release.
July 2005	2	Product in full production