Features

- TS68000/TS68008 Microprocessor Core Supporting a 16- or 8-bit TS68000 Family
- System Integration Block Including:
  - Independent Direct Memory Access (IDMA) Controller
  - Interrupt Controller with Two Modes of Operation
  - Parallel Input/output (I/O) Ports, some with Interrupt Capability
  - On-chip Usable 1152 bytes of Dual-port Random-access Memory (RAM)
  - Three Timers, including a Watchdog Timer
  - Four Programmable Chip-select Lines with Wait-state Logic
  - Programmable Address Mapping of Dual-port RAM and IMP Registers
  - On-chip Clock Generator with an Output Clock Signal
  - System Control:
    - System Control Register
    - Bus Arbitration Logic with Low Interrupt Latency Support
    - Hardware Watchdog for Monitoring Bus Activity
    - Low Power (Standby) Modes
    - Disable CPU Logic (TS68000)
    - Freeze Control for Debugging Selected On-chip Peripherals
    - DRAM Refresh Controller
- Communications Processor Including:
  - Main Controller (RISC Processor)
  - Three Full-duplex Serial Communication Controllers (SCCs)
  - Six Serial Direct Memory Access (SDMA) Channels Dedicated to the Three SCCs
  - Flexible Physical Interface Accessible by SCCs for Interchip Digital Link (IDL) General Circuit Interface (GCI, see note), Pulse Code Modulation (PCM), and Nonmultiplexed Serial Interface (NMSI) Operation
  - Serial Communication Port (SCP) for Synchronous Communication, Clock Rate up to 4.096 MHz
  - Serial Management Controllers (SMCs) for IDL and GCI Channels
- Frequency of Operation: 16.67 MHz
- Power Supply: 5 V_{DC} ± 10%

Description

The IMP is a very large-scale integration (VLSI) device incorporating the main building blocks needed for the design of a wide variety of controllers. The device is especially suitable to applications in the communications industry. The IMP is the first device to offer the benefits of a closely coupled, industry-standard, TS68000/TS68008 microprocessor core and a flexible communications architecture. This multichannel communications device may be configured to support a number of popular industry interfaces, including those for the integrated services digital network (ISDN) basic rate and terminal adapter applications. Through a combination of architectural and programmable features, concurrent operation of different protocols is easily achieved using the IMP. Data concentrators, line cards, bridges, and gateways are examples of suitable applications for this versatile device.

The IMP is a high-density complementary metal-oxide semiconductor (HCMOS) device consisting of a TS68000/TS68008 microprocessor core, a system integration block (SIB), and a communications processor (CP). The TS68302 block diagram is shown in Figure 1.

Note: GCI is sometimes referred to as IOM2.

Integrated Multiprotocol Processor (IMP)

TS68302

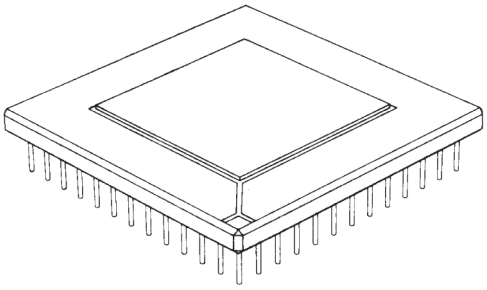
Rev. 2117A–HIREL–11/02

Screening/Quality

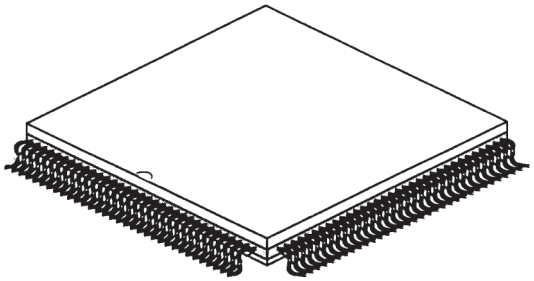
This product is manufactured in full compliance with either:

- MIL-STD-883 (class B)
- DESC. Drawing 5962-93159
- Or according to Atmel standards

R suffix
PGA 132
(Ceramic Pin Grid Array)



A suffix
CERQUAD 132
(Ceramic Quad Flat Pack)



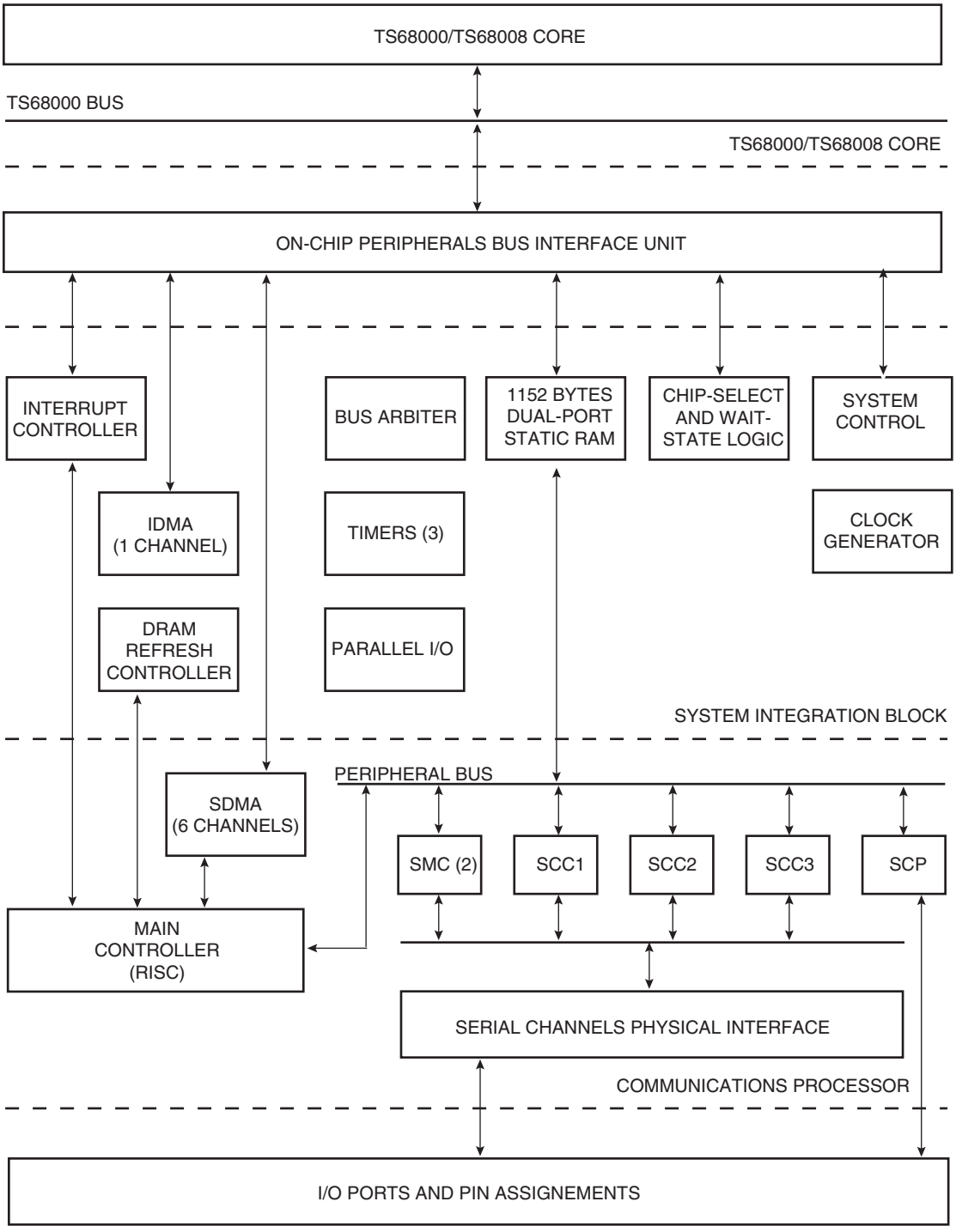
Introduction

The TS68302 integrated multiprotocol processor (IMP) is a very large-scale integration (VLSI) device incorporating the main building blocks needed for the design of a wide variety of controllers. The device is especially suitable to applications in the communications industry. The IMP is the first device to offer the benefits of a closely coupled, industry-standard TS68000 microprocessor core and a flexible communications architecture. The IMP may be configured to support a number of popular industry interfaces, including those for the Integrated Services Digital Network (ISDN) basic rate and terminal adapter applications. Concurrent operation of different protocols is easily achieved through a combination of architectural and programmable features. Data concentrators, line cards, bridges, and gateways are examples of suitable applications for this device.

The IMP is a high-density complementary metal-oxide semiconductor (HCMOS) device consisting of a TS68000 microprocessor core, a system integration block (SIB), and a communications processor (CP).

Figure 1 is a block diagram of the TS68302. The processor can be divided into two main sections: the bus controller and the micromachine. This division reflects the autonomy with which the sections operate.

Figure 1. TS68302 Block Diagram



Pin Assignments

Figure 2. PGA Terminal Designation

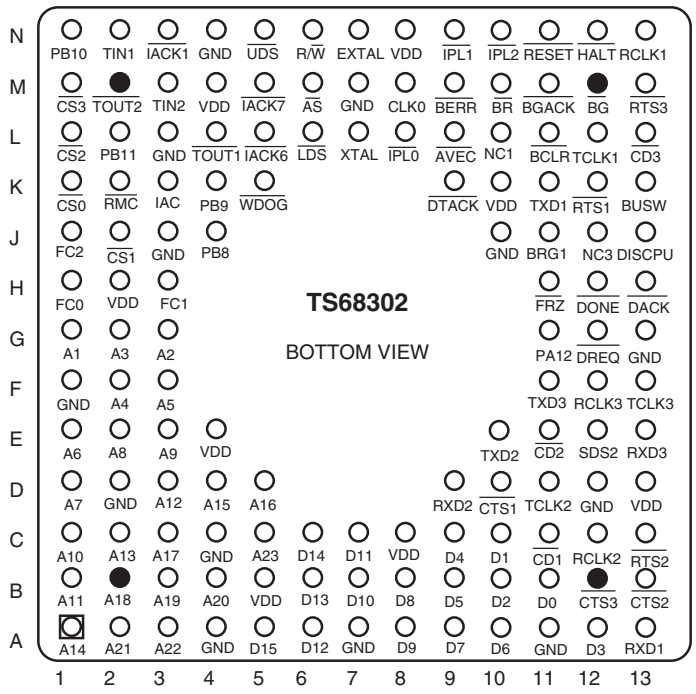


Figure 3. CERQUAD Terminal Designation

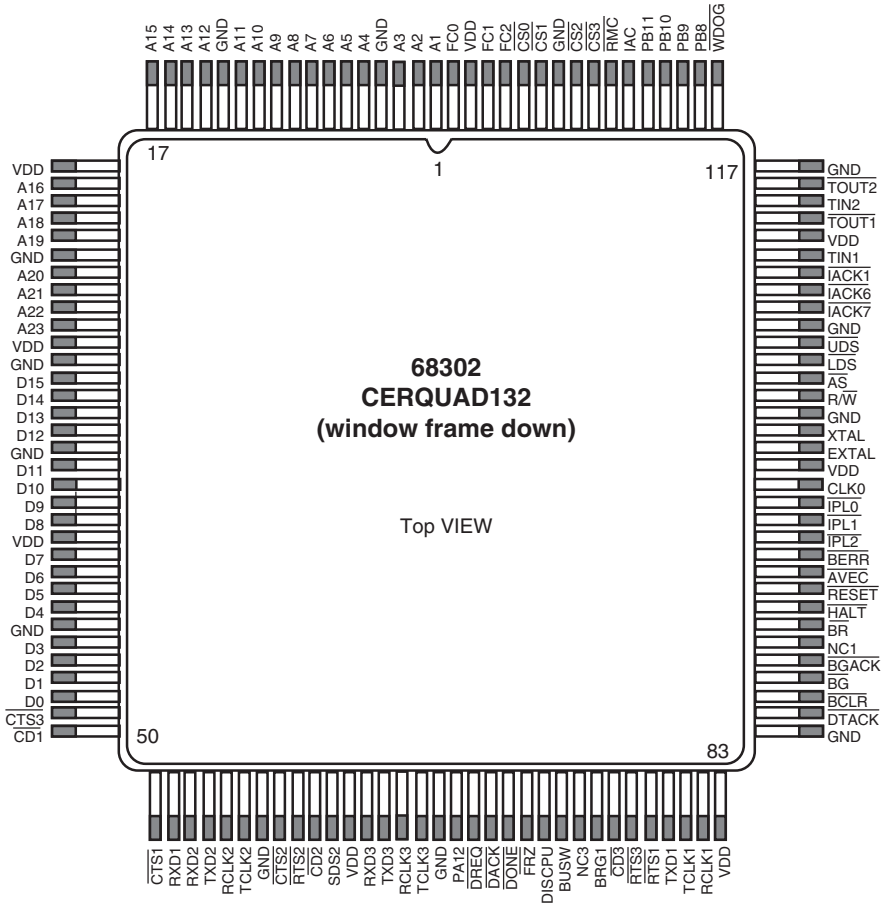
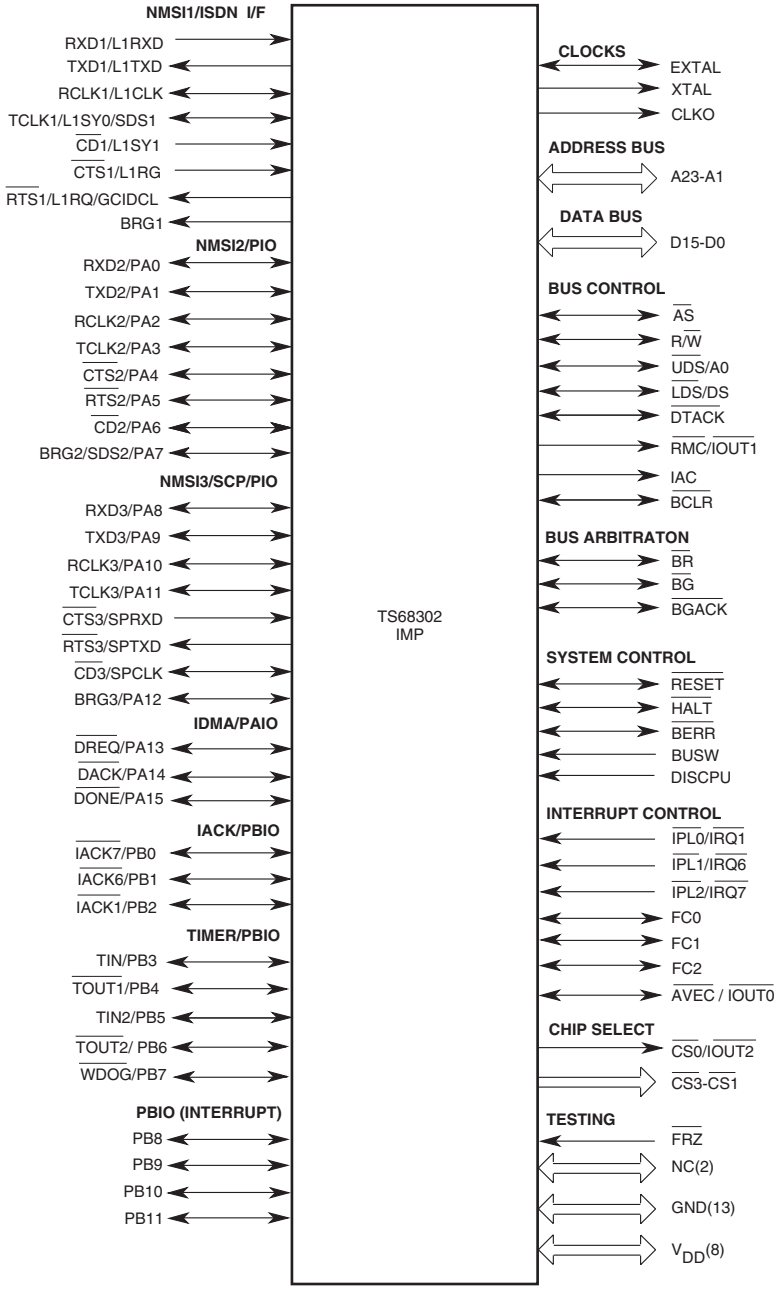


Figure 4. Functional Signal Groups



Signal Descriptions

The input and output signals of the TS68302 are organized into functional groups as shown in Table 1. Refer to TS68302 Integrated Multiprotocol Processor User's Manual, for detailed information on the TS68302 signals.

Table 1. Signal Definitions

Functional Group	Signals	Number
Clocks	XTAL, EXTAL, CLKO	3
System Control	$\overline{\text{RESET}}$, $\overline{\text{HALT}}$, $\overline{\text{BERR}}$, BUSW, DISCPU	5
Address Bus	A23-A1	23
Data Bus	D15-D0	16
Bus Control	$\overline{\text{AS}}$, R/$\overline{\text{W}}$, $\overline{\text{UDS}}$/A0, $\overline{\text{LDS}}$/$\overline{\text{DS}}$, $\overline{\text{DTACK}}$	5
Bus Control	$\overline{\text{RMC}}$, IAC, $\overline{\text{BCLR}}$	3
Bus Arbitration	$\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{BGACK}}$	3
Interrupt Control	$\overline{\text{IPL2}}$-$\overline{\text{IPL0}}$, FC2-FC0, $\overline{\text{AVEC}}$	7
NMSI1/ISDN I/F	RXD, TXD, RCLK, TCLK, $\overline{\text{CD}}$, $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, BRG1	8
NMSI2/PIO	RXD, TXD, RCLK, TCLK, $\overline{\text{CD}}$, $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, SDS2	8
NMSI3/SCP/PIO	RXD, TXD, RCLK, TCLK, $\overline{\text{CD}}$, $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, PA12	8
IDMA/PAIO	$\overline{\text{DREQ}}$, $\overline{\text{DACK}}$, $\overline{\text{DONE}}$	3
IACK/PBIO	$\overline{\text{IACK7}}$, $\overline{\text{IACK6}}$, $\overline{\text{IACK1}}$	3
Timer/PBIO	TIN2, TIN1, $\overline{\text{TOUT2}}$, $\overline{\text{TOUT1}}$, $\overline{\text{WDOG}}$	5
PBIO	PB11-PB8	4
Chip Select	$\overline{\text{CS3}}$-$\overline{\text{CS0}}$	4
Testing	$\overline{\text{FRZ}}$ (2 Spare)	3
V_{DD}	Power supply	8
GND	Ground connection	13

Scope

This drawing describes the specific requirements for the processor TS68302, 16.67 MHz, in compliance either with MIL-STD-883 class B or with Atmel standards.

Applicable Documents

MIL-STD-883

1. MIL-STD-883: test methods and procedures for electronics.
2. MIL-M-38535: general specifications for microcircuits.
3. Desc Drawing: 5962-93159 (planned).

Requirements

General

The microcircuits are in accordance with the applicable document and as specified herein.

Design and Construction

Terminal Connections

Depending on the package, the terminal connections shall be as shown in Figure 2 and Figure 3.

Lead Material and Finish

Lead material and finish shall be any option of MIL-M-38535.

Package

The macrocircuits are packaged in hermetically sealed ceramic packages, which conform to case outlines of MIL-M-38535 appendix A (when defined):

- 132-pin Ceramic Pin Grid Array (PGA),
- 132-pin Ceramic Quad Flat Pack (CERQUAD).

The precise case outlines are described in Figure 2 and Figure 3.

Electrical Characteristics

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
P_D	Power Dissipation (typical at 16.67 MHz)(1)	53	64	mA
P_D	Power Dissipation (typical at 8 MHz)(1)	26	31	mA
LP_D	Low Power Mode Dissipation (typical at 16.67 MHz)(2)		36	mA
LP_D	Lowest Power Mode Dissipation (typical at 16.67 MHz)(3)		32	mA
LP_D	Lowest Power Mode Dissipation (typical at 50 MHz)(4)		1	mA

Notes:
1. The values shown are typical. The typical value varies as shown, based on how many IMP on-chip peripherals are enabled and the rate at which they are clocked.
2. LPREC = 0. Divider = 2.
3. LPREC = 1. Divider = 1024.
4. The stated frequency must be externally applied to EXTAL only after the IMP has been placed in the lowest power mode with LPREC = 1. The 68000 core is not specified to operate at this frequency, but the rest of the IMP is. In this configuration, the user does not divide the clock internally using the LPCD4-LPCD0 bits in the system control register.

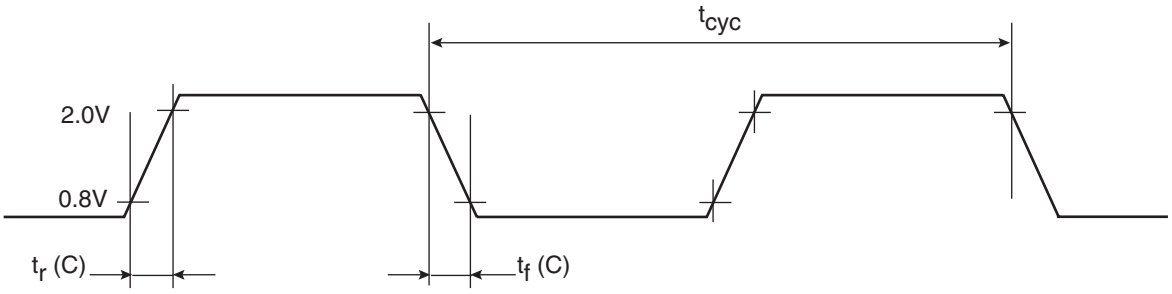
Unless otherwise stated, all voltages are referenced to the reference terminal (see Table 1).

Table 3. Recommended Condition of Use

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Low Level Input Voltage	-0.3	+0.5	V
V_{IH}	High Level Input Voltage	2.4	5.5	V
T_{case}	Operating Temperature	-55	+125	°C
$t_r(c)$	Clock Rise Time - See Figure 5		5	ns
$t_f(c)$	Clock Fall Time Resistance - Figure 5		5	ns
f_c	Clock Frequency - See Figure 5	8	16.67	MHz
t_{cyc}	Cycle Time - See Figure 5	60	125	ns

This device contains protective circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD}).

Figure 5. Clock Input Timing Diagram



Note: Timing measurements are referenced to and from a low voltage of 0.8V and a voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise or fall will be linear between 0.8V and 2.0V.

Table 4. Thermal Characteristics at 25°C

Package	Symbol	Parameter	Value	Unit
PGA 132	θ_{JA}	Thermal Resistance - Ceramic Junction To Ambient	33	°C/W
	θ_{JC}	Thermal Resistance - Ceramic Junction To Case	5	°C/W
CERQUAD 132	θ_{JA}	Thermal Resistance - Ceramic Junction To Ambient	46	°C/W
	θ_{JC}	Thermal Resistance - Ceramic Junction To Case	2	°C/W

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad \textbf{(1)}$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \cdot V_{CC}$, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output pins - user determined

Note: For T_A = 70°C and P_D = 0.5 W at 12.5 MHz T_j = 88°C.

For most applications $P_{I/O} < 0{,}30\ P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273) \quad \textbf{(2)}$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273) + \theta_{JA} \cdot P_D 2 \quad \textbf{(3)}$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad \textbf{(4)}$$

θ_{JC} is device-related and cannot be influenced by the user. However, θ_{CA} is user-dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

Mechanical and Environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or Atmel standards.

Marking

The document that defines the marking is identified in the related reference documents. Each microcircuit is legible and permanently marked with the following information as minimum:

- Atmel Logo
- Manufacturer's part number
- Class B identification
- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

Quality Conformance Inspection

DESC/MIL-STD-883

Those quality levels are in accordance with MIL-M-38535 and method 5005 of MIL-STD-883. Groups A and B inspections are performed on each production lot. Groups C and D inspection are performed on a periodical basis.

Electrical Characteristics

General Requirements

All static and dynamic electrical characteristics specified. For inspection purposes, refer to relevant specification:

- DESC see "DESC/MIL-STD-883" on page 9

Table 5 and Table 6: Static Electrical Characteristics for all electrical variants. Test methods refer to IEC 748-2 method number, where existing.

Table 7 and Table 8: Dynamic Electrical Characteristics. Test methods refer to this specification.

Table 5. DC Electrical Characteristics

V_{CC} = 5.0 V_{dc} ± 10%; GND = 0 V_{dc}; Tc = -55°C/+125°C or -40°C/+85°C

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input High Voltage (except EXTAL)	2.0	V_{DD}	V
V_{IL}	Input Low Voltage (except EXTAL)	V_{SS} - 0.3	0.8	V
V_{CIH}	Input High Voltage (EXTAL)	4.0	V_{DD}	V
V_{CIL}	Input Low Voltage (EXTAL)	V_{SS} - 0.3	0.6	V
I_{IN}	Input Leakage Current		20	µA
C_{IN}	Input Capacitance All Pins		15	pF
I_{TSI}	Three-state Leakage Current (2.4V/0.5V)		20	µA
I_{OD}	Open Drain Leakage Current (2.4V)		20	µA
V_{OH}	Output High Voltage (I_{OH} = 400 µA)	V_{DD} - 1.0		V
V_{OL}	Output Low Voltage			
	(I_{OL} = 3.2 mA) A1-A23, PB0-PB11, FC0-FC3, $\overline{CS0}$-$\overline{CS3}$, IAC, $\overline{AVEC}$, BG, RCLK1, RCLK2, RCLK3, TCLK1, TCLK2, TCLK3, $\overline{RTS1}$, $\overline{RTS2}$, $\overline{RTS3}$, SDS2, PA12, RXD2, RXD3, $\overline{CTS2}$, $\overline{CD2}$, $\overline{CD3}$, $\overline{DREQ}$		0.5	V
	(I_{OL} = 5.3 mA) $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$, $\overline{BERR}$, $\overline{BGACK}$, $\overline{BCLR}$, $\overline{DTACK}$, $\overline{DACK}$, $\overline{RMC}$, $\overline{RMC}$, D0-D15, $\overline{RESET}$		0.5	V
	(I_{OL} = 7.0 mA) TXD1, TXD2, TXD3		0.5	V
	(I_{OL} = 8.9 mA) $\overline{BR}$, $\overline{DONE}$, $\overline{HALT}$, ($\overline{BR}$ as output)		0.5	V
	(I_{OL} = 3.2 mA) CLKO		0.4	V
O_{CLK}	Output Drive CLKO		50	pF
O_{GCI}	Output Drive ISDN I/F (GCI mode)		150	pF
O_{ALL}	Output Drive All Other Pins		130	pF

Table 6. DC Electrical Characteristics - NMSI1 in IDL mode

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DD}	Power		4.5	5.0	5.5	V
V_{SS}	Common		0	0	0	V
T	Temperature	Operating range	-55	25	+125	°C
Input Pin Characteristics: L1CLK, L1SY1, L1R x D, L1GR						
V_{IL}	Input Low Level Voltage	(% of V_{DD})	-10%		+20%	V
V_{IH}	Input High Level Voltage		V_{DD} - 20%		V_{DD} + 10%	V
I_{IH}	Input Low Level Current	$V_{in} = V_{SS}$			±10	µA
I_{IH}	Input High Level Current	$V_{in} = V_{DD}$			±10	µA
Output Pin Characteristics: L1T x D, SDS1-SDS2, L1RQ						
V_{OL}	Output Low Level Voltage	I_{OL} = 2.0 mA	0		0.50	V
V_{OH}	Output High Level Voltage	I_{OH} = 2.0 mA	V_{DD} - 0.5		V_{DD}	V

Dynamic (Switching) Characteristics

The limits and values given in this section apply over the full case temperature range -55°C to +125°C or -40°C to +85°C depending on selection see “Ordering Information” on page Reference 2 and VCC in the range 4.5V to 5.5V V_{IL} = 0.5V and V_{IH} = 2.4V.

The INTERVAL numbers (NUM) refer to the timing diagrams. See Figure 6 to Figure 25.

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock (CLKO pin) and possibly to one or more other signals.

Figure 6. Clock Timing Diagram

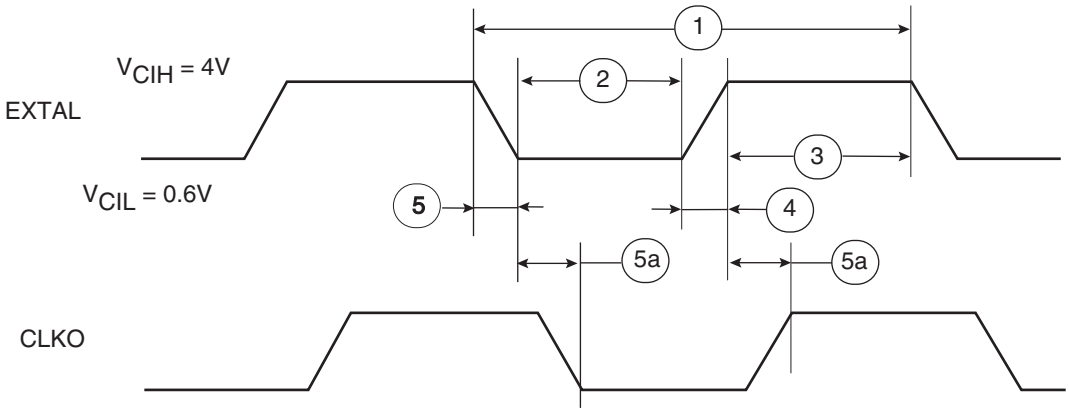


Table 7. AC Electrical Specifications - Clock Timing (see Figure 7)

Num.	Symbol	Parameter	Min	Max	Unit
	f	Frequency of Operation	8	16.67	MHz
1	t_{cyc}	Clock Period (EXTAL)	60	125	ns
2, 3	t_{CL}, t_{CH}	Clock Pulse Width (EXTAL)	25	62.5	ns
4, 5	t_{Cr}, t_{Cf}	Clock Rise and Fall Times (EXTAL)		5	ns
5a	t_{CD}	EXTAL to CLKO delay[1][2]	2	11	ns

Notes: 1. CLKO loading is 50 pF max.
2. CLKO skew from the rising and falling edges of EXTAL will not differ from each other more than 1 ns, if the EXTAL rise time equals the EXTAL fall time.

Table 8. AC Electrical Specifications
IMP Bus Master Cycles (see Figure 7, Figure 8 and Figure 9) f = 16.67 MHz

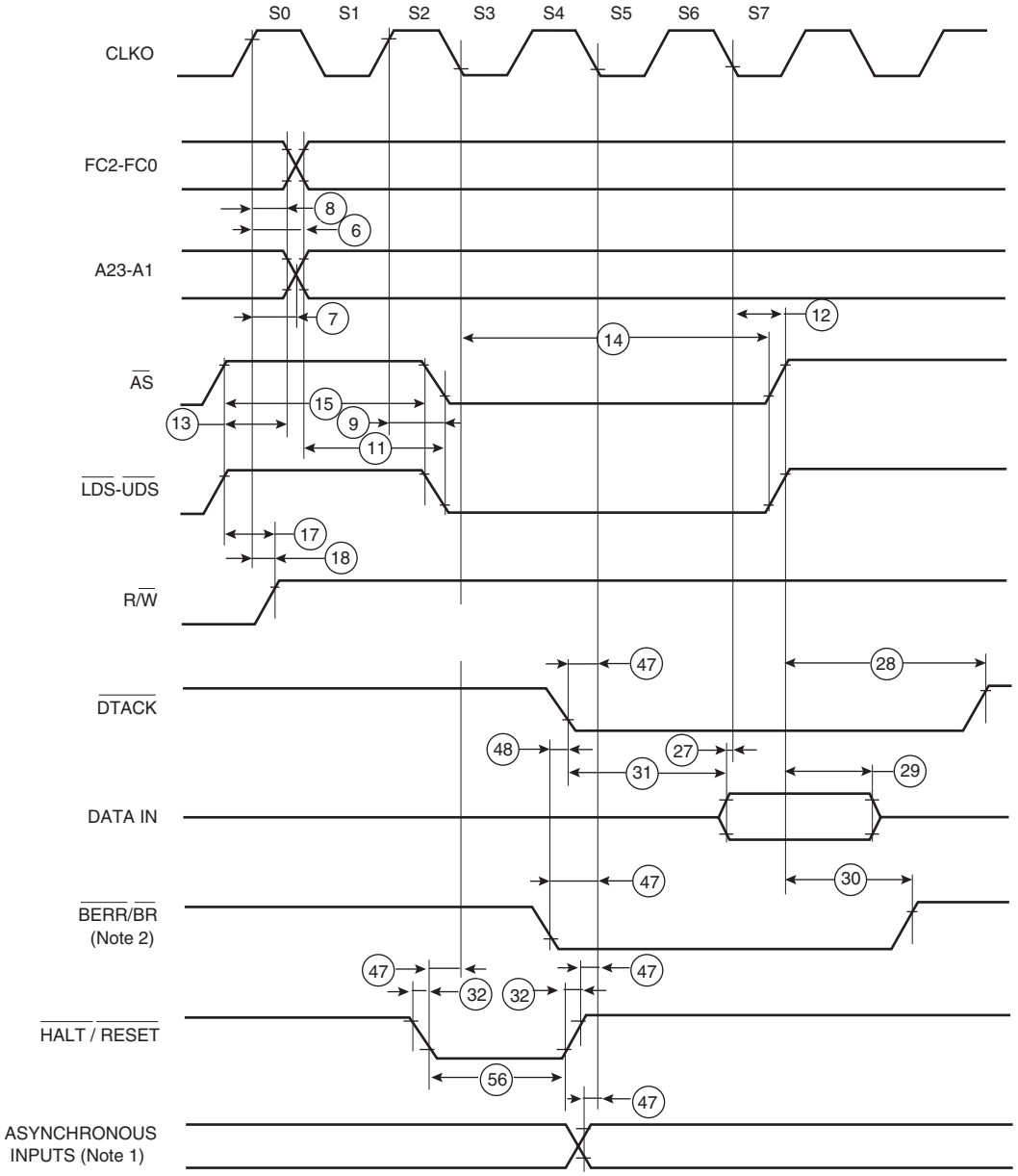
Num.	Symbol	Parameter	Min	Max	Unit
6	$t_{CHFCADV}$	Clock high to FC, address valid		45	ns
7	t_{CHADZ}	Clock high to address, data bus high impedance (maximum)		50	ns
8	t_{CHAFI}	Clock high to address, FC invalid (minimum)	0		ns
9	t_{CHSL}	Clock high to $\overline{AS}$, $\overline{DS}$ asserted(1)	3	30	ns
11	t_{AFCVSL}	Address, FC valid to $\overline{AS}$, $\overline{DS}$ asserted (read)/$\overline{AS}$ asserted (write)(2)	15		ns
12	t_{CLSH}	Clock low to $\overline{AS}$, $\overline{DS}$ negated(1)		30	ns
13	t_{SHAFI}	$\overline{AS}$, $\overline{DS}$ negated to address, FC invalid(2)	15		ns
14	t_{SL}	$\overline{AS}$ (and $\overline{DS}$ read) width asserted(2)	120		ns
14A	t_{DSL}	$\overline{DS}$ width asserted, write(2)	60		ns
15	t_{SH}	$\overline{AS}$, $\overline{DS}$ width negated(2)	60		ns
16	t_{CHCZ}	Clock high to control bus high impedance		50	ns
17	t_{SHRH}	$\overline{AS}$, $\overline{DS}$ negated to R/$\overline{W}$ invalid(2)	15		ns
18	t_{CHRH}	Clock high to R/$\overline{W}$ high(1)		30	ns
20	t_{CHRL}	Clock high to R/$\overline{W}$ low(1)		30	ns
20A	t_{ASRV}	$\overline{AS}$ asserted to R/$\overline{W}$ low (write)(2)(3)		10	ns
21	t_{AFCVRL}	Address FC valid to R/$\overline{W}$ low (write)(2)	15		ns
22	t_{RLSL}	R/$\overline{W}$ low to $\overline{DS}$ asserted (write)(2)	30		ns
23	t_{CLDO}	Clock low to data-out valid		30	ns
25	t_{SHDOI}	$\overline{AS}$, DS, negated to data-out invalid (write)(2)	15		ns
26	t_{DOSL}	Data-out valid to $\overline{DS}$ asserted (write)(2)	15		ns
27	t_{DICL}	Data-in valid to clock low (Setup time on read)(4)	7		ns
28	t_{SHDAH}	$\overline{AS}$, $\overline{DS}$ negated to $\overline{DTACK}$ negated (asynchronous hold)(2)	0	110	ns
29	t_{SHDII}	$\overline{AS}$, $\overline{DS}$ negated to data-in invalid (hold time on read)	0		ns
30	t_{SHBEH}	$\overline{AS}$, $\overline{DS}$ negated to $\overline{BEER}$ negated	0		ns
31	t_{DALDI}	$\overline{DTACK}$ asserted to data-in valid (setup time)(2)(4)		50	ns
32	t_{RHr}, t_{RHf}	$\overline{HALT}$ and $\overline{RESET}$ input transition time		150	ns
33	t_{CHGL}	Clock high to $\overline{BG}$ asserted		30	ns
34	t_{CHGH}	Clock high to $\overline{BG}$ negated		30	ns
35	t_{BRLGL}	$\overline{BR}$ asserted to $\overline{BG}$ asserted	2.5	4.5	clks
36	t_{BRHGH}	$\overline{BR}$ negated to $\overline{BG}$ negated(5)	1.5	2.5	clks
37	t_{GALGH}	$\overline{BGACK}$ asserted to $\overline{BG}$ negated	2.5	4.5	clks
37A	t_{GALBRH}	$\overline{BGACK}$ asserted to $\overline{BG}$ negated(6)	10	1.5	ns/clks
38	t_{GLZ}	BG asserted to control, address, data bus high impedance ($\overline{AS}$ negated)		50	ns
39	t_{GH}	$\overline{BG}$ width negated	1.5		clks

Table 8. AC Electrical Specifications
IMP Bus Master Cycles (see Figure 7, Figure 8 and Figure 9) f = 16.67 MHz (Continued)

Num.	Symbol	Parameter	Min	Max	Unit
44	t_{SHVPH}	$\overline{AS}$, $\overline{DS}$ negated to $\overline{AVEC}$ negated	0	50	ns
46	t_{GAL}	$\overline{BGACK}$ width low	1.5		clks
47	t_{ASI}	Asynchronous input setup time(4)	10		ns
48	t_{BELDAL}	$\overline{BERR}$ asserted to $\overline{DTACK}$ asserted(2)(7)	10		ns
53	t_{CHDOI}	Data-out hold from clock high	0		ns
55	t_{RLDBD}	R/$\overline{W}$ asserted to data bus impedance change	0		ns
56	t_{HRPW}	$\overline{HALT}$/$\overline{RESET}$ pulse width(8)	10		clks
57	t_{GASD}	$\overline{BGACK}$ negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ driven	1.5		clks
57A	t_{GAFD}	$\overline{BGACK}$ negated to FC	1		clks
58	f_{RHSD}	$\overline{BR}$ negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ driven(5)	1.5		clks
58A	t_{RHFD}	$\overline{BR}$ negated to FC(5)	1		clks
60	t_{CHBCL}	Clock high to $\overline{BCLR}$ asserted		30	ns
61	t_{CHBCH}	Clock high to $\overline{BCLR}$ negated(9)		30	ns
62	t_{CLRML}	Clock low (S0 falling edge during read) to $\overline{RMC}$ asserted		30	ns
63	t_{CHRMH}	Clock high (S7 rising edge during write) to $\overline{RMC}$ negated		30	ns
64	t_{RMHGL}	$\overline{RMC}$ negated to $\overline{BG}$ asserted(10)		30	ns

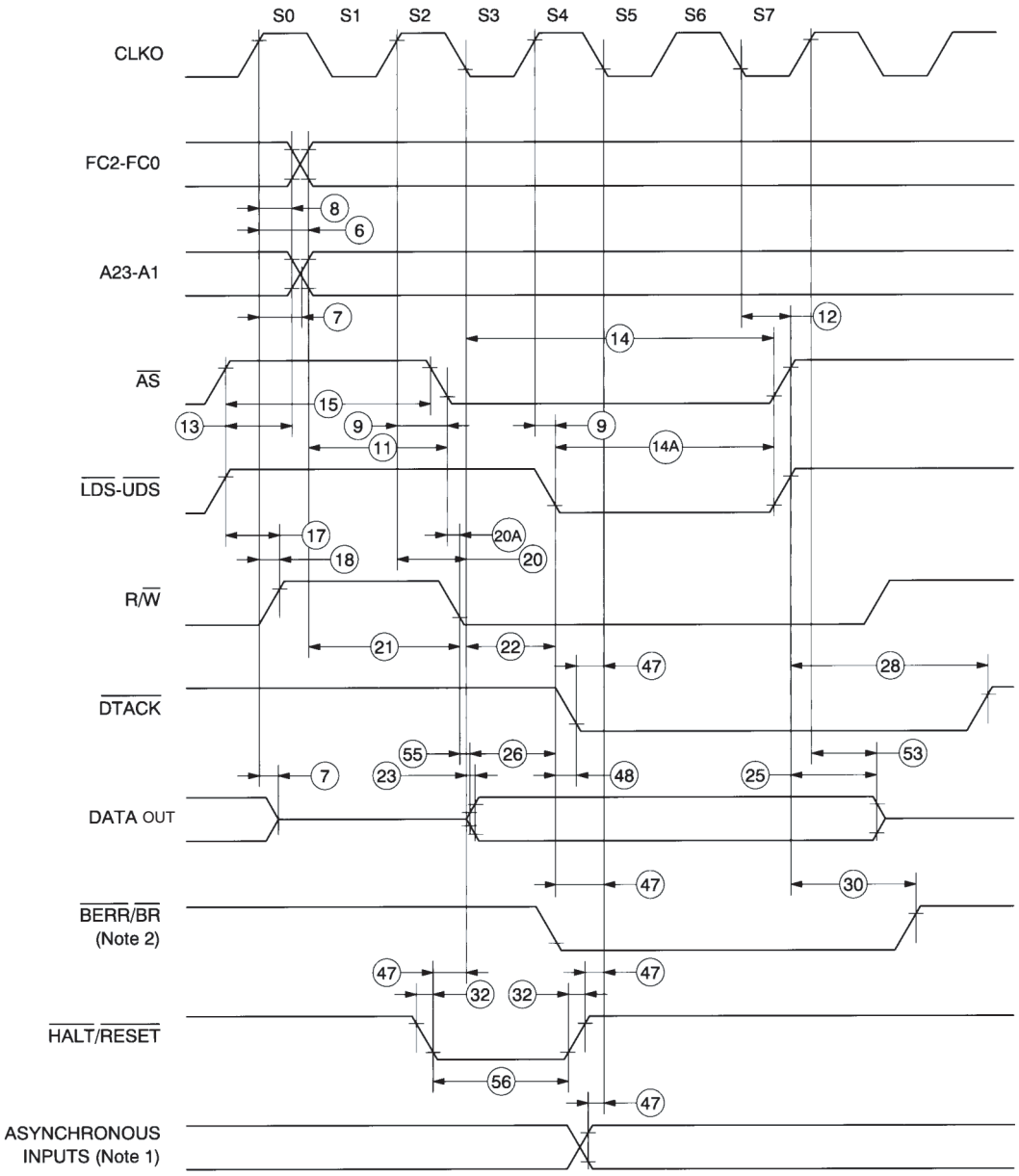
Notes:
1. For loading capacitance of less than or equal to 50 pF, subtract 4 ns from the value given in the maximum columns.
2. Actual value depends on clock period.
3. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), subtract 5 ns from the values given in these columns.
4. If the asynchronous input setup (#47) requirement is satisfied for $\overline{DTACK}$, the $\overline{DTACK}$ asserted to data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (#27) for the following clock cycle.
5. The TS68302 will negate $\overline{BG}$ and begin driving the bus if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
6. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, BG may be reasserted.
7. If #47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, #48 may be ignored. In the absence of $\overline{DTACK}$, $\overline{BERR}$ is a synchronous input using the asynchronous input setup time (#47).
8. For power-up, the TS68302 must be held in the reset state for 100 ms to allow stabilization of on-chip circuit. After the system is powered up #56 refers to the minimum pulse width required to reset the processor.
9. Occurs on S0 of SDMA read/write access when the SDMA becomes bus master.
10. This specification is valid only when the RMCST bit is set in the SCR register.

Figure 7. Read Cycle Timing Diagram



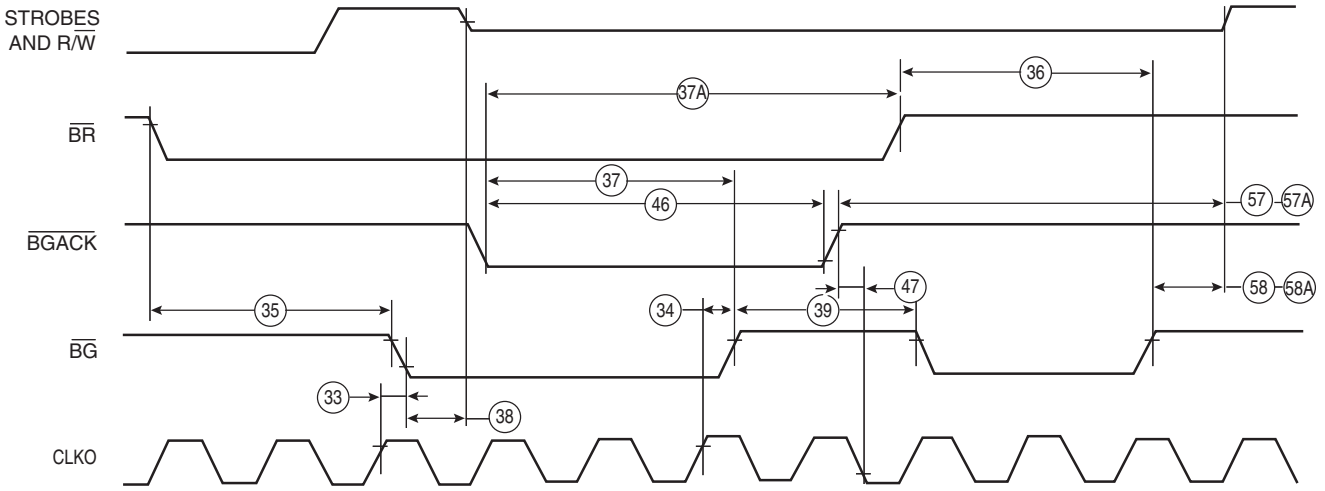
Notes:
1. Setup time for asynchronous inputs $\overline{IPL2}$-$\overline{IPL0}$ guarantees their recognition at the next falling edge of the clock.
2. $\overline{BR}$ needs to fall at this time only to ensure being recognized at the end of the bus cycle.
3. Timing measurements are reinforced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8V and 2.0V.

Figure 8. Write Cycle Timing Diagram



Notes:
1. Timing measurements are referenced to and from a low voltage of 0.8V and a high of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise and fall is linear between 0.8V and 2.0V.
2. Because of loading variations, R/$\overline{W}$ may be valid after $\overline{AS}$ even though both are initiated by the rising edge of S2 (specification #20A).

Figure 9. Bus Arbitration Timing Diagram



Note: Setup time to the clock (#47) for the asynchronous inputs BERR, BGACK, BR, DTACK, and IPL2-IPL0 guarantees their recognition at the next falling edge of the clock.

Table 9. AC Electrical Specifications - DMA (see Figure 10) f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
80	t_{REQASI}	DREQ asynchronous setup time(1)	15		ns
81	t_{REQL}	DREQ width low(2)	2		clk
82	$t_{REQLBRL}$	DREQ low to BR low(3)(4)		2	clk
83	t_{CHBRL}	Clock high to BR low(3)(4)		30	ns
84	t_{CHBRZ}	Clock high to BR high impedance(3)(4)		30	ns
85	t_{BKLBRZ}	BGACK low to BR high impedance(3)(4)	30		ns
86	t_{CHBKL}	Clock high to BGACK low		30	ns
87	t_{ABHBKL}	AS and BGACK high (the latest one) to BGACK low (when BG is asserted)	1.5	2.5 + 30	clk ns
88	t_{BGLBKL}	AS low to BGACK low (no other bus master)(3)(4)		2.5 + 30	clk ns
89	t_{BRHBGH}	BR high impedance to BG high(3)(4)	0		ns
90	$t_{CLBKLAL}$	Clock on which BGACK low to clock on which AS low	2	2	clk
91	t_{CHBKH}	Clock high to BGACK high		30	ns
92	t_{CLBKZ}	Clock low to BGACK high impedance		15	ns
93	t_{CHACKL}	Clock high to DACK low		30	ns
94	t_{CLACKH}	Clock high to DACK high		30	ns
95	t_{CHDNL}	Clock high to DONE low (output)		30	ns
96	t_{CLDNZ}	Clock low to DONE high impedance		30	ns
97	t_{DNLTCH}	DONE input low to clock high (asynchronous setup)	15		ns

Notes:
1. DREQ is sampled on the falling edge of CLK in cycle steal and burst modes.
2. If #80 is satisfied for DREQ, #81 may be ignored.
3. BR will not be asserted while AS, HALT, or BERR is asserted.
4. Specifications are for DISABLE CPU mode only.

Figure 10. DMA Timing Diagram

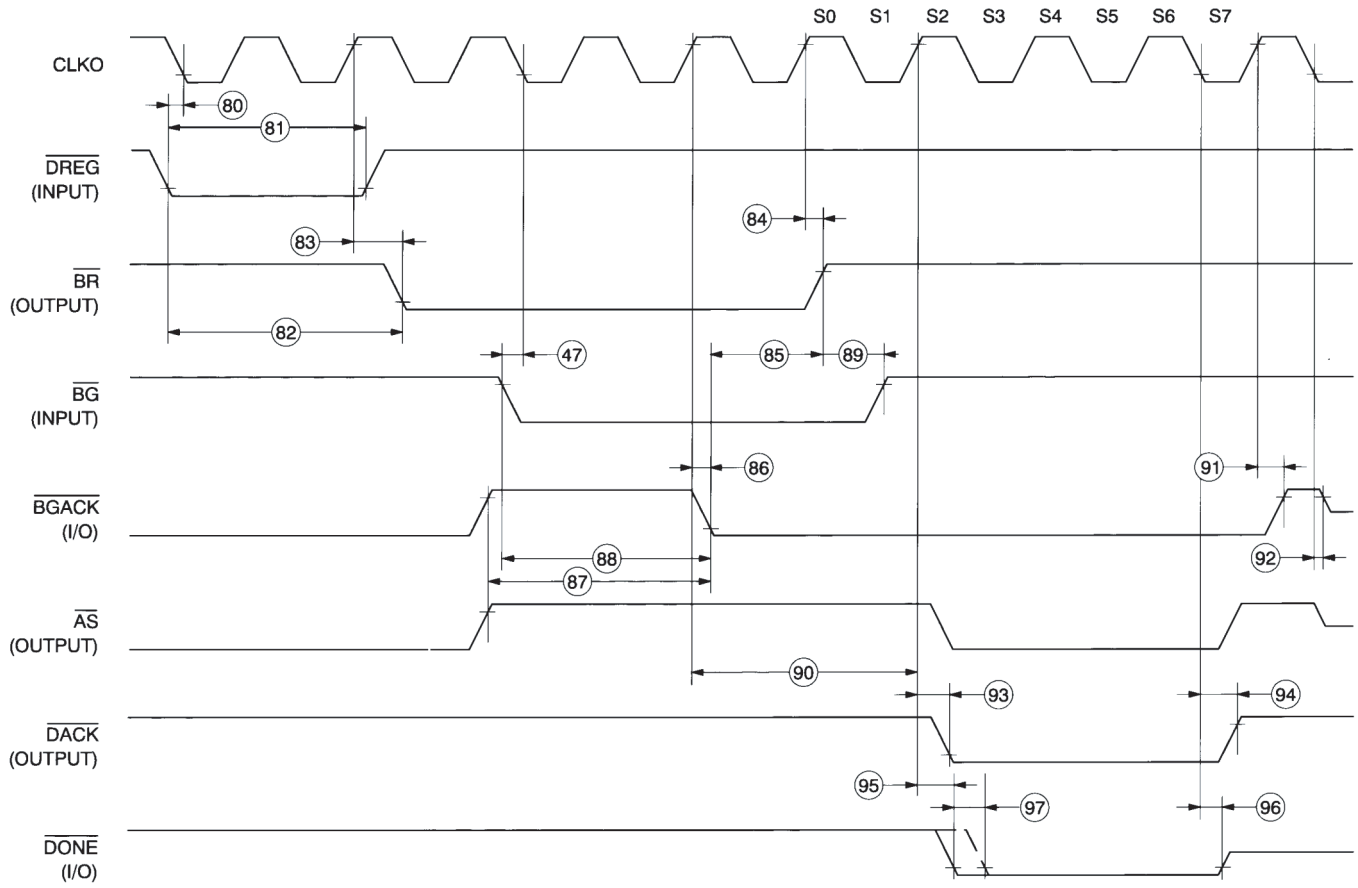


Table 10. AC Electrical Specifications - External Master Internal Asynchronous Read/write Cycles[2] f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
100	t_{RWVDSL}	R/$\overline{W}$ valid to $\overline{DS}$ low	0		ns
101	t_{DSLDIV}	$\overline{DS}$ low to data in valid		30	ns
102	t_{DKLDH}	$\overline{DTACK}$ low to data in hold time	0		ns
103	t_{ASVDSL}	$\overline{AS}$ valid to $\overline{DS}$ low	0		ns
104	t_{DKLDSH}	$\overline{DTACK}$ low to $\overline{DS}$ high	0		ns
105	t_{DSHDKH}	$\overline{DS}$ high to $\overline{DTACK}$ high		45	ns
106	t_{DSIASI}	$\overline{DS}$ inactive to $\overline{AS}$ inactive	0		ns
107	t_{DSHRWH}	$\overline{DS}$ high to R/$\overline{W}$ high	0		ns
108	t_{DSHDZ}	$\overline{DS}$ high to data high impedance		45	ns
108A	t_{DSHDH}	$\overline{DS}$ high to data out hold time	0		ns
109	t_{DSHDOH}	$\overline{DS}$ high to data in hold time[1]	0		ns
109A	t_{DOVDKL}	Data out valid to $\overline{DTACK}$ low	15		ns

Note: 1. If $\overline{AS}$ is negated before $\overline{DS}$, the data bus could be three-stated (spec 126) before $\overline{DS}$ is negated.

2. See Figure 11 and Figure 12.

Figure 11. External Master Internal Asynchronous Read Cycle Timing Diagram

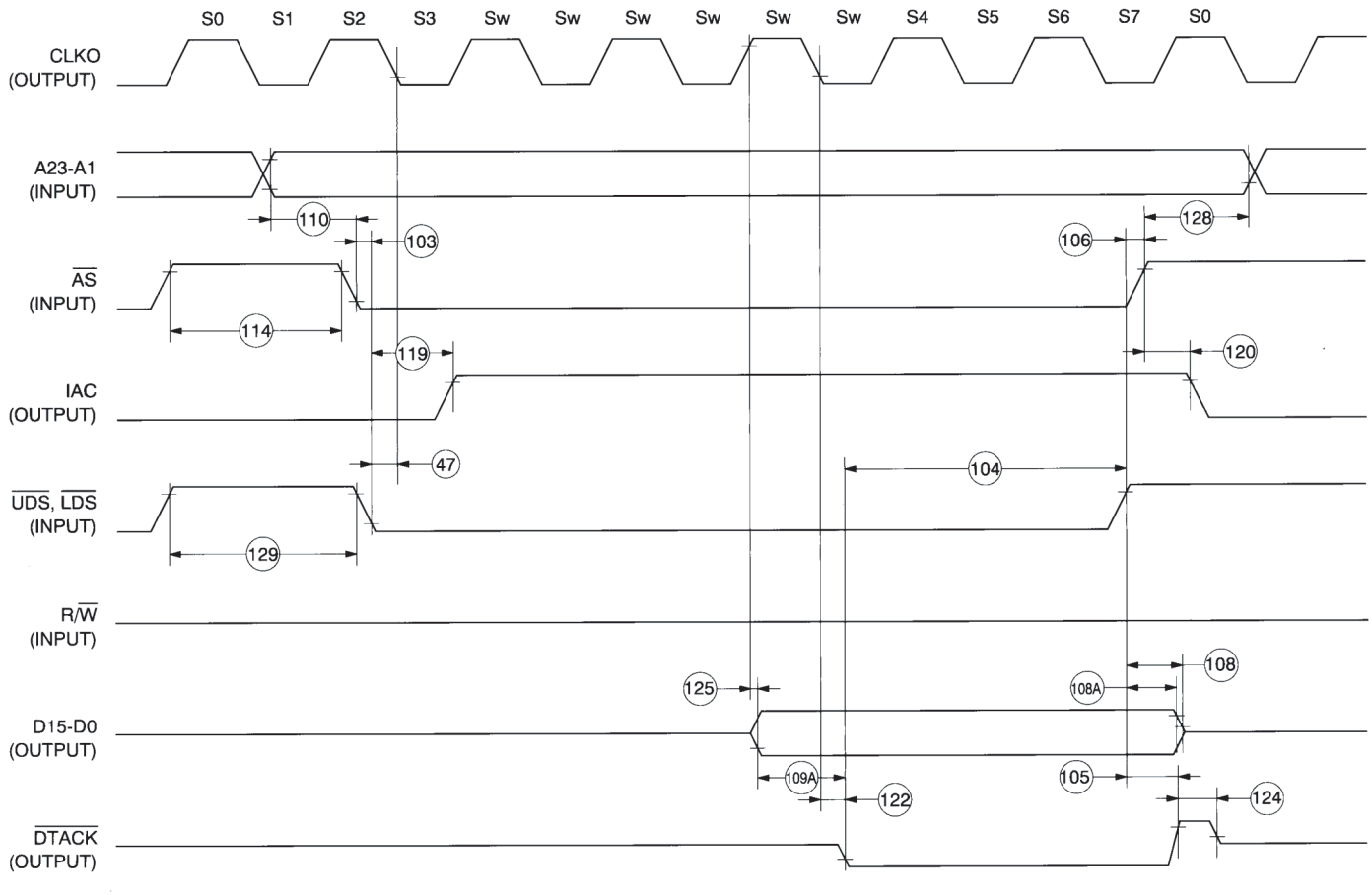


Figure 12. External Master Internal Asynchronous Write Cycle Timing Diagram

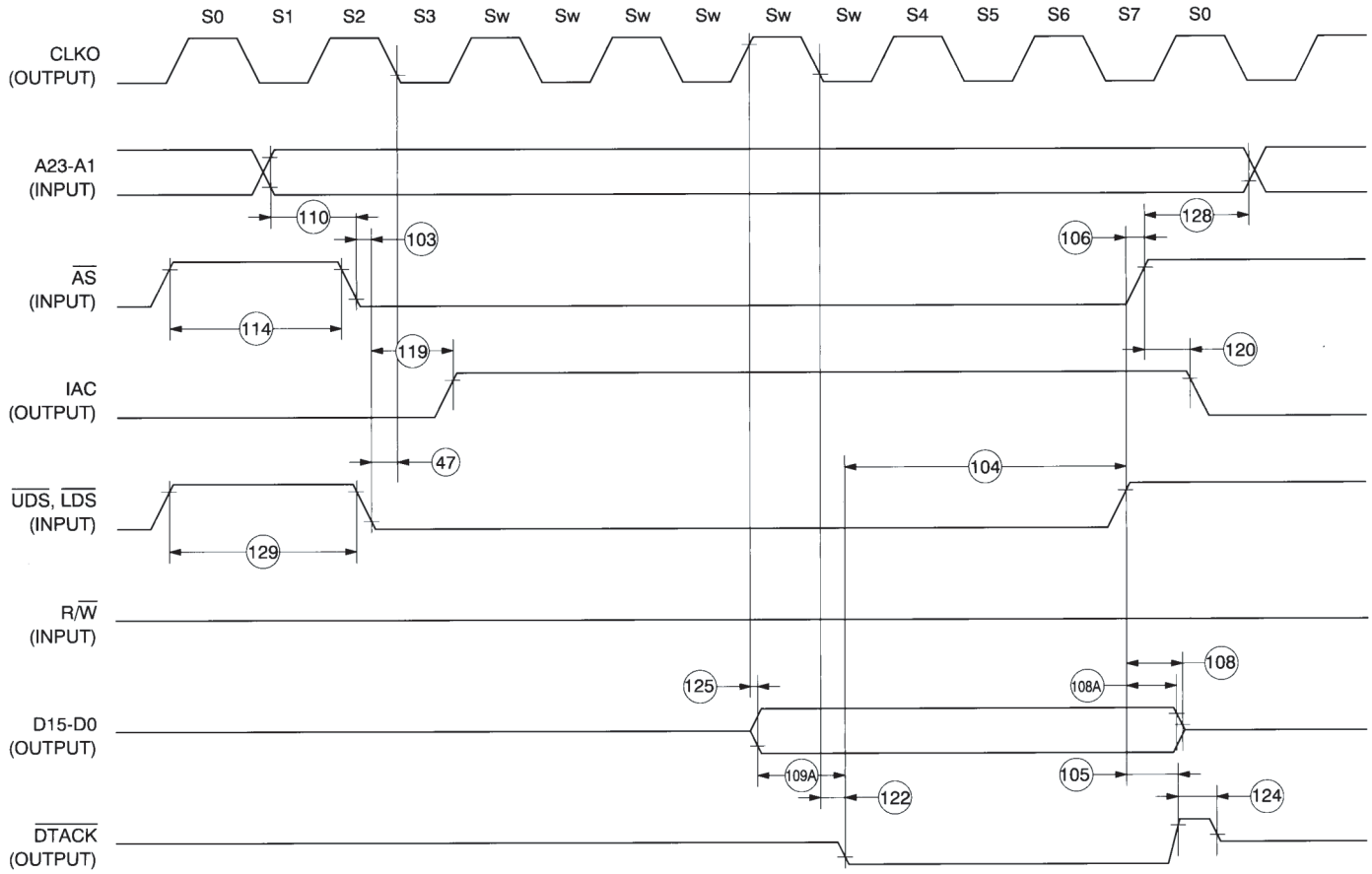


Table 11. AC Electrical Specifications[2]
External Master Internal Synchronous Read/write Cycles[1] f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
110	t_{AVASL}	Address valid to $\overline{AS}$ low	15		ns
111	t_{ASLCH}	$\overline{AS}$ low to clock high	30		ns
112	t_{CLASH}	Clock low as to $\overline{AS}$ high		45	ns
113	t_{ASHAH}	$\overline{AS}$ high to address hold time on write	0		ns
114	t_{ASH}	$\overline{AS}$ inactive time	1		clk
115	t_{SLCH}	$\overline{UDS}/\overline{LDS}$ low to clock high	40		ns
116	t_{CLSH}	Clock low to $\overline{UDS}/\overline{LDS}$ high		45	ns
117	t_{RWVCH}	R/$\overline{W}$ valid to clock high	30		ns
118	t_{CHRWH}	Clock high to R/$\overline{W}$ high		45	ns
119	t_{ASLIAH}	$\overline{AS}$ low to IAC high		40	ns
120	t_{ASHIAL}	$\overline{AS}$ high to IAC low		40	ns
121	t_{ASLDTL}	$\overline{AS}$ low to $\overline{DTACK}$ low (0 wait state)		45	ns
122	t_{CLDTL}	Clock low to $\overline{DTACK}$ low (1 wait state)		30	ns

Table 11. AC Electrical Specifications[2]
External Master Internal Synchronous Read/write Cycles[1] f = 16.67 MHz (Continued)

Num.	Symbol	Parameter	Min	Max	Unit
123	t_{ASHDTH}	$\overline{AS}$ high to $\overline{DTACK}$ high		45	ns
124	t_{DTHDTZ}	$\overline{DTACK}$ high to $\overline{DTACK}$ high impedance		15	ns
125	t_{CHDOV}	Clock high to data out valid		30	ns
126	t_{ASHDZ}	$\overline{AS}$ high to data high impedance		45	ns
127	t_{ASHDOI}	$\overline{AS}$ high to data out hold time	0		ns
128	t_{ASHAI}	$\overline{AS}$ high to address hold time on read	0		ns
129	t_{SH}	$\overline{UDS}$/$\overline{LDS}$ inactive time	1		clk
130	t_{CLDIV}	Data in valid to clock low	30		ns
131	t_{CLDIH}	Clock low to data in hold time	15		ns

Notes: 1. See Figure 13, Figure 14 and Figure 15.
2. Specifications are valid only when SAM = 1 in the SCR.

Figure 13. External Master Internal Synchronous Read Cycle Timing Diagram

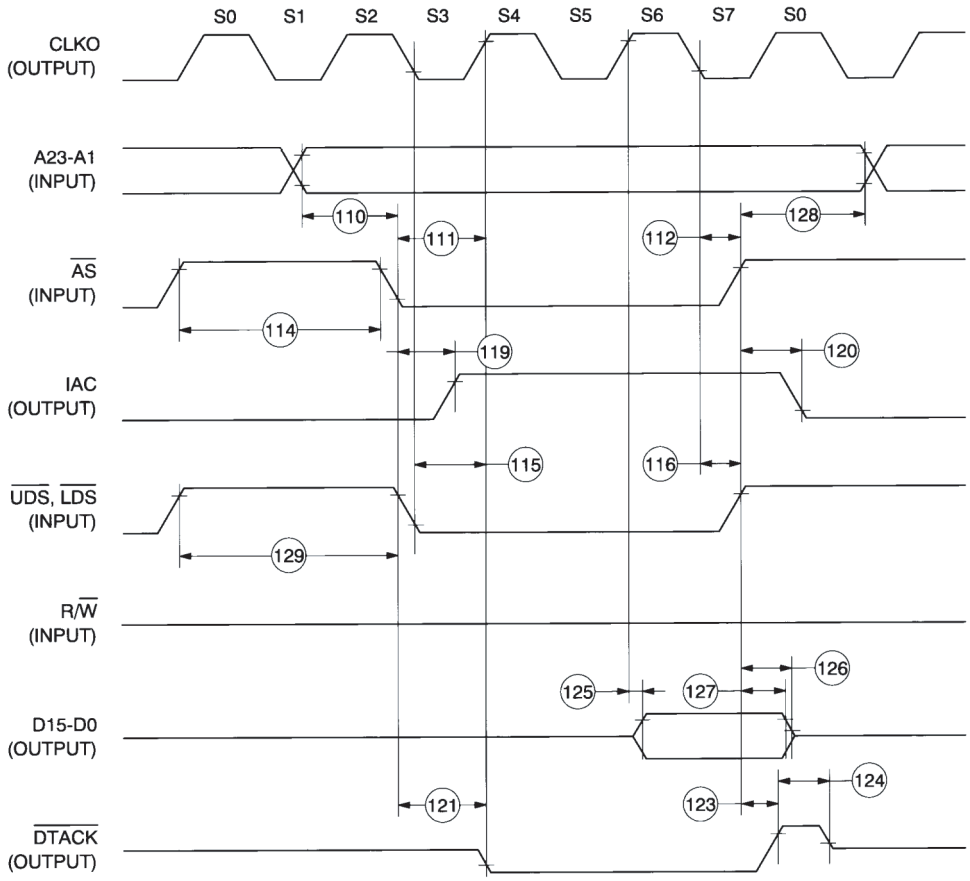


Figure 14. External Master Internal Synchronous Read Cycle Timing Diagram (One Wait State)

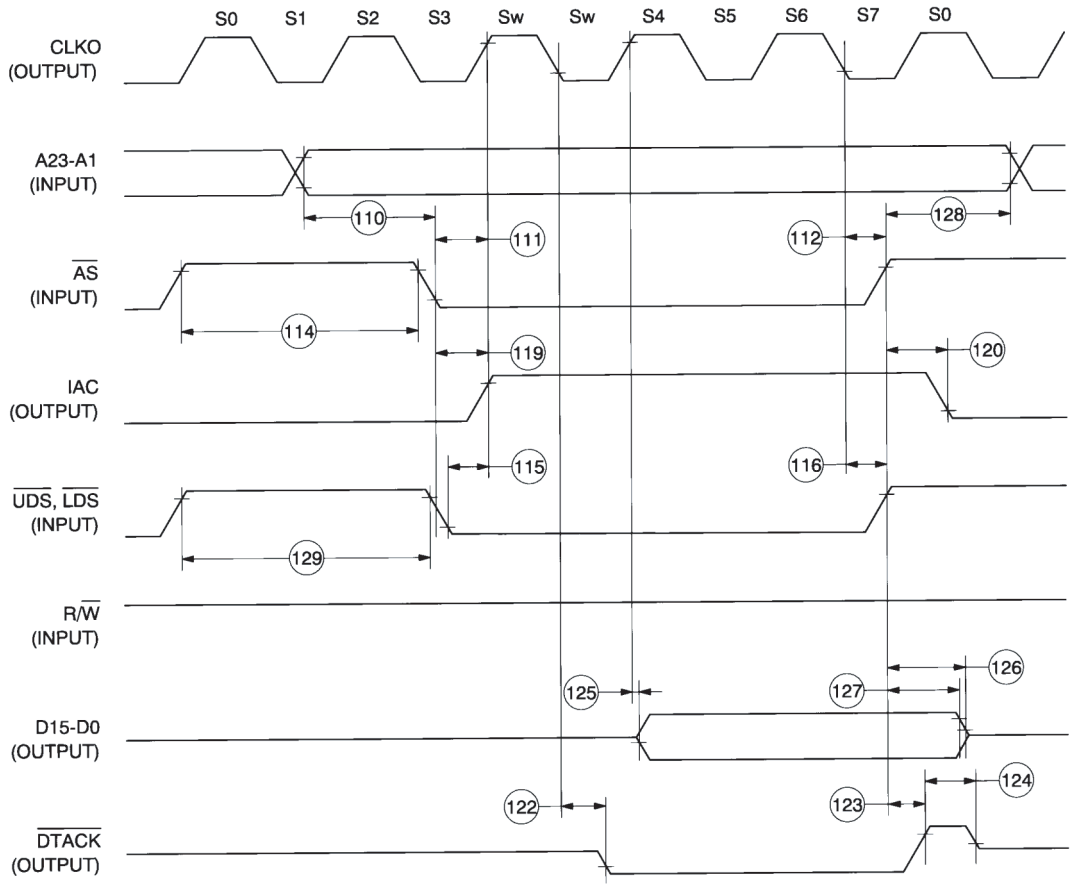


Figure 15. External Master Internal Synchronous Write Cycle Timing Diagram

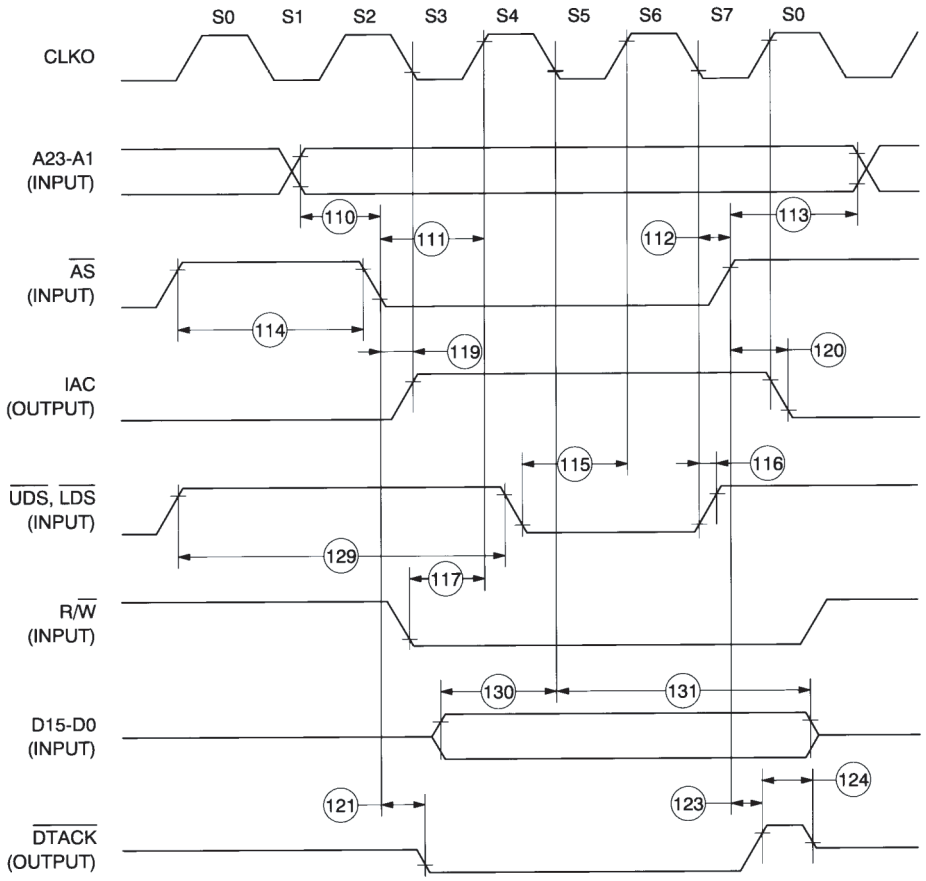


Table 12. AC Electrical Specifications - Internal Master Read/write Cycles[1] f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
140	t_{CHIAH}	Clock high to IAC high		40	ns
141	t_{CLIAL}	Clock low to IAC low		40	ns
142	t_{CHDTL}	Clock high to $\overline{DTACK}$ low (0 wait state)		45	ns
143	t_{CLDTH}	Clock low to $\overline{DTACK}$ high		40	ns
144	t_{CHDOV}	Clock high to data out valid		30	ns
145	t_{ASHDOH}	$\overline{AS}$ high to data out hold time	0		ns

Note: 1. See Figure 16.

Figure 16. Internal Master Internal Read Cycle Timing Diagram

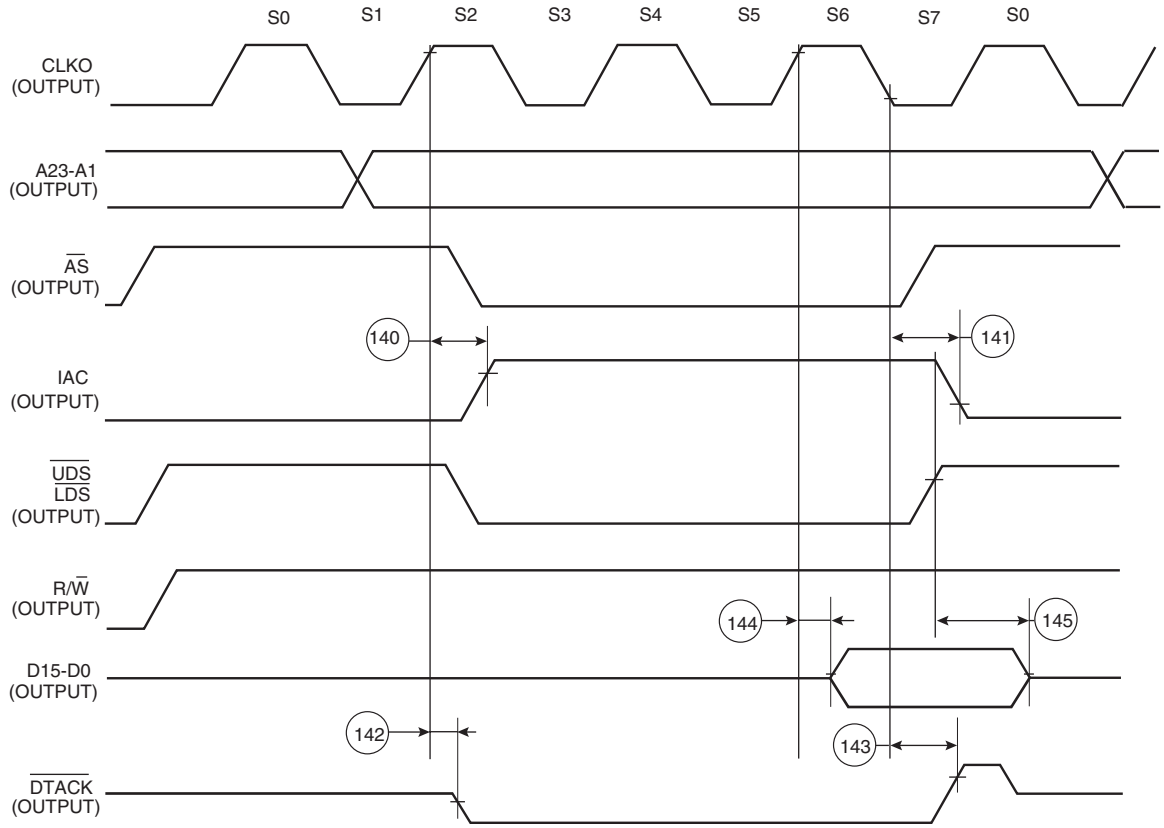


Table 13. AC Electrical Specifications - Chip-select Timing Internal Master[3] f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
150	$t_{CHCSIAKL}$	Clock high to $\overline{CS}$, $\overline{IACK}$ low[1]		40	ns
151	$t_{CLCSIAKH}$	Clock low to $\overline{CS}$, $\overline{IACK}$ high[1]		40	ns
152	t_{CSH}	$\overline{CS}$ width negated	60		ns
153	t_{CHDTKL}	Clock high to $\overline{DTACK}$ low (0 wait state)		45	ns
154	t_{CLDTKL}	Clock low to $\overline{DTACK}$ low (1 - 6 wait states)		30	ns
155	t_{CLDTKH}	Clock low to $\overline{DTACK}$ high		40	ns
156	t_{CHBERL}	Clock high to $\overline{BERR}$ low[2]		40	ns
157	t_{CLBERH}	Clock low to $\overline{BERR}$ high impedance[2]		40	ns
158	$t_{DTKHDTKZ}$	$\overline{DTACK}$ high to $\overline{DTACK}$ high impedance		15	ns
171	t_{IDHCL}	Input data hold time from S6 low	5		ns
172	t_{CSNDOI}	$\overline{CS}$ negated to data out invalid (write)[4]	10		ns
173	t_{AFVCSA}	Address, FC valid to $\overline{CS}$ asserted[4]	15		ns
174	t_{CSNAFI}	CS negated to address, FC invalid[4]	15		ns
175	t_{CSLT}	$\overline{CS}$ low time (0 wait states)[4]	120		ns

Table 13. AC Electrical Specifications - Chip-select Timing Internal Master[3] f = 16.67 MHz (Continued)

Num.	Symbol	Parameter	Min	Max	Unit
176	t_{CSNRWI}	$\overline{CS}$ negated to R/$\overline{W}$ invalid[4]	10		ns
177	t_{CSARWL}	$\overline{CS}$ asserted to R/$\overline{W}$ low (write)[4]		10	ns
178	t_{CSNDII}	$\overline{CS}$ negated to data in invalid (hold time on read)[4]	0		ns

Notes: 1. For loading capacitance less than or equal to 50 pF, subtract 4 ns from the maximum value given.
2. This specification is valid only when the ADCE or WPVE bits in the SCR are set.
3. See Figure 17.
4. Specs 172-178 do not have diagrams. However, similar diagrams for AS are shown as 25-11-13-14-17-20A and 29.

Figure 17. Internal Master Chip-select Timing Diagram

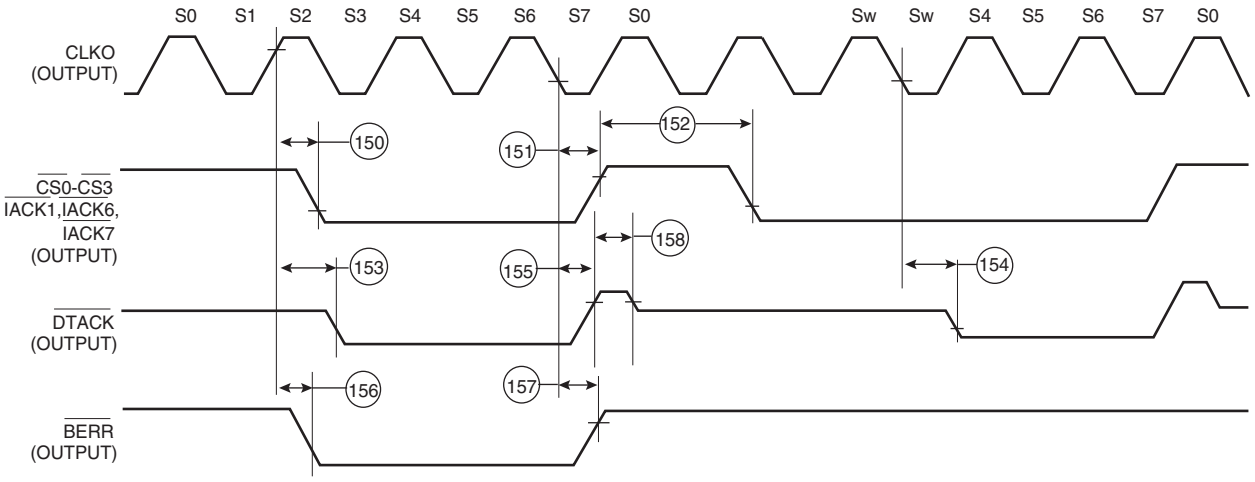


Table 14. AC Electrical Specifications - Chip-select Timing External Master[4] f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
154	t_{CLDTKL}	Clock low to $\overline{DTACK}$ low (1-6 wait states)		30	ns
160	t_{ASLCSL}	$\overline{AS}$ low to $\overline{CS}$ low		30	ns
161	t_{ASHCSH}	$\overline{AS}$ high to $\overline{CS}$ high		30	ns
162	t_{AVASL}	Address valid to $\overline{AS}$ Low	15		ns
163	t_{RWVASL}	R/$\overline{W}$ valid to $\overline{AS}$ Low[1]	15		ns
164	t_{ASHAI}	$\overline{AS}$ negated to Address hold time	0		ns
165	$t_{ASLDTKL}$	$\overline{AS}$ low to $\overline{DTACK}$ low (0 wait state)		45	ns
167	$t_{ASHDTKH}$	$\overline{AS}$ high to $\overline{DTACK}$ high		30	ns
168	$t_{ASLBERL}$	$\overline{AS}$ low to $\overline{BERR}$ low[2]		30	ns
169	$t_{ASHBERH}$	$\overline{AS}$ high to $\overline{BERR}$ high[2][3]		30	ns

Notes: 1. The minimum value must be met to guarantee write protection operation.
2. This specification is valid when the DCE or WPVE bits in the SCR are set.
3. Also applies after a timeout of the hardware watchdog.
4. See Figure 18

Figure 18. External Master Chip-select Timing Diagram

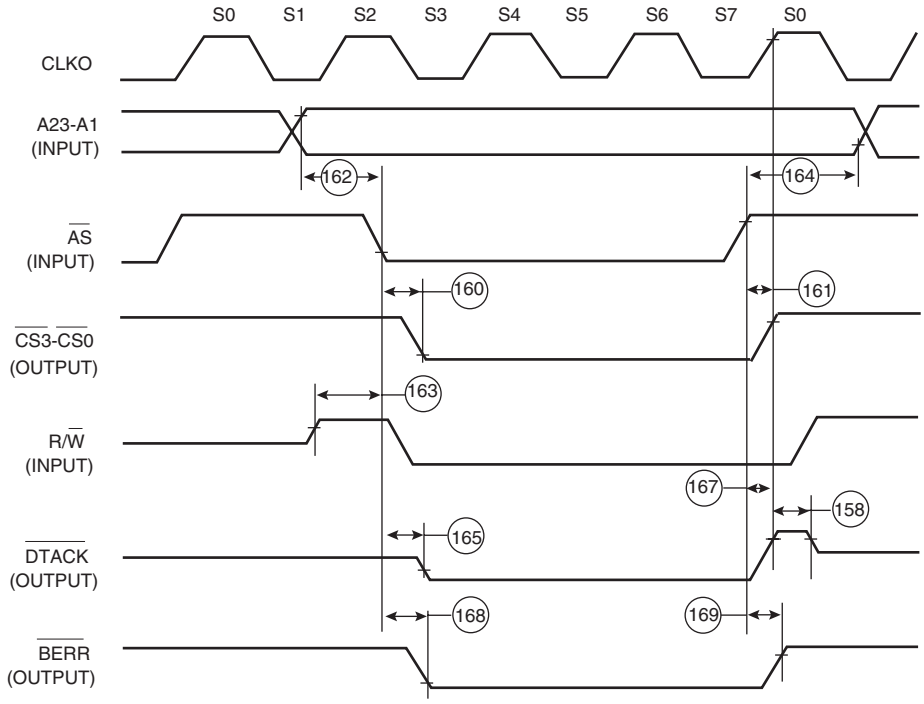


Table 15. AC Electrical Specifications - Parallel I/O[1] f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
180	t_{DSU}	Input Data Setup Time (to clock low)	20		ns
181	t_{DH}	Input Data Hold Time (from clock low)	10		ns
182	t_{CHDOV}	Clock High to Data Out Valid (CPU writes data, control, or direction) 35		35	ns

Note: 1. See Figure 19

Figure 19. Parallel I/O Data In/data Out Timing Diagram

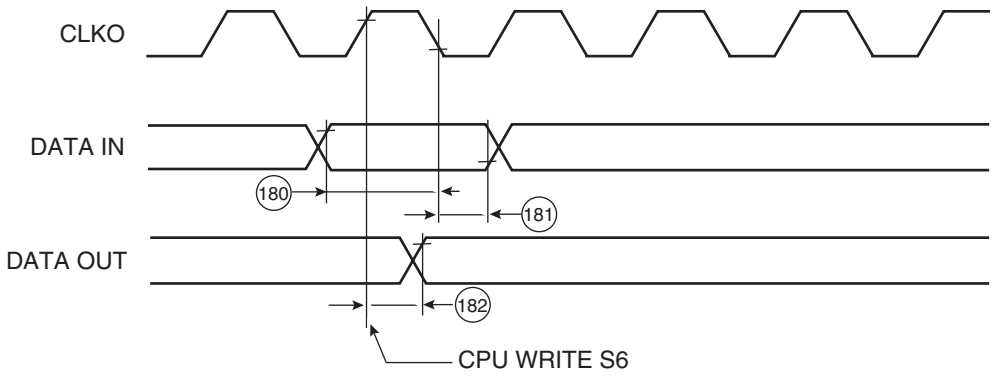


Table 16. AC Electrical Specifications - Interrupts[2] f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
190	t_{IPW}	Interrupt pulse width low $\overline{IRQ}$ (edge triggered mode)	50		ns
191	t_{AEMT}	Minimum time between active edges	3		clk

Note: 1. Set up time for the asynchronous inputs IPL2-IPL0 and AVEC guarantees their recognition at the next falling edge of the clock.

2. See Figure 20.

Figure 20. Interrupts Timing Diagram

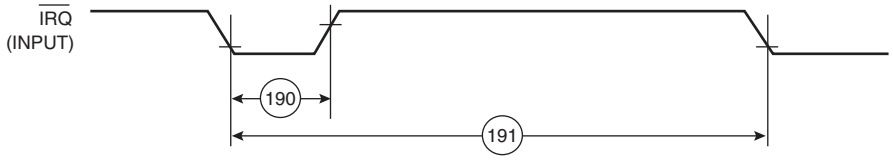


Table 17. AC Electrical Specifications - Timers[2] f = 16.67 MHz

Num.	Symbol	Parameter	Min	Max	Unit
200	t_{TPW}	Timer input capture pulse width	50		ns
201	t_{TICLT}	TIN clock low pulse width	50		ns
202	t_{TICHT}	TIN clock high pulse width	2		clk
203	t_{cyc}	TIN clock cycle time	3		clk
204	t_{CHTOV}	Clock high to TOUT valid		35	ns
205	t_{FRZSU}	$\overline{FRZ}$ input setup time (to clock high)[1]	20		ns
206	t_{FRZHT}	$\overline{FRZ}$ input hold time (from clock high)	10		ns

Note: 1. FRZ should be negated during total system reset.

2. See Figure 21.

Figure 21. Timers Timing Diagram

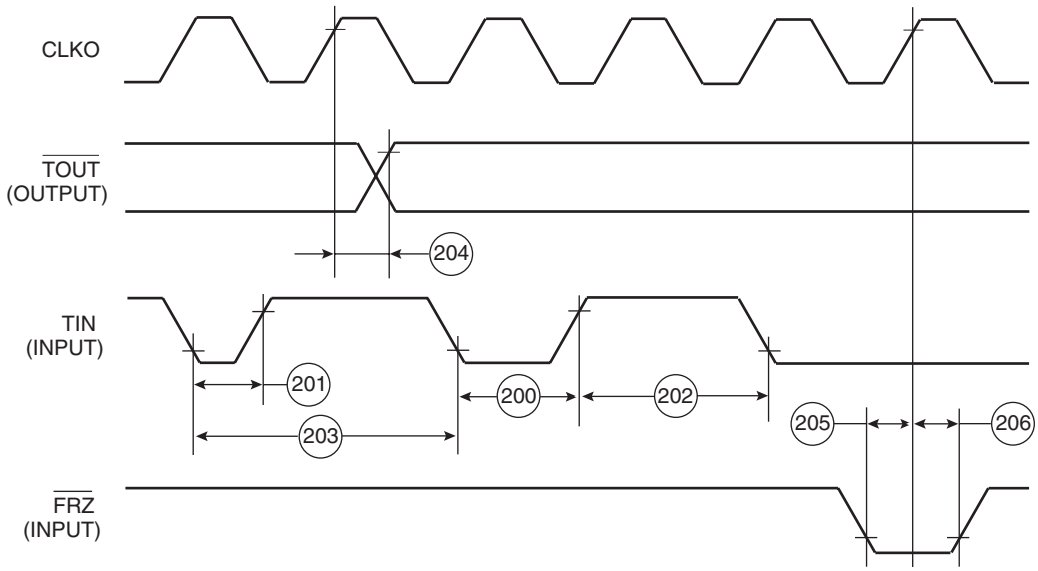


Table 18. AC Electrical Specifications - Serial Communication Port[2] f = 16.67 MHz

Num.	Parameter	Min	Max	Unit
250	SPCLK clock output period	4	64	clks
251	SPCLK clock output rise/fall time		15	ns
252	Delay from SPCLK to transmit[1]	0	40	ns
253	SCP receive setup time[1]	40		ns
254	SPC receive hold time[1]	10		ns

Note: 1. This also applies when SPCLK is inverted by CI in the SPMODE register. The enable signals for the slaves may be implemented by the parallel I/O pins.

2. See Figure 22.

Figure 22. Serial Communication Port Timing Diagram

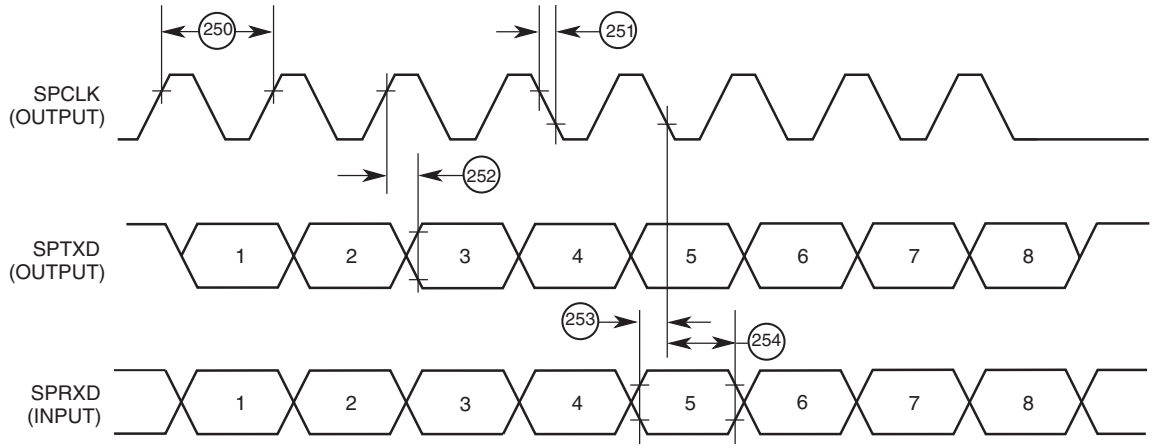


Table 19. AC Electrical Specifications - Idle Timing[3] f = 16.67 MHz All timing measurements, unless otherwise specified, are referenced to the L1CLK at 50% point of VDD

Num.	Parameter	Min	Max	Unit
260	L1CLK (IDL clock) frequency[1]		6.66	MHz
261	L1CLK width low	55		ns
262	L1CLK width high	60		ns
263	L1T x D, L1RQ, SDS1-SDS2 rising/falling time		20	ns
264	L1SY1 (sync) setup time (to L1CLK falling edge)	30		ns
265	L1SY1 (sync) hold time (to L1CLK falling edge)	50		ns
266	L1SY1 (sync) inactive before 4th L1CLK	0		ns
267	L1T x D active delay (from L1CLK rising edge)	0	75	ns
268	L1T x D to high impedance (from L1CLK rising edge)[2]	0	50	ns
269	L1R x D setup time (to L1CLK falling edge)	50		ns
270	L1R x D hold time (from L1CLK falling edge)	50		ns
271	Time between successive IDL syncs	20		L1CLK
272	L1RQ valid before falling edge of L1SY1	1		L1CLK
273	L1GR setup time (to L1SY1 falling edge)	50		ns

Table 19. AC Electrical Specifications - Idle Timing[3] f = 16.67 MHz All timing measurements, unless otherwise specified, are referenced to the L1CLK at 50% point of VDD (Continued)

Num.	Parameter	Min	Max	Unit
274	L1GR hold time (from L1SY1 falling edge)	50		ns
275	SDS1-SDS2 active delay from L1CLK rising edge	10	75	ns
276	SDS1-SDS2 inactive delay from L1CLK falling edge	10	75	ns

Notes: 1. The ratio CLK/L1CLK must be greater than 2.5/1.
2. High impedance is measured at the 30% and 70% of VDD points, with the line at VDD/2 through 10K in parallel with 130 pF.
3. See Figure 23.

Figure 23. IDL Timing Diagram

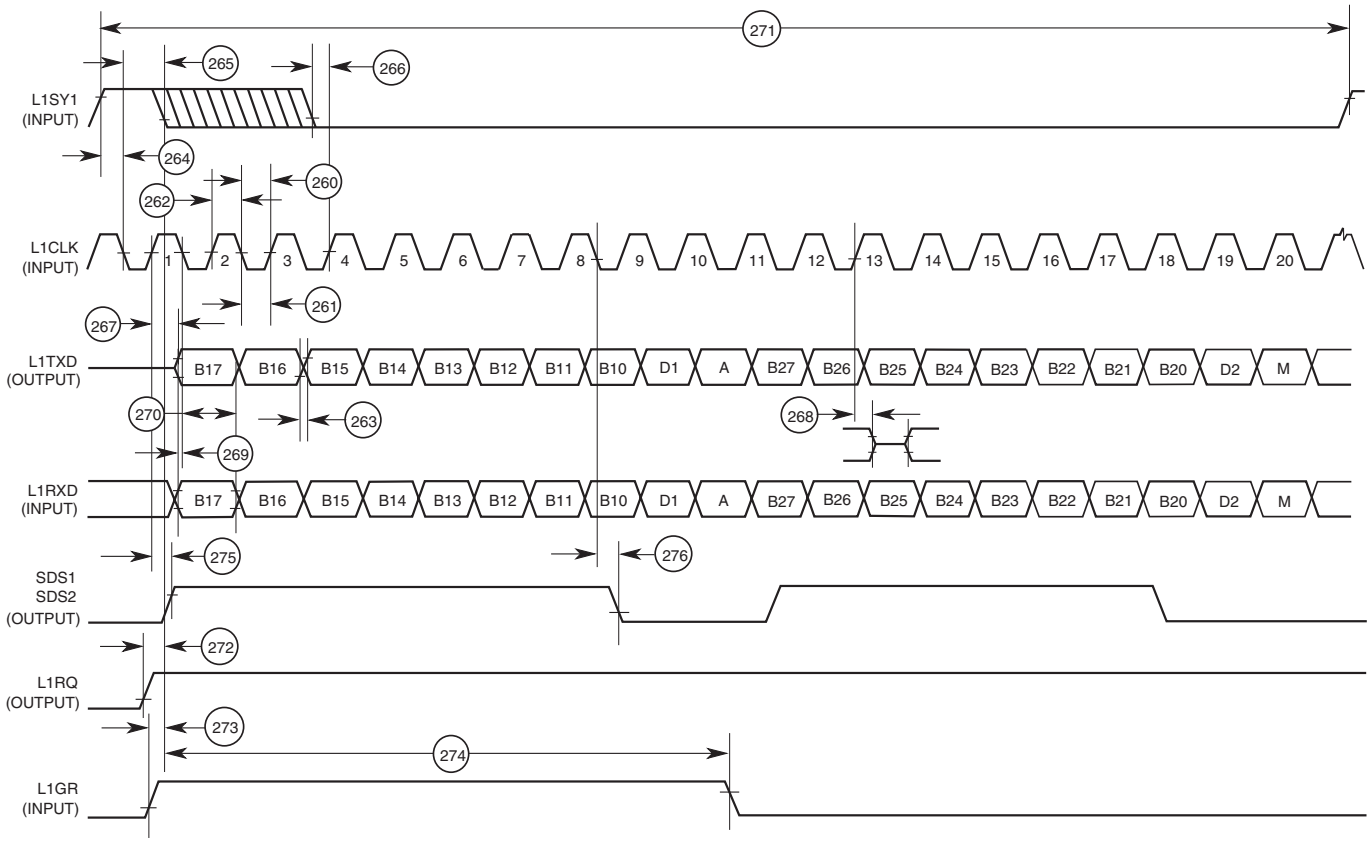


Table 20. AC Electrical Specifications - GCI Timing[5] f = 16.67 MHz

GCI supports the NORMAL mode and the GCI channel 0 (GCN0) in MUX mode. Normal mode uses 512 kHz clock rate (256K bit rate). MUX mode uses 256 x n - 3068K bits/sec (clock rate is data rate x 2). The ratio CLK/L1CLK must be greater than 2.5/1.

Num.	Parameter	Min	Max	Unit
	L1CLK GCI clock frequency (normal mode)[1]		512	kHz
280	L1CLK clock period normal mode[1]	1800	2100	ns
281	L1CLK width low/high normal mode	840	1450	ns
282	L1CLK rise/fall time normal mode[2]	-	-	ns
	L1CLK (GCI clock) period (MUX mode)[1]		6.668	MHz
280	L1CLK clock period MUX mode[1]	150		ns
281	L1CLK width low/high MUX mode	55		ns
282	L1CLK rise/fall time MUX mode[2]	-	-	ns
283	L1SY1 sync setup time to L1CLK falling edge	30		ns
284	L1SY1 sync hold time from L1CLK falling edge	50		ns
285	L1T x D active delay (from L1CLK rising edge)[3]	0	100	ns
286	L1T x D active delay (from L1SY1 rising edge)[3]	0	100	ns
287	L1R x D setup time to L1CLK rising edge	20		ns
288	L1R x D hold time from L1CLK rising edge	50		ns
289	Time between successive L1SY1 in normal mode SCIT mode	64 192		L1CLK L1CLK
290	SDS1-SDS2 active delay from L1CLK riding edge[4]	10	90	ns
291	SDS1-SDS2 active delay from L1SY1 rising edge[4]	10	90	ns
292	SDS1-SDS2 inactive delay from L1CLK falling edge	10	90	ns
293	GCIDCL (GCI Data clock) active delay	0	50	ns

Notes:
1. The ratio CLK/L1CLK must be greater than 2.5/1.
2. Schmitt trigger used on input buffer.
3. Condition C_L = 150 pF. L1T x D becomes valid after the L1CLK rising edge or L1SY1, whichever is later.
4. SDS1-SDS2 become valid after the L1CLK rising edge or L1SY1, whichever is later.
5. See Figure 24.

Figure 24. GSI Timing Diagram

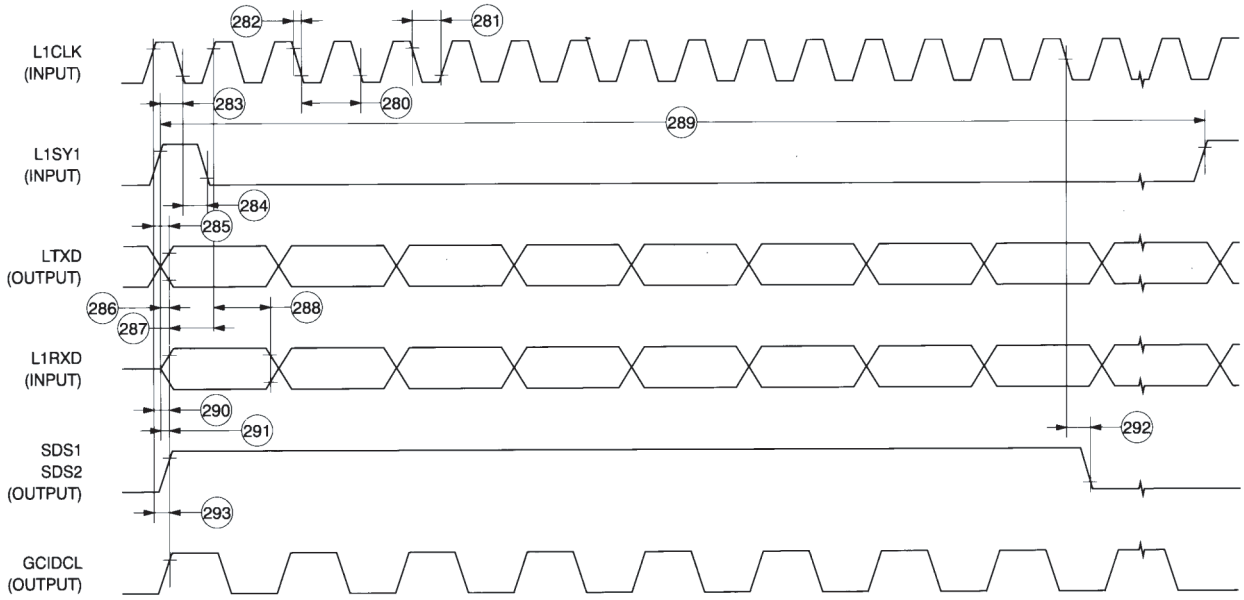


Table 21. AC Electrical Specifications - PCM Timing[4] f = 16.67 MHz

There are two sync types:
Short frame - Sync signals are one clock cycle prior to the data.
Long frame - Sync signals are N-bits that envelope the data, N > 0.

Num.	Parameter	Min	Max	Unit
300	L1CLK (PCM clock) frequency[1]		6.66	MHz
301	L1CLK width low/high	55		ns
302	L1SY0-L1SY1 setup time to L1CLK falling edge	20		ns
303	L1SY0-L1SY1 hold time from L1CLK falling edge	40		ns
304	L1SY0-L1SY1 width low	1		L1CLK
305	Time between successive sync signals (short frame)	8		L1CLK
306	L1T x D data valid after L1CLK rising edge[2]	0	70	ns
307	L1T x D to high impedance (from L1CLK rising edge)	0	50	ns
308	L1R x D setup time (to L1CLK falling edge)[3]	20		ns
309	L1R x D hold time (from L1CLK falling edge)[3]	50		ns
310	L1T x D data valid after syncs rising edge (long)[2]	0	100	ns
311	L1T x D to high impedance (from L1SY0-L1SY1 falling edge) (long)	0	70	ns

Notes:
1. The ratio CLK/TCLK1 must be greater than 2.5/1.
2. L1T x D becomes valid after the L1CLK rising edge or the sync enable, whichever is later, if long frames are used.
3. Specification valid for both sync methods.
4. See Figure 25.

Table 22. AC Electrical Specifications - NMSI Timing[4]

The NMSI mode uses two clocks, one for receive and one for transmit. Both clocks can be internal or external. When the clock is internal, it is generated by the internal baud rate generator and it is output on L1R x D or L1T x D. All the timing is related to the external clock pin. The timing is specified for NMSI1. It is also valid for NMS12 and NMS13.

Num.	Parameter	Internal Clock		External Clock		Unit
		Min	Max	Min	Max	
315	RCLK1 and TCLK1 frequency[1]		5.12		6.668	MHz
316	RCLK1 and TCLK1 low/high	70		55		ns
317	RCLK1 and TCLK1 rise/fall time[2]	—	—	—	—	ns
318	T x D1 active delay TCLK1 falling edge	0	40	0	70	ns
319	RTS1 active/inactive delay from TCLK1 falling edge	0	40	0	100	ns
320	CTS1 setup time to TCLK1 rising edge	50		10		ns
321	R x D1 setup time to RCLK1 rising edge	50		10		ns
322	R x D1 hold time from RCLK1 rising edge[3]	10		50		ns
323	CD1 setup time to RCLK1 rising edge	50		10		ns

Notes: 1. The ratio CLK/TCLK1 and CLK/RCLK1 must be greater than 2.5/1 for external clock. For internal clock the ratio must be greater than 3/1 (the input clock to the baud rate generator may be either CLK or TIM1), in both cases the maximum frequency is limited to 16.67 MHz. In asynchronous mode (UART), the bit rate is 1/16 of the clock rate.
2. Schmitt triggers used on input buffers.
3. Also applies to $\overline{CD}$ hold time when $\overline{CD}$ is used as an external sync in BISYNC or totally transparent mode.
4. See Figure 26.

Figure 25. PCM Timing Diagram

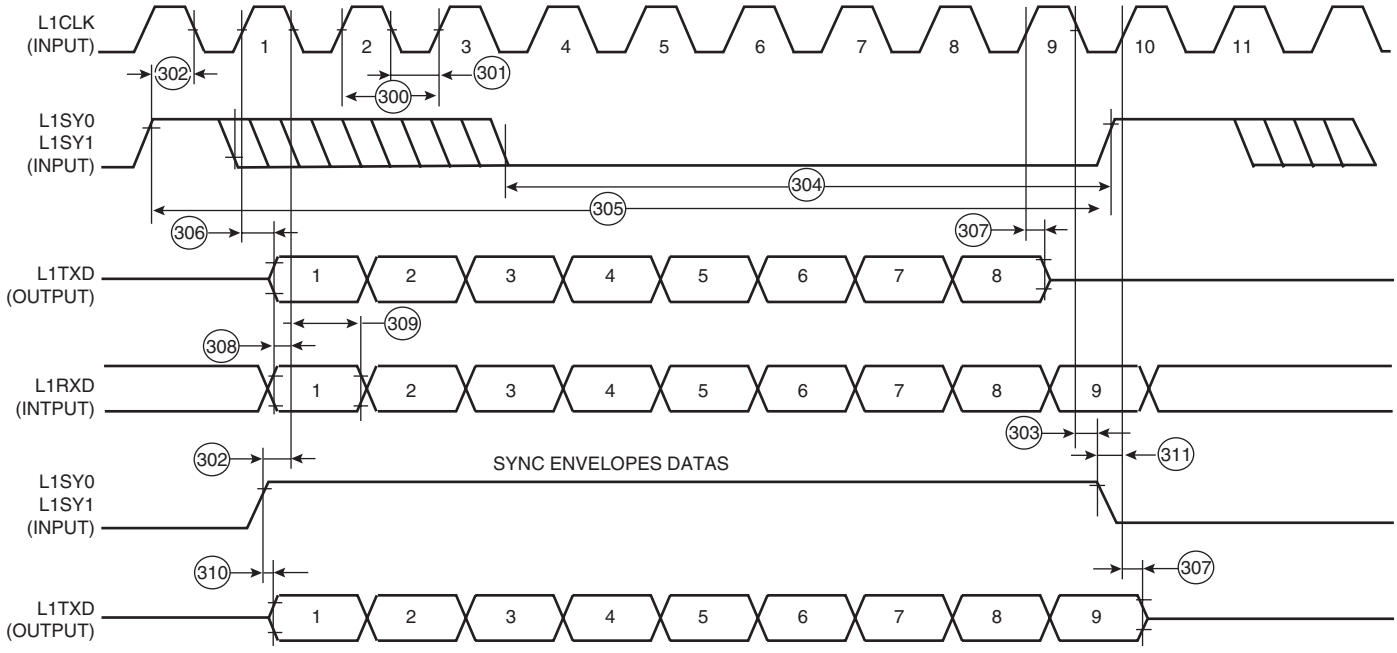
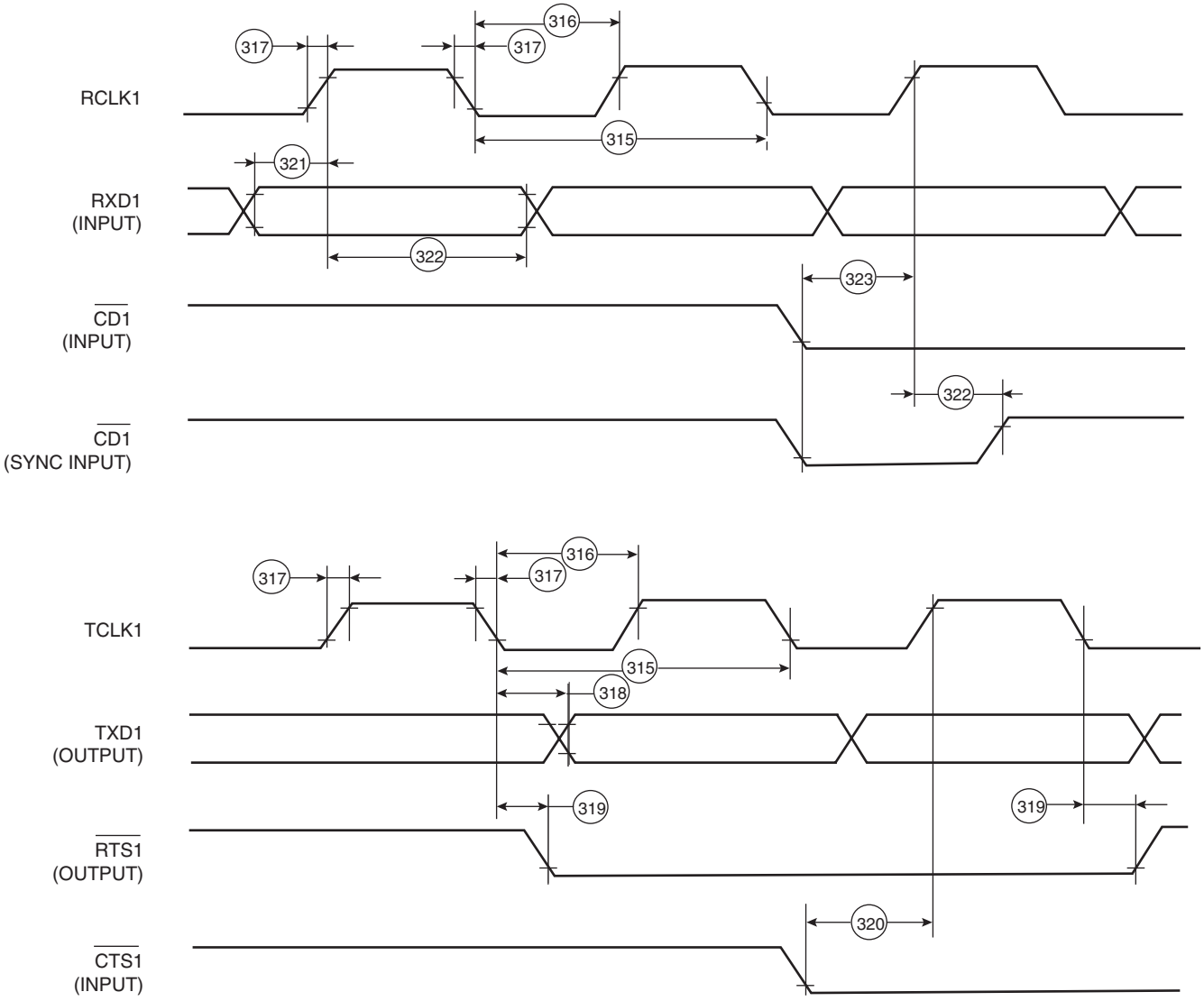


Figure 26. NMSI Timing Diagram



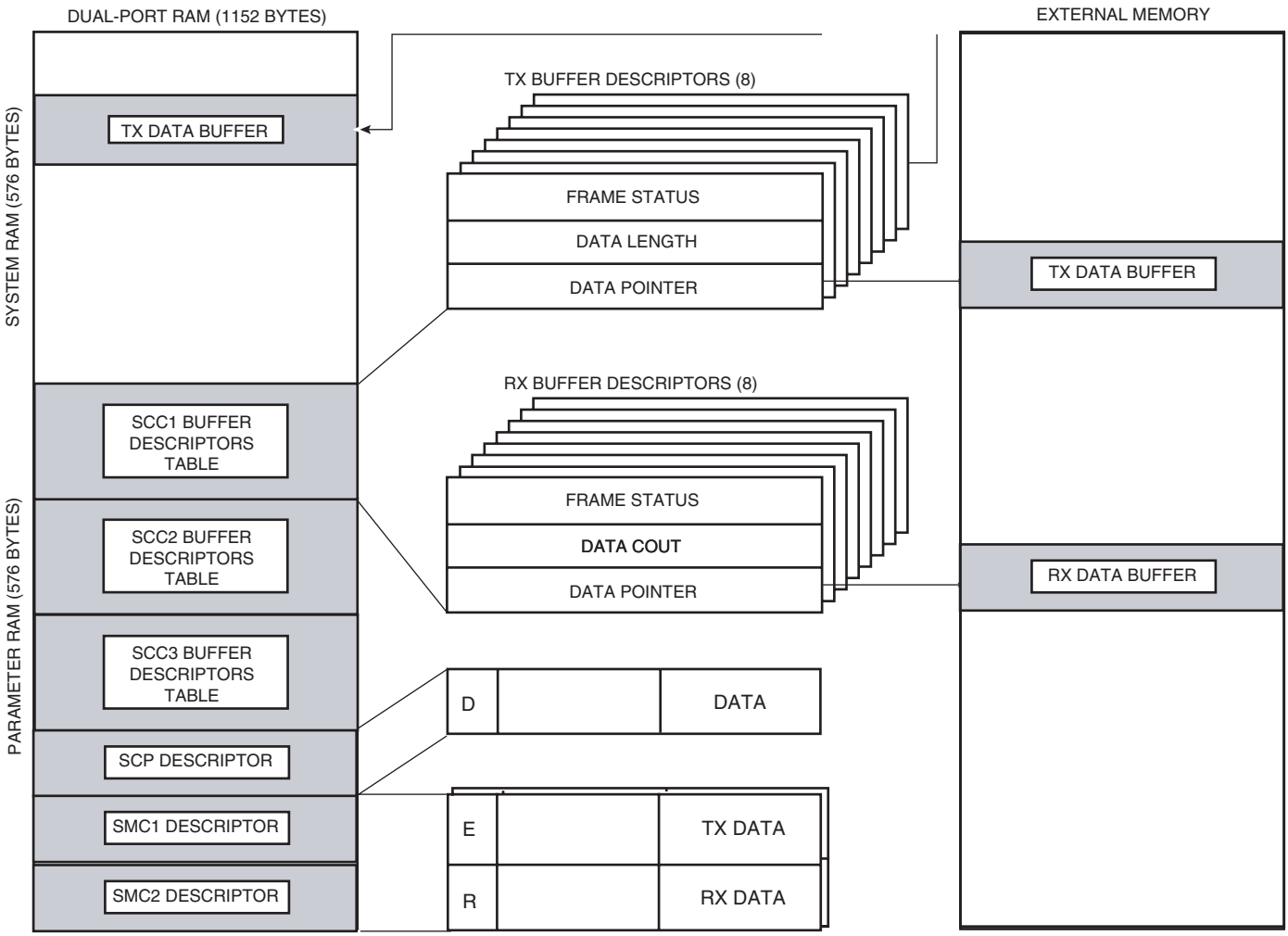
Functional Description

The TS68302 uses a microprocessor architecture which has peripheral devices connected to the system bus through a dual-port memory. Various parameters, counters, and all memory buffer descriptor tables reside in the dual-port RAM. The receive and transmit data buffer may be located in this on-chip RAM or in the off-chip system RAM (see Figure 29). Six DMA channels are dedicated to the six serial ports (receive and transmit for each of the three SCC channels). If an SCC channel's data is programmed to be located in the external RAM, the CP main controller (RISC processor) will program the corresponding DMA channel to perform the required accesses. If the data resides in the on-chip dual-port RAM, then the CP main controller accesses the RAM with one clock cycle access and no arbitration delays.

The buffer memory structure of the TS68302 can be configured by the software to closely match I/O channel requirements. The interrupt structure is also programmable to relieve the on-chip 68000/68008 core from bit manipulation functions for peripherals, allowing the processor to perform application software or protocol processing.

In some cases, the interface to equipment or proprietary networks may require the use of standard control and data signals. For these signals, the TS68302 can be programmed to use the NMSI mode. This mode is available for one, two, or all three SCC ports; remaining ports may then use one of the multiplexed interface modes: IDL, GCI, or PCM.

Figure 27. Buffer Memory Structure



68000/68008 Core Overview

The TS68302 allows operation either in the full 68000 mode with a 16-bit data bus or in the 68008 mode with an 8-bit data bus.

System Integration Block (SIB)

The TS68302 has an SIB which simplifies the task of hardware and software design. The IDMA controller eliminates the need for an external DMA controller on the system board. In addition, there is an interrupt controller that can be used in a dedicated mode to generate interrupt acknowledge signals without external logic. Similarly, the chip-select signals and wait-state logic eliminate the need to generate these signals externally.

The SIB includes the IDMA controller, interrupt controller, parallel I/O ports, dual-port RAM, three timers, chip-select logic, clock generator, and system control.

IDMA Controller

The TS68302 has one IDMA channel and six serial DMA channels which operate concurrently with other CPU operations. The IDMA can operate in different modes of data transfer as programmed by the user. The six serial DMA channels for the three full-duplex SCC channels are transparent to the user, implementing bus-cycle-stealing data transfers controlled by the TS68302's internal RISC controller. These six channels have priority over the separate IDMA channels.

The IDMA controller can transfer data between any combination of memory and I/O devices. In addition, data may be transferred in either byte or word quantities, and the source and destination addresses may be either odd or even. Every IDMA cycle requires between two and four bus cycles, depending on the address boundary and transfer size. If both the source and destination addresses are even, the IDMA fetches one word of data and then immediately deposits it. If either the source or destination block begins on an odd boundary, the transfer takes more bus cycles.

The IDMA features are as follows:

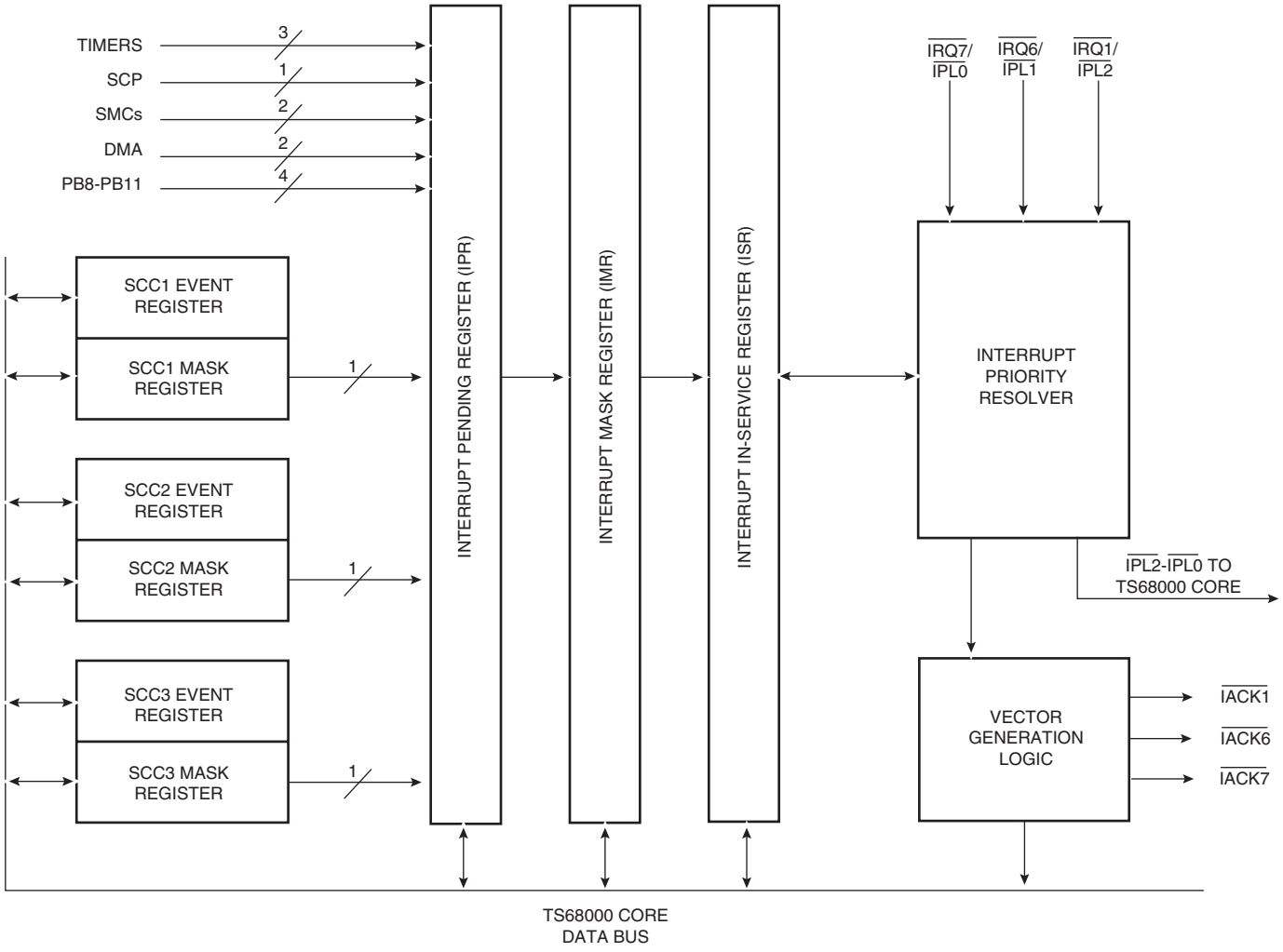
- memory-memory, memory-peripheral, or peripheral-memory data transfers,
- operation with data blocks located at even or odd addresses,
- packing and unpacking of operands,
- fast transfer rates: up to 4 MBps at 16 MHz with no wait states,
- full support of all bus exceptions: halt, bus error, and retry,
- flexible request generation
- two address pointer registers and one counter register,
- three I/O lines for externally requested data transfers,
- asynchronous bus structure with 24-bit address and 8- to 16-bit data bus.

Interrupt Controller

The interrupt controller, which manages the priority of internal and external interrupt requests, generates a vector number during the CPU interrupt acknowledge cycle. Nested interrupts are fully supported.

The interrupt controller receives requests from internal sources (INRQ interrupts) such as the timers, the IDMA, the serial controllers, and the parallel I/O pins (port B). The interrupt controller allows the masking of each INRQ interrupt source. When multiple events within a peripheral can cause the interrupt, each of these events is also maskable.

Figure 28. Interrupt Controller Block Diagram



The interrupt controller also receives external (EXRQ) requests. EXRQ interrupts are received by the IMP according to the operational mode selected. In the normal operational mode, EXRQ interrupts are encoded onto the $\overline{IPL}$ lines. In the dedicated operational mode, EXRQ interrupts are presented directly as $\overline{IRQ}7$, $\overline{IRQ}6$, and $\overline{IRQ}1$.

The interrupt controller block diagram is shown in Figure 28. The interrupt controller features are as follows:

- two operational modes: normal and dedicated,
- eighteen priority-organized interrupt sources (internal and external),
- fully nested interrupt environment,
- unique vector number for each internal/external source,
- three selectable interrupt request/interrupt acknowledge pairs.

Parallel I/O Ports

Port A and port B are two general-purpose I/O ports. Each pin in the 16-bit port A may be configured as a general-purpose I/O pin or as a dedicated peripheral interface pin. Port B has 12 pins. Eight pins may be configured as general-purpose pins or as dedicated peripheral interface pins, and four are general-purpose pins, each with interrupt capability.

Dual-Port RAM

The IMP has 1152 bytes of RAM configured as a dual-port memory. The RAM can be accessed by the internal RISC controller or one of three bus masters: the 68000 core, an external bus master, or the IDMA. All internal bus masters synchronously access the RAM with no wait states. External bus masters can access the RAM and registers synchronously or asynchronously.

The RAM is divided into two parts. There are 576 bytes used as a parameter RAM, which includes pointers, counters, and registers for the serial ports. The other 576 bytes may be used for system RAM, which may include data buffers, or may be used for other purposes such as a no-wait-state cache.

Timers

There are three timer units. Two units are identical, general-purpose timers; the third unit can be used to implement a watchdog timer function.

The two general-purpose timers are implemented with a timer mode register (TMR), a timer capture register (TCR), a timer counter (TCN), a timer reference register (TRR), and a timer event register (TER). The TMR contains the prescaler value programmed by the user. The watchdog timer, which has a TRR and TCN, uses a fixed prescaler value.

The timer features are as follows:

- Two general-purpose timer units:
  - maximum period of 16 seconds (at 16.67 MHz),
  - 60-nanosecond resolution (at 16.67 MHz),
  - programmable sources for the clock input,
  - input capture capability,
  - output compare with programmable mode for the output pin,
  - free run and restart modes.
- One watchdog timer with a 16-bit counter and a reference register:
  - maximum period of 16 seconds (16.67 MHz),
  - 0.5-millisecond resolution (at 16 MHz),
  - output signal (WDOG),
  - interrupt capability.

External Chip-select Signals and Wait-state Logic

The TS68302 has a set of four programmable chip-select signals. Each chip select has an identical structure. For each memory area, an internally generated cycle-termination signal ($\overline{\text{DTACK}}$) may be defined with up to six wait states to avoid using board space for cycle-termination logic. The four signals may each support four different classes of memory, such as high-speed static RAM, slower dynamic RAM, EPROM, and nonvolatile RAM. The chip-select and wait-state generation logic is active for all potential bus masters.

Clock Generator

The TS68302 has an on-chip clock generator which supplies internal and external high-speed clocks (up to 16.67 MHz). The clock circuitry uses three dedicated pins: EXTAL, XTAL, and CLKO.

System Control

The IMP system control consists of a system control register (SCR) containing bits for the following system control functions:

- system status and control logic,
- bus arbitration logic with low interrupt latency,
- hardware watchdog,
- low power (standby) modes,
- disable CPU logic (68000),
- freeze control for debugging on-chip peripherals,
- $\overline{AS}$ control during read-modify-write cycles.

System Control Register

The SCR is a 32-bit register that consists of system status and control bits, a bus arbiter control bit, hardware watchdog control bits, low power control bits, and freeze select bits. The eight most significant bits of the SCR report events recognized by the system control logic and set the corresponding bit in the SCR.

The low power modes are used, when no processing is required from the 68000/68008 core, to reduce the system power consumption to its minimum value. The low power modes may be exited by an interrupt from an on-chip peripheral.

Disable CPU Logic (68000)

This control allows an external processor direct connection to the bus and to the IMP's peripherals while the on-chip 68000 core is disabled. Entered during a system reset ($\overline{RESET}$ and $\overline{HALT}$ asserted together), this mode configures the IMP on-chip peripherals for use with other TS68032 units or other processors and is an effective configuration for systems needing more than three SCCs.

Freeze Control

This control is used to freeze the activity of selected peripherals and to debug systems. The IMP freezes its activity with no new interrupt requests, no memory accesses (internal or external), and no access of the serial channels. The IDMA controller completes any bus cycle in progress and releases bus ownership. No further bus cycles will be started as long as $\overline{FRZ}$ remains asserted.

DRAM Refresh Controller

The CP main (RISC) controller can optionally handle the dynamic RAM (DRAM) refresh task without any intervention from the 68000 core. The refresh request can be generated from a TS68302 timer, baud rate generator, or externally. The DRAM refresh controller performs a standard 68000-type read cycle at programmable address sequences, with user-provided RAS and CAS generation.

Communications Processor

The CP in the TS68302 includes the main controller, six serial DMA channels, three SCCs, an SCP, and two SMCs.

Host software configures each communications channel, as required by the application, to include parameters, baud rates, physical channel interfaces desired, and interrupting conditions. Buffer structures are set up for receive and transmit channels. Up to eight frames may be received or transmitted without host software involvement. Selection of the interrupt interface is also set by register bits in register space of the device.

Data is transmitted and received using the appropriate buffer descriptors and buffer data space for a channel. The CP operates is a modified polling mode on each channel and buffer descriptor to identify buffers awaiting transmission and channels requiring servicing. The user sets a bit in the buffer descriptor of a transmit frame; when the CP polls and detects this bit, it will begin transmission. Generally, no other action is required to accomplish transmission.

Main Controller

The main controller is a microcode RISC processor that services all the serial channels. The main controller transfers data between the serial channels and internal/external RAM, executes host commands, and generates interrupts to the interrupt controller.

Data is transferred from the serial channel to the dual-port RAM or to the external memory through the peripheral bus. If data is transferred between the SCC channels and external memory, the main controller uses up to six serial DMA channels for the transfer. The main controller also controls all character and address comparison and cyclic redundancy check (CRD) generation and checking.

The execution unit includes the arithmetic logic unit (ALU), which performs arithmetic and logic operations on the registers.

Serial Communication Controllers

The TS68302 has three independent SCCs. Each SCC can be configured to implement different protocols - for example, to perform a gateway function or to interface to an ISDN basic rate channel. To simplify programming, each protocol implementation uses identical data structures.

Five protocols are supported: high-level data link control (HDLC), binary synchronous communication (BISYNC), synchronous/asynchronous digital data communications message protocol (DDCMP), V.110, universal asynchronous receiver transmitter (UART), and a fully transparent mode. To aid system diagnostics, each SCC may be configured to operate in either an echo or loopback mode. In echo mode, the IMP retransmits any signals received; in loopback mode, the IMP locally receives signals originating from itself.

The clock pins (RCLK, TCLK) for each SCC can be programmed for either an external or internal source, with user-programmable baud rates available for each SCC channel.

Each SCC also supports the standard modem control signals: request to send ($\overline{\text{RTS}}$), clear to send ($\overline{\text{CTS}}$), and carrier detect (CD). Other modem signals may be provided through the parallel I/O pins.

The SCC features are as follows:

- programmable baud rate generator driven by the internal or external clock,
- data may be clocked by the programmable baud rate generator or directly by an external clock,
- provides modem signals $\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$,
- Full-duplex operation,
- Automatic echo mode,
- Local loopback mode,
- Baud rate generator outputs available externally.

The SCC HDLC mode key features are as follows:

- flexible data buffers with multiple buffers per frame allowed,
- separate interrupts for frames and buffers (receive and transmit),
- four address comparison registers with mask,
- maintenance of five 16-bit counters,
- flag/abort/idle generation/detection,
- zero insertion/deletion,
- NRZ/NRZI data encoding,
- 16-bit or 32-bit CRC-CCITT generation/checking,
- detection of non-octet aligned frames,

- detection of frames that are too long,
- programmable 0 - 15 FLAGS between successive frames,
- automatic retransmission in case of collision.

The SCC BISYNC mode key features are as follows:

- flexible data buffers,
- eight control recognition registers,
- automatic SYNC1 and SYNC2 detection,
- SYNC/DLE stripping and insertion,
- CRC-16 and LRC generation/checking,
- parity (VRC) generation/checking,
- supports BISYNC transparent operation (use of DLE characters),
- supports promiscuous (totally transparent) reception and transmission,
- maintains parity error counter,
- external SYNC support,
- reverse data mode.

The SCC DDCMP mode key features are as follows:

- synchronous and asynchronous DDCMP links supported,
- flexible data buffers,
- four address comparison registers with mask,
- automatic frame synchronization,
- automatic message synchronization by searching for SOH, ENQ, or DLE,
- CRC-16 generation/checking,
- NRZ/NRZI data encoding,
- maintenance of four 16-bit error counters.

The SCC V.110 mode key features are as follows:

- provides synchronization and reception of 80-bit frames,
- automatic detection of framing errors,
- allows transmission of the 80-bit frame.

The SCC UART mode key features are as follows:

- flexible message-oriented data buffers,
- multidrop operation,
- receiver wakeup on idle line or address mode,
- eight control character comparison registers,
- two address comparison registers,
- four 16-bit error counters,
- programmable data length (7 - 8 bits),
- programmable 1 or 2 stop bits with fractional stop bits,
- even/odd/force/no parity generation,
- even/odd/no parity check,
- frame error, noise error, break, and idle detection,
- transmits idle and break sequences,
- freeze transmission option,

- maintenance of four 16-bit error counters,
- provides asynchronous link over which DDCMP may be used,
- Flow control character transmission supported.

Serial Communication Port

The SCP is a full-duplex, synchronous, character-oriented channel which provides a three-wire interface (TXD, RXD, and clock). The SCP consists of independent transmitter and receiver sections and a common SCP clock generator. The transmitter and receiver section use the same clock, which is derived from the main clock by an on-chip baud rate generator. The TS68302 is an SCP master, generating both the enable and the clock signals. The enable signals may be generated by the general-purpose I/O pins.

The SCP allows the TS68302 to communicate with a variety of serial devices for the exchange of status and control information using a subset of the Motorola serial peripheral interface (SPI). Such devices may include industry-standard CODECs and other microcontrollers and peripherals.

The SCP can be configured to operate in a local loopback mode, which is useful for diagnostic functions. The receiver and the transmitter operate normally in these modes.

The SCP features are as follows:

- three-wire interface (SPTXD, SPRXD, and SPCLK),
- full-duplex operation,
- clock rate up to 4.096 MHz,
- programmable baud rate generator,
- local loopback capability for testing purposes.

Serial Management Controllers

The SMCs are two synchronous, full-duplex ports that may be configured to operate in either IDL or GCI mode to handle the maintenance and control portions of these interfaces. The SMC ports are not used in PCM or NMSI modes.

The SMC features are as follows:

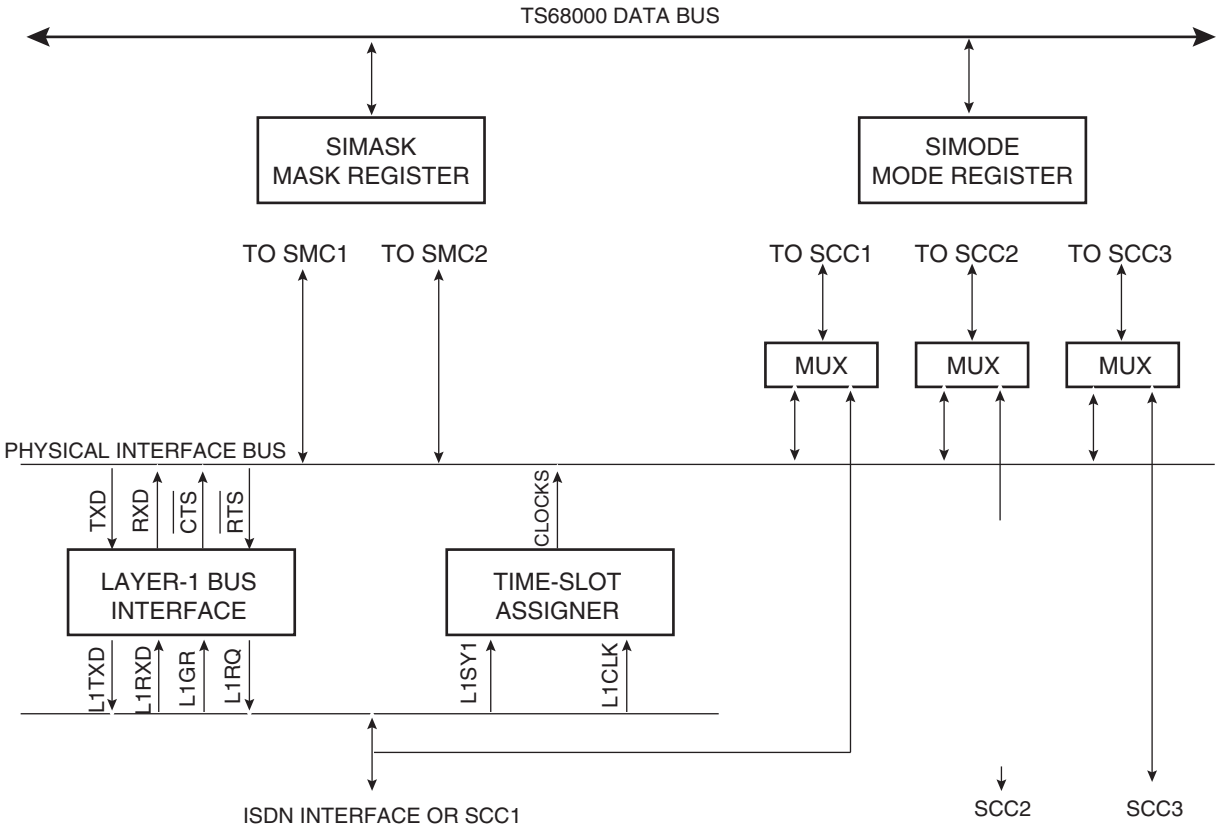
- two modes of operation - IDL and GCI,
- local loopback capability for testing purposes,
- full-duplex operation,
- SMC1 in GCI mode detects collisions on the D channel.

Serial Channels Physical Interface

The serial channels physical interface connects the physical layer serial lines and the serial controllers (three SCCs and two SMCs). The interface implements both the routing and the time-division multiplexing for the full ISDN bandwidth. It supports four buses: IDL, GCI, PCM, and NMSI (a nonmultiplexed modem interface). The multiplexed modes (IDL, GCI, and PCM) also allow multiple channels (e.g., ISDN B channels) or user-defined subchannels to be assigned to a given SCC. The serial interface also supports two testing modes: echo and loopback.

For the IDL and GSI buses, support of management functions in the frame structure is provided by the SCP or SMCs, respectively. Refer to Figure 29 for the serial channels physical interface block diagram.

Figure 29. Serial Channels Physical Interface Block Diagram



Preparation For Delivery

Packaging

Microcircuits are prepared for delivery in accordance with MIL-STD-1835.

Certificate of Compliance

Atmel offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or Atmel standards and guaranteeing the parameters are tested at extreme temperatures for the entire temperature range.

Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a) Device should be handled on benches with conductive and grounded surfaces.

b) Ground test equipment, tool and operator.

c) Do not handle devices by the leads.

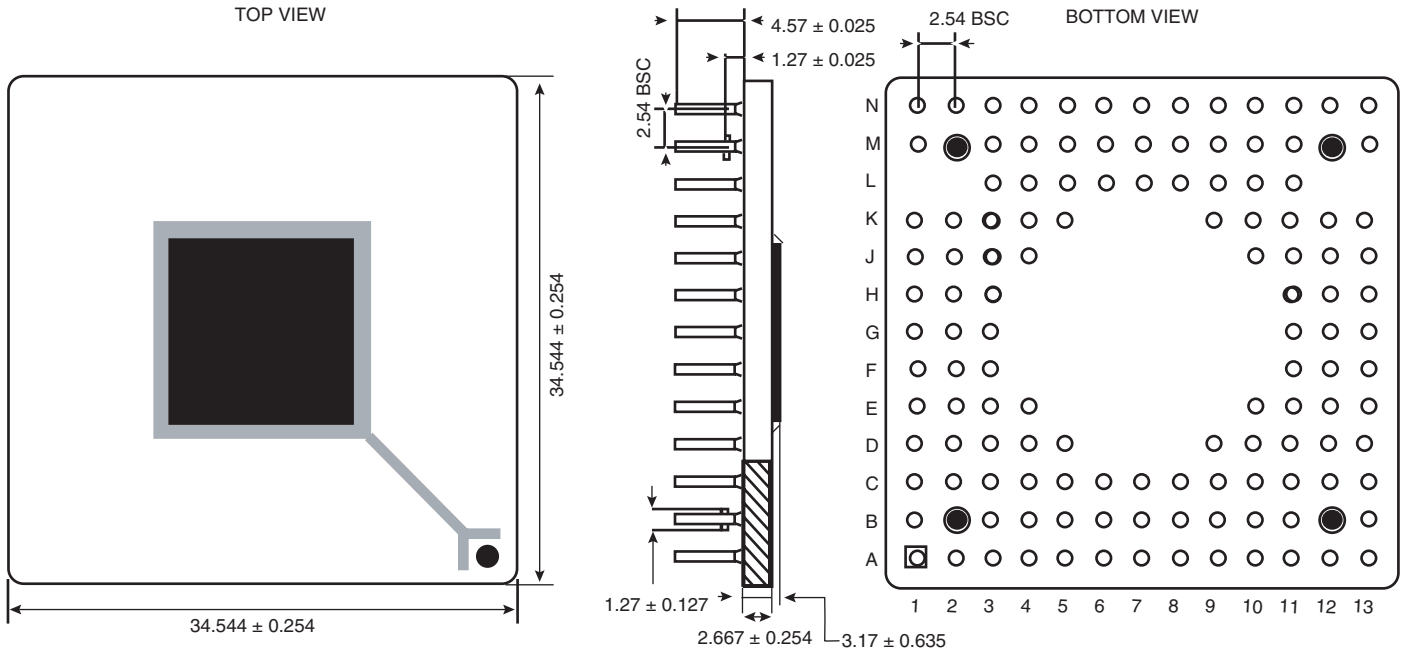
d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

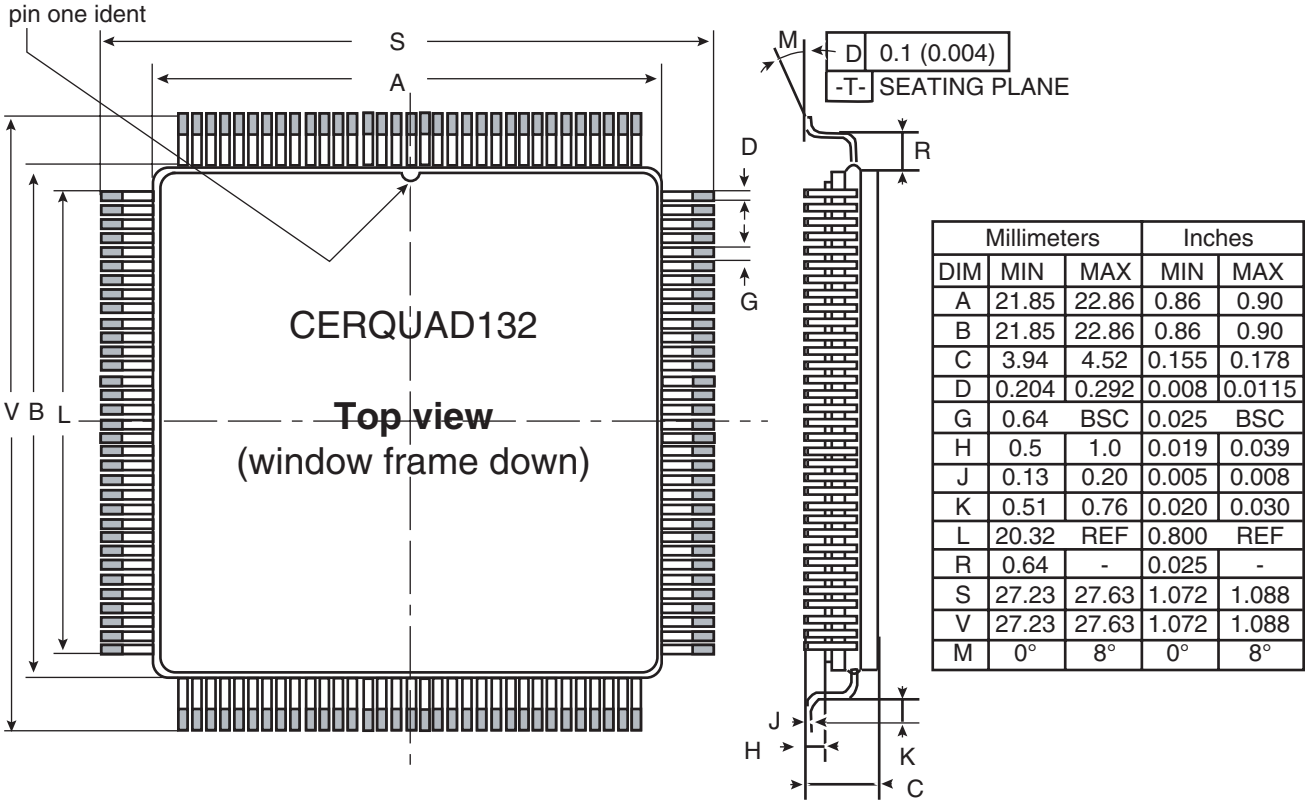
f) Maintain relative humidity above 50%, if practical.

Package Mechanical Data

132-pin - Ceramic Pin Grid Array (in millimeter)



132-pin - Ceramic Quad Flat Pack/CERQUAD



Millimeters			Inches	
DIM	MIN	MAX	MIN	MAX
A	21.85	22.86	0.86	0.90
B	21.85	22.86	0.86	0.90
C	3.94	4.52	0.155	0.178
D	0.204	0.292	0.008	0.0115
G	0.64	BSC	0.025	BSC
H	0.5	1.0	0.019	0.039
J	0.13	0.20	0.005	0.008
K	0.51	0.76	0.020	0.030
L	20.32	REF	0.800	REF
R	0.64	-	0.025	-
S	27.23	27.63	1.072	1.088
V	27.23	27.63	1.072	1.088
M	0°	8°	0°	8°

Terminal Connections

132-pin - Ceramic Pin Grid Array See Figure 2.

132-pin - Ceramic Quad Flat Pack/CERQUAD See Figure 3.

Ordering Information

HI-REL Product

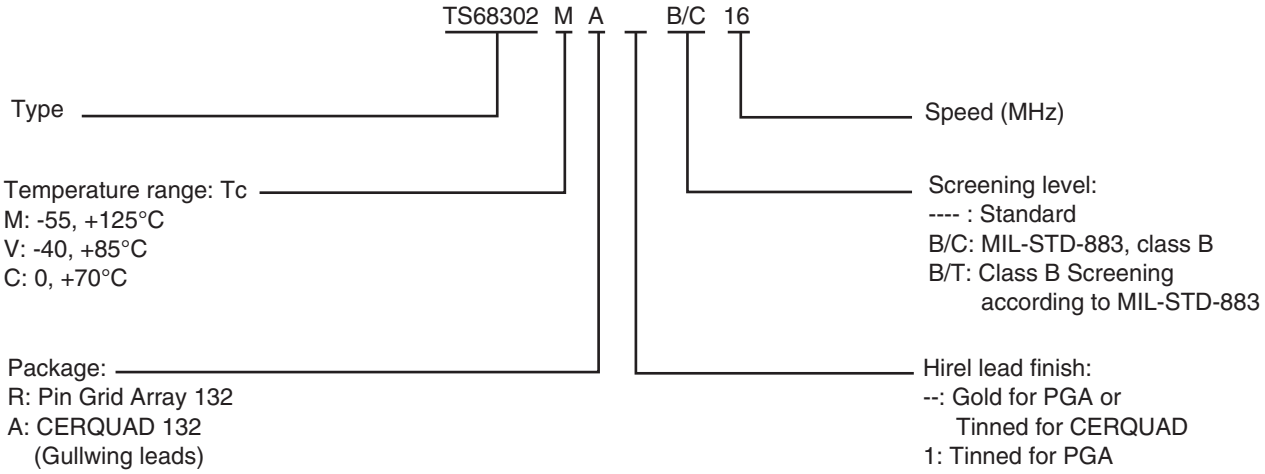
Commercial Atmel Part-Number	Norms	Package	Temperature Range Tc (°C)	Frequency MHz	Drawing Number
TS68302MRB/C16	MIL-STD-883	PGA 132	-55/+125	16.67	-
TS68302MAB/C16	MIL-STD-883	CERQUAD 132	-55/+125	16.67	-
TS68302DESC01QXC	DESC	PGA 132(1)	-55/+125	16.67	5962-93159
TS68302DESC01QYA	DESC	CERQUAD 132(1)	-55/+125	16.67	5962-93159

Note: 1. Gullwing leads.

Standard Product

Commercial Atmel Part-Number	Norms	Package	Temperature Range Tc (°C)	Frequency MHz	Drawing Number
TS68302VR16	Atmel Standard	PGA 132	-40/+85	16.67	Internal
TS68302MR16	Atmel Standard	PGA 132	-55/+125	16.67	Internal
TS68302VA16	Atmel Standard	CERQUAD 132(1)	-40/+85	16.67	Internal
TS68302MA16	Atmel Standard	CERQUAD 132(1)	-55/+125	16.67	Internal

Note: 1. Gullwing leads.



Note: For availability of the different versions, contact your local Atmel sales office.

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