SGS-THOMSON MICROELECTRONICS

TS7515

SINGLE CHIP DPSK AND FSK MODEM

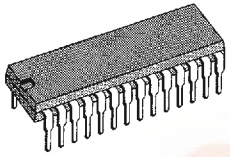
- MONOLITHIC DEVICE (INCLUDES BOTH TRANSMIT AND RECEIVE FILTERS)
- MIXING ANALOG AND DIGITAL TECHNICS
- STANDARD LOW COST CRYSTAL (4.9152MHz)
- AVAILABLE CLOCK FOR MICROPROCESSOR AT 4.9152MHz
- LOW POWER DISSIPATION (CMOS technology)
- SHARP ADJACENT CHANNEL REJECTION
- FIXED COMPROMIZE EQUALIZATION IN TRANSMITTER AND RECEIVER
- TEST LOOPS (local analog, local digital and remote digital loopbacks)
- CARRIER DETECTION OUTPUT
- CCITT AND BELL SIGNALING TONE
- 1200BPS AND 600BPS BIT SYNCHRONOUS FORMAT IN DPSK
- 1200BPS AND 600BPS +1%, -2.5% OR +2.3%, -2.5% CHARACTER ASYNCHRONOUS FORMAT (8, 9, 10 or 11 bits) IN DPSK
- 0 TO 300BPS IN FSK
- AUTOMATIC DIAL LINE MONITORING CAPABILITY
- BREAK SIGNAL SUPERVISION
- EXTERNAL VOICE BAND TONE FILTERING AVAILABLE (i.e. 550Hz or DTMF)
- CMOS AND TTL COMPATIBLE
- DIRECT INTERFACE TO STANDARD MICROPROCESSOR FAMILIES

DESCRIPTION

The TS7515 is a single chip DPSK and FSK voiceband modem, compatible with the BELL 103, 212A and CCITT V.22 A/B recommended standards.

MAIN OPERATING MODES

- Standard selection (Bell 212A/Bell 103/V.22)
- Answer tone selection (2100 or 2225Hz)
- Low speed mode selection
- Channel selection (answer/originate)
- Synchronous/asynchronous mode selection
- 8 bits to 11 bits word length selection in character asynchronous format mode
- Overspeed selection in character asynchronous format mode
- Scrambler selection
- 1800Hz guard tone selection in V.22
- Test loop selection (Digital/Analog)



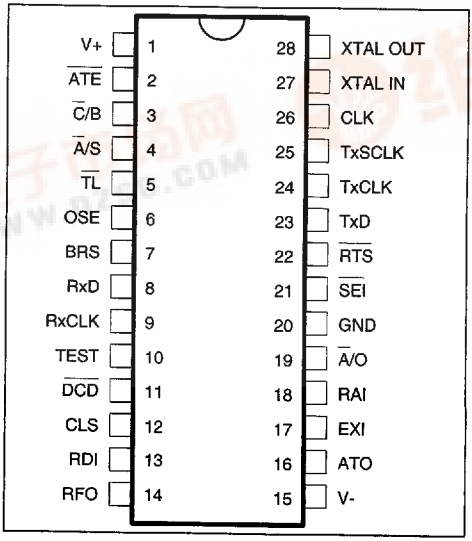
DIP28
(Plastic Package)

ORDERING INFORMATION

Part Number	Temperature Range	Package
TS7515CP	0 to +70°C	DIP28
TS7515IP	-25 to +85°C	DIP28

7515-01.TBL

PIN CONNECTIONS



7515-01 EPS

PIN DESCRIPTION

Name	Pin Type	N°	Function	Description
COMMON SECTION (supply, clock, handshaking and mode selection)				
V^+	I	1	Positive Power Supply	+5V
V^-	I	15	Negative Power Supply	-5V
GND	I	20	Ground	0V
XIN	I	27	Oscillator Input	This pin corresponds to the input of the oscillator. It is normally connected to an external crystal but may also be connected to a pulse generator. The nominal frequency of the oscillator is 4.9152MHz.
XOUT	O	28	Oscillator Output	This pin corresponds to the output of an inverter with sufficient loop gain to start and maintain the crystal oscillating.
CLK	O	26	Clock	This pin delivers a clock signal, the frequency of which is the crystal frequency. It may be used as a buffered clock a microcontroller.
$\overline{C}$/B	I	3	CCITT/BELL Selection	This three-state input selects the features corresponding to CCITT or BELL recommandation.
$\overline{A}$/S	I	4	Synchronous/ Asynchronous Selection	This three-state input selects the synchronous bit format or the asynchronous character format mode in DPSK transmission. This input allows also character length selection (refer to table 8).
CLS	I	12	Character Length	This input selects the character length in conjunction with $\overline{A}$/S input (refer to table 8).
OSE	I	6	Over-speed Selection	This input selects the over-speed in asynchronous character format mode required by CCITT recommandation (refer to table 8).
BRS	I	7	Binary Rate Selection	A Logic "0" on this input turns chip on1200 bps rate. A logic "1" turns the chip on 600bps or 0-300bps according to C/B selection.
$\overline{A}$/O	I	19	Answer/Orig. Selection	A logic "0" on this input turns the chip on answer mode. A logic "1" turns the chip on originate mode.
$\overline{TL}$	I	5	Test Loop Selection	This three-state input, selects the test loops mode (refer to table 6).
TRANSMIT SECTION				
TxD	I	23	Transmit Data	Data bits to be transmitted are serially presented on this input. A mark corresponds to a logic "1" and a space to a logic "0". This data determines which phase or frequency appears at any instant at the ATO pin in DPSK or FSK modes.
ATO	O	16	Analog Transmit Output	The analog output is the modulated carrier or the answer tone to be conditionned and sent over the phone line mixed with the filtered signal from EXI.
EXI	I	17	External Tone Input	This analog input allows external tone to be filtered by an internal low-pass filter. Filtered signal appears at ATO whatever RTS.
$\overline{ATE}$	I	2	Answer Tone Enable	A logic "0" on this input instructs the chip to enter answer signaling tone mode according C/B selection. A logic "1" turns the chip on transmit data mode (refer to table 9).
$\overline{SEI}$	I	21	Scrambler Enable Input	A logic "0" on this input enables the internal scrambler. A logic "1" instructs the chip to bypass the scrambler.
TxCLK	O	24	Transmit Clock from Modem	This output delivers a transmit bit clock generated by chip in synchronous mode. When TxSCLK is used, TxCLK is locked on TxSCLK. This output generates a logic "1" in asynchronous mode.
TxSCLK	I	25	Transmit Clock from Terminal	This input receives a bit clock supplied by the DTE. This clock synchronizes the internal transmit clock of the chip. In line monitoring mode this input receives the filters clock.
$\overline{RTS}$	I	22	Request to Send Terminal	When a logic "0" is present on this input, the chip delivers on ATO a modulated signal or a signaling tone and the filtered signal from EXI. When a logic "1" is present on this input, ATO delivers only the filtered signal from EXI. When a logic "-1" is present on this input, the receive section may be used for line monitoring and ATO delivers only the filtered signal from EXI.

PIN DESCRIPTION (continued)

Name	Pin Type	N°	Function	Description
RECEIVE SECTION				
RAI	I	18	Receive Analog Input	This input receives the analog signal from the hybrid. It corresponds to the input of the receive filters.
RFO	O	14	Receive Filter Output	This analog output is the signal received on RAI once filtered. The receive filter also equalizes the signal for adaptation to most existing lines. This output must be connected to RDI through a capacitor to meet the level detection conditions.
RDI	I	13	Receive Demodulator Input	This pin is the input of the carrier detection logic and of the demodulator
$\overline{DCD}$	O	11	Data Carrier Detect	A logic "0" on this output indicates that a valid carrier signal is present on RAI. A logic "1" means that no valid signal is being received. The hysteresis meet standards recommendation.
RxD	O	8	Receive Data	Data bits demodulated are available serially at this output.
RxCLK	O	9	Receive Clock	This output delivers a receive bit clock generated by the chip. In asynchronous mode this clock is 16 times the modulation rate. In synchronous mode the clock is equal to the bit rate.
TEST	O	10	Test	This output is an intermediate demodulator output intended for handshake and test purposes.

7515-03 TBL

The TS7515 is a general purpose monolithic DPSK and FSK modem implemented with double poly CMOS process.

It is capable of generating and receiving phase modulated signals at data rates of 1200bps or 600bps as well as frequency modulated signals at data rates up to 300bps on voice-grade telephone lines.

It is offered in a 28 or 44 in plastic package and is able to operate in full-duplex mode according to three pin selectable standards :

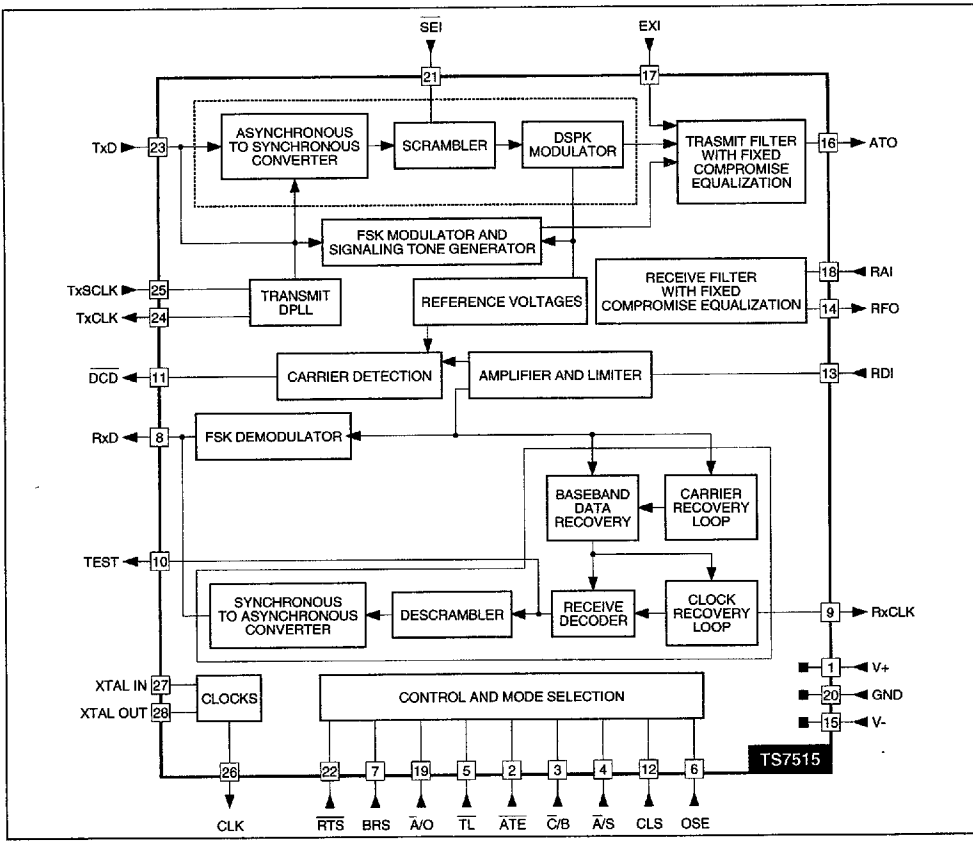
- CCITT V.22 A-B
- Bell 212A with its low speed mode
- Bell 103

All filtering functions required for frequency generation, out-of-band noise rejection and demodulation are performed by on-chip switched capacitor filters.

In phase modulation the modem provides all data buffering and scrambling functions necessary for bit synchronous format and asynchronous character format modes of operation.

Internal frequencies are generated from a 4.9152MHz crystal reference.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V^+	Supply Voltage	+7	V
V^-	Supply Voltage	-7	V
V_{in}	Analog Input	$V^- < V_{in} < V^+$	V
V_i	Digital Input (except three-state inputs)	$GND < V_i < V^+$	V
V_{i3}	Three-state Input	$V^- < V_{i3} < V^+$	V
T_{amb}	Operating Temperature	0 to 70	°C
T_{stg}	Storage Temperature	-55, 125	°C
T_S	Pin Temperature (soldering, 10s)	260	°C

Stresses above those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

ELECTRICAL OPERATING CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Supply Voltage	4.75	5	5.25	V
V^-	Negative Supply Voltage	-5.25	-5	-4.75	V
I^+	V^+ Operating Current	–	10	30	mA
I^-	V^- Operating Current	-20	-7	–	mA

7515-05 TBL

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V^+ = +5V \pm 5\%$, $V^- = -5V \pm 5\%$, GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit
DIGITAL INTERFACE					
I_L	Input Current (V_{IL}min < V_I < V_{IH} max)	-50	–	50	µA
I_{OL}	Output Low Level Current (V_{OL} = 0.4V)	800	–	–	µA
I_{OH}	Output High Level Current (V_{OH} = 2.4V)	–	–	-40	µA
V_{IL}	Input Low Voltage	GND	–	0.8	V
V_{IH}	Input High Voltage	2	–	V^+	V
V_{in}	Input Negative Voltage	V^-	–	-4	V
ANALOG INTERFACE, FILTERS INPUTS AND OUTPUTS (RAI-RFO, EXI-ATO)					
I_L	Input leakage Current (– 3V < V_{IN} < + 3V)	-10	–	10	µA
R_I	Input Resistance		3	–	MΩ
V_{IN}	Input Voltage Swing	-3	–	+3	V
V_{OF}	Output Offset Voltage	-500	–	+ 500	mV
V_{OS}	Output Voltage Swing (R_L > 10kΩ)	-2	–	+2	V
O_L	Load Capacitance	–	–	20	pF
R_L	Load Resistance	10	–		kΩ
D	Signal Distortion		-40		dB
ANALOG INTERFACE, TRANSMIT OUTPUT (ATO) EXI CONNECTED TO GND					
V_{OF}	Output Offset Voltage	-500	–	+ 500	mV
V_O	Output Voltage Swing (R_L/10kΩ, C_L = 20pF) - Carriers - Guard Tone 1800Hz/Data Signal	 -7	 2.2 -6	 -5	 V_{pp} dB
A_T	$\overline{RTS}$ Attenuation	55	–	–	dB
ANALOG INTERFACE, RECEIVE DEMODULATOR INPUT (RDI)					
Clink **	Serial Capacitor from RFO	+1	1	–	µF
N1	Maximum Detection Level to Valid $\overline{DCD}$ Output	–	–	5.5	mV_{RMS}
N2	minimum Detection Level to Valid $\overline{DCD}$ Output	3.1	–	–	mV_{RMS}
N1/N2	Hysteresis Effect	2	–	5	dB

7515-06 TBL

* Typical values are for T_{amb} = 25°C and nominal power supply values.
* * This capacitor must be unpolarized type capacitor

DYNAMIC CHARACTERISTICS

RECEIVE FILTER TRANSFER CHARACTERISTICS IN DSPK

Symbol	Parameter		Min.	Typ. *	Max.	Unit
Low Channel						
GA	Absolute Passband Gain at :	1200Hz	–	+9.5	–	dB
GR	Relative Gain to GA at :	600Hz	–	-45	–	dB
		900Hz	–	-0.5	–	dB
		1500Hz	–	+0.8	–	dB
		1800Hz	–	-50	–	dB
		2400Hz	–	-65	–	dB
High Channel						
GA	Absolute Passband Gain at :	2400Hz	–	+9.5	–	dB
GR	Relative Gain to GA at :	2100Hz		-0.2		dB
		2700Hz	–	+0.7	–	dB
		1800Hz	–	-25	–	dB
		1200Hz	–	-68	–	dB

7515-07 TBL

RECEIVE FILTER TRANSFER CHARACTERISTICS IN FSK

In FSK the receive filter is the same as in DSPK but the sampling frequency is multiplied be a 14/15 ratio (i.e. 2400Hz in DSPK becomes 2240Hz in FSK).

Symbol	Parameter		Min.	Typ. *	Max.	Unit
Low Channel						
GA	Absolute Passband Gain at :	1120Hz	–	9.5	–	dB
High Channel						
GA	Absolute Passband Gain at :	2240Hz	–	9.5	–	dB

7515-08 TBL

* Typical values are for T_{amb} = 25°C and nominal power supply values.

DEVICE OPERATION

Transmitter

The transmitter consists of two analog signal generators followed by switched capacitor and continuous filters. In phase modulation operation mode the DPSK signal generator is preceded by a selectable scrambler and an asynchronous to synchronous converter is included in character asynchronous format mode.

Tone allocation : the modem on the end of the line which initiates the call is called the originate modem. In normal transmission operation it transmits in low channel and receives in high channel. The other modem is the answer modem which transmits in high channel and receives in low channel.

Modulators

DPSK modulator : the phase modulation type is differential quadrature four phase shift keying (see Table 1). The 1200bps data stream to be transmitted is converted into two 300 dibits per second streams which modulate alternatively two independant carriers. Consequently the base band shaping is included is a 5-bit address ROM which generates samples for a 8-bit switched capacitor DAC at a frequency equals to 8 times the carrier frequency.

Table 1 : DPSK Modulation

BRS	TxD		Phase Shift
	n – 1	n	
0	0	0	+90 °
		1	0 °
	1	1	+270 °
		0	+180 °
1	X *	0	+90 °
		1	+270 °

* x : don't care.

FKS modulator and tone generator : a frequency synthesizer provides accurate clocks to a switched capacitor sine wave generator (see Table 2). Phase continuity is maintained when a frequency shift occurs.

Table 2 : FSK Modulation (BELL 103)

$\overline{A}$/0	TxD	Standard Frequency
0	0	2025Hz
	1	2225Hz
1	0	1070Hz
	1	1270Hz

Transmit Filters

To avoid unwanted frequency components to be echoed by the hybrid in the reception path, to maintain the level of spurious out-of-band signals transmitted to the telephone line below the limits specified by administrations (see figure 1) and to complete statistical amplitude and phase equalization, the analog signals are processed by ten poles sharp pass-band switched capacitor filters. The response of these filters depends on the selected channel (Answer/Originate) and the selected standard (BELL 212 - V.22 BELL 103). A continuous filter eliminates parasitic sampling effects. An additional low-pass filter input is provided. This allows to mix and filter such tones as DTMF signals or special guard tones (550Hz) to the transmitted signal.

Scrambler

The scrambler used during phase modulation ensures the transmission of a continuously changing pattern. This avoids the receiving modem to drop out of lock on certain continuous repetitious data patterns.

This scrambler may be disabled during handshaking procedures. In V.22 a special unlocking sequence is performed on 64 spaces pattern at scrambler output.

Asynchronous To Synchronous Converter

The DPSK signal is synchronous in nature but the modem has both an asynchronous as well as a synchronous mode of operation in DPSK. So a data buffer is necessary to convert variable rate asynchronous character data to an equivalent bit oriented synchronous data stream. This is done by inserting or deleting stop bits. If serial input data contains a break signal through one character (including start and stop bits). One break will be extended to at least $2 \cdot M + 3$ bits long (where N is the number of transmitted bit/character).

Figure 1 : Transmitted Signal Template

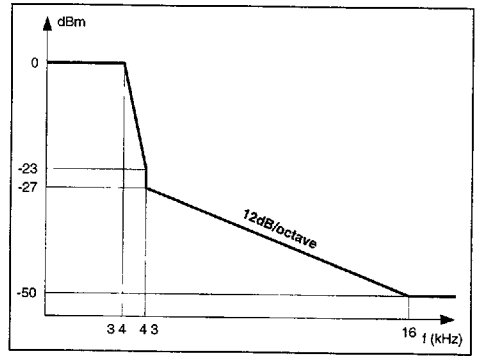


Table 3 : Output Frequency Deviation

Standard Frequency	Frequency Using 4.91MHz	% Deviation from Standard	Mode
1070Hz	1066.7Hz	-0.3%	BELL 103 Originate
1200Hz	1200Hz		BELL 212A or V22, Originate
1270Hz	1269.4Hz	-0.05%	BELL 103 Originate
1800Hz	1807.4Hz	+0.4%	Guard Tone V.22
2025Hz	2021Hz	-0.2%	BELL 103 Answer
2100Hz	2104.1Hz	+0.2%	Answer Tone CCITT
2225Hz	2226.1Hz	+0.05%	BELL 103 Answer or Answer Tone BELL
2400Hz	2400Hz		BELL 212A or V.22, Answer

RECEIVER

The receiver includes two band-pass filters followed by an amplifier and a hard limiter. Depending on selected standard, the detector output is passed through a DPSK demodulator or a FSK demodulator. The DPSK demodulator is followed by a descrambler and a selectable synchronous to asynchronous converter. In addition a carrier detector monitors the level of the received signal.
Tone allocation : in normal transmission operation the originate modem receives in high channel and transmits in low channel. The answer modem receives in low channel and transmits in high channel.

Receive Filters

The signal delivered by the hybrid to the receive analog input is a mixture of transmitted signal, received signal and noise with a level in the range from -48dBm to -0dBm. Depending on the operating mode and the selected standard the 20 poles receive switched capacitor band-pass filter selects the frequency band of the low channel or the high channel. A ratio of 14/15 is applied on the sampling clock frequency between FSK and DPSK in the same operating mode (Answer/Originate). These filter reject out-of-band transmission noise components and undesirable adjacent channel echo signals which can be fed from the transmit section into the receive section. Fixed equalization is included in order to assure low error rate.

Amplifier And Hard Limiter

Once filtered the received signal is amplified and fed to the carrier detector. In order to limit analog parts in the design all the demodulator techniques used in the TS7515 are based on zero crossing detection. So the received signal is just limited before entering demodulator.

Demodulators

DPSK demodulator : a DPLL is used to recover the carrier signal. This DPLL has a lock range of ±2Hz but as the incoming carrier may present an offset of ±7Hz a second loop allows the first DPLL to lock on the exact frequency of the carrier with an accuracy of ±1Hz and to follow its slow variations in 1200 bands mode only. Then the limited received signal is mixed through exclusive-Or with the recovered carrier and with the 90 degrees phase shifted recovered carrier. The results are processed through four poles Bessel filters wich provide a good amplitude propagation time compromise. The received sampling clock recovered from these base and data with a simple DPLL. The received data are sampled by this clock and then converted into a serial synchronous bit stream.

FSK demodulator : the zero crossing detector output is passed through a shift register whose length depends on the operating mode (Answer/Originate). The output of the shift register and the detector are mixed into an exlusive Or. Then they are processed through a four poles Bessel filter and a slicer.

Test Output

Once demodulated DPSK data are generally processed (cf next paragraph) but during call set-up procedures or data set testing it is of importante to monitor the demodulator output. So in DPSK mode demodulated data are available on TEST pin.

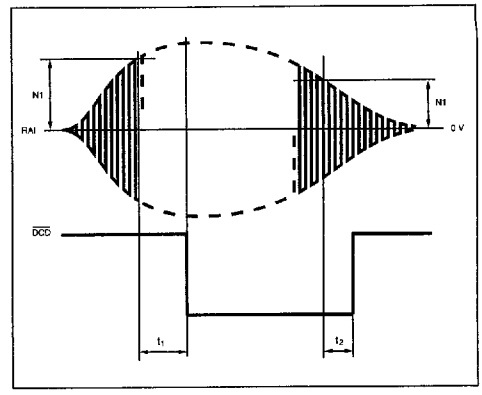
Descrambler and Synchronous to Asynchronous Converter

Data coming from the DPSK demodulator are unscrambled. In V.22 the unlocking sequence is detected at descrambler input and the original data are decoded before descrambling. In asynchronous character format mode of operation a data buffer is able to detect missing stop bits and reinsert them. The converter is able to recognize the break signal and transmits it without modification.

Carrier Detector

Whenever valid signals are being received at the input of the demodulator and are acceptable for demodulation, carrier detect output is pulled down. A delay is timed out before the carrier received or carrier lost signal changes carrier detect output to provide immunity against noise bursts. The modem also provides at least 2dB of hysteresis between the carrier ON and the carrier OFF thresholds (see Figure 2).

Figure 2



In DPSK mode 105ms ≤ t_1 ≤ 205ms 10ms ≤ t_2 ≤ 24ms
In FSK mode 105ms ≤ t_1 ≤ 205ms 25ms ≤ t_2 ≤ 75ms

LOOP TEST

Loop 3

This loop is called the analog loop. When it is selected the receive filters and the modulators are configured to process the same channel as the transmit section. The transmit carrier has to be looped back externally to the receive analog input. This loop allows the user or the DTE to check the satisfactory working of the local DCE.

Loop 2

This loop is called the digital loop. When it is selected received data, receive clock and data carrier detect signals are respectively and internally looped back on transmit data, transmit clock from terminal and request to send . This loop allows the user or the DTE to check the satisfactory working of the line and the remote DCE.

Clocks

In synchronous mode of operation TxCLK, TxSCLK and RxCLK are respectively working as the V.24 circuits C114, C13 and C15. In asynchronous mode of operation RxCLK can be used as baud rate clock to synchronize the transmit and the receive sections of a UART (see table 4).

Oscillator Output

The buffered master clock (4.9152MHz) is made available at output CLK. It can be used as a clock for a microcontroller.

Voltage Reference

A temperature compensated voltage reference build with a zener is included in the chip. This vol-tage is used to calibrate transmit levels and to generate the carrier detection thresholds.

LINE MONITORING

A special mode has been included in the TS7515 to monitor the line during an automatic call. When this mode is selected ($\overline{A}/S$ = 0, $\overline{RTS}$ = -1) receive filters clock is directly derived from TxSCLK which allows the user to precisely observe broad frequency bands. Furthermore the DCD performs a fast carrier detection equivalent to an envelope detection. As the center frequency of the receive filters is proportional to TxSCLK frequency in this mode it is possible to tune the passband according to the frequency to be detected (see Table 5).

TxSCLK : must be created from the TS7515 master clock (4.9152MHz).

Table 4 : Clock Operation

$\overline{A}/S$	$\overline{C}/B$	BRS	TxCLK	RxCLK	Mode
-1 or 0	-1 or 0	0	1	19.2kHz	V.22 Asynchronous
		1	1	9.6kHz	
	1	0	1	19.2kHz	BELL 212A Asynchronous and BELL 103
		1	1	4.8kHz	
1	-1 or 0	0	1200Hz	1200Hz	V.22 Synchronous
		1	600Hz	600Hz	
	1	0	1200Hz	1200Hz	BELL 212A Synchronous and BELL 103
		1	1	4.8kHz	

Table 5

TxSCLK	Originate ($\overline{A}/O$ = 1)		Answer ($\overline{A}/O$ = 0)		Application
	Center Frequency	Passband at 3dB	Center Frequency	Passband at 3dB	
210kHz	2400Hz	±400Hz	1200Hz	±400Hz	Voice Detection
45kHz	510Hz	±85Hz			440Hz Detection
			260Hz	±85Hz	330Hz Detection
76.8kHz			440Hz	±150Hz	Dial Tone and Busy Tone Detection

APPLICATION INFORMATION

In a typical application a microcontroller provides control and interface to the Data Terminal Equipment (DTE), and a Direct Access Arrangement provides connection to the telephone line. Then the TS7515 can communicate with the most popular modems (BELL 103 and BELL 212A) in countries under BELL standards and popular modems (V.22) in countries under CCITT recommendations.

Power Supplies Decoupling and Layout Considerations

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performances of the TS7515 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout.

The power supplies should be bypassed with tantalum or electrolytic capacitors to obtain noise free operation. These capacitors should be located close to the TS7515. The electrolytic type capacitors should be bypassed with ceramic capacitors for improved high frequency performance.

Power supplies connections should be short and direct. Ground loops should be avoided.

Coupling between analog inputs and digital lines should be minimized by careful layout. The RDI input (Pin 13) is extremely sensitive to noise.

The connection between this point and RFO (Pin 14) through a ceramic type capacitor should be as short as possible and coupling between this connection and digital signals should be minimized by careful layout.

Carrier Recovery Loop

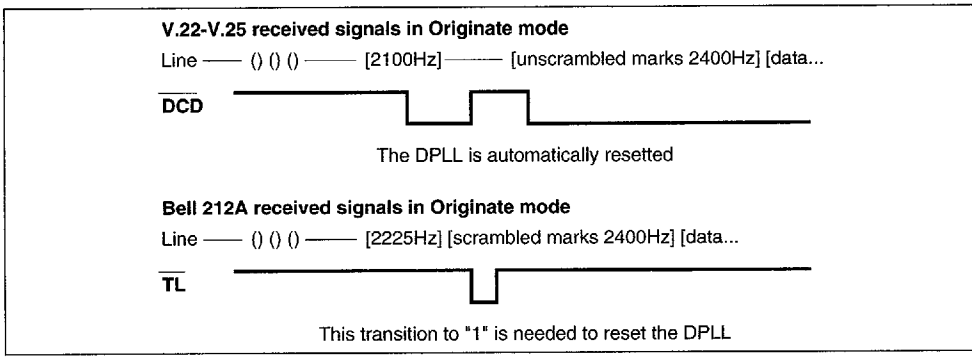
The carrier recovery loop utilizes a digital phase lock loop. Performances of the TS7515 depend directly on this DPLL which needs to be resetted before receiving a DPSK carrier.

Three ways of resetting the DPLL exist on the TS7515 :

- A trailing edge on $\overline{DCD}$.
- Changing FSK mode to DPSK mode or reversely.
- Changing receive channel.

These three ways of resetting the DPLL should be used in the software included in the microcontroller to perform the various set-up procedures and handshakes.

Figure 3 : Examples



TYPICAL PERFORMANCES

The typical performances listed below are achieved with the environment described in the previous paragraph.

- Dynamic range : 0dBm to - 45dBm.
- BER performances :

Conditions : Xmit level = - 10dBm,
Rec level = - 25dBm,
Message 511 bits on CCETT lines 1, 2, 3, 4 and CNET lines QN and 3 VHF and US lines C4, C2, and C0.

1200 bps operation
- BER 10^{-3} for a 7 dB SNR
- BER 10^{-6} for a 11 dB SNR

300 bps operation
- BER 10^{-3} for a 3 dB SNR
- BER 10^{-6} for a 8 dB SNR

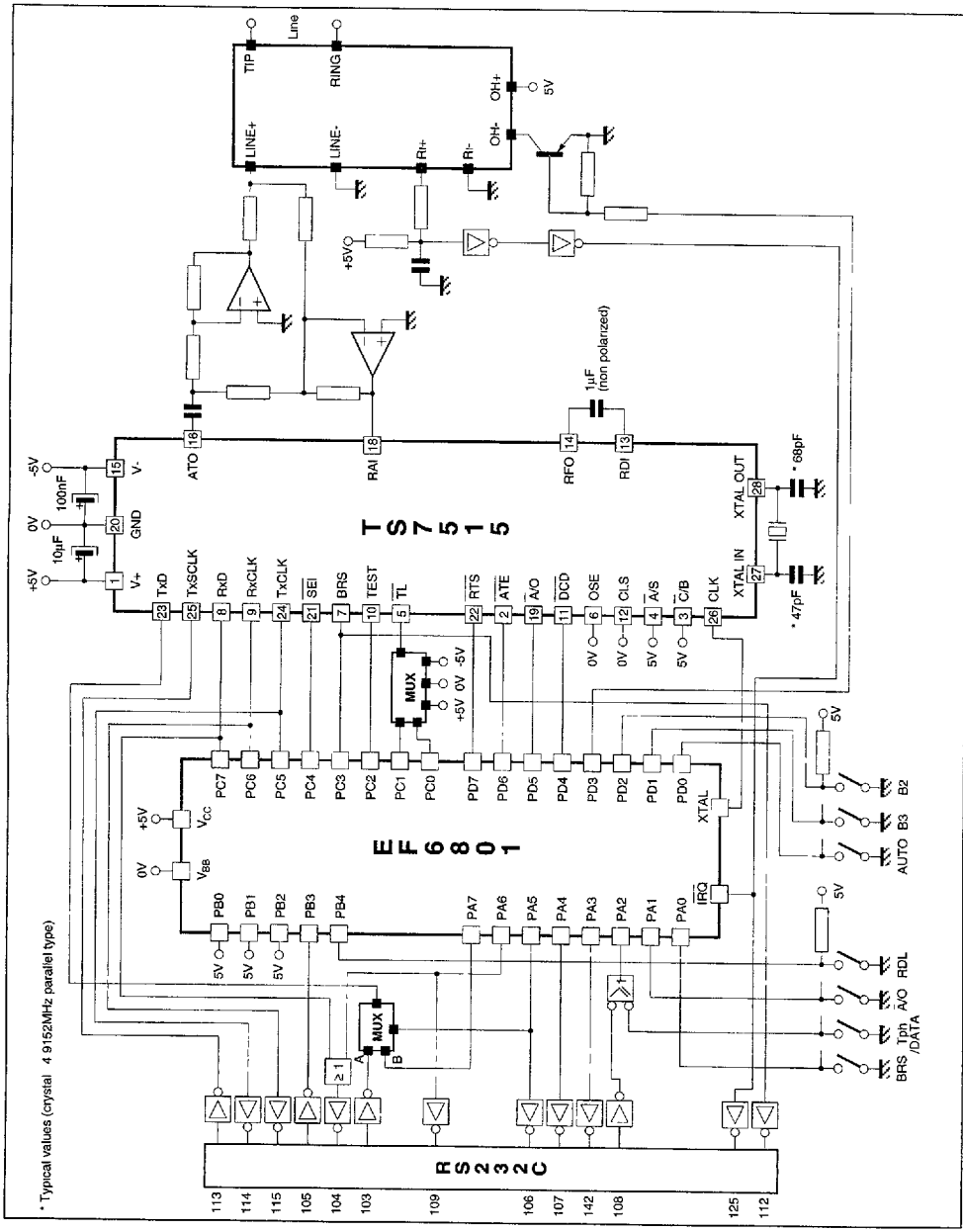
- Specific DPSK performances

Phase hits sensitivity	:	25 degree	BER $< 10^{-6}$
Phase Jitter	:	35 degree	
Amplitude hits sensitivity	:	± 10dB	
Offset carrier sensitivity	:	SNR increase < +1dB	
1800Hz guard tone sensitivity	:	SNR increase < +2dB	

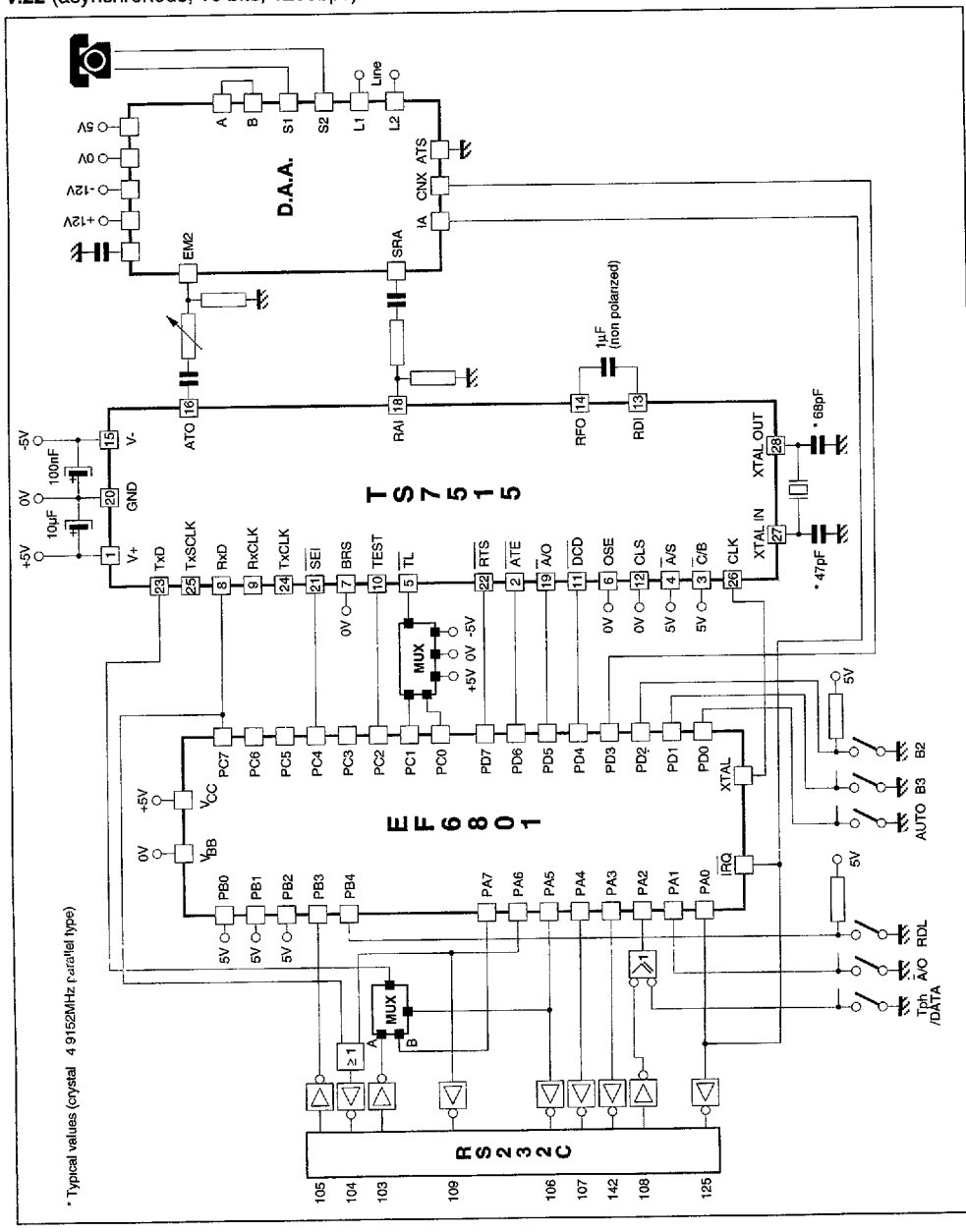
- Specific FSK performances

Bias Distortion : less than 5 %
Jitter : less than 12 %

BELL 212A APPLICATION (synchronous)



V.22 (asynchronous, 10 bits, 1200bps)



SELECTION MODE TABLES

SYNTHESIS OF DIFFERENT MODES FOR RECEIVE SECTION

Table 6

C/B	BRS	TL	A/0	Receive	Mode
-1 ou 0	X	-1	0	DPSK Originate Loop 3	V.22
			1	DPSK Answer Loop 3	
		0	0	DPSK Answer Loop 2	
			1	DPSK Originate Loop 2	
		1	0	DPSK Answer	
			1	DPSK Originate	
1	0	-1	0	DPSK Originate Loop 3	BELL 212 A including BELL 103
			1	DPSK Answer Loop 3	
		0	0	DPSK Answer Loop 2	
			1	DPSK Originate Loop 2	
		1	0	DPSK Answer	
			1	DPSK Originate	
	1	-1	0	FSK Originate Loop 3	
			1	FSK Answer Loop 3	
		0	0	FSK Answer Loop 2	
			1	FSK Originate Loop 2	
		1	0	FSK Answer	
			1	FSK Originate	

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Answer : Receive in low channel
Originate : Receive in high channel
Loop 3 : Analog loop
Loop 2 : Digital loop

SYNTHESIS OF DIFFERENT MODES FOR TRANSMIT SECTION

Table 7

ATE	C/B	BRS	A/0	Transmit	Mode
0	– 1 or 0	X	X	2100Hz	Answer Tone
	1			2225Hz	
1	– 1	0	0	DPSK 1200bps Answer	V.22 without Guard Tone
			1	DPSK 1200bps Originate	
		1	0	DPSK 600bps Answer	
			1	DPSK 600bps Originate	
	0	0	0	DPSK 1200bps Answer	V.22 with 1800Hz Guard Tone
			1	DPSK 1200bps Originate	
		1	0	DPSK 600bps Answer	
			1	DPSK 600bps Originate	
	1	0	0	DPSK 1200bps Answer	BELL 212A
			1	DPSK 1200bps Originate	
		1	0	FSK 0-300bps Answer	
			1	FSK 0-300bps Originate	

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Answer : Receive in high channel
Onginate : Receive in low channel

SELECTION MODE TABLES (continued)

MODE SELECTION IN PHASE MODULATION TRANSMISSION

Table 8

$\overline{A/S}$	CLS	OSE
-1	0	0
		1
	1	0
		1
0	0	0
		1
	1	0
		1
1	0	0

Transmission Mode	Length	Over-speed
Asynchronous	8	+1%, -2.5%
		+2.3%, -2.5%
	11	+1%, -2.5%
		+2.3%, -2.5 %
	9	+1%, -2.5%
		+2.3%, -2.5%
	10	+1%, -2.5%
		+2.3%, -2.5%
Synchronous		

TEST PIN

Table 9

$\overline{ATE}$	$\overline{C/B}$	BRS
0	-1 or 0	0
		1
	1	0
		1
1	-1	0
		1
	0	0
		1
	1	0
		1

Transmit	Receive	Test
2100Hz	V.22 DPSK 600bps	DDO
	V.22 DPSK 1200bps	DDO
2225Hz	BELL 212A DPSK 1200bps	DDO
	BELL 103 FSK 0-300bps	HLO
V.22 without Guard Tone DPSK 1200bps		DDO
V.22 without Guard Tone DPSK 600bps		DDO
V.22 with Guard Tone DPSK 1200bps		DDO
V.22 with Guard Tone DPSK 600bps		DDO
BELL 212A DPSK 1200bps		DDO
BELL 103 FSK 0-300bps		HLO

DDO : DPSK demodulator output
HLO . Hard limiter output

SUMMARY OF THE DIFFERENCES BETWEEN BELL 212A AND V.22 A-B

Table 10

Feature	BELL 212A	V.22
Low Speed Mode	0-300bps FSK	600bps DPSK
Guard Tone	No	1800Hz Optional *
Answer Tone	2225Hz	2100Hz
Character Length is Asynchronous Mode in DPSK	9, 10 bits	8, 9, 10, 11 bits **
Over Speed Mode in Asynchronous Mode in DPSK	No	Yes **
64 Spaces Detection	No	Yes

* 550Hz may be externally generated and added to the transmit signal through EXI.
** Features of V.22 are available in BELL 212A on the chip.
All these differences are taken into consideration inside the TS7515.