TSB12LV21A
(PCILynx) IEEE 1394-1995 BUS TO PCI BUS INTERFACE

SLLS273 – APRIL 1997

- **Supports Provisions of IEEE 1394-1995 (1394) Standard for High-Performance Serial Bus†**
- **Performs the Function of a 1394 Cycle Master**
- **Supports 1394 Transfer Rates of 100, 200 and 400 Mbit/s**
- **Provides Three Sizes of Programmable FIFOs**
- **Provides PCI Bus Master Function for Supporting DMA Operations**
- **Compliant With PCI Specification 2.1**
- **Provides PCI Slave Function for Read/Write Access of Internal Registers**
- **Supports the Plug-and-Play (PnP) Specification**
- **Provides an 8-/16-bit Zoom Video (ZV) Port for the Transferring of Video Data Directly to an External Motion Video Memory Area**
- **Operates from a 3.3-V Power Supply While Maintaining 5-V Tolerant Inputs**
- **High-Performance 176-Pin PQFP (PGF) Package**

description

The TSB12LV21A (PCILynx) provides a high-performance IEEE 1394-1995 interface with the capability to transfer data between the 1394 phy-link interface, the PCI bus interface, and external devices connected to the local bus interface. The 1394 phy-link interface provides the connection to the 1394 physical layer device and is supported by the on-board link layer controller (LLC). The LLC provides the control for transmitting and receiving 1394 packet data between the FIFO and phy-link interface at rates of 100 Mbit/s, 200 Mbit/s, and 400 Mbit/s. The link layer also provides the capability to receive status from the physical layer device and to access the physical layer control and status registers by the application software.

An internal 1K-byte memory is provided that can be configured as multiple variable-size FIFOs and eliminates the need for external FIFOs. Separate FIFOs can be user configured to support 1394 receive, asynchronous transmit, and isochronous transmit transfer operations.

The PCI interface supports 32-bit burst transfers up to 33 MHz and is capable of operating as both master and target devices. Configuration registers can be loaded from an external serial EEPROM, allowing board and system designers to assign their own unique identification codes. An autoboot mode allows data-moving systems (such as docking stations) to be designed to operate on the PCI bus without the need for a host CPU.

The DMA controller uses packet control list (PCL) data structures to control the transfer of data and allow the DMA to operate without host CPU intervention. These PCLs can reside in PCI memory or in memory that is connected to the local bus port. The PCLs implement an instruction set that allows linking, conditional branching, 1394 data transfer control, auxiliary support commands, and status reporting. Five DMA channels are provided to accommodate programmable data types. PCLs can be chained together to form a channel control program that can be developed to support each DMA channel. Data can be stored in either big endian or little endian format eliminating the need for the host CPU to perform byte swapping. Data can be transferred to either 4-byte aligned locations to provide the highest performance or to nonaligned locations to provide the best memory use.

† This serial bus implements technology covered by one or more patents of Apple Computer, Incorporated and SGS Thomson, Limited.

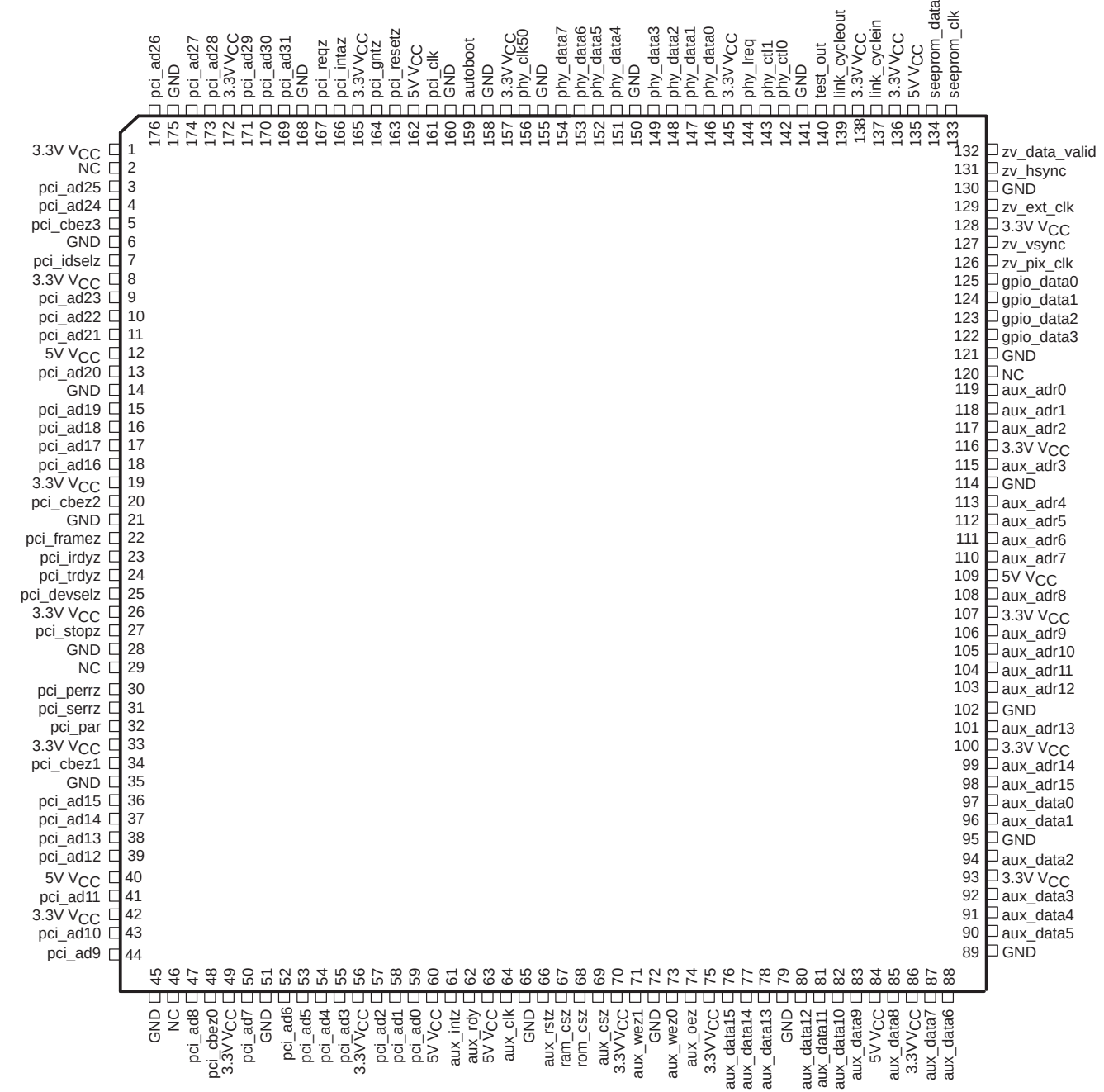
description (continued)

The RAM, ROM, AUX, ZV, and general purpose I/O (GPIO) ports collectively implement the local bus interface. These ports are mapped into the PCI address can be accessed either through the PCI bus or internal DMA transactions. Internal transactions do not appear on the external PCI bus, thereby conserving PCI bandwidth. DMA packet control lists or other data that may be stored in external RAM or ROM attached to the local bus interface. This further reduces PCI use and generally improves performance. The ZV local bus port is designed to transfer data from 1394 video devices to an external device connected to the PCILynx ZV port. This interface provides a method of receiving 1394 digital camera packets directly to a ZV-compliant device attached to the local bus interface.

Built-in test registers, a dedicated test output terminal, and four GPIO terminals allow observation of internal states and provides a convenient software debug capability. Programmable interrupts are available to inform driver software of important events such as 1394 bus resets and DMA-to-PCL transfer completion.

The 3.3-V internal operation provides reduced power consumption while maintaining compatibility with 5-V signaling environments. The PCI interface is compatible with both 3-V and 5-V PCI systems.

PGF PACKAGE
(TOP VIEW)



NC – No internal connection

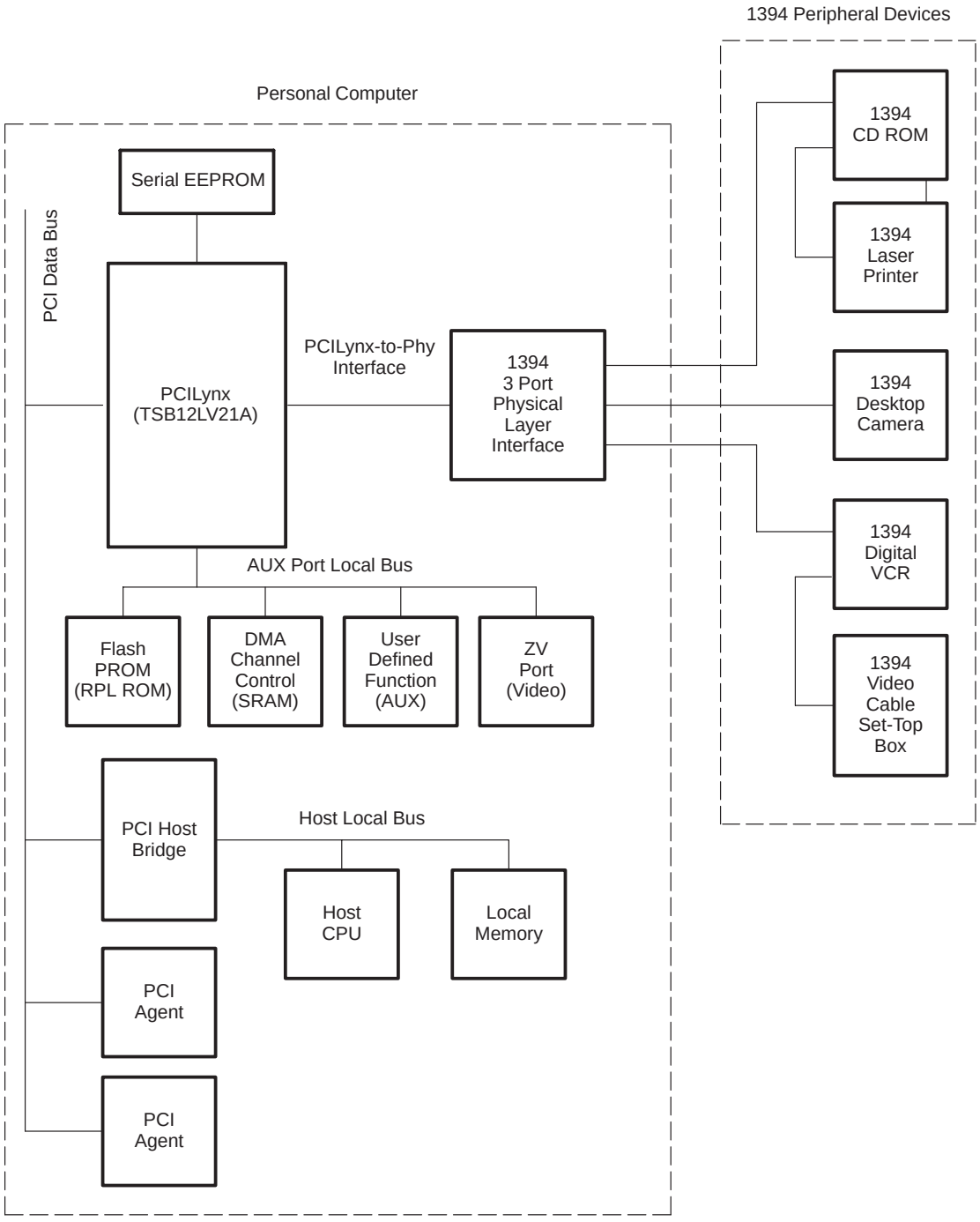
Terminal Functions

Terminal Name	Terminal No.	I/O	Description
3.3V V_{CC}	1,8,19,26,33,42,49 56,70,75,86,93,100 107,116,128,136,138, 145,157,165,172	I	3.3-V power input
5V V_{CC}	12,40,60,63 84,109,135,162	I	5-V tolerant power input. When interfacing with a 3.3-V parts, these terminals should be connected to 3.3-V power.
autoboot	159	I	Autoboot to select autoboot mode
aux_adr15–0	98,99,101,103–106 108,110–113,115 117–119	O	Auxiliary port address lines
aux_clk	64	O	Auxiliary port clock out (output at frequency of PCI clock)
aux_csz	69	O	Auxiliary port chip select
aux_data15–0	76–78,80–83,85,87 88,90–92,94,96,97	I/O	Auxiliary port bidirectional data bus to external logic
aux_intz	61	I	Auxiliary port interrupt
aux_oez	74	O	Auxiliary port output enable
aux_rdy	62	I	Auxiliary port ready indication (from external logic)
aux_rstz	66	O	Auxiliary port reset out
aux_wez1–0	71,73	O	Auxiliary port write strobes (to external logic)
GND	6,14,21,28,35,45 51,65,72,79,89,95 102,114,121,130,141 150,155,158,160,168 175	I	Ground
gpio_data3–0	122–125	I/O	Auxiliary port general purpose programmable I/O signals
link_cyclein	137	I	Optional external 8-kHz clock
link_cycleout	139	O	Cycle timer 8-kHz cycle clock out
N/C	2,29,46,120		Not connected
pci_ad31–0	169–171,173,174,176 3,4,9–11,13,15–18 36–39,41,43,44,47,50 52–55,57–59	I/O	PCI multiplexed address/data bus signals
pci_cbez3–0	5,20,34,48	I/O	PCI multiplexed command/byte enable signals
pci_clk	161	I	PCI system clock
pci_devselz	25	I/O	PCI device select
pci_framez	22	I/O	PCI frame signal

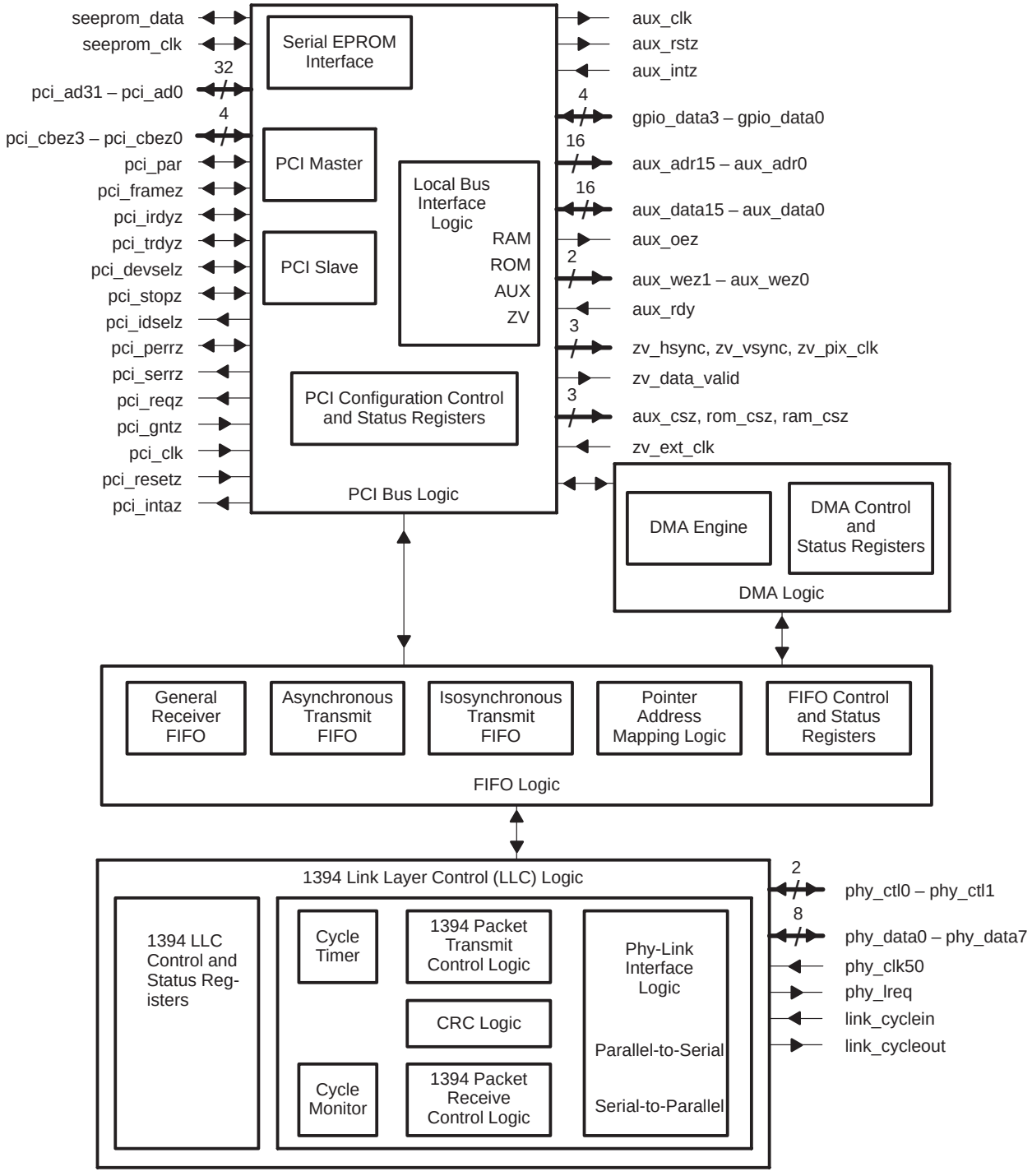
Terminal Functions (continued)

Terminal Name	Terminal No.	I/O	Description
pci_gntz	164	I	PCI bus grant signal (from PCI bus arbiter)
pci_idselz	7	I/O	PCI initialization device select
pci_intaz	166	OD	PCI system interrupt A. This is an open drain signal.
pci_irdyz	23	I/O	PCI initiator-ready signal
pci_par	32	I/O	PCI parity signal
pci_perrz	30	I/O	PCI data-parity-error signal
pci_reqz	167	O	PCI master bus request (to PCI bus arbiter)
pci_resetz	163	I	PCI system reset
pci_serrz	31	OD	PCI system-error signal. This is an open drain signal.
pci_stopz	27	I/O	PCI stop signal
pci_trdyz	24	I/O	PCI target-ready signal
phy_clk50	156	I	50-MHz system clock (from PHY chip)
phy_ctl0 –1	142,143	I/O	Phy-link bidirectional control lines
phy_data0–7	146–149,151–154	I/O	Phy-link bidirectional data lines
phy_lreq	144	O	Phy-link request signal
ram_csz	67	O	External RAM chip select
rom_csz	68	O	External ROM chip select
seeprom_clk	133	I/O	External serial EEPROM data clock
seeprom_data	134	I/O	External serial EEPROM read/write data line
test_out	140	O	Test MUX out
zv_data_valid	132	O	Zoom port data-valid signal
zv_ext_clk	129	I	Zoom port external clock input
zv_hsync	131	O	Zoom port horizontal-sync output
zv_pix_clk	126	O	Zoom port pixel clock
zv_vsync	127	O	Zoom port vertical-sync output

system block diagram



functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC(3V)}$ (V_{CC} = 3 V) . . . . . –0.5 V to 4.0 V
Supply voltage range, $V_{CC(5V)}$ (V_{CC} = 5 V) . . . . . –0.5 V to 5.5 V
Input voltage range, V_I . . . . . –0.5 V to $V_{CC(5v)}$ +0.5 V
Output voltage range at any output, V_O . . . . . –0.5 V to $V_{CC(5v)}$ + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}5) . . . . . ± 20 mA
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	V_{CC} = 3 V	3	3.3	3.6	V
	V_{CC} = 5 V	4.5	5	5.5	
Input voltage, V_I		0		$V_{CC(5v)}$	V
Output voltage, V_O		0		$V_{CC(3V)}$	V
High-level input voltage, V_{IH}	PCI terminals	0.475 × $V_{CC(3V)}$		$V_{CC(5V)}$	V
	All other terminals	2		$V_{CC(5V)}$	
Low-level input voltage, V_{IL}	PCI terminals			0.325 $V_{CC(3V)}$	V
	All other terminals			0.8	
Rise time, input, t_r	PCI terminals			6	ns
	All other terminals			6	
Fall time, input, t_f	PCI terminals			6	ns
	All other terminals			6	
Junction temperature, T_J		0		115	°C

PCI interface switching characteristics, see Figure 1

PARAMETER		MEASURED	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{su1}	Setup time, pci_xx low or high to pci_clk high†	40% to 40%		7			ns
t_{h1}	Hold time, pci_clk high to pci_xx low or high†, pci_gntz low or high	40% to 40%		0			ns
t_{d1}	Delay time, pci_clk high to pci_xx low or high†	40% to 40%		2		11	ns
t_{su2}	Setup time, pci_gntz low or high to pci_clk high	40% to 40%		10			ns
t_{d2}	Delay time, pci_clk high to pci_intaz low or high	40% to 40%		2		13	ns

† In this case, pci_xx refers to the following signals; pci_ad31–0, pci_cbez3–0, pci_par, pci_framez, pci_irdyz, pci_trdyz, pci_devselz, pci_stopz, pci_idselz, pci_perrz, pci_serrz, pci_reqz.

phy-link interface switching characteristics, see Figure 2

PARAMETER		MEASURED	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{su3}	Setup time, phy_xx low or high to phy_clk high†	1.3 V to 1.3 V		4			ns
t_{h2}	Hold time, phy_clk high to phy_xx, link_cyclein low or high	1.3 V to 1.3 V		1			ns
t_{d3}	Delay time, phy_clk high to phy_xx, phy_lreq low or high†	1.3 V to 1.3 V		3		11	ns
t_{su4}	Setup time, phy_clk high to link_cyclein low or high	1.3 V to 1.3 V		5			ns
t_{d4}	Delay time, phy_clk high to lynk_cycleout low or high	1.3 V to 1.3 V		3		13	ns

† In this case, phy_xx refers to the following bidirectional signals; phy_ctl1–0, phy_data7–0.

local bus switching characteristics, see Figure 3

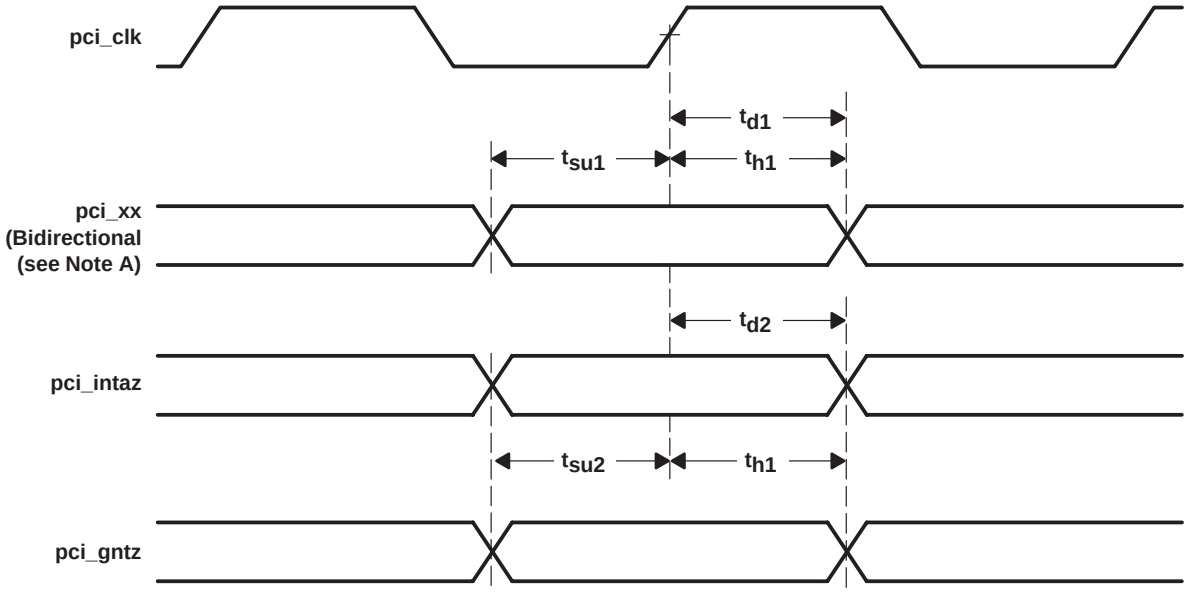
PARAMETER		MEASURED	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{d5}	Delay time, aux_clk high to aux_adr, aux_data15–0 (write), aux_oez valid†	1.3 V to 1.3 V		0		15	ns
t_{d6}	Delay time, aux_clk high to rom_csz, ram_csz, aux_csz valid	1.3 V to 1.3 V		0		20	ns
t_{d7}	Delay time, aux_wez0, aux_wez1 high (deasserted) to aux_adr, aux_data15–0 (write), aux_oez, rom_csz, ram_csz, aux_csz valid	1.3 V to 1.3 V		0.5			ns
t_{d8}	Delay time, aux_clk low to aux_wez0, aux_wez1 low (asserted)	1.3 V to 1.3 V		0		10	ns
t_{d9}	Delay time, aux_clk high to aux_wez0, aux_wez1 high (deasserted)	1.3 V to 1.3 V		0		10	ns
t_{d10}	Delay time, aux_clk high to gpio_data3–0 valid	1.3 V to 1.3 V		2		15	ns
t_{su5}	Setup time, aux_adr, adr_data15–0 (write), auxoez, rom_csz, ram_csz, aux_csz valid before aux_wez0, aux_wez1 low (asserted)	1.3 V to 1.3 V		5			ns
t_{su6}	Setup time, aux_data15–0 (read), aux_rdyz, gpio_data3–0 valid before aux_clk high	1.3 V to 1.3 V		10			ns
t_{h3}	Hold time, aux_data15–0 (read), auxrdyz, gpio_data3–1 invalid after aux_clk high	1.3 V to 1.3 V		0			ns

† These signals are asserted asynchronously when a ZOOM port transfer imediately preceeds the local bus transfer. In all cases, the setup time to aux_wez and the number of waitstates remain the same.

zoom video port switching characteristics, source clock = 30 ns with a 50% duty cycle

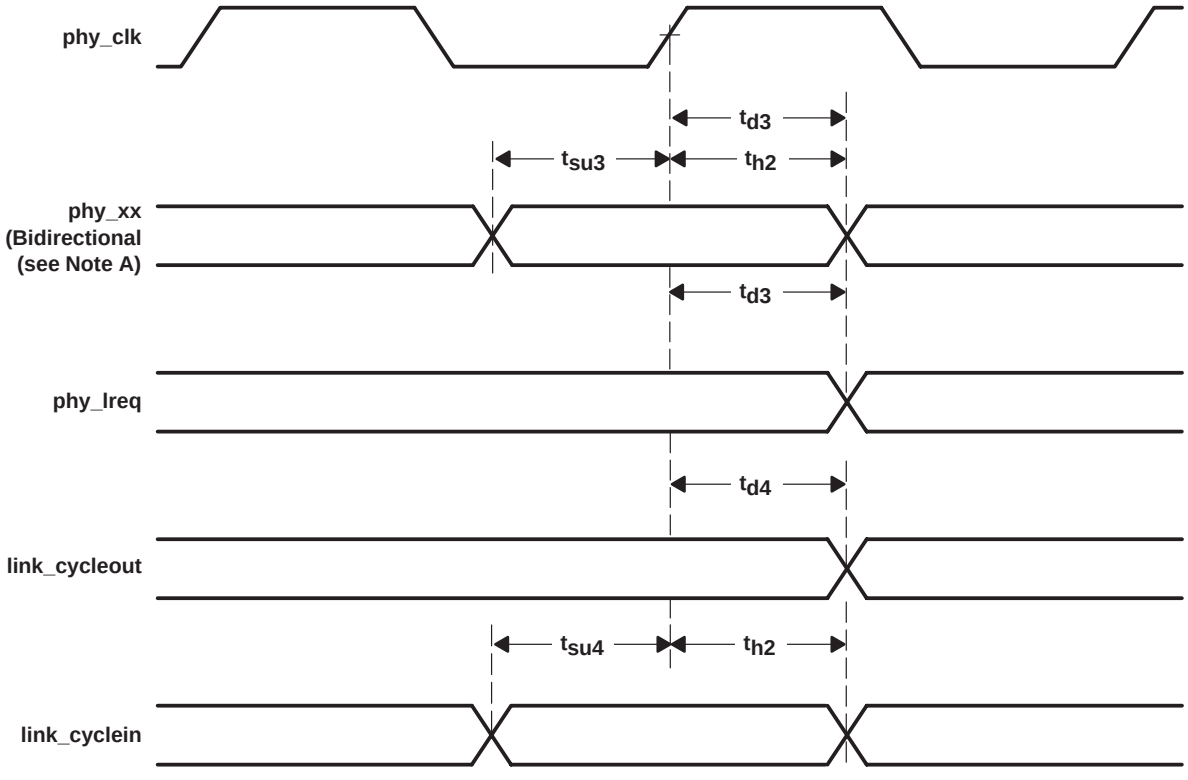
PARAMETER		MEASURED	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{su7}	Setup time, zv_hsync low, zv_vsync, zv_data_valid high before zv_pix_clk high	1.3 V to 1.3 V	See Figure 4	12			ns
t_{h4}	Hold time, zv_hsync high, zv_vsync, zv_data_valid low after zv_pix_clk low	1.3 V to 1.3 V	See Figure 4	14			ns
t_{su8}	Setup time, aux_data7–0 valid before zv_pix_clk high or low	1.3 V to 1.3 V	See Figure 4	10			ns
t_{h5}	Hold time, aux_data7–0 valid after zv_pix_clk high or low	1.3 V to 1.3 V	See Figure 4	14			ns
t_{d11}	Delay time, zv_hsync low, zv_vsync, zv_data_valid high after zv_pix_clk low	1.3 V to 1.3 V	See Figure 5	–1		3	ns
t_{d12}	Delay time, aux_data7–0 invalid after zv_pix_clk low	1.3 V to 1.3 V	See Figure 5	–1		5	ns
t_{su9}	Setup time, zv_hsync low before zv_pix_clk high	1.3 V to 1.3 V	See Figure 6	25			ns
t_{h6}	Hold time, zv_hsync high after zv_pix_clk high	1.3 V to 1.3 V	See Figure 6	14			ns
t_{su10}	Setup time, zv_vsync high before zv_pix_clk high	1.3 V to 1.3 V	See Figure 6	10			ns
t_{su11}	Setup time, aux_data7–0 valid, zv_data_valid high before zv_pix_clk high	1.3 V to 1.3 V	See Figure 6	25			ns
t_{h7}	Hold time, aux_data7–0 valid, zv_data-valid low after zv_pix_clk high	1.3 V to 1.3 V	See Figure 6	14			ns

PARAMETER MEASUREMENT INFORMATION



NOTE A: In this case, pci_xx refers to the following bidirectional signals; pci_ad31–0, pci_cbez3–0, pci_par, pci_framez, pci_irdyz, pci_trdyz, pci_devselz, pci_stopz, pci_idselz, pci_perrz, pci_serrz, pci_reqz.

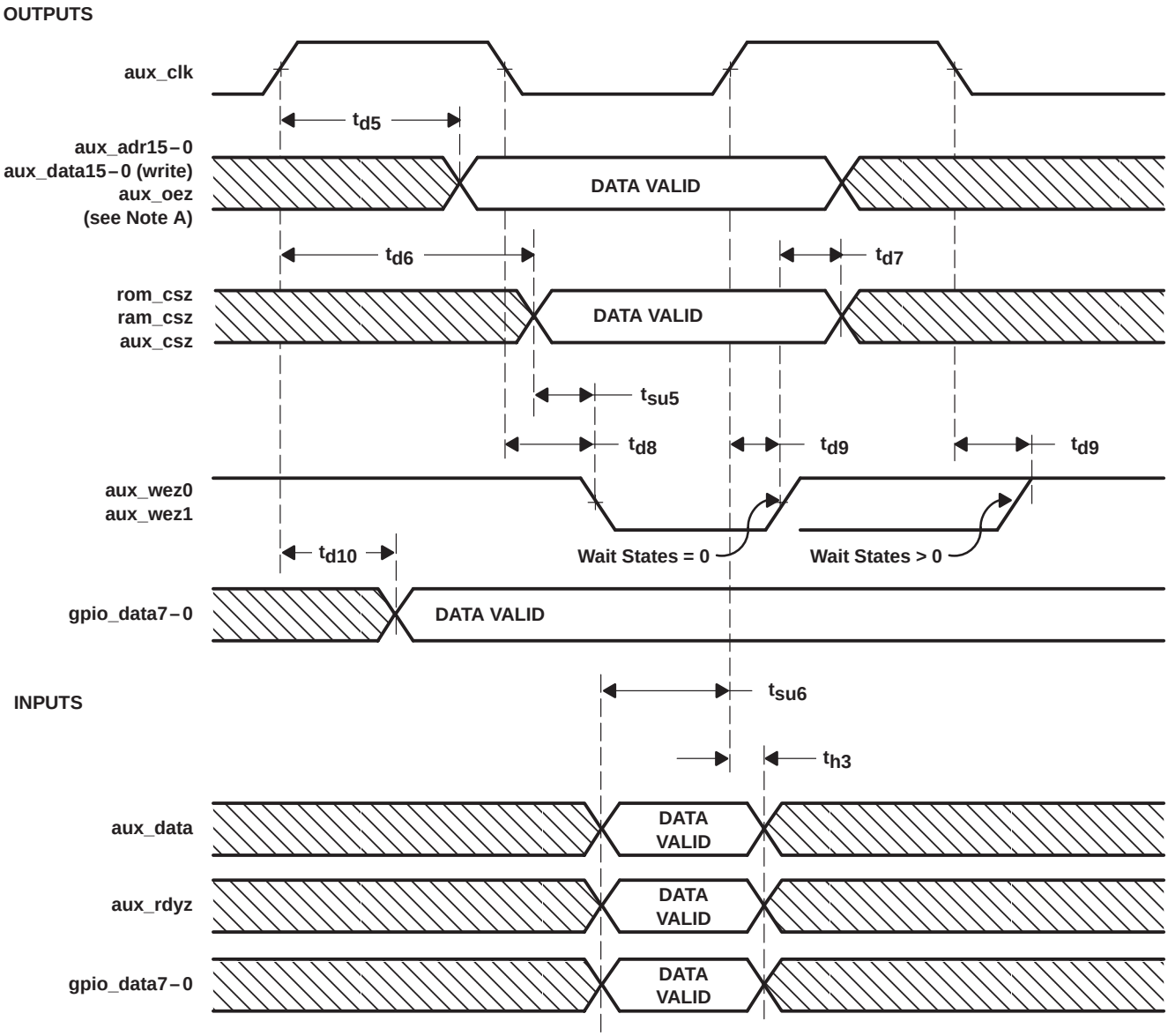
Figure 1. PCI Interface Timing Waveforms



NOTE A: In this case, phy_xx refers to the following bidirectional signals; phy_ctl1–0, phy_data7–0.

Figure 2. Phy-Link Interface Timing Waveforms

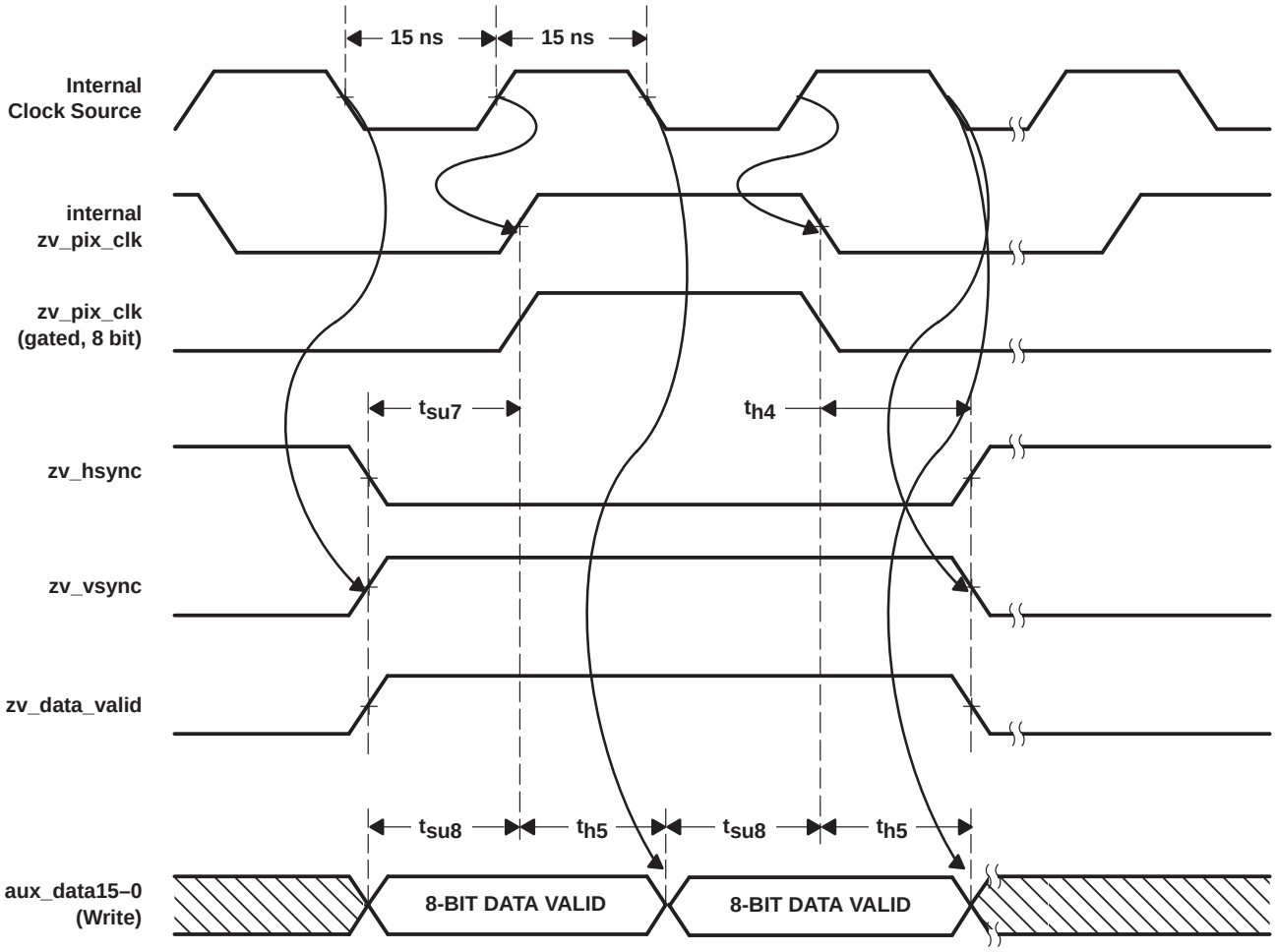
PARAMETER MEASUREMENT INFORMATION



NOTE A: These signals are asserted asynchronlusly when a ZOOM port transfer immediately preceeds the local bus transfer. In all cases, the setup time to aux_wez and the number of waitstates reamins valid.

Figure 3. Local Bus Timing Waveforms

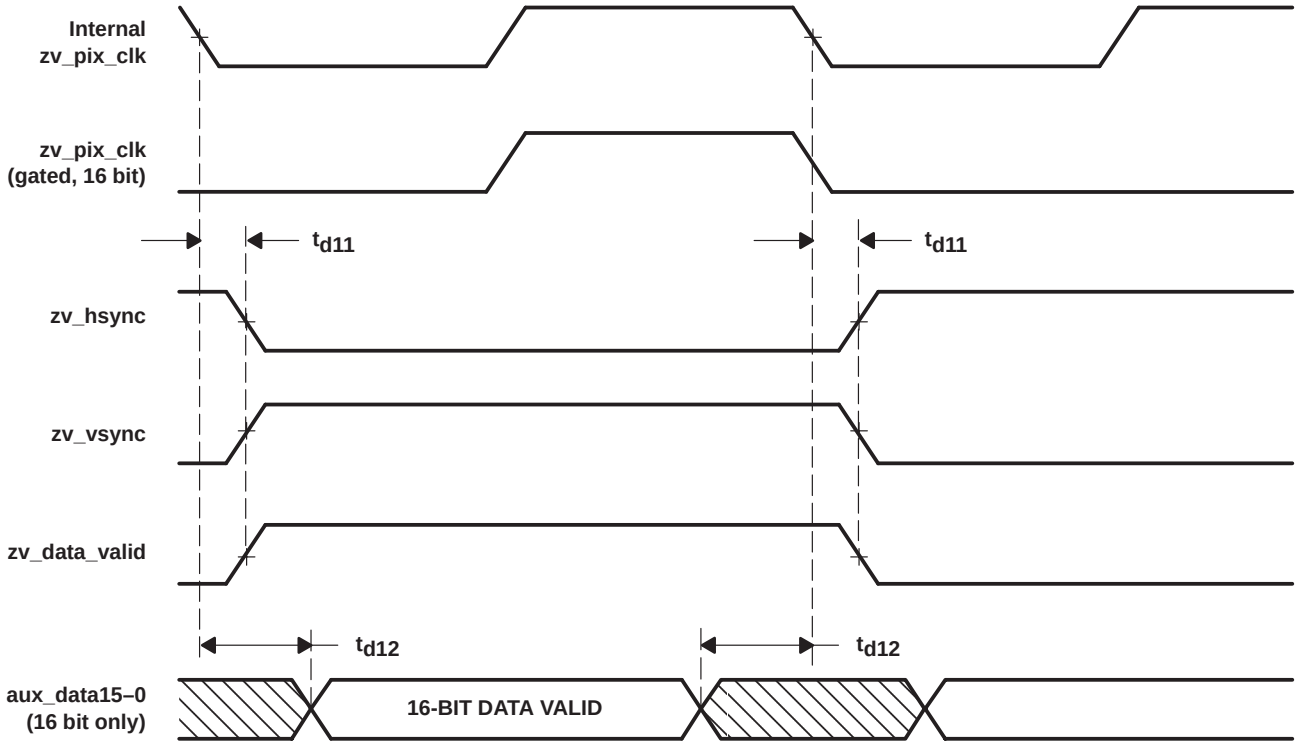
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The data is in 8-bit mode and zv_pix_clk is in divide-by-2 mode.
B. The timing for these waveforms is for write access to zoom address space.
C. The aux_datax signal meets timing while the zv_data_valid signal is asserted. The aux_datax signal can be asynchronous to zv_pix_clk at other times.
D. The polarity of zv_pix_clk depends on the setting of the invert_zv_clk register bit. The polarity shown in this figure is with invert_zv_clk = 0.
E. The timing of these waveforms is with a 30-ns source clock and a 50/50 duty cycle.

Figure 4. Zoom Video IF Timing Waveforms (8 Bit, Divide-By-2 Mode)

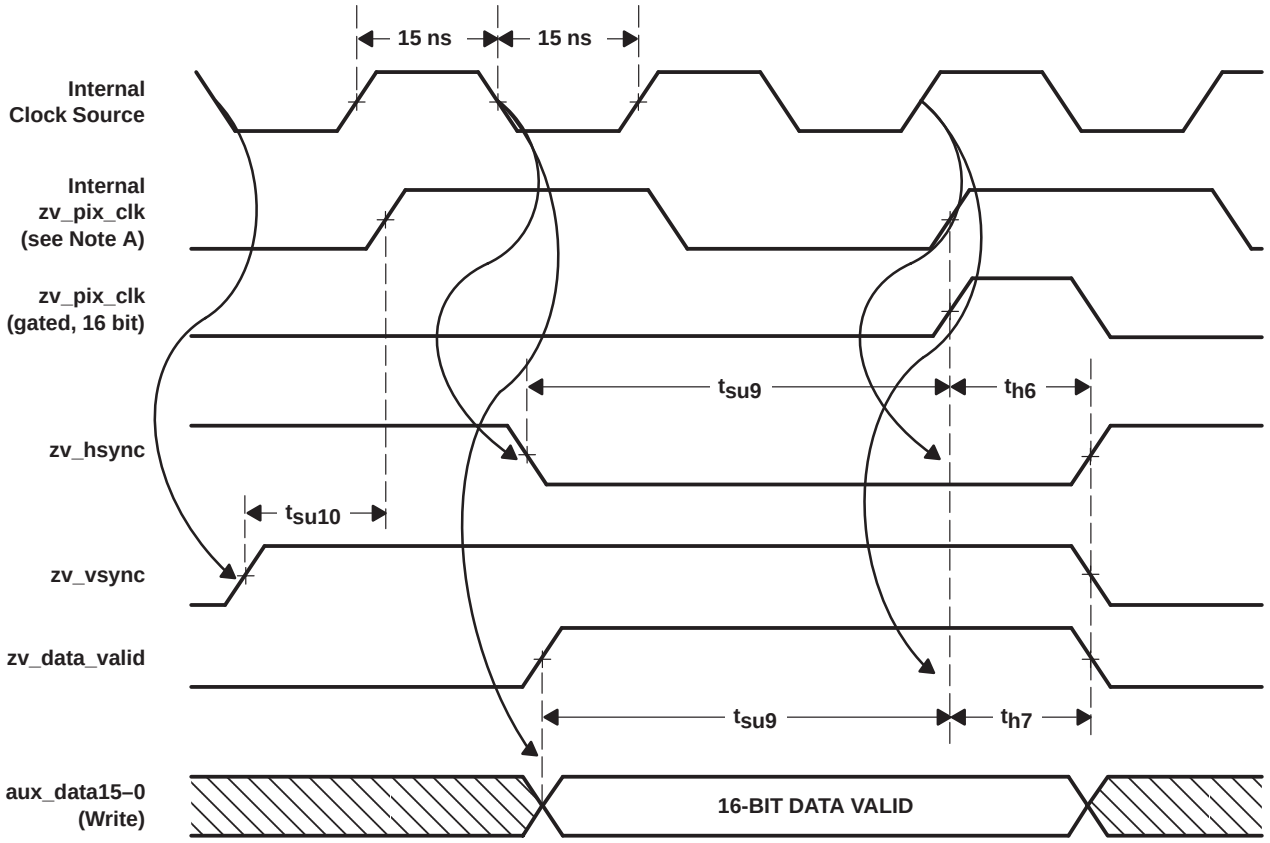
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The data is in 16-bit mode and zv_pix_clk is in divide-by-1 mode.
B. The timing for these waveforms is for write access to zoom address space.
C. The aux_datax signal meets timing while the zv_data_valid signal is asserted. The aux_datax signal can be asynchronous to zv_pix_clk at other times.
D. The polarity of zv_pix_clk depends on the setting of the invert_zv_clk register bit. The polarity shown in this figure is with invert_zv_clk = 0.

Figure 5. Zoom Video IF Timing Waveforms (16 Bit, Divide-By-1 Mode)

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The data is in 16-bit mode and zv_pix_clk is in divide-by-2 mode.
B. The timing for these waveforms is for write access to zoom address space.
C. The aux_datax signal meets timing while the zv_data_valid signal is asserted. The aux_datax signal can be asynchronous to zv_pix_clk at other times.
D. The polarity of zv_pix_clk depends on the setting of the invert_zv_clk terminal. The polarity shown in this figure is with invert_zv_clk = 0.
E. The timing of these waveforms is with a 30-ns source clock and a 50/50 duty cycle.

Figure 6. Zoom Video IF Timing Waveforms (16 Bit, Divide-By-2 Mode)

APPLICATION INFORMATION

power supply sequencing

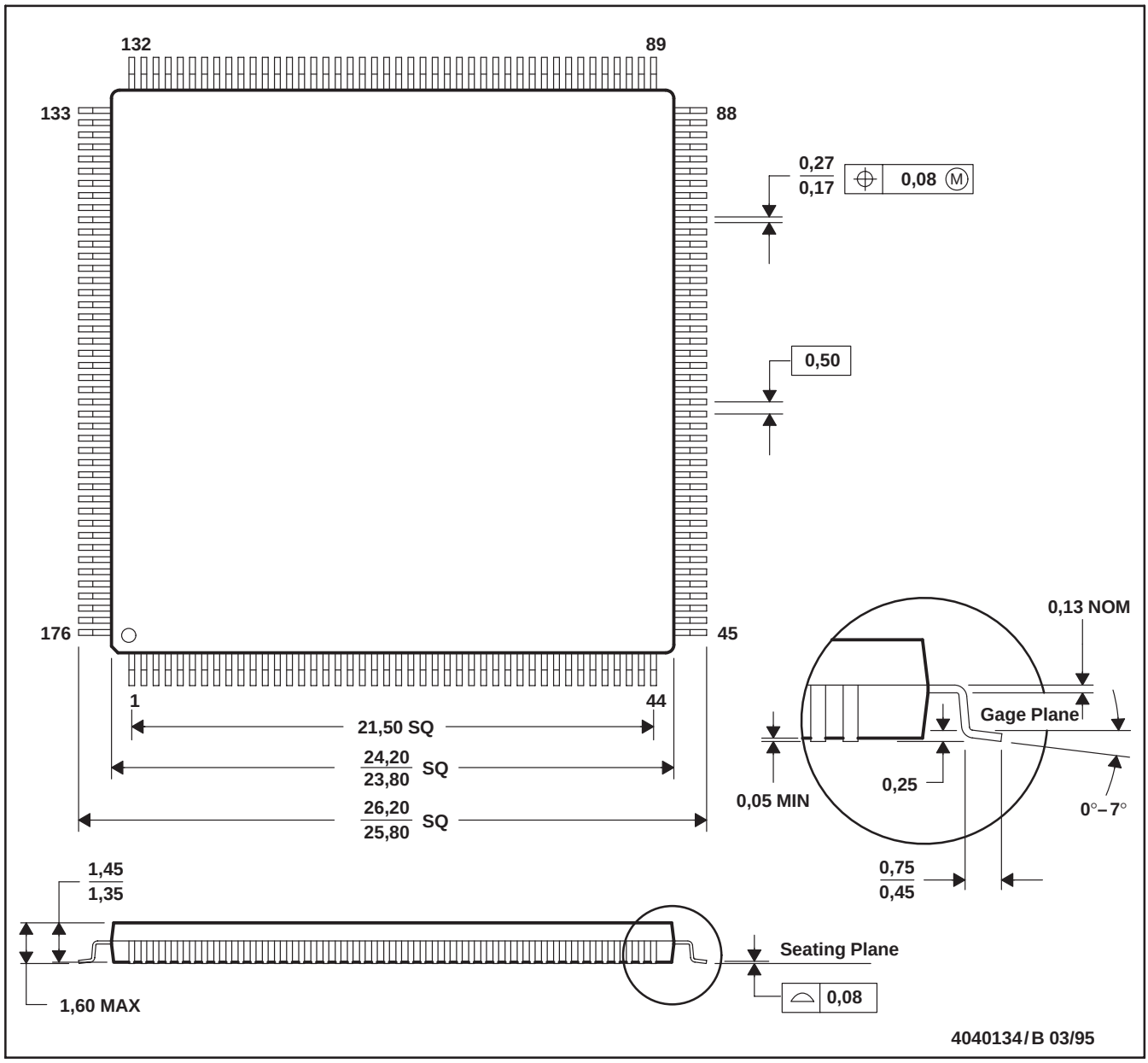
Turning power supplies on and off within a mixed 5-V/3.3-V system is an important consideration. A few basic rules need to be observed to avoid damaging PCILynx devices. Check with the manufacturers of all components used in the 3.3-V to 5-V interface to ensure that no unique device characteristics exist that would lead to more restrictive rules.

- When the 3.3-V supply is turned on before turning on the 5-V supply. PCILynx output buffers in a logic 1 state can supply large amounts of current through their clamp diodes to the 5-V supply terminals (5V V_{CC}). This can lead to excessive power dissipation and violation of current density limits. However, if the 5-V supply is turned on before the 3.3-V supply, the maximum drain-to-gate voltage of the n-channel transistors in the 5-V tolerant buffers exceeds the recommended value and the effects of channel-hot carries can be accelerated.
- When turning on the power supply, all 3.3-V and 5-V supplies should start ramping up from 0 V and reach 95% of their end-point values within a 25-ms time window. All bus contention between the PCILynx and external devices is eliminated by the end of the 25-ms time window. The preferred order of supply ramping is to ramp the 3.3-V supply followed by the 5-V supply. This order is not mandatory, but it allows a larger cumulative number of power-supply events than the reverse order.
- When turning off the power supply, all 3.3-V and 5-V supplies should start ramping down from steady state values and reach 5% of these values within a 25-ms window. All bus contention between the PCILynx and external devices is eliminated by the end of the 25-ms time window. The preferred order of supply ramping is to ramp down the 5-V supply followed by the 3.3-V supply. This order is not mandatory, but it allows a larger cumulative number of power-supply off events than the reverse order.
- A cumulative total of 250 seconds of power supply turn-on and turn-off events is allowed during the operating lifetime of the PCILynx under worst-case conditions. Worst-case conditions are where the 5-V supply is ramped up before the 3.3-V supply and the 3.3-V supply is ramped down before the 5-V supply. If the maximum time window of the 25 ms is used, a total of 10,000 power supply on or off events can occur as long as the 25-ms time window is observed.
- An additional precaution must be observed when the PCILynx is connected to a 5-V IEEE 1394 physical-layer device that is powered from the 1394 cable. In this case, it is possible for the physical-layer device to have power while the PCILynx does not. It is essential that the physical-layer device must not supply a high signal on any terminal that connects to the PCILynx while the PCILynx power is off. This is normally achieved through the use of the link-power status terminal on the physical-layer device.

If any of these precautions and guidelines are not followed, the PCILynx device can experience possible failures related to overheating, accumulation of channel-hot carriers, and/or metal migration due to excessive current density.

MECHANICAL INFORMATION

PGF (S-PQFP-G176) **PLASTIC QUAD FLATPACK**



NOTES: F. All linear dimensions are in millimeters.
G. This drawing is subject to change without notice.
H. Falls within JEDEC MO-136

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