TEXAS INSTRUMENTS

TSB43AA22

Integrated 1394a-2000 OHCI PHY/Link Layer Controller

Data Manual

2000

1394 Host Controller Solutions

SLLS358B

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1 Introduction

This chapter provides an overview of the Texas Instruments TSB43AA22 device and its features.

1.1 Description

The Texas Instruments TSB43AA22 device is an integrated 1394a-2000 OHCI PHY/link layer controller device that is fully compliant with the *PCI Local Bus Specification*, the *PCI Bus Power Management Interface Specification*, the IEEE 1394-1995 standard, the IEEE 1394a-2000 supplement, and the *1394 Open Host Controller Interface Specification*. It is capable of transferring data between the 33-MHz PCI bus and 1394 bus at 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s. The TSB43AA22 device provides two 1394 ports which have separate cable bias (TPBIAS). The TSB43AA22 device also supports IEEE 1394a-2000 power-down features for battery-operated applications and arbitration enhancements.

As required by the *1394 Open Host Controller Interface Specification* (OHCI) and the IEEE 1394a-2000 specification, internal control registers are memory-mapped and nonprefetchable. The PCI configuration header is accessed through configuration cycles specified by PCI, and provides plug-and-play (PnP) compatibility. Furthermore, the TSB43AA22 device is compliant with the *PCI Bus Power Management Interface Specification* as specified by the *PC 99 Design Guide* requirements. The TSB43AA22 device supports the D0, D2, and D3 power states.

The TSB43AA22 design provides PCI bus master bursting, and it is capable of transferring a cacheline of data at 132 Mbytes/s after connection to the memory controller. Because PCI latency can be large, deep FIFOs are provided to buffer the 1394 data.

The TSB43AA22 device provides physical write posting buffers and a highly tuned physical data path for SBP-2 performance. The TSB43AA22 device also provides multiple isochronous contexts, multiple cacheline burst transfers, advanced internal arbitration, and bus holding buffers.

An advanced CMOS process is used to achieve low power consumption that allows the TSB43AA22 device to operate at PCI clock rates up to 33 MHz.

The TSB43AA22 device provides the digital and analog transceiver functions needed to implement a two-port node in a cable-based IEEE 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission.

The TSB43AA22 device requires only an external 24.576-MHz crystal as a reference for the cable ports. An external clock may be provided instead of a crystal. An internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216-MHz reference signal. This reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded strobe and data information. A 49.152-MHz clock signal is supplied to the integrated LLC for synchronization and is used for resynchronization of the received data.

Data bits to be transmitted through the cable ports are received from the integrated LLC and are latched internally in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304, 196.608, or 393.216 Mbits/s (referred to as S100, S200, and S400 speeds, respectively) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception, the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are resynchronized to the local 49.152-MHz system clock and sent to the integrated LLC. The received data is also transmitted (repeated) on the other active (connected) cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the

arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted-pair bias voltage.

The TSB43AA22 device provides a 1.86-V nominal bias voltage at the TPBIAS terminal for port termination. The PHY device contains two independent TPBIAS circuits. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1.0 μF.

The line drivers in the TSB43AA22 device operate in a high-impedance current mode and are designed to work with external 112-Ω line-termination resistor networks in order to match the 110-Ω cable impedance. One network is provided at each end of a twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair-A terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair-B terminals is coupled to ground through a parallel R-C network with recommended values of 5 kΩ and 220 pF. The values of the external line termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits. An external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents. This current setting resistor has a value of 6.34 kΩ ±1%.

When the power supply of the TSB43AA22 device is off while the twisted-pair cables are connected, the TSB43AA22 transmitter and receiver circuitry present a high impedance to the cable and will not load the TPBIAS voltage at the other end of the cable.

When the device is in a low-power state, for example, D2 or D3, the TSB43AA22 device automatically enters a low-power mode if all ports are inactive (disconnected, disabled, or suspended). In this low-power mode, the TSB43AA22 device disables its internal clock generators and also disables various voltage and current reference circuits depending on the state of the ports (some reference circuitry must remain active in order to detect new cable connections, disconnections, or incoming TPBIAS, for example). The lowest power consumption (the *ultra low-power sleep* mode) is attained when all ports are either disconnected or disabled with the port interrupt enable bit cleared. The TSB43AA22 device exits the low-power mode when bit 19 (LPS) in the host controller control register (offset 50h/54h, see Section 4.16) is set or when a port event occurs which requires that the TSB43AA22 device to become active in order to respond to the event or to notify the LLC of the event (for example, incoming bias is detected on a suspended port, a disconnection is detected on a suspended port, a new connection is detected on a nondisabled port, etc.). The internal 49.153-MHz clock becomes active (and the integrated PHY device becomes operative) within 2 ms after bit 19 (LPS) in the host controller control register (offset 50h/54h, see Section 4.16) is set when the TSB43AA22 device is in the low-power mode.

1.2 Features

The TSB43AA22 device supports the following features:

- Fully supports provisions of IEEE 1394-1995 standard for high-performance serial bus† and the IEEE 1394a-2000 supplement
- Fully interoperable with FireWire™ and i.LINK™ implementation of IEEE Std 1394
- Meets Intel™ Mobile Power Guideline 2000
- Full IEEE 1394a-2000 support includes: connection debounce, arbitrated short reset, multispeed concatenation, arbitration acceleration, fly-by concatenation, and port disable/suspend/resume
- Power-down features to conserve energy in battery-powered applications include: automatic device power down during suspend, PCI power management for link-layer, and inactive ports powered down
- Ultra-low-power sleep mode
- Provides two IEEE 1394a-2000 fully compliant cable ports at 100/200/400 megabits per second (Mbits/s)
- Cable ports monitor line conditions for active connection to remote node
- Cable power presence monitoring
- Separate cable bias (TPBIAS) for each port
- 3.3-V core logic with universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments
- Physical write posting of up to three outstanding transactions
- Implements PCI burst transfers and deep FIFOs to tolerate large host latency
- Supports $\overline{\text{PCI-CLKRUN}}$ protocol
- External cycle timer control for customized synchronization
- Extended resume signaling for compatibility with legacy DV components
- PHY-Link logic performs system initialization and arbitration functions
- PHY-Link encode and decode functions included for data-strobe bit level encoding
- PHY-Link incoming data resynchronized to local clock
- Low-cost 24.576-MHz crystal provides transmit and receive data at 100, 200, and 400 Mbits/s
- Node power class information signaling for system power management
- Serial ROM interface supports 2-wire devices
- Provides two general-purpose I/Os
- Register bits give software control of contender bit, power class bits, link active control bit, and IEEE 1394a-2000 features
- Fabricated in advanced low-power CMOS process

† Implements technology covered by one or more patents of Apple Computer, Incorporated and SGS Thompson, Limited.

1.3 Related Documents

- *1394 Open Host Controller Interface Specification* (Revision 1.0)
- *IEEE Standard for a High-Performance Serial Bus—Amendment 1* (IEEE 1394a-2000)
- *PC 99 Design Guide*
- *PCI Bus Power Management Interface Specification* (Revision 1.1)
- *PCI Local Bus Specification* (Revision 2.2)
- *Mobile Power Guideline 2000*
- *P1394 Standard for a High-Performance Serial Bus* (IEEE 1394-1995)
- *Serial Bus Protocol 2* (SBP-2)

1.4 Trademarks

1.5 Ordering Information

ORDERING NUMBER	NAME	VOLTAGE	PACKAGE
TSB43AA22	iOHCI-Lynx	3.3 V	PDT

2 Terminal Descriptions

This section provides the terminal descriptions for the TSB43AA22 device. Figure 2–1 shows the signal assigned to each terminal in the package. Table 2–1 and Table 2–2 provide cross-reference between the number of each terminal and the name of the signal on that terminal. Table 2–1 is arranged in terminal number order, and Table 2–2 lists signals in alphabetical order.

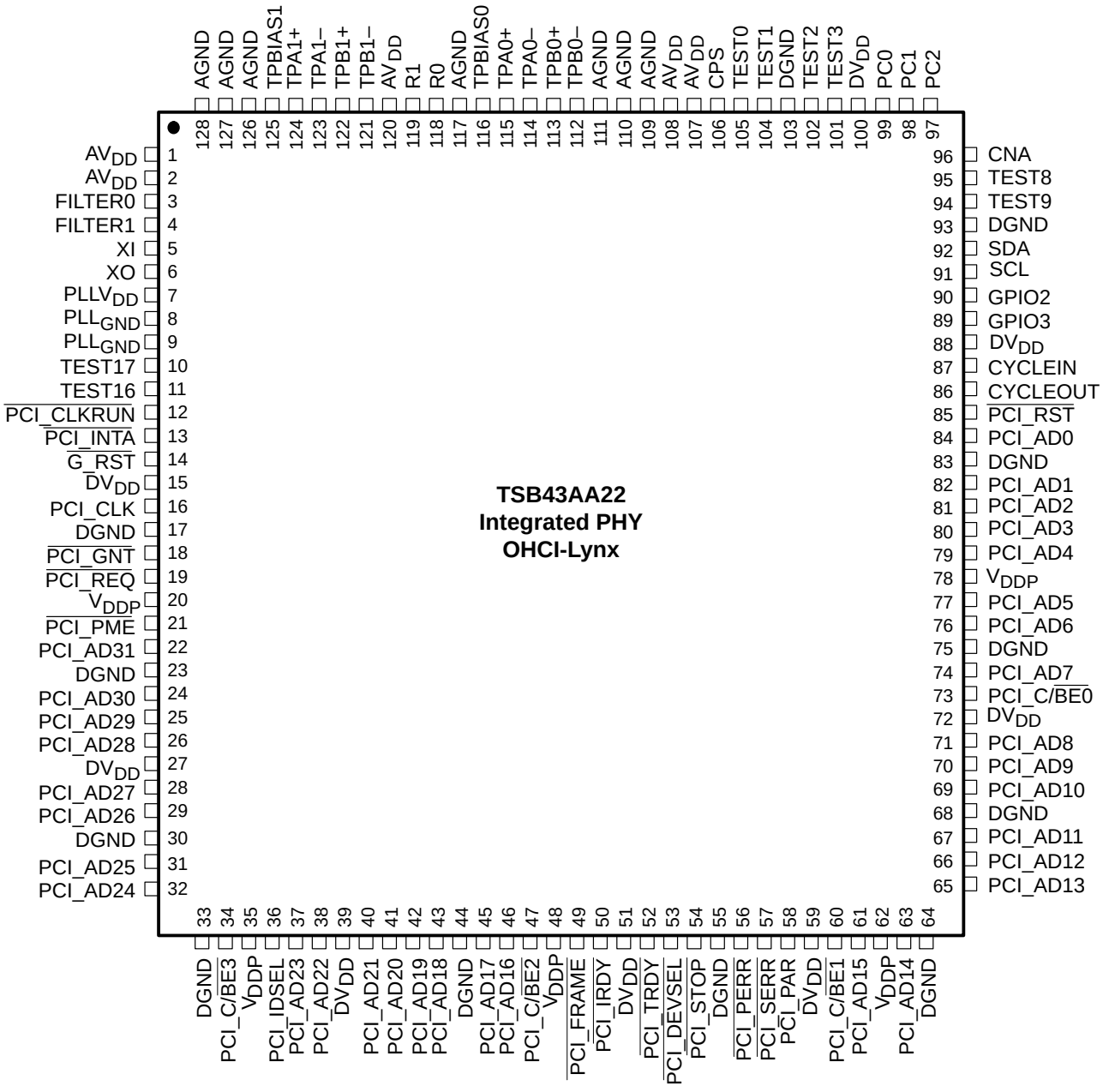


Figure 2–1. TSB43AA22 Terminal Assignments

Table 2–1. Signals Sorted by Terminal Number

NO.	TERMINAL NAME	NO.	TERMINAL NAME	NO.	TERMINAL NAME	NO.	TERMINAL NAME
1	AV_{DD}	33	DGND	65	PCI_AD13	97	PC2
2	AV_{DD}	34	PCI_C/$\overline{BE3}$	66	PCI_AD12	98	PC1
3	FILTER0	35	V_{DDP}	67	PCI_AD11	99	PC0
4	FILTER1	36	PCI_IDSEL	68	DGND	100	DV_{DD}
5	XI	37	PCI_AD23	69	PCI_AD10	101	TEST3
6	XO	38	PCI_AD22	70	PCI_AD9	102	TEST2
7	$PLLV_{DD}$	39	DV_{DD}	71	PCI_AD8	103	DGND
8	PLL_{GND}	40	PCI_AD21	72	DV_{DD}	104	TEST1
9	PLL_{GND}	41	PCI_AD20	73	PCI_C/$\overline{BE0}$	105	TEST0
10	TEST17	42	PCI_AD19	74	PCI_AD7	106	CPS
11	TEST16	43	PCI_AD18	75	DGND	107	AV_{DD}
12	$\overline{PCI\_CLKRUN}$	44	DGND	76	PCI_AD6	108	AV_{DD}
13	$\overline{PCI\_INTA}$	45	PCI_AD17	77	PCI_AD5	109	AGND
14	$\overline{G\_RST}$	46	PCI_AD16	78	V_{DDP}	110	AGND
15	DV_{DD}	47	PCI_C/$\overline{BE2}$	79	PCI_AD4	111	AGND
16	PCI_CLK	48	V_{DDP}	80	PCI_AD3	112	TPB0–
17	DGND	49	$\overline{PCI\_FRAME}$	81	PCI_AD2	113	TPB0+
18	$\overline{PCI\_GNT}$	50	$\overline{PCI\_IRDY}$	82	PCI_AD1	114	TPA0–
19	$\overline{PCI\_REQ}$	51	DV_{DD}	83	DGND	115	TPA0+
20	V_{DDP}	52	$\overline{PCI\_TRDY}$	84	PCI_AD0	116	TPBIAS0
21	$\overline{PCI\_PME}$	53	$\overline{PCI\_DEVSEL}$	85	$\overline{PCI\_RST}$	117	AGND
22	PCI_AD31	54	$\overline{PCI\_STOP}$	86	CYCLEOUT	118	R0
23	DGND	55	DGND	87	CYCLEIN	119	R1
24	PCI_AD30	56	$\overline{PCI\_PERR}$	88	DV_{DD}	120	AV_{DD}
25	PCI_AD29	57	$\overline{PCI\_SERR}$	89	GPIO3	121	TPB1–
26	PCI_AD28	58	PCI_PAR	90	GPIO2	122	TPB1+
27	DV_{DD}	59	DV_{DD}	91	SCL	123	TPA1–
28	PCI_AD27	60	PCI_C/$\overline{BE1}$	92	SDA	124	TPA1+
29	PCI_AD26	61	PCI_AD15	93	DGND	125	TPBIAS1
30	DGND	62	V_{DDP}	94	TEST9	126	AGND
31	PCI_AD25	63	PCI_AD14	95	TEST8	127	AGND
32	PCI_AD24	64	DGND	96	CNA	128	AGND

Table 2–2. Signal Names Sorted Alphanumerically to Terminal Number

TERMINAL NAME	NO.	TERMINAL NAME	NO.	TERMINAL NAME	NO.	TERMINAL NAME	NO.
AGND	109	DV_{DD}	59	PCI_AD20	41	PLL_{GND}	8
AGND	110	DV_{DD}	72	PCI_AD21	40	PLL_{GND}	9
AGND	111	DV_{DD}	88	PCI_AD22	38	$PLLV_{DD}$	7
AGND	117	DV_{DD}	100	PCI_AD23	37	R0	118
AGND	126	FILTER0	3	PCI_AD24	32	R1	119
AGND	127	FILTER1	4	PCI_AD25	31	SCL	91
AGND	128	GPIO2	90	PCI_AD26	29	SDA	92
AV_{DD}	1	GPIO3	89	PCI_AD27	28	TEST0	105
AV_{DD}	2	$\overline{G\_RST}$	14	PCI_AD28	26	TEST1	104
AV_{DD}	107	PC0	99	PCI_AD29	25	TEST2	102
AV_{DD}	108	PC1	98	PCI_AD30	24	TEST3	101
AV_{DD}	120	PC2	97	PCI_AD31	22	TEST8	95
CNA	96	PCI_AD0	84	PCI_C/$\overline{BE0}$	73	TEST9	94
CPS	106	PCI_AD1	82	PCI_C/$\overline{BE1}$	60	TEST16	11
CYCLEIN	87	PCI_AD2	81	PCI_C/$\overline{BE2}$	47	TEST17	10
CYCLEOUT	86	PCI_AD3	80	PCI_C/$\overline{BE3}$	34	TPA0–	114
DGND	17	PCI_AD4	79	PCI_CLK	16	TPA0+	115
DGND	23	PCI_AD5	77	$\overline{PCI\_CLKRUN}$	12	TPA1–	123
DGND	30	PCI_AD6	76	$\overline{PCI\_DEVSEL}$	53	TPA1+	124
DGND	33	PCI_AD7	74	$\overline{PCI\_FRAME}$	49	TPB0–	112
DGND	44	PCI_AD8	71	$\overline{PCI\_GNT}$	18	TPB0+	113
DGND	55	PCI_AD9	70	PCI_IDSEL	36	TPB1–	121
DGND	64	PCI_AD10	69	$\overline{PCI\_INTA}$	13	TPB1+	122
DGND	68	PCI_AD11	67	$\overline{PCI\_IRDY}$	50	TPBIAS0	116
DGND	75	PCI_AD12	66	PCI_PAR	58	TPBIAS1	125
DGND	83	PCI_AD13	65	$\overline{PCI\_PERR}$	56	V_{DDP}	20
DGND	93	PCI_AD14	63	$\overline{PCI\_PME}$	21	V_{DDP}	35
DGND	103	PCI_AD15	61	$\overline{PCI\_REQ}$	19	V_{DDP}	48
DV_{DD}	15	PCI_AD16	46	$\overline{PCI\_RST}$	85	V_{DDP}	62
DV_{DD}	27	PCI_AD17	45	$\overline{PCI\_SERR}$	57	V_{DDP}	78
DV_{DD}	39	PCI_AD18	43	$\overline{PCI\_STOP}$	54	XI	5
DV_{DD}	51	PCI_AD19	42	$\overline{PCI\_TRDY}$	52	XO	6

The terminals are grouped in tables by functionality, such as PCI system function and power supply function (see Table 2–3 through Table 2–8). The terminal numbers are also listed for convenient reference.

Table 2–3. PCI System

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{G\_RST}}$	14	I	Global power reset. This reset brings all of the TSB43AA22 internal registers to their default states, including those registers not reset by $\overline{\text{PCI\_RST}}$. When $\overline{\text{G\_RST}}$ is asserted, the device is completely nonfunctional. When implementing wake capabilities from the 1394 host controller, it is necessary to implement two resets to the TSB43AA22 device. $\overline{\text{G\_RST}}$ should be a one-time power-on reset.
PCI_CLK	16	I	PCI bus clock. Provides timing for all transactions on the PCI bus. All PCI signals are sampled at rising edge of PCI_CLK.
$\overline{\text{PCI\_INTA}}$	13	O	Interrupt signal. This output signals interrupts from the TSB43AA22 device to the host. This terminal is implemented as open-drain.
$\overline{\text{PCI\_RST}}$	85	I	PCI reset. When this bus reset is asserted, the TSB43AA22 device places all output buffers in a high-impedance state and resets all internal registers except device power management context- and vendor-specific bits initialized by host power-on software. When $\overline{\text{PCI\_RST}}$ is asserted, the device is completely nonfunctional. This terminal should be connected to the PCI bus $\overline{\text{RST}}$ signal.

Table 2–4. PCI Address and Data

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PCI_AD31	22	I/O	PCI address/data bus. These signals make up the multiplexed PCI address and data bus on the PCI interface. During the address phase of a PCI cycle, AD31–AD0 contain a 32-bit address or other destination information. During the data phase, AD31–AD0 contain data.
PCI_AD30	24		
PCI_AD29	25		
PCI_AD28	26		
PCI_AD27	28		
PCI_AD26	29		
PCI_AD25	31		
PCI_AD24	32		
PCI_AD23	37		
PCI_AD22	38		
PCI_AD21	40		
PCI_AD20	41		
PCI_AD19	42		
PCI_AD18	43		
PCI_AD17	45		
PCI_AD16	46		
PCI_AD15	61		
PCI_AD14	63		
PCI_AD13	65		
PCI_AD12	66		
PCI_AD11	67		
PCI_AD10	69		
PCI_AD9	70		
PCI_AD8	71		
PCI_AD7	74		
PCI_AD6	76		
PCI_AD5	77		
PCI_AD4	79		
PCI_AD3	80		
PCI_AD2	81		
PCI_AD1	82		
PCI_AD0	84		

Table 2–5. PCI Interface Control

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PCI_CLKRUN	12	I/O	Clock run. This terminal provides clock control through the CLKRUN protocol. An internal pulldown resistor is implemented on this terminal. This terminal is implemented as open-drain.
PCI_C/BE0 PCI_C/BE1 PCI_C/BE2 PCI_C/BE3	73 60 47 34	I/O	PCI bus commands and byte enables. The command and byte enable signals are multiplexed on the same PCI terminals. During the address phase of a bus cycle PCI_C/BE3–PCI_C/BE0 defines the bus command. During the data phase, this 4-bit bus is used as byte enables.
PCI_DEVSEL	53	I/O	PCI device select. The TSB43AA22 device asserts this signal to claim a PCI cycle as the target device. As a PCI initiator, the TSB43AA22 device monitors this signal until a target responds. If no target responds before time-out occurs, then the TSB43AA22 device terminates the cycle with an initiator abort.
PCI_FRAME	49	I/O	PCI cycle frame. This signal is driven by the initiator of a PCI bus cycle. PCI_FRAME is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When PCI_FRAME is deasserted, the PCI bus transaction is in the final data phase.
PCI_GNT	18	I	PCI bus grant. This signal is driven by the PCI bus arbiter to grant the TSB43AA22 device access to the PCI bus after the current data transaction has completed. This signal may or may not follow a PCI bus request, depending upon the PCI bus parking algorithm.
PCI_IDSEL	36	I	Initialization device select. PCI_IDSEL selects the TSB43AA22 device during configuration space accesses. PCI_IDSEL can be connected to 1 of the upper 24 PCI address lines on the PCI bus.
PCI_IRDY	50	I/O	PCI initiator ready. PCI_IRDY indicates the PCI bus initiator's ability to complete the current data phase of the transaction. A data phase is completed upon a rising edge of PCI_CLK where both PCI_IRDY and PCI_TRDY are asserted.
PCI_PAR	58	I/O	PCI parity. In all PCI bus read and write cycles, the TSB43AA22 device calculates even parity across the PCI_AD and PCI_C/BE buses. As an initiator during PCI cycles, the TSB43AA22 device outputs this parity indicator with a one-PCI_CLK delay. As a target during PCI cycles, the calculated parity is compared to the initiator parity indicator; a miscompare can result in a parity error assertion (PCI_PERR).
PCI_PERR	56	I/O	PCI parity error indicator. This signal is driven by a PCI device to indicate that calculated parity does not match PCI_PAR when bit 6 (PERR_ENB) is set in the command register (offset 04h, see Section 3.4).
PCI_PME	21	O	Power management event. This terminal indicates wake events to the host.
PCI_REQ	19	O	PCI bus request. Asserted by the TSB43AA22 device to request access to the bus as an initiator. The host arbiter asserts the PCI_GNT signal when the TSB43AA22 device has been granted access to the bus.
PCI_SERR	57	O	PCI system error. When bit 8 (SERR_ENB) in the command register (offset 04h, see Section 3.4) is set, the output is pulsed, indicating an address parity error has occurred. The TSB43AA22 device need not be the target of the PCI cycle to assert this signal. This terminal is implemented as open-drain.
PCI_STOP	54	I/O	PCI cycle stop signal. This signal is driven by a PCI target to request the initiator to stop the current PCI bus transaction. This signal is used for target disconnects, and is commonly asserted by target devices which do not support burst data transfers.
PCI_TRDY	52	I/O	PCI target ready. PCI_TRDY indicates the PCI bus target's ability to complete the current data phase of the transaction. A data phase is completed upon a rising edge of PCI_CLK where both PCI_IRDY and PCI_TRDY are asserted; until which wait states are inserted.

Table 2–6. Miscellaneous Terminals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CNA	96	I/O	Cable not active. This terminal is asserted high when there are no ports receiving incoming bias voltage. If not used, this terminal can be strapped either to DV_{DD} or to GND. To enable the CNA terminal, bit 3 at word offset 14h of ROM or BIOS must be set. For more information, see Section 5, *Serial ROM Interface*.
CYCLEIN	87	I/O	The CYCLEIN terminal allows an external 8-kHz clock to be used as a cycle timer for synchronization with other system devices. If this terminal is not implemented, then it should be pulled high to DV_{DD} through a 4.7 kΩ resistor.
CYCLEOUT	86	I/O	This terminal provides an 8-kHz cycle timer synchronization signal. If not implemented, this terminal should be left unconnected.
GPIO2	90	I/O	General-purpose I/O [2]. This terminal defaults as an input and if it is not implemented, then it is recommended that it be pulled low to ground with a 220-Ω resistor.
GPIO3	89	I/O	General-purpose I/O [3]. This terminal defaults as an input and if it is not implemented, then it is recommended that it be pulled low to ground with a 220-Ω resistor.
SCL	91	I/O	Serial clock. This terminal provides the serial clock signaling and is implemented as open-drain. For normal operation (a ROM is implemented in the design), this terminal should be pulled high to the ROM V_{CC} with a 2.7-kΩ resistor. Otherwise, it should be pulled low to ground with a 220-Ω resistor.
SDA	92	I/O	Serial data. At $\overline{\text{PCI\_RST}}$, the SDA signal is sampled to determine if a two-wire serial ROM is present. If the serial ROM is detected, then this terminal provides the serial data signaling. This terminal is implemented as open-drain, and for normal operation (a ROM is implemented in the design), this terminal should be pulled high to the ROM V_{CC} with a 2.7-kΩ resistor. Otherwise, it should be pulled low to ground with a 220-Ω resistor.
TEST17 TEST16 TEST9 TEST8 TEST3 TEST2 TEST1 TEST0	10 11 94 95 101 102 104 105	I/O	Terminals TEST[17, 9, 8, 3, 2, 1, 0] are used for factory test of the TSB43AA22 device and should be strapped directly to ground for normal operation. Terminal TEST16 must be strapped to DV_{DD}.

Table 2–7. Physical Layer Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	I/O	DESCRIPTION
CPS	106	CMOS	I	Cable power status input. This terminal is normally connected to cable power through a 400-kΩ resistor. This circuit drives an internal comparator that is used to detect the presence of cable power.
FILTER0 FILTER1	3 4	CMOS	I/O	PLL filter terminals. These terminals are connected to an external capacitance to form a lag-lead filter required for stable operation of the internal frequency multiplier PLL running off of the crystal oscillator. A 0.1 μF ±10% capacitor is the only external component required to complete this filter.
PC0 PC1 PC2	99 98 97	CMOS	I	Power class programming inputs. On hardware reset, these inputs set the default value of the power class indicated during self-ID. Programming is done by tying these terminals high or low.
R0 R1	118 119	Bias	–	Current-setting resistor terminals. These terminals are connected to an external resistance to set the internal operating currents and cable driver output currents. A resistance of 6.34 kΩ ±1% is required to meet the IEEE Std 1394-1995 output voltage limits.
TPA0+ TPA0–	115 114	Cable	I/O	Twisted-pair cable A differential signal terminals. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPA1+ TPA1–	124 123	Cable	I/O	
TPB0+ TPB0–	113 112	Cable	I/O	Twisted-pair cable B differential signal terminals. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPB1+ TPB1–	122 121	Cable	I/O	
TPBIAS0 TPBIAS1	116 125	Cable	I/O	Twisted-pair bias output. This provides the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers, and for signaling to the remote nodes that there is an active cable connection. Each of these pins must be decoupled with a 1.0-μF capacitor to ground.
XI XO	5 6	Crystal	–	Crystal oscillator inputs. These pins connect to a 24.576-MHz parallel resonant fundamental mode crystal. The optimum values for the external shunt capacitors are dependent on the specifications of the crystal used (see *Crystal Selection*, Section 8.2).

Table 2–8. Power Supply

TERMINAL NAME	TERMINAL NO.	TYPE	I/O	DESCRIPTION
AGND	109–111, 117, 126–128	Supply	–	Analog circuit ground terminals. These terminals should be tied together to the low-impedance circuit board ground plane.
AV_{DD}	1, 2, 107, 108, 120	Supply	–	Analog circuit power terminals. A combination of high frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10-μF filtering capacitors are also recommended. These supply terminals are separated from $PLLV_{DD}$ and DV_{DD} internal to the device to provide noise isolation. They should be tied at a low-impedance point on the circuit board.
DGND	17, 23, 30, 33, 44, 55, 64, 68, 75, 83, 93, 103	Supply	–	Digital circuit ground terminals. These terminals should be tied together to the low-impedance circuit board ground plane.
DV_{DD}	15, 27, 39, 51, 59, 72, 88, 100	Supply	–	Digital circuit power terminals. A combination of high frequency decoupling capacitors near each DV_{DD} terminal is suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10-μF filtering capacitors are also recommended. These supply terminals are separated from $PLLV_{DD}$ and AV_{DD} internal to the device to provide noise isolation. They should be tied at a low-impedance point on the circuit board.
PLL_{GND}	8, 9	Supply	–	PLL circuit ground terminals. These terminals should be tied together to the low-impedance circuit board ground plane.
$PLLV_{DD}$	7	Supply	–	PLL circuit power terminals. A combination of high frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10-μF filtering capacitors are also recommended. These supply terminals are separated from DV_{DD} and AV_{DD} internal to the device to provide noise isolation. They should be tied at a low-impedance point on the circuit board.
V_{DDP}	20, 35, 48, 62, 78	Supply	–	PCI signaling clamp voltage power input. PCI signals are clamped per the *PCI Local Bus Specification*. In addition, if a 5-V ROM is used, the V_{DDP} should be connected to 5 V.

3 TSB43AA22 1394 OHCI Controller Programming Model

This section describes the internal PCI configuration registers used to program the TSB43AA22 1394 open host controller interface. All registers are detailed in the same format: a brief description for each register is followed by the register offset and a bit table describing the reset state for each register.

A bit description table, typically included when the register contains bits of more than one type or purpose, indicates bit field names, a detailed field description, and field access tags which appear in the *type* column. Table 3–1 describes the field access tags.

Table 3–1. Bit Field Access Tag Descriptions

ACCESS TAG	NAME	MEANING
R	Read	Field may be read by software.
W	Write	Field may be written by software to any value.
S	Set	Field may be set by a write of 1. Writes of 0 have no effect.
C	Clear	Field may be cleared by a write of 1. Writes of 0 have no effect.
U	Update	Field may be autonomously updated by the TSB43AA22 device.

3.1 PCI Configuration Registers

The TSB43AA22 device is a single-function PCI device that is configured as a PCI device. The configuration header is compliant with the *PCI Local Bus Specification* as a standard header. Table 3–2 illustrates the PCI configuration header that includes both the predefined portion of the configuration space and the user-definable registers.

Table 3–2. PCI Configuration Register Map

REGISTER NAME				OFFSET
Device ID		Vendor ID		00h
Status		Command		04h
Class code			Revision ID	08h
BIST	Header type	Latency timer	Cache line size	0Ch
OHCI base address				10h
TI extension base address				14h
Reserved				18h–28h
Subsystem ID		Subsystem vendor ID		2Ch
Reserved				30h
Reserved			PCI power management capabilities pointer	34h
Reserved				38h
Maximum latency	Minimum grant	Interrupt pin	Interrupt line	3Ch
OHCI control				40h
Power management capabilities		Next item pointer	Capability ID	44h
PM data	PMCSR_BSE	Power management control and status		48h
Reserved				4Ch–ECh
Miscellaneous configuration				F0h
Link enhancement control				F4h
Subsystem device ID alias		Subsystem vendor ID alias		F8h
GPIO3	GPIO2	Reserved		FCh

3.2 Vendor ID Register

The vendor ID register contains a value allocated by the PCI SIG and identifies the manufacturer of the PCI device. The vendor ID assigned to Texas Instruments is 104Ch.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Vendor ID															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0

Register: **Vendor ID**
Offset: 00h
Type: Read-only
Default: 104Ch

3.3 Device ID Register

The device ID register contains a value assigned to the TSB43AA22 device by Texas Instruments. The device identification for the TSB43AA22 device is 8021h.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Device ID															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

Register: **Device ID**
Offset: 02h
Type: Read-only
Default: 8021h

3.4 Command Register

The command register provides control over the TSB43AA22 interface to the PCI bus. All bit functions adhere to the definitions in the *PCI Local Bus Specification*, as seen in the following bit descriptions. See Table 3–3 for a complete description of the register contents.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Command															
Type	R	R	R	R	R	R	R	R/W	R	R/W	R	R/W	R	R/W	R/W	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Command**
Offset: 04h
Type: Read/Write, Read-only
Default: 0000h

Table 3–3. Command Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–10	RSVD	R	Reserved. Bits 15–10 return 0s when read.
9	FBB_ENB	R	Fast back-to-back enable. The TSB43AA22 device does not generate fast back-to-back transactions; therefore, this bit returns 0 when read.
8	SERR_ENB	R/W	$\overline{\text{PCI\_SERR}}$ enable. When this bit is set, the TSB43AA22 $\overline{\text{PCI\_SERR}}$ driver is enabled. $\overline{\text{PCI\_SERR}}$ can be asserted after detecting an address parity error on the PCI bus.
7	STEP_ENB	R	Address/data stepping control. The TSB43AA22 device does not support address/data stepping; therefore, this bit is hardwired to 0.
6	PERR_ENB	R/W	Parity error enable. When this bit is set, the TSB43AA22 device is enabled to drive $\overline{\text{PCI\_PERR}}$ response to parity errors through the $\overline{\text{PCI\_PERR}}$ signal.
5	VGA_ENB	R	VGA palette snoop enable. The TSB43AA22 device does not feature VGA palette snooping. This bit returns 0 when read.
4	MWI_ENB	R/W	Memory write and invalidate enable. When this bit is set, the TSB43AA22 device is enabled to generate MWI PCI bus commands. If this bit is cleared, then the TSB43AA22 device generates memory write commands instead.
3	SPECIAL	R	Special cycle enable. The TSB43AA22 function does not respond to special cycle transactions. This bit returns 0 when read.
2	MASTER_ENB	R/W	Bus master enable. When this bit is set, the TSB43AA22 device is enabled to initiate cycles on the PCI bus.
1	MEMORY_ENB	R/W	Memory response enable. Setting this bit enables the TSB43AA22 device to respond to memory cycles on the PCI bus. This bit must be set to access OHCI registers.
0	IO_ENB	R	I/O space enable. The TSB43AA22 device does not implement any I/O mapped functionality; therefore, this bit returns 0 when read.

3.5 Status Register

The status register provides status over the TSB43AA22 interface to the PCI bus. All bit functions adhere to the definitions in the *PCI Local Bus Specification*, as seen in the following bit descriptions. See Table 3–4 for a complete description of the register contents.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Status															
Type	RCU	RCU	RCU	RCU	RCU	R	R	RCU	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0

Register: **Status**
Offset: 06h
Type: Read/Clear/Update, Read-only
Default: 0210h

Table 3–4. Status Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15	PAR_ERR	RCU	Detected parity error. This bit is set when either an address parity or data parity error is detected.
14	SYS_ERR	RCU	Signaled system error. This bit is set when $\overline{\text{PCI\_SERR}}$ is enabled and the TSB43AA22 device has signaled a system error to the host.
13	MABORT	RCU	Received master abort. This bit is set when a cycle initiated by the TSB43AA22 device on the PCI bus has been terminated by a master abort.
12	TABORT_REC	RCU	Received target abort. This bit is set when a cycle initiated by the TSB43AA22 device on the PCI bus was terminated by a target abort.
11	TABORT_SIG	RCU	Signaled target abort. This bit is set by the TSB43AA22 device when it terminates a transaction on the PCI bus with a target abort.
10–9	PCI_SPEED	R	DEVSEL timing. Bits 10–9 encode the timing of $\overline{\text{PCI\_DEVSEL}}$ and are hardwired to 01b indicating that the TSB43AA22 device asserts this signal at a medium speed on nonconfiguration cycle accesses.
8	DATAPAR	RCU	Data parity error detected. This bit is set when the following conditions have been met: a. $\overline{\text{PCI\_PERR}}$ was asserted by any PCI device including the TSB43AA22 device. b. The TSB43AA22 device was the bus master during the data parity error. c. Bit 6 (PERR_EN) is set in the command register (offset 04h, see Section 3.4).
7	FBB_CAP	R	Fast back-to-back capable. The TSB43AA22 device cannot accept fast back-to-back transactions; therefore, this bit is hardwired to 0.
6	UDF	R	User-definable features (UDF) supported. The TSB43AA22 device does not support the UDF; therefore, this bit is hardwired to 0.
5	66MHZ	R	66-MHz capable. The TSB43AA22 device operates at a maximum PCI_CLK frequency of 33 MHz; therefore, this bit is hardwired to 0.
4	CAPLIST	R	Capabilities list. This bit returns 1 when read, indicating that capabilities additional to standard PCI are implemented. The linked list of PCI power management capabilities is implemented in this function.
3–0	RSVD	R	Reserved. Bits 3–0 return 0s when read.

3.6 Class Code and Revision ID Register

The class code and revision ID register categorizes the TSB43AA22 device as a serial bus controller (0Ch), controlling an IEEE 1394 bus (00h), with an OHCI programming model (10h). Furthermore, the TI chip revision is indicated in the least significant byte. See Table 3–5 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Class code and revision ID															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Class code and revision ID															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1

Register: **Class code and revision ID**
Offset: 08h
Type: Read-only
Default: 0C00 1001h

Table 3–5. Class Code and Revision ID Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–24	BASECLASS	R	Base class. This field returns 0Ch when read, which broadly classifies the function as a serial bus controller.
23–16	SUBCLASS	R	Subclass. This field returns 00h when read, which specifically classifies the function as controlling an IEEE 1394 serial bus.
15–8	PGMIF	R	Programming interface. This field returns 10h when read, indicating that the programming model is compliant with the *1394 Open Host Controller Interface Specification*.
7–0	CHIPREV	R	Silicon revision. This field returns 01h when read, indicating the silicon revision of the TSB43AA22 device.

3.7 Latency Timer and Class Cache Line Size Register

The latency timer and class cache line size register is programmed by host BIOS to indicate system cache line size and the latency timer associated with the TSB43AA22 device. See Table 3–6 for a complete description of the register contents.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Latency timer and class cache line size															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Latency timer and class cache line size**
Offset: 0Ch
Type: Read/Write
Default: 0000h

Table 3–6. Latency Timer and Class Cache Line Size Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8	LATENCY_TIMER	R/W	PCI latency timer. The value in this register specifies the latency timer for the TSB43AA22 device, in units of PCI clock cycles. When the TSB43AA22 device is a PCI bus initiator and asserts $\overline{\text{PCI\_FRAME}}$, the latency timer begins counting from zero. If the latency timer expires before the TSB43AA22 transaction has terminated, then the TSB43AA22 device terminates the transaction when its $\overline{\text{PCI\_GNT}}$ is deasserted.
7–0	CACHELINE_SZ	R/W	Cache line size. This value is used by the TSB43AA22 device during memory write and invalidate, memory read line, and memory read multiple transactions.

3.8 Header Type and BIST Register

The header type and BIST register indicates the TSB43AA22 PCI header type, and indicates no built-in self-test. See Table 3–7 for a complete description of the register contents.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Header type and BIST															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Header type and BIST**
Offset: 0Eh
Type: Read-only
Default: 0000h

Table 3–7. Header Type and BIST Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8	BIST	R	Built-in self-test. The TSB43AA22 device does not include a built-in self-test; thus, this field returns 00h when read.
7–0	HEADER_TYPE	R	PCI header type. The TSB43AA22 device includes the standard PCI header, and this is communicated by returning 00h when this field is read.

3.9 OHCI Base Address Register

The OHCI base address register is programmed with a base address referencing the memory-mapped OHCI control. When BIOS writes all 1s to this register, the value read back is FFFF F800h, indicating that at least 2K bytes of memory address space are required for the OHCI registers. See Table 3–8 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OHCI base address															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OHCI base address															
Type	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **OHCI base address**
Offset: 10h
Type: Read/Write, Read-only
Default: 0000 0000h

Table 3–8. OHCI Base Address Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–11	OHCIREG_PTR	R/W	OHCI register pointer. Specifies the upper 21 bits of the 32-bit OHCI base address register.
10–4	OHCI_SZ	R	OHCI register size. This field returns 0s when read, indicating that the OHCI registers require a 2-Kbyte region of memory.
3	OHCI_PF	R	OHCI register prefetch. This bit returns 0 when read, indicating that the OHCI registers are nonprefetchable.
2–1	OHCI_MEMTYPE	R	OHCI memory type. This field returns 0s when read, indicating that the OHCI base address register is 32 bits wide and mapping can be done anywhere in the 32-bit memory space.
0	OHCI_MEM	R	OHCI memory indicator. This bit returns 0 when read, indicating that the OHCI registers are mapped into system memory space.

3.10 TI Extension Base Address Register

The TI extension base address register is programmed with a base address referencing the memory-mapped TI extension registers. See *OHCI Base Address Register*, Section 3.9, for bit field details.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TI extension base address															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TI extension base address															
Type	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **TI extension base address**
Offset: 14h
Type: Read/Write, Read-only
Default: 0000 0000h

3.11 Subsystem Identification Register

The subsystem identification register is used for system and option card identification purposes. This register can be initialized from the serial ROM or programmed via the subsystem access register (offset F8h, see Section 3.22). See Table 3–9 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Subsystem identification															
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Subsystem identification															
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Subsystem identification**
Offset: 2Ch
Type: Read/Update
Default: 0000 0000h

Table 3–9. Subsystem Identification Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	OHCI_SSID	RU	Subsystem device ID. This field indicates the subsystem device ID.
15–0	OHCI_SSVID	RU	Subsystem vendor ID. This field indicates the subsystem vendor ID.

3.12 Power Management Capabilities Pointer Register

The power management capabilities pointer register provides a pointer into the PCI configuration header where the power management register block resides. The TSB43AA22 configuration header doublewords at offsets 44h and 48h provide the power management registers. This register is read-only and returns 44h when read.

Bit	7	6	5	4	3	2	1	0
Name	Power management capabilities pointer							
Type	R	R	R	R	R	R	R	R
Default	0	1	0	0	0	1	0	0

Register: **Power management capabilities pointer**
Offset: 34h
Type: Read-only
Default: 44h

3.13 Interrupt Line and Pin Register

The interrupt line and pin register is used to communicate interrupt line routing information. See Table 3–10 for a complete description of the register contents.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Interrupt line and pin															
Type	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Register: **Interrupt line and pin**
Offset: 3Ch
Type: Read/Write
Default: 0100h

Table 3–10. Interrupt Line and Pin Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8	INTR_PIN	R	Interrupt pin. This field returns 01h when read, indicating that the TSB43AA22 PCI function signals interrupts on the PCI_INTA pin.
7–0	INTR_LINE	R/W	Interrupt line. This field is programmed by the system and indicates to software which interrupt line the TSB43AA22 PCI_INTA is connected to.

3.14 MIN_GNT and MAX_LAT Register

The MIN_GNT and MAX_LAT register is used to communicate to the system the desired setting of bits 15–8 in the latency timer and class cache line size register (offset 0Ch, see Section 3.7). If a serial ROM is detected, then the contents of this register are loaded through the serial ROM interface after a $\overline{\text{PCI\_RST}}$. If no serial ROM is detected, then this register returns a default value that corresponds to the MAX_LAT = 4, MIN_GNT = 2. See Table 3–11 for a complete description of the register contents.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_GNT and MAX_LAT															
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Default	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

Register: **MIN_GNT and MAX_LAT**
Offset: 3Eh
Type: Read/Update
Default: 0402h

Table 3–11. MIN_GNT and MAX_LAT Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8	MAX_LAT	RU	Maximum latency. The contents of this register may be used by host BIOS to assign an arbitration priority level to the TSB43AA22 device. The default for this register indicates that the TSB43AA22 device may need to access the PCI bus as often as every 0.25 μs; thus, an extremely high priority level is requested. The contents of this field may also be loaded through the serial ROM.
7–0	MIN_GNT	RU	Minimum grant. The contents of this register may be used by host BIOS to assign a latency timer register value to the TSB43AA22 device. The default for this register indicates that the TSB43AA22 device may need to sustain burst transfers for nearly 64 μs and thus request a large value be programmed in bits 15–8 of the TSB43AA22 latency timer and class cache line size register (offset 0Ch, see Section 3.7).

3.15 OHCI Control Register

The PCI OHCI control register is defined by the *1394 Open Host Controller Interface Specification* and provides a bit for big endian PCI support. See Table 3–12 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OHCI control															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OHCI control															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **OHCI control**
Offset: 40h
Type: Read/Write, Read-only
Default: 0000 0000h

Table 3–12. OHCI Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–1	RSVD	R	Reserved. Bits 31–1 return 0s when read.
0	GLOBAL_SWAP	R/W	When this bit is set, all quadlets read from and written to the PCI interface are byte swapped (big endian). This bit is loaded from ROM and should be cleared for normal operation.

3.16 Capability ID and Next Item Pointer Registers

The capability ID and next item pointer register identifies the linked list capability item and provides a pointer to the next capability item. See Table 3–13 for a complete description of the register contents.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Capability ID and next item pointer															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Register: **Capability ID and next item pointer**
Offset: 44h
Type: Read-only
Default: 0001h

Table 3–13. Capability ID and Next Item Pointer Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8	NEXT_ITEM	R	Next item pointer. The TSB43AA22 device supports only one additional capability that is communicated to the system through the extended capabilities list; thus, this field returns 00h when read.
7–0	CAPABILITY_ID	R	Capability identification. This field returns 01h when read, which is the unique ID assigned by the PCI SIG for PCI power management capability.

3.17 Power Management Capabilities Register

The power management capabilities register indicates the capabilities of the TSB43AA22 device related to PCI power management. See Table 3–14 for a complete description of the register contents.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Power management capabilities															
Type	RU	RU	RU	RU	RU	RU	R	R	R	R	R	R	R	R	R	R
Default	0	1	1	0	0	1	0	0	0	0	0	0	0	0	1	0

Register: **Power management capabilities**
Offset: 46h
Type: Read/Update, Read-only
Default: 6402h

Table 3–14. Power Management Capabilities Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15	PME_D3COLD	RU	$\overline{\text{PCI\_PME}}$ support from $D3_{cold}$. This bit can be set to 1 or cleared to 0 via bit 15 (PME_D3COLD) in the miscellaneous configuration register (offset F0h, see Section 3.20). The miscellaneous configuration register is loaded from ROM. When this bit is set to 1, it indicates that the TSB43AA22 device is capable of generating a $\overline{\text{PCI\_PME}}$ wake event from $D3_{cold}$. This bit state is dependent upon the TSB43AA22 V_{AUX} implementation and may be configured by using bit 15 (PME_D3COLD) in the miscellaneous configuration register (see Section 3.20).
14–11	PME_SUPPORT	RU	$\overline{\text{PCI\_PME}}$ support. This 4-bit field indicates the power states from which the TSB43AA22 device may assert $\overline{\text{PCI\_PME}}$. This field returns a value of 1100b by default, indicating that $\overline{\text{PCI\_PME}}$ may be asserted from the $D3_{hot}$ and D2 power states. Bit 13 may be modified by host software using bit 13 (PME_SUPPORT_D2) in the miscellaneous configuration register (offset F0h, see Section 3.20).
10	D2_SUPPORT	RU	D2 support. This bit can be set or cleared via bit 10 (D2_SUPPORT) in the miscellaneous configuration register (offset F0h, see Section 3.20). The miscellaneous configuration register is loaded from ROM. When this bit is set, it indicates that D2 support is present. When this bit is cleared, it indicates that D2 support is not present. For normal operation, this bit is set to 1.
9	D1_SUPPORT	R	D1 support. This bit returns a 0 when read, indicating that the TSB43AA22 device does not support the D1 power state.
8–6	AUX_CURRENT	R	Auxiliary current. This 3-bit field reports the 3.3-V_{AUX} auxiliary current requirements. When bit 15 (PME_D3COLD) is cleared, this field returns 000b; otherwise, it returns 001b. 000b = Self-powered 001b = 55 mA (3.3-V_{AUX} maximum current required)
5	DSI	R	Device-specific initialization. This bit returns 0 when read, indicating that the TSB43AA22 device does not require special initialization beyond the standard PCI configuration header before a generic class driver is able to use it.
4	RSVD	R	Reserved. This bit returns 0 when read.
3	PME_CLK	R	$\overline{\text{PCI\_PME}}$ clock. This bit returns 0 when read, indicating that no host bus clock is required for the TSB43AA22 device to generate $\overline{\text{PCI\_PME}}$.
2–0	PM_VERSION	R	Power management version. This field returns 010b when read, indicating that the TSB43AA22 device is compatible with the registers described in the *PCI Bus Power Management Interface Specification* (Revision 1.1).

3.18 Power Management Control and Status Register

The power management control and status register implements the control and status of the PCI power management function. This register is not affected by the internally generated reset caused by the transition from the $D3_{hot}$ to D0 state. See Table 3–15 for a complete description of the register contents.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Power management control and status															
Type	RC	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Power management control and status**
Offset: 48h
Type: Read/Clear, Read/Write, Read-only
Default: 0000h

Table 3–15. Power Management Control and Status Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15	PME_STS	RC	This bit is set when the TSB43AA22 device would normally be asserting the $\overline{\text{PCI\_PME}}$ signal, independent of the state of bit 8 (PME_ENB). This bit is cleared by a writeback of 1, and this also clears the $\overline{\text{PCI\_PME}}$ signal driven by the TSB43AA22 device. Writing a 0 to this bit has no effect.
14–13	DATA_SCALE	R	This field returns 0s because the data register is not implemented.
12–9	DATA_SELECT	R	This field returns 0s because the data register is not implemented.
8	PME_ENB	R/W	When bit 8 = 1, $\overline{\text{PME}}$ assertion is enabled. When bit 8 = 0, $\overline{\text{PME}}$ assertion is disabled. This bit defaults to 0 if the function does not support $\overline{\text{PME}}$ generation from $D3_{cold}$. If the function supports $\overline{\text{PME}}$ from $D3_{cold}$, then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded. Functions that do not support $\overline{\text{PME}}$ generation from any D-state (that is, bits 15–11 in the power management capabilities register (offset 46h, see Section 3.17) equal 00000b and may hardwire this bit to be read-only and always return a 0 when read by system software.
7–2	RSVD	R	Reserved. Bits 7–2 return 0s when read.
1–0	PWR_STATE	R/W	Power state. This 2-bit field is used to set the TSB43AA22 device power state and is encoded as follows: 00 = Current power state is D0. 01 = Current power state is D1 (not supported by this device). 10 = Current power state is D2. 11 = Current power state is D3.

3.19 Power Management Extension Registers

The power management extension register provides extended power management features not applicable to the TSB43AA22 device, thus it is read-only and returns 0 when read. See Table 3–16 for a complete description of the register contents.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Power management extension															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Power management extension**
Offset: 4Ah
Type: Read-only
Default: 0000h

Table 3–16. Power Management Extension Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–0	RSVD	R	Reserved. Bits 15–0 return 0s when read.

3.20 Miscellaneous Configuration Register

The miscellaneous configuration register provides miscellaneous PCI-related configuration. See Table 3–17 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Miscellaneous configuration															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Miscellaneous configuration															
Type	R/W	R	R/W	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Register: **Miscellaneous configuration**
Offset: F0h
Type: Read/Write, Read-only
Default: 0000 2400h

Table 3–17. Miscellaneous Configuration Register

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	RSVD	R	Reserved. Bits 31–16 return 0s when read.
15	PME_D3COLD	R/W	$\overline{\text{PCI\_PME}}$ support from $D3_{cold}$. This bit is used to program bit 15 (PME_D3COLD) in the power management capabilities register (offset 46h, see Section 3.17).
14	RSVD	R	Reserved. Bit 14 returns 0 when read.
13	PME_SUPPORT_D2	R/W	$\overline{\text{PCI\_PME}}$ support. This bit is used to program bit 13 (PME_SUPPORT_D2) in the power management capabilities register (offset 46h, see Section 3.17). If wake from the D2 power state implemented in the TSB43AA22 device is not desired, then this bit may be cleared to indicate to power management software that wake-up from D2 is not supported.
12–11	RSVD	R	Reserved. Bits 12–11 return 0s when read.
10	D2_SUPPORT	R/W	D2 support. This bit is used to program bit 10 (D2_SUPPORT) in the power management capabilities register (offset 46h, see Section 3.17). If the D2 power state in the TSB43AA22 device is not desired, then this bit may be cleared to indicate to power management software that D2 is not supported.
9–5	RSVD	R	Reserved. Bits 9–5 return 0s when read.
4	DIS_TGT_ABT	R/W	This bit defaults to 0, which provides OHCI-Lynx™ compatible target abort signaling. When this bit is set to 1, it enables the no-target-abort mode, in which the TSB43AA22 device returns indeterminate data instead of signaling target abort. The TSB43AA22 LLC is divided into the PCI_CLK and SCLK domains. If software tries to access registers in the link that are not active because the SCLK is disabled, a target abort is issued by the link. On some systems this can cause a problem resulting in a fatal system error. Enabling this bit allows the link to respond to these types of requests by returning FFh. It is recommended that this bit be set to 1.
3	GP2IIC	R/W	When this bit is set to 1, the GPIO3 and GPIO2 signals are internally routed to the SCL and SDA, respectively. The GPIO3 and GPIO2 terminals are also placed in high-impedance state.
2	DISABLE_SCLKGATE	R/W	When this bit is set, the internal SCLK runs identically with the chip input. This is a test feature only and should normally be reset to 0.
1	DISABLE_PCIGATE	R/W	When this bit is set, the internal PCI clock runs identically with the chip input. This is a test feature only and should normally be reset to 0.
0	KEEP_PCLK	R/W	When this bit is set, the PCI clock is always kept running through the $\overline{\text{PCI\_CLKRUN}}$ protocol. When this bit is cleared, the PCI clock may be stopped using $\overline{\text{PCI\_CLKRUN}}$.

3.21 Link Enhancement Control Register

The link enhancement control register implements TI-proprietary bits that are initialized by software or by a serial ROM, if present. After these bits are set, their functionality is enabled only if bit 22 (aPhyEnhanceEnable) in the host controller control register (offset 50h/54h, see Section 4.16) is set. See Table 3–18 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Link enhancement control															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Link enhancement control															
Type	R	R	R/W	R/W	R	R	R	R	R/W	R	R	R	R	R/W	R/W	R
Default	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Link enhancement control**
Offset: F4h
Type: Read/Write, Read-only
Default: 0000 1000h

Table 3–18. Link Enhancement Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–14	RSVD	R	Reserved. Bits 31–14 return 0s when read.
13–12	atx_thresh	R/W	This field sets the initial AT threshold value, which is used until the AT FIFO is underrun. When the TSB43AA22 device retries the packet, it uses a 2-Kbyte threshold resulting in a store-and-forward operation. 00 = Threshold ~ 2K bytes resulting in a store-and-forward operation 01 = Threshold ~ 1.7K bytes (default) 10 = Threshold ~ 1K bytes 11 = Threshold ~ 512 bytes These bits fine tune the asynchronous transmit threshold. For most applications the 1.7-K threshold is optimal. Changing this value may increase or decrease the 1394 latency depending on the average PCI bus latency. Setting the AT threshold to 1.7K, 1K, or 512 bytes results in data being transmitted at these thresholds, or when an entire packet has been checked into the FIFO. If the packet to be transmitted is larger than the AT threshold, then the remaining data must be received before the AT FIFO is emptied; otherwise, an underrun condition will occur, resulting in a packet error at the receiving node. As a result, the link will then commence store-and-forward operation, that is, wait until it has the complete packet in the FIFO before retransmitting it on the second attempt, to ensure delivery. An AT threshold of 2K results in store-and-forward operation, which means that asynchronous data will not be transmitted until an end-of-packet token is received. Restated, setting the AT threshold to 2K results in only complete packets being transmitted. Note that this device will always use store-and-forward when the asynchronous transmit retries register (OHCI offset 08h, see Section 4.3) is cleared.
11–8	RSVD	R	Reserved. Bits 11–8 return 0s when read.
7	enab_unfair	R/W	Enable asynchronous priority requests. OHCI-Lynx™ compatible. Setting this bit to 1 enables the link to respond to requests with priority arbitration. It is recommended that this bit be set to 1.
6	RSVD	R	This bit is not assigned in the TSB43AA22 follow-on products since this bit location loaded by the serial ROM from the enhancements field corresponds to bit 23 (programPhyEnable) in the host controller control register (OHCI offset 50h/54h, see Section 4.16).
5–3	RSVD	R	Reserved. Bits 5–3 return 0s when read.

Table 3–18. Link Enhancement Control Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
2	enab_insert_idle	R/W	Enable insert idle. OHCI-Lynx™ compatible. When the PHY device has control of the PHY_CTL0–PHY_CTL1 internal control lines and PHY_DATA0–PHY_DATA7 internal data lines and the link requests control, the PHY device drives 11b on the PHY_CTL0–PHY_CTL1 internal lines. The link can then start driving these lines immediately. Setting this bit to 1 inserts an idle state, so the link waits one clock cycle before it starts driving the lines (turnaround time). It is recommended that this bit be set to 1.
1	enab_accel	R/W	Enable acceleration enhancements. OHCI-Lynx™ compatible. When set to 1, this bit notifies the PHY device that the link supports the IEEE 1394a-2000 acceleration enhancements, that is, ack-accelerated, fly-by concatenation, etc. It is recommended that this bit be set to 1.
0	RSVD	R	Reserved. Bit 0 returns 0 when read.

3.22 Subsystem Access Register

Write access to the subsystem access register updates the subsystem identification registers identically to OHCI-Lynx™. The system ID value written to this register may also be read back from this register. See Table 3–19 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Subsystem access															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Subsystem access															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Subsystem access**
Offset: F8h
Type: Read/Write
Default: 0000 0000h

Table 3–19. Subsystem Access Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	SUBDEV_ID	R/W	Subsystem device ID alias. This field indicates the subsystem device ID.
15–0	SUBVEN_ID	R/W	Subsystem vendor ID alias. This field indicates the subsystem vendor ID.

3.23 GPIO Control Register

The GPIO control register has the control and status bits for the GPIO2 and GPIO3 ports. See Table 3–20 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO control															
Type	R/W	R	R/W	R/W	R	R	R	RWU	R/W	R	R/W	R/W	R	R	R	RWU
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO control															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **GPIO control**
Offset: FCh
Type: Read/Write/Update, Read/Write, Read-only
Default: 0000 0000h

Table 3–20. General-Purpose Input/Output Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	INT_3EN	R/W	When this bit is set, a TSB43AA22 general-purpose interrupt event occurs on a level change of the GPIO3 input. This event may generate an interrupt, with mask and event status reported through the OHCI interrupt mask (OHCI offset 88h/8Ch, see Section 4.22) and interrupt event (OHCI offset 80h/84h, see Section 4.21) registers.
30	RSVD	R	Reserved. Bit 30 returns 0 when read.
29	GPIO_INV3	R/W	GPIO3 polarity invert. When this bit is set, the polarity of GPIO3 is inverted.
28	GPIO_ENB3	R/W	GPIO3 enable control. When this bit is set, the output is enabled. Otherwise, the output is high impedance.
27–25	RSVD	R	Reserved. Bits 27–25 return 0s when read.
24	GPIO_DATA3	RWU	GPIO3 data. Reads from this bit return the logical value of the input to GPIO3. Writes to this bit update the value to drive to GPIO3 when output is enabled.
23	INT_2EN	R/W	When this bit is set, a TSB43AA22 general-purpose interrupt event occurs on a level change of the GPIO2 input. This event may generate an interrupt, with mask and event status reported through the OHCI interrupt mask (OHCI offset 88h/8Ch, see Section 4.22) and interrupt event (OHCI offset 80h/84h, see Section 4.21) registers.
22	RSVD	R	Reserved. Bit 22 returns 0 when read.
21	GPIO_INV2	R/W	GPIO2 polarity invert. When this bit is set, the polarity of GPIO2 is inverted.
20	GPIO_ENB2	R/W	GPIO2 enable control. When this bit is set, the output is enabled. Otherwise, the output is high impedance.
19–17	RSVD	R	Reserved. Bits 19–17 return 0s when read.
16	GPIO_DATA2	RWU	GPIO2 data. Reads from this bit return the logical value of the input to GPIO2. Writes to this bit update the value to drive to GPIO2 when the output is enabled.
15–0	RSVD	R	Reserved. Bits 15–0 return 0s when read.

4 OHCI Registers

The OHCI registers defined by the *1394 Open Host Controller Interface Specification* are memory-mapped into a 2-Kbyte region of memory pointed to by the OHCI base address register at offset 10h in PCI configuration space (see Section 3.9). These registers are the primary interface for controlling the TSB43AA22 IEEE 1394 link function.

This section provides the register interface and bit descriptions. Several set/clear register pairs in this programming model are implemented to solve various issues with typical read-modify-write control registers. There are two addresses for a set/clear register: RegisterSet and RegisterClear. See Table 4–1 for an illustration. A 1 bit written to RegisterSet causes the corresponding bit in the set/clear register to be set; a 0 bit leaves the corresponding bit unaffected. A 1 bit written to RegisterClear causes the corresponding bit in the set/clear register to be cleared; a 0 bit leaves the corresponding bit in the set/clear register unaffected.

Typically, a read from either RegisterSet or RegisterClear returns the contents of the set or clear register, respectively. However, sometimes reading the RegisterClear provides a masked version of the set or clear register. The interrupt event register is an example of this behavior.

Table 4–1. OHCI Register Map

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
—	OHCI version	Version	00h
	GUID ROM	GUID_ROM	04h
	Asynchronous transmit retries	ATRetries	08h
	CSR data	CSRData	0Ch
	CSR compare	CSRCompareData	10h
	CSR control	CSRControl	14h
	Configuration ROM header	ConfigROMhdr	18h
	Bus identification	BusID	1Ch
	Bus options	BusOptions	20h
	GUID high	GUIDHi	24h
	GUID low	GUIDLo	28h
	Reserved	—	2Ch–30h
	Configuration ROM mapping	ConfigROMmap	34h
	Posted write address low	PostedWriteAddressLo	38h
	Posted write address high	PostedWriteAddressHi	3Ch
	Vendor ID	VendorID	40h
	Reserved	—	44h–4Ch
	Host controller control	HCControlSet	50h
		HCControlClr	54h
	Reserved	—	58h–5Ch

Table 4–1. OHCI Register Map (Continued)

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
Self-ID	Reserved	—	60h
	Self-ID buffer pointer	SelfIDBuffer	64h
	Self-ID count	SelfIDCount	68h
	Reserved	—	6Ch
—	Isochronous receive channel mask high	IRChannelMaskHiSet	70h
		IRChannelMaskHiClear	74h
	Isochronous receive channel mask low	IRChannelMaskLoSet	78h
		IRChannelMaskLoClear	7Ch
	Interrupt event	IntEventSet	80h
		IntEventClear	84h
	Interrupt mask	IntMaskSet	88h
		IntMaskClear	8Ch
	Isochronous transmit interrupt event	IsoXmitIntEventSet	90h
		IsoXmitIntEventClear	94h
	Isochronous transmit interrupt mask	IsoXmitIntMaskSet	98h
		IsoXmitIntMaskClear	9Ch
—	Isochronous receive interrupt event	IsoRecvIntEventSet	A0h
		IsoRecvIntEventClear	A4h
	Isochronous receive interrupt mask	IsoRecvIntMaskSet	A8h
		IsoRecvIntMaskClear	ACh
	Reserved		B0–D8h
	Fairness control	FairnessControl	DCh
	Link control	LinkControlSet	E0h
		LinkControlClear	E4h
	Node identification	NodeID	E8h
	PHY layer control	PhyControl	ECh
	Isochronous cycle timer	Isocyctimer	F0h
	Reserved		F4h
	Reserved		F8h
	Reserved		FCh
	Asynchronous request filter high	AsyncRequestFilterHiSet	100h
		AsyncRequestFilterHiClear	104h
	Asynchronous request filter low	AsyncRequestFilterLoSet	108h
		AsyncRequestFilterLoClear	10Ch
	Physical request filter high	PhysicalRequestFilterHiSet	110h
		PhysicalRequestFilterHiClear	114h
	Physical request filter low	PhysicalRequestFilterLoSet	118h
		PhysicalRequestFilterLoClear	11Ch
	Physical upper bound	PhysicalUpperBound	120h
	Reserved	—	124h–17Ch

Table 4–1. OHCI Register Map (Continued)

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
Asynchronous Request Transmit [ATRQ]	Asynchronous context control	ContextControlSet	180h
		ContextControlClear	184h
	Reserved	—	188h
	Asynchronous context command pointer	CommandPtr	18Ch
	Reserved	—	190h–19Ch
Asynchronous Response Transmit [ATRS]	Asynchronous context control	ContextControlSet	1A0h
		ContextControlClear	1A4h
	Reserved	—	1A8h
	Asynchronous context command pointer	CommandPtr	1ACh
	Reserved	—	1B0h–1BCh
Asynchronous Request Receive [ARRQ]	Asynchronous context control	ContextControlSet	1C0h
		ContextControlClear	1C4h
	Reserved	—	1C8h
	Asynchronous context command pointer	CommandPtr	1CCh
	Reserved	—	1D0h–1DCh
Asynchronous Response Receive [ARRS]	Asynchronous context control	ContextControlSet	1E0h
		ContextControlClear	1E4h
	Reserved	—	1E8h
	Asynchronous context command pointer	CommandPtr	1ECh
	Reserved	—	1F0h–1FCh
Isochronous Transmit Context n n = 0, 1, 2, 3, …, 7	Isochronous transmit context control	ContextControlSet	200h + 16*n
		ContextControlClear	204h + 16*n
	Reserved	—	208h + 16*n
	Isochronous transmit context command pointer	CommandPtr	20Ch + 16*n
	Reserved	—	210h–3FCh
Isochronous Receive Context n n = 0, 1, 2, 3	Isochronous receive context control	ContextControlSet	400h + 32*n
		ContextControlClear	404h + 32*n
	Reserved	—	408h + 32*n
	Isochronous receive context command pointer	CommandPtr	40Ch + 32*n
	Isochronous receive context match	ContextMatch	410h + 32*n

4.1 OHCI Version Register

This register indicates the OHCI version support, and whether or not the serial ROM is present. See Table 4–2 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OHCI version															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	X	0	0	0	0	0	0	0	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	OHCI version															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **OHCI version**
Offset: 00h
Type: Read-only
Default: 0X01 0000h

Table 4–2. OHCI Version Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–25	RSVD	R	Reserved. Bits 31–25 return 0s when read.
24	GUID_ROM	R	The TSB43AA22 device sets this bit if the serial ROM is detected. If the serial ROM is present, then the Bus_Info_Block is automatically loaded on hardware reset.
23–16	version	R	Major version of the OHCI. The TSB43AA22 device is compliant with the *1394 Open Host Controller Interface Specification*; thus, this field reads 01h.
15–8	RSVD	R	Reserved. Bits 15–8 return 0s when read.
7–0	revision	R	Minor version of the OHCI. The TSB43AA22 device is compliant with the *1394 Open Host Controller Interface Specification*; thus, this field reads 00h.

4.2 GUID ROM Register

The GUID ROM register is used to access the serial ROM, and is only applicable if bit 24 (GUID_ROM) in the OHCI version register (OHCI offset 00h, see Section 4.1) is set. See Table 4–3 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GUID ROM															
Type	RSU	R	R	R	R	R	RSU	R	RU	RU	RU	RU	RU	RU	RU	RU
Default	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUID ROM															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **GUID ROM**
Offset: 04h
Type: Read/Set/Update, Read/Update, Read-only
Default: 00XX 0000h

Table 4–3. GUID ROM Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	addrReset	RSU	Software sets this bit to reset the GUID ROM address to 0. When the TSB43AA22 device completes the reset, it clears this bit. The TSB43AA22 device does not automatically fill bits 23–16 (rdData field) with the 0^{th} byte.
30–26	RSVD	R	Reserved. Bits 30–26 return 0s when read.
25	rdStart	RSU	A read of the currently addressed byte is started when this bit is set. This bit is automatically cleared when the TSB43AA22 device completes the read of the currently addressed GUID ROM byte.
24	RSVD	R	Reserved. Bit 24 returns 0 when read.
23–16	rdData	RU	This field contains the data read from the GUID ROM.
15–0	RSVD	R	Reserved. Bits 15–0 return 0s when read.

4.3 Asynchronous Transmit Retries Register

The asynchronous transmit retries register indicates the number of times the TSB43AA22 device attempts a retry for asynchronous DMA request transmit and for asynchronous physical and DMA response transmit. See Table 4–4 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Asynchronous transmit retries															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Asynchronous transmit retries															
Type	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Asynchronous transmit retries**
Offset: 08h
Type: Read/Write, Read-only
Default: 0000 0000h

Table 4–4. Asynchronous Transmit Retries Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–29	secondLimit	R	The second limit field returns 0s when read, because outbound dual-phase retry is not implemented.
28–16	cycleLimit	R	The cycle limit field returns 0s when read, because outbound dual-phase retry is not implemented.
15–12	RSVD	R	Reserved. Bits 15–12 return 0s when read.
11–8	maxPhysRespRetries	R/W	This field tells the physical response unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node.
7–4	maxATRespRetries	R/W	This field tells the asynchronous transmit response unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node.
3–0	maxATReqRetries	R/W	This field tells the asynchronous transmit DMA request unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node.

4.4 CSR Data Register

The CSR data register is used to access the bus management CSR registers from the host through compare-swap operations. This register contains the data to be stored in a CSR if the compare is successful.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR data															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR data															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Register: **CSR data**
Offset: 0Ch
Type: Read-only
Default: XXXX XXXXh

4.5 CSR Compare Register

The CSR compare register is used to access the bus management CSR registers from the host through compare-swap operations. This register contains the data to be compared with the existing value of the CSR resource.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR compare															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR compare															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Register: **CSR compare**
Offset: 10h
Type: Read-only
Default: XXXX XXXXh

4.6 CSR Control Register

The CSR control register is used to access the bus management CSR registers from the host through compare-swap operations. This register is used to control the compare-swap operation and to select the CSR resource. See Table 4–5 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSR control															
Type	RU	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSR control															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X

Register: **CSR control**
Offset: 14h
Type: Read/Write, Read/Update, Read-only
Default: 8000 000Xh

Table 4–5. CSR Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	csrDone	RU	This bit is set by the TSB43AA22 device when a compare-swap operation is complete. It is reset whenever this register is written.
30–2	RSVD	R	Reserved. Bits 30–2 return 0s when read.
1–0	csrSel	R/W	This field selects the CSR resource as follows: 00 = BUS_MANAGER_ID 01 = BANDWIDTH_AVAILABLE 10 = CHANNELS_AVAILABLE_HI 11 = CHANNELS_AVAILABLE_LO

4.7 Configuration ROM Header Register

The configuration ROM header register externally maps to the first quadlet of the 1394 configuration ROM, offset FFFF F000 0400h. See Table 4–6 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Configuration ROM header															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Configuration ROM header															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Register: **Configuration ROM header**
Offset: 18h
Type: Read/Write
Default: 0000 XXXXh

Table 4–6. Configuration ROM Header Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–24	info_length	R/W	IEEE 1394 bus management field. Must be valid when bit 17 (linkEnable) of the host controller control register (OHCI offset 50h/54h, see Section 4.16) is set.
23–16	crc_length	R/W	IEEE 1394 bus management field. Must be valid when bit 17 (linkEnable) of the host controller control register (OHCI offset 50h/54h, see Section 4.16) is set.
15–0	rom_crc_value	R/W	IEEE 1394 bus management field. Must be valid at any time bit 17 (linkEnable) of the host controller control register (OHCI offset 50h/54h, see Section 4.16) is set. The reset value is undefined if no serial ROM is present. If a serial ROM is present, then this field is loaded from the serial ROM.

4.8 Bus Identification Register

The bus identification register externally maps to the first quadlet in the Bus_Info_Block, and contains the constant 3133 3934h, which is the ASCII value of 1394.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Bus identification															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	1	1	0	0	0	1	0	0	1	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Bus identification															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	0

Register: **Bus identification**
Offset: 1Ch
Type: Read-only
Default: 3133 3934h

4.9 Bus Options Register

The bus options register externally maps to the second quadlet of the Bus_Info_Block. See Table 4–7 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Bus options															
Type	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	0	0	0	0	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Bus options															
Type	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R	R	R	R	R	R
Default	1	0	1	0	0	0	0	0	X	X	0	0	0	0	1	0

Register: **Bus options**
Offset: 20h
Type: Read/Write, Read-only
Default: X0XX A0X2h

Table 4–7. Bus Options Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	irmc	R/W	Isochronous resource manager capable. IEEE 1394 bus management field. Must be valid when bit 17 (linkEnable) of the host controller control register (OHCI offset 50h/54h, see Section 4.16) is set.
30	cmc	R/W	Cycle master capable. IEEE 1394 bus management field. Must be valid when bit 17 (linkEnable) of the host controller control register (OHCI offset 50h/54h, see Section 4.16) is set.
29	isc	R/W	Isochronous support capable. IEEE 1394 bus management field. Must be valid when bit 17 (linkEnable) of the host controller control register (OHCI offset 50h/54h, see Section 4.16) is set.
28	bmc	R/W	Bus manager capable. IEEE 1394 bus management field. Must be valid when bit 17 (linkEnable) of the host controller control register (OHCI offset 50h/54h, see Section 4.16) is set.
27	pmc	R/W	Power management capable. When set, this indicates that the node is power management capable. Must be valid when bit 17 (linkEnable) of the host controller control register (OHCI offset 50h/54h, see Section 4.16) is set.
26–24	RSVD	R	Reserved. Bits 26–24 return 0s when read.
23–16	cyc_clk_acc	R/W	Cycle master clock accuracy, in parts per million. IEEE 1394 bus management field. Must be valid when bit 17 (linkEnable) of the host controller control register (OHCI offset 50h/54h, see Section 4.16) is set.
15–12	max_rec	R/W	Maximum request. IEEE 1394 bus management field. Hardware initializes this field to indicate the maximum number of bytes in a block request packet that is supported by the implementation. This value, max_rec_bytes must be 512 or greater, and is calculated by 2^(max_rec + 1). Software may change this field; however, this field must be valid at any time bit 17 (linkEnable) of the host controller control register (OHCI offset 50h/54h, see Section 4.16) is set. A received block write request packet with a length greater than max_rec_bytes may generate an ack_type_error. This field is not affected by a soft reset, and defaults to value indicating 2048 bytes on a hard reset.
11–8	RSVD	R	Reserved. Bits 11–8 return 0s when read.
7–6	g	R/W	Generation counter. This field is incremented if any portion of the configuration ROM has been incremented since the prior bus reset.
5–3	RSVD	R	Reserved. Bits 5–3 return 0s when read.
2–0	Lnk_spd	R	Link speed. This field returns 010, indicating that the link speeds of 100, 200, and 400 Mbits/s are supported.

4.10 GUID High Register

The GUID high register represents the upper quadlet in a 64-bit global unique ID (GUID) which maps to the third quadlet in the Bus_Info_Block. This register contains node_vendor_ID and chip_ID_hi fields. This register initializes to 0s on a hardware reset, which is an illegal GUID value. If a serial ROM is detected, then the contents of this register are loaded through the serial ROM interface after a PCI_RST. At that point, the contents of this register cannot be changed. If no serial ROM is detected, then the contents of this register are loaded by the BIOS after a PCI_RST. At that point, the contents of this register cannot be changed.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GUID high															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GUID high															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **GUID high**
Offset: 24h
Type: Read-only
Default: 0000 0000h

4.11 GUID Low Register

The GUID low register represents the lower quadlet in a 64-bit global unique ID (GUID) which maps to chip_ID_lo in the Bus_Info_Block. This register initializes to 0s on a hardware reset and behaves identical to the GUID high register (OHCI offset 24h, see Section 4.10).

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GUID low															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	GUID low															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **GUID low**
Offset: 28h
Type: Read-only
Default: 0000 0000h

4.12 Configuration ROM Mapping Register

The configuration ROM mapping register contains the start address within system memory that maps to the start address of 1394 configuration ROM for this node. See Table 4–8 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Configuration ROM mapping															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Configuration ROM mapping															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Configuration ROM mapping**
Offset: 34h
Type: Read/Write
Default: 0000 0000h

Table 4–8. Configuration ROM Mapping Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–10	configROMaddr	R/W	If a quadlet read request to 1394 offset FFFF F000 0400h through offset FFFF F000 07FFh is received, then the low-order 10 bits of the offset are added to this register to determine the host memory address of the read request.
9–0	RSVD	R	Reserved. Bits 9–0 return 0s when read.

4.13 Posted Write Address Low Register

The posted write address low register is used to communicate error information if a write request is posted and an error occurs while the posted data packet is being written. See Table 4–9 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Posted write address low															
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Posted write address low															
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Register: **Posted write address low**
Offset: 38h
Type: Read/Update
Default: XXXX XXXXh

Table 4–9. Posted Write Address Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–0	offsetLo	RU	The lower 32 bits of the 1394 destination offset of the write request that failed.

4.14 Posted Write Address High Register

The posted write address high register is used to communicate error information if a write request is posted and an error occurs while writing the posted data packet. See Table 4–10 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Posted write address high															
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Posted write address high															
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Register: **Posted write address high**
Offset: 3Ch
Type: Read/Update
Default: XXXX XXXXh

Table 4–10. Posted Write Address High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	sourceID	RU	This field is the 10-bit bus number (bits 31–22) and 6-bit node number (bits 21–16) of the node that issued the write request that failed.
15–0	offsetHi	RU	The upper 16 bits of the 1394 destination offset of the write request that failed.

4.15 Vendor ID Register

The vendor ID register holds the company ID of an organization that specifies any vendor-unique registers. The TSB43AA22 device does not implement Texas Instruments unique behavior with regards to OHCI. Thus, this register is read-only and returns 0s when read.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Vendor ID															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Vendor ID															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Vendor ID**
Offset: 40h
Type: Read-only
Default: 0000 0000h

4.16 Host Controller Control Register

The host controller control set/clear register pair provides flags for controlling the TSB43AA22 device. See Table 4–11 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Host controller control															
Type	R	RSC	R	R	R	R	R	R	RC	RSC	R	R	RSC	RSC	RSC	RSCU
Default	0	X	0	0	0	0	0	0	0	0	0	0	0	X	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Host controller control															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Host controller control**
Offset: 50h set register
54h clear register
Type: Read/Set/Clear/Update, Read/Set/Clear, Read/Clear, Read-only
Default: X00X 0000h

Table 4–11. Host Controller Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	RSVD	R	Reserved. Bit 31 returns 0 when read.
30	noByteSwapData	RSC	This bit is used to control whether physical accesses to locations outside the TSB43AA22 device itself as well as any other DMA data accesses should be swapped.
29–24	RSVD	R	Reserved. Bits 29–24 return 0s when read.
23	programPhyEnable	RC	This bit informs upper level software that lower level software has consistently configured the IEEE 1394a-2000 enhancements in the link and PHY device. When this bit is 1, generic software such as the OHCI driver is responsible for configuring IEEE 1394a-2000 enhancements in the PHY device and bit 22 (aPhyEnhanceEnable) in the TSB43AA22 device. When this bit is 0, the generic software may not modify the IEEE 1394a-2000 enhancements in the TSB43AA22 or PHY device and cannot interpret the setting of bit 22 (aPhyEnhanceEnable). This bit is initialized from serial ROM.
22	aPhyEnhanceEnable	RSC	When bits 23 (programPhyEnable) and 17 (linkEnable) are 1, the OHCI driver can set this bit to use all IEEE 1394a-2000 enhancements. When bit 23 (programPhyEnable) is set to 0, the software does not change PHY enhancements or this bit.
21–20	RSVD	R	Reserved. Bits 21–20 return 0s when read.
19	LPS	RSC	This bit is used to control the link power status. Software must set this bit to 1 to permit the link-PHY communication. A 0 prevents link-PHY communication. The OHCI-link is divided into two clock domains (PCI_CLK and PHY_SCLK). If software tries to access any register in the PHY_SCLK domain while the PHY_SCLK is disabled, then a target abort issued by the link. This problem can be avoided by setting bit 4 (DIS_TGT_ABT) to 1 in the miscellaneous configuration register (offset F0h, see Section 3.20). This allows the link to respond to these types of request by returning all F's (hex). OHCI registers at offsets DCh–F0h and 100h–11Ch are in the SCLK domain. After setting LPS software should wait at least 10 ms before attempting to access any of the OHCI registers. This gives the PHY_SCLK time to stabilize.
18	postedWriteEnable	RSC	This bit is used to enable (1) or disable (0) posted writes. Software should change this bit only when bit 17 (linkEnable) is 0.
17	linkEnable	RSC	This bit is cleared to 0 by either a hardware or software reset. Software must set this bit to 1 when the system is ready to begin operation and then force a bus reset. This bit is necessary to keep other nodes from sending transactions before the local system is ready. When this bit is cleared, the TSB43AA22 device is logically and immediately disconnected from the 1394 bus, no packets are received or processed nor are packets transmitted.

Table 4–11. Host Controller Control Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
16	SoftReset	RSCU	When this bit is set, all TSB43AA22 states are reset, all FIFOs are flushed, and all OHCI registers are set to their hardware reset values unless otherwise specified. PCI registers are not affected by this bit. This bit remains set while the soft reset is in progress and reverts back to 0 when the reset has completed.
15–0	RSVD	R	Reserved. Bits 15–0 return 0s when read.

4.17 Self-ID Buffer Pointer Register

The self-ID buffer pointer register points to the 2-Kbyte aligned base address of the buffer in host memory where the self-ID packets are stored during bus initialization. Bits 31–11 are read/write accessible. Bits 10–0 are reserved and return 0s when read.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Self-ID buffer pointer															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Self-ID buffer pointer															
Type	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0

Register: **Self-ID buffer pointer**
Offset: 64h
Type: Read/Write, Read-only
Default: XXXX XX00h

4.18 Self-ID Count Register

The self-ID count register keeps a count of the number of times the bus self-ID process has occurred, flags self-ID packet errors, and keeps a count of the self-ID data in the self-ID buffer. See Table 4–12 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Self-ID count															
Type	RU	R	R	R	R	R	R	R	RU	RU	RU	RU	RU	RU	RU	RU
Default	X	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Self-ID count															
Type	R	R	R	R	R	RU	RU	RU	RU	RU	RU	RU	RU	RU	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Self-ID count**
Offset: 68h
Type: Read/Update, Read-only
Default: X0XX 0000h

Table 4–12. Self-ID Count Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	selfIDError	RU	When this bit is 1, an error was detected during the most recent self-ID packet reception. The contents of the self-ID buffer are undefined. This bit is cleared after a self-ID reception in which no errors are detected. Note that an error can be a hardware error or a host bus write error.
30–24	RSVD	R	Reserved. Bits 30–24 return 0s when read.
23–16	selfIDGeneration	RU	The value in this field increments each time a bus reset is detected. This field rolls over to 0 after reaching 255.
15–11	RSVD	R	Reserved. Bits 15–11 return 0s when read.
10–2	selfIDSize	RU	This field indicates the number of quadlets that have been written into the self-ID buffer for the current bits 23–16 (selfIDGeneration field). This includes the header quadlet and the self-ID data. This field is cleared to 0 when the self-ID reception begins.
1–0	RSVD	R	Reserved. Bits 1–0 return 0s when read.

4.19 Isochronous Receive Channel Mask High Register

The isochronous receive channel mask high set/clear register is used to enable packet receives from the upper 32 isochronous data channels. A read from either the set register or clear register returns the content of the isochronous receive channel mask high register. See Table 4–13 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Isochronous receive channel mask high															
Type	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Isochronous receive channel mask high															
Type	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Register: **Isochronous receive channel mask high**
Offset: 70h set register
74h clear register
Type: Read/Set/Clear
Default: XXXX XXXXh

Table 4–13. Isochronous Receive Channel Mask High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	isoChannel63	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 63.
30	isoChannel62	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 62.
29	isoChannel61	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 61.
28	isoChannel60	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 60.
27	isoChannel59	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 59.
26	isoChannel58	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 58.
25	isoChannel57	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 57.
24	isoChannel56	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 56.
23	isoChannel55	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 55.
22	isoChannel54	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 54.
21	isoChannel53	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 53.
20	isoChannel52	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 52.
19	isoChannel51	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 51.
18	isoChannel50	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 50.
17	isoChannel49	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 49.
16	isoChannel48	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 48.
15	isoChannel47	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 47.
14	isoChannel46	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 46.
13	isoChannel45	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 45.
12	isoChannel44	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 44.
11	isoChannel43	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 43.
10	isoChannel42	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 42.
9	isoChannel41	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 41.
8	isoChannel40	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 40.
7	isoChannel39	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 39.

Table 4–13. Isochronous Receive Channel Mask High Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
6	isoChannel38	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 38.
5	isoChannel37	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 37.
4	isoChannel36	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 36.
3	isoChannel35	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 35.
2	isoChannel34	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 34.
1	isoChannel33	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 33.
0	isoChannel32	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 32.

4.20 Isochronous Receive Channel Mask Low Register

The isochronous receive channel mask low set/clear register is used to enable packet receives from the lower 32 isochronous data channels. See Table 4–14 for a complete description of the register contents.

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Isochronous receive channel mask low															
Type	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Isochronous receive channel mask low															
Type	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Register: **Isochronous receive channel mask low**
Offset: 78h set register
7Ch clear register
Type: Read/Set/Clear
Default: XXXX XXXXh

Table 4–14. Isochronous Receive Channel Mask Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	isoChannel31	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 31.
30	isoChannel30	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 30.
⋮	⋮	⋮	Bits 29 through 2 follow the same pattern.
1	isoChannel1	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 1.
0	isoChannel0	RSC	When this bit is set, the TSB43AA22 device is enabled to receive from iso channel number 0.

4.21 Interrupt Event Register

The interrupt event set/clear register reflects the state of the various TSB43AA22 interrupt sources. The interrupt bits are set by an asserting edge of the corresponding interrupt signal or by writing a 1 in the corresponding bit in the set register. The only mechanism to clear the bits in this register is to write a 1 to the corresponding bit in the clear register.

This register is fully compliant with the *1394 Open Host Controller Interface Specification* and the TSB43AA22 device adds a vendor-specific interrupt function to bit 30. When the interrupt event register is read, the return value is the bitwise AND function of the interrupt event and interrupt mask registers. See Table 4–15 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Interrupt event															
Type	R	RSC	R	R	R	RSCU	RSCU	RSCU	RSCU	RSCU	RSCU	RSCU	RSCU	R	RSCU	RSCU
Default	0	X	0	0	0	X	X	X	X	X	X	X	X	0	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Interrupt event															
Type	R	R	R	R	R	R	RSCU	RSCU	RU	RU	RSCU	RSCU	RSCU	RSCU	RSCU	RSCU
Default	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X

Register: **Interrupt event**
Offset: 80h set register
84h clear register [returns the content of the interrupt event register bitwise ANDed with the interrupt mask register when read]
Type: Read/Set/Clear/Update, Read/Set/Clear, Read/Update, Read-only
Default: XXXX 0XXXh

Table 4–15. Interrupt Event Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	RSVD	R	Reserved. Bit 31 returns 0 when read.
30	vendorSpecific	RSC	This vendor-specific interrupt event is reported when either of the general-purpose interrupts which are enabled via INT_3EN and INT_2EN (bits 31 and 23, respectively) of the GPIO control register (offset FCh, see Section 3.23).
29–27	RSVD	R	Reserved. Bits 29–27 return 0s when read.
26	phyRegRcvd	RSCU	The TSB43AA22 device has received a PHY register data byte which can be read from bits 23–16 in the PHY layer control register (OHCI offset ECh, see Section 4.30).
25	cycleTooLong	RSCU	If bit 21 (cycleMaster) of the link control register (OHCI offset E0h/E4h, see Section 4.28) is set, then this indicates that over 125 µs has elapsed between the start of sending a cycle start packet and the end of a subaction gap. The link control register bit 21 (cycleMaster) is cleared by this event.
24	unrecoverableError	RSCU	This event occurs when the TSB43AA22 device encounters any error that forces it to stop operations on any or all of its subunits, for example, when a DMA context sets its dead bit. While this bit is set, all normal interrupts for the context(s) that caused this interrupt are blocked from being set.
23	cycleInconsistent	RSCU	A cycle start was received that had values for cycleSeconds and cycleCount fields that are different from the values in bits 31–25 (cycleSeconds field) and bits 24–12 (cycleCount field) of the isochronous cycle timer register (OHCI offset F0h, see Section 4.31).
22	cycleLost	RSCU	A lost cycle is indicated when no cycle_start packet is sent/received between two successive cycleSynch events. A lost cycle can be predicted when a cycle_start packet does not immediately follow the first subaction gap after the cycleSynch event or if an arbitration reset gap is detected after a cycleSynch event without an intervening cycle start. This bit may be set either when a lost cycle occurs or when logic predicts that one will occur.
21	cycle64Seconds	RSCU	Indicates that the 7^{th} bit of the cycle second counter has changed.
20	cycleSynch	RSCU	Indicates that a new isochronous cycle has started. This bit is set when the low order bit of the cycle count toggles.
19	phy	RSCU	Indicates that the PHY device requests an interrupt through a status transfer.
18	RSVD	R	Reserved. Bit 18 returns 0 when read.

Table 4–15. Interrupt Event Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
17	busReset	RSCU	Indicates that the PHY device has entered bus reset mode.
16	selfIDcomplete	RSCU	A self-ID packet stream has been received. It is generated at the end of the bus initialization process. This bit is turned off simultaneously when bit 17 (busReset) is turned on.
15–10	RSVD	R	Reserved. Bits 15–10 return 0s when read.
9	lockRespErr	RSCU	Indicates that the TSB43AA22 device sent a lock response for a lock request to a serial bus register, but did not receive an ack_complete.
8	postedWriteErr	RSCU	Indicates that a host bus error occurred while the TSB43AA22 device was trying to write a 1394 write request, which had already been given an ack_complete, into system memory.
7	isochRx	RU	Isochronous receive DMA interrupt. Indicates that one or more isochronous receive contexts have generated an interrupt. This is not a latched event, it is the logical OR of all bits in the isochronous receive interrupt event (OHCI offset A0h/A4h, see Section 4.25) and isochronous receive interrupt mask (OHCI offset A8h/ACh, see Section 4.26) registers. The isochronous receive interrupt event register indicates which contexts have interrupted.
6	isochTx	RU	Isochronous transmit DMA interrupt. Indicates that one or more isochronous transmit contexts have generated an interrupt. This is not a latched event, it is the logical OR of all bits in the isochronous transmit interrupt event (OHCI offset 90h/94h, see Section 4.23) and isochronous transmit interrupt mask (OHCI offset 98h/9Ch, see Section 4.24) registers. The isochronous transmit interrupt event register indicates which contexts have interrupted.
5	RSPkt	RSCU	Indicates that a packet was sent to an asynchronous receive response context buffer and the descriptor xferStatus and resCount fields have been updated.
4	RQPkt	RSCU	Indicates that a packet was sent to an asynchronous receive request context buffer and the descriptor xferStatus and resCount fields have been updated.
3	ARRS	RSCU	Asynchronous receive response DMA interrupt. This bit is conditionally set upon completion of an ARRS DMA context command descriptor.
2	ARRQ	RSCU	Asynchronous receive request DMA interrupt. This bit is conditionally set upon completion of an ARRQ DMA context command descriptor.
1	respTxComplete	RSCU	Asynchronous response transmit DMA interrupt. This bit is conditionally set upon completion of an ATRS DMA command.
0	reqTxComplete	RSCU	Asynchronous request transmit DMA interrupt. This bit is conditionally set upon completion of an ATRQ DMA command.

4.22 Interrupt Mask Register

The interrupt mask set/clear register is used to enable the various TSB43AA22 interrupt sources. Reads from either the set register or the clear register always return the contents of the interrupt mask register. In all cases except masterIntEnable (bit 31) and vendorSpecific (bit 30), the enables for each interrupt event align with the interrupt event register bits detailed in Table 4–15.

This register is fully compliant with the *1394 Open Host Controller Interface Specification* and the TSB43AA22 device adds an interrupt function to bit 30. See Table 4–16 for a complete description of bits 31 and 30.

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Interrupt mask															
Type	RSCU	RSC	R	R	R	RSCU	RSCU	RSCU	RSCU	RSCU	RSCU	RSCU	RSCU	R	RSCU	RSCU
Default	X	X	0	0	0	X	X	X	X	X	X	X	X	0	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Interrupt mask															
Type	R	R	R	R	R	R	RSCU	RSCU	RU	RU	RSCU	RSCU	RSCU	RSCU	RSCU	RSCU
Default	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X

Register: **Interrupt mask**
Offset: 88h set register
8Ch clear register
Type: Read/Set/Clear/Update, Read/Set/Clear, Read/Update, Read-only
Default: XXXX 0XXXh

Table 4–16. Interrupt Mask Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	masterIntEnable	RSCU	Master interrupt enable. If this bit is set, then external interrupts are generated in accordance with the interrupt mask register. If this bit is cleared, then external interrupts are not generated regardless of the interrupt mask register settings.
30	VendorSpecific	RSC	When this bit is set, this vendor-specific interrupt mask enables interrupt generation when bit 30 (vendorSpecific) of the interrupt event register (OHCI offset 80h/84h, see Section 4.21) is set.
29–0			See Table 4–15.

4.23 Isochronous Transmit Interrupt Event Register

The isochronous transmit interrupt event set/clear register reflects the interrupt state of the isochronous transmit contexts. An interrupt is generated on behalf of an isochronous transmit context if an OUTPUT_LAST* command completes and its interrupt bits are set. Upon determining that the isochTx (bit 6) interrupt has occurred in the interrupt event register (OHCI offset 80h/84h, see Section 4.21), software can check this register to determine which context(s) caused the interrupt. The interrupt bits are set by an asserting edge of the corresponding interrupt signal, or by writing a 1 in the corresponding bit in the set register. The only mechanism to clear a bit in this register is to write a 1 to the corresponding bit in the clear register. See Table 4–17 for a complete description of the register contents.

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Isochronous transmit interrupt event															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Isochronous transmit interrupt event															
Type	R	R	R	R	R	R	R	R	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

Register: **Isochronous transmit interrupt event**
Offset: 90h set register
94h clear register [returns the contents of the isochronous transmit interrupt event register bitwise ANDed with the isochronous transmit interrupt mask register when read]
Type: Read/Set/Clear, Read-only
Default: 0000 00XXh

Table 4–17. Isochronous Transmit Interrupt Event Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–8	RSVD	R	Reserved. Bits 31–8 return 0s when read.
7	isoXmit7	RSC	Isochronous transmit channel 7 caused the interrupt event register bit 6 (isochTx) interrupt.
6	isoXmit6	RSC	Isochronous transmit channel 6 caused the interrupt event register bit 6 (isochTx) interrupt.
5	isoXmit5	RSC	Isochronous transmit channel 5 caused the interrupt event register bit 6 (isochTx) interrupt.
4	isoXmit4	RSC	Isochronous transmit channel 4 caused the interrupt event register bit 6 (isochTx) interrupt.
3	isoXmit3	RSC	Isochronous transmit channel 3 caused the interrupt event register bit 6 (isochTx) interrupt.
2	isoXmit2	RSC	Isochronous transmit channel 2 caused the interrupt event register bit 6 (isochTx) interrupt.
1	isoXmit1	RSC	Isochronous transmit channel 1 caused the interrupt event register bit 6 (isochTx) interrupt.
0	isoXmit0	RSC	Isochronous transmit channel 0 caused the interrupt event register bit 6 (isochTx) interrupt.

4.24 Isochronous Transmit Interrupt Mask Register

The isochronous transmit interrupt mask set/clear register is used to enable the isochTx interrupt source on a per-channel basis. Reads from either the set register or the clear register always return the contents of the isochronous transmit interrupt mask register. In all cases the enables for each interrupt event align with the isochronous transmit interrupt event register bits detailed in Table 4–17.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Isochronous transmit interrupt mask															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Isochronous transmit interrupt mask															
Type	R	R	R	R	R	R	R	R	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

Register: **Isochronous transmit interrupt mask**
Offset: 98h set register
9Ch clear register
Type: Read/Set/Clear, Read-only
Default: 0000 00XXh

4.25 Isochronous Receive Interrupt Event Register

The isochronous receive interrupt event set/clear register reflects the interrupt state of the isochronous receive contexts. An interrupt is generated on behalf of an isochronous receive context if an INPUT_* command completes and its interrupt bits are set. Upon determining that the isochRx (bit 7) interrupt in the interrupt event register (OHCI offset 80h/84h, see Section 4.21) has occurred, software can check this register to determine which context(s) caused the interrupt. The interrupt bits are set by an asserting edge of the corresponding interrupt signal, or by writing a 1 in the corresponding bit in the set register. The only mechanism to clear a bit in this register is to write a 1 to the corresponding bit in the clear register. See Table 4–18 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Isochronous receive interrupt event															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Isochronous receive interrupt event															
Type	R	R	R	R	R	R	R	R	R	R	R	R	RSC	RSC	RSC	RSC
Default	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X

Register: **Isochronous receive interrupt event**
Offset: A0h set register
A4h clear register [returns the contents of isochronous receive interrupt event register bitwise ANDed with the isochronous receive mask register when read]
Type: Read/Set/Clear, Read-only
Default: 0000 000Xh

Table 4–18. Isochronous Receive Interrupt Event Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–4	RSVD	R	Reserved. Bits 31–4 return 0s when read.
3	isoRecv3	RSC	Isochronous receive channel 3 caused the interrupt event register bit 7 (isochRx) interrupt.
2	isoRecv2	RSC	Isochronous receive channel 2 caused the interrupt event register bit 7 (isochRx) interrupt.
1	isoRecv1	RSC	Isochronous receive channel 1 caused the interrupt event register bit 7 (isochRx) interrupt.
0	isoRecv0	RSC	Isochronous receive channel 0 caused the interrupt event register bit 7 (isochRx) interrupt.

4.26 Isochronous Receive Interrupt Mask Register

The isochronous receive interrupt mask register is used to enable the isochRx interrupt source on a per-channel basis. Reads from either the set register or the clear register always return the contents of the isochronous receive interrupt mask register. In all cases the enables for each interrupt event align with the isochronous receive interrupt event register bits detailed in Table 4–18.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Isochronous receive interrupt mask															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Isochronous receive interrupt mask															
Type	R	R	R	R	R	R	R	R	R	R	R	R	RSC	RSC	RSC	RSC
Default	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X

Register: **Isochronous receive interrupt mask**
Offset: A8h set register
ACh clear register
Type: Read/Set/Clear, Read-only
Default: 0000 000Xh

4.27 Fairness Control Register

The fairness control register provides a mechanism by which software can direct the host controller to transmit multiple asynchronous requests during a fairness interval. See Table 4–19 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Fairness control															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Fairness control															
Type	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Fairness control**
Offset: DCh
Type: Read-only
Default: 0000 0000h

Table 4–19. Fairness Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–8	RSVD	R	Reserved. Bits 31–8 return 0s when read.
7–0	pri_req	R/W	This field specifies the maximum number of priority arbitration requests for asynchronous request packets that the link is permitted to make of the PHY device during a fairness interval.

4.28 Link Control Register

The link control set/clear register provides the control flags that enable and configure the link core protocol portions of the TSB43AA22 device. It contains controls for the receiver and cycle timer. See Table 4–20 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Link control															
Type	R	R	R	R	R	R	R	R	R	RSC	RSCU	RSC	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	X	X	X	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Link control															
Type	R	R	R	R	R	RSC	RSC	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	X	X	0	0	0	0	0	0	0	0	0

Register: **Link control**
Offset: E0h set register
E4h clear register
Type: Read/Set/Clear/Update, Read/Set/Clear, Read-only
Default: 00X0 0X00h

Table 4–20. Link Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–23	RSVD	R	Reserved. Bits 31–23 return 0s when read.
22	cycleSource	RSC	When this bit is set, the cycle timer uses an external source (CYCLEIN) to determine when to roll over the cycle timer. When this bit is cleared, the cycle timer rolls over when the timer reaches 3072 cycles of the 24.576-MHz clock (125 µs).
21	cycleMaster	RSCU	When bit 21 is set, the TSB43AA22 device is root and it generates a cycle start packet every time the cycle timer rolls over, based on the setting of bit 22 (cycleSource). When bit 21 is cleared, the OHCI-Lynx™ accepts received cycle start packets to maintain synchronization with the node which is sending them. Bit 21 is automatically cleared when bit 25 (cycleTooLong) of the interrupt event register (OHCI offset 80h/84h, see Section 4.21) is set. Bit 21 cannot be set until bit 25 (cycleTooLong) is cleared.
20	CycleTimerEnable	RSC	When this bit is set, the cycle timer offset counts cycles of the 24.576-MHz clock and rolls over at the appropriate time based on the settings of the above bits. When this bit is cleared, the cycle timer offset does not count.
19–11	RSVD	R	Reserved. Bits 19–11 return 0s when read.
10	RcvPhyPkt	RSC	When this bit is set, the receiver accepts incoming PHY packets into the AR request context if the AR request context is enabled. This does not control receipt of self-identification packets.
9	RcvSelfID	RSC	When this bit is set, the receiver accepts incoming self-identification packets. Before setting this bit to 1, software must ensure that the self-ID buffer pointer register contains a valid address.
8–0	RSVD	R	Reserved. Bits 8–0 return 0s when read.

4.29 Node Identification Register

The node identification register contains the address of the node on which the OHCI-Lynx™ chip resides, and indicates the valid node number status. The 16-bit combination of the busNumber field (bits 15–6) and the NodeNumber field (bits 5–0) is referred to as the node ID. See Table 4–21 for a complete description of the register contents.

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Node identification															
Type	RU	RU	R	R	RU	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Node identification															
Type	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RU	RU	RU	RU	RU	RU
Default	1	1	1	1	1	1	1	1	1	1	X	X	X	X	X	X

Register: **Node identification**
Offset: E8h
Type: Read/Write/Update, Read/Update, Read-only
Default: 0000 FFXXh

Table 4–21. Node Identification Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	iDValid	RU	This bit indicates whether or not the TSB43AA22 device has a valid node number. It is cleared when a 1394 bus reset is detected and set when the TSB43AA22 device receives a new node number from the PHY device.
30	root	RU	This bit is set during the bus reset process if the attached PHY device is root.
29–28	RSVD	R	Reserved. Bits 29–28 return 0s when read.
27	CPS	RU	Set if the PHY device is reporting that cable power status is OK.
26–16	RSVD	R	Reserved. Bits 26–16 return 0s when read.
15–6	busNumber	RWU	This number is used to identify the specific 1394 bus the TSB43AA22 device belongs to when multiple 1394-compatible buses are connected via a bridge.
5–0	NodeNumber	RU	This number is the physical node number established by the PHY device during self-identification. It is automatically set to the value received from the PHY device after the self-identification phase. If the PHY device sets the nodeNumber to 63, then software should not set bit 15 (run) of the asynchronous context control register (see Section 4.37) for either of the AT DMA contexts.

4.30 PHY Layer Control Register

The PHY layer control register is used to read or write a PHY register. See Table 4–22 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PHY layer control															
Type	RU	R	R	R	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PHY layer control															
Type	RWU	RWU	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **PHY layer control**
Offset: ECh
Type: Read/Write/Update, Read/Write, Read/Update, Read-only
Default: 0000 0000h

Table 4–22. PHY Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	rdDone	RU	This bit is cleared to 0 by the TSB43AA22 device when either bit 15 (rdReg) or bit 14 (wrReg) is set. This bit is set when a register transfer is received from the PHY device.
30–28	RSVD	R	Reserved. Bits 30–28 return 0s when read.
27–24	rdAddr	RU	This is the address of the register most recently received from the PHY device.
23–16	rdData	RU	This field is the contents of a PHY register that has been read.
15	rdReg	RWU	This bit is set by software to initiate a read request to a PHY register and is cleared by hardware when the request has been sent. Bits 14 (wrReg) and 15 (rdReg) must not both be set simultaneously.
14	wrReg	RWU	This bit is set by software to initiate a write request to a PHY register and is cleared by hardware when the request has been sent. Bits 14 (wrReg) and 15 (rdReg) must not both be set simultaneously.
13–12	RSVD	R	Reserved. Bits 13–12 return 0s when read.
11–8	regAddr	R/W	This field is the address of the PHY register to be written or read.
7–0	wrData	R/W	This field is the data to be written to a PHY register and is ignored for reads.

4.31 Isochronous Cycle Timer Register

The isochronous cycle timer register indicates the current cycle number and offset. When the TSB43AA22 device is cycle master, this register is transmitted with the cycle start message. When the TSB43AA22 device is not cycle master, this register is loaded with the data field in an incoming cycle start. In the event that the cycle start message is not received, the fields can continue incrementing on their own (if programmed) to maintain a local time reference. See Table 4–23 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Isochronous cycle timer															
Type	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Isochronous cycle timer															
Type	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Register: **Isochronous cycle timer**
Offset: F0h
Type: Read/Write/Update
Default: XXXX XXXXh

Table 4–23. Isochronous Cycle Timer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–25	cycleSeconds	RWU	This field counts seconds [rollovers from bits 24–12 (cycleCount field)] modulo 128.
24–12	cycleCount	RWU	This field counts cycles [rollovers from bits 11–0 (cycleOffset field)] modulo 8000.
11–0	cycleOffset	RWU	This field counts 24.576-MHz clocks modulo 3072, that is, 125 µs. If an external 8-kHz clock configuration is being used, then this bit must be set to 0 at each tick of the external clock.

4.32 Asynchronous Request Filter High Register

The asynchronous request filter high set/clear register is used to enable asynchronous receive requests on a per-node basis, and handles the upper node IDs. When a packet is destined for either the physical request context or the ARRQ context, the source node ID is examined. If the bit corresponding to the node ID is not set in this register, then the packet is not acknowledged and the request is not queued. The node ID comparison is done if the source node is on the same bus as the TSB43AA22 device. Nonlocal bus-sourced packets are not acknowledged unless bit 31 in this register is set. See Table 4–24 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Asynchronous request filter high															
Type	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Asynchronous request filter high															
Type	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Asynchronous request filter high**
Offset: 100h set register
104h clear register
Type: Read/Set/Clear
Default: 0000 0000h

Table 4–24. Asynchronous Request Filter High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	asynReqAllBuses	RSC	If this bit is set, then all asynchronous requests received by the TSB43AA22 device from nonlocal bus nodes are accepted.
30	asynReqResource62	RSC	If this bit is set for local bus node number 62, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
29	asynReqResource61	RSC	If this bit is set for local bus node number 61, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
28	asynReqResource60	RSC	If this bit is set for local bus node number 60, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
27	asynReqResource59	RSC	If this bit is set for local bus node number 59, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
26	asynReqResource58	RSC	If this bit is set for local bus node number 58, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
25	asynReqResource57	RSC	If this bit is set for local bus node number 57, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
24	asynReqResource56	RSC	If this bit is set for local bus node number 56, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
23	asynReqResource55	RSC	If this bit is set for local bus node number 55, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
22	asynReqResource54	RSC	If this bit is set for local bus node number 54, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
21	asynReqResource53	RSC	If this bit is set for local bus node number 53, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
20	asynReqResource52	RSC	If this bit is set for local bus node number 52, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
19	asynReqResource51	RSC	If this bit is set for local bus node number 51, then asynchronous requests received by the TSB43AA22 device from that node are accepted.

Table 4–24. Asynchronous Request Filter High Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
18	asynReqResource50	RSC	If this bit is set for local bus node number 50, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
17	asynReqResource49	RSC	If this bit is set for local bus node number 49, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
16	asynReqResource48	RSC	If this bit is set for local bus node number 48, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
15	asynReqResource47	RSC	If this bit is set for local bus node number 47, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
14	asynReqResource46	RSC	If this bit is set for local bus node number 46, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
13	asynReqResource45	RSC	If this bit is set for local bus node number 45, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
12	asynReqResource44	RSC	If this bit is set for local bus node number 44, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
11	asynReqResource43	RSC	If this bit is set for local bus node number 43, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
10	asynReqResource42	RSC	If this bit is set for local bus node number 42, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
9	asynReqResource41	RSC	If this bit is set for local bus node number 41, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
8	asynReqResource40	RSC	If this bit is set for local bus node number 40, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
7	asynReqResource39	RSC	If this bit is set for local bus node number 39, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
6	asynReqResource38	RSC	If this bit is set for local bus node number 38, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
5	asynReqResource37	RSC	If this bit is set for local bus node number 37, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
4	asynReqResource36	RSC	If this bit is set for local bus node number 36, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
3	asynReqResource35	RSC	If this bit is set for local bus node number 35, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
2	asynReqResource34	RSC	If this bit is set for local bus node number 34, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
1	asynReqResource33	RSC	If this bit is set for local bus node number 33, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
0	asynReqResource32	RSC	If this bit is set for local bus node number 32, then asynchronous requests received by the TSB43AA22 device from that node are accepted.

4.33 Asynchronous Request Filter Low Register

The asynchronous request filter low set/clear register is used to enable asynchronous receive requests on a per-node basis, and handles the lower node IDs. Other than filtering different node IDs, this register behaves identically to the asynchronous request filter high register. See Table 4–25 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Asynchronous request filter low															
Type	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Asynchronous request filter low															
Type	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Asynchronous request filter low**
Offset: 108h set register
10Ch clear register
Type: Read/Set/Clear
Default: 0000 0000h

Table 4–25. Asynchronous Request Filter Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	asynReqResource31	RSC	If this bit is set for local bus node number 31, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
30	asynReqResource30	RSC	If this bit is set for local bus node number 30, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
⋮	⋮	⋮	Bits 29 through 2 follow the same pattern.
1	asynReqResource1	RSC	If this bit is set for local bus node number 1, then asynchronous requests received by the TSB43AA22 device from that node are accepted.
0	asynReqResource0	RSC	If this bit is set for local bus node number 0, then asynchronous requests received by the TSB43AA22 device from that node are accepted.

4.34 Physical Request Filter High Register

The physical request filter high set/clear register is used to enable physical receive requests on a per-node basis and handles the upper node IDs. When a packet is destined for the physical request context and the node ID has been compared against the ARRQ registers, then the comparison is done again with this register. If the bit corresponding to the node ID is not set in this register, then the request is handled by the ARRQ context instead of the physical request context. The node ID comparison is done if the source node is on the same bus as the TSB43AA22 device. Nonlocal bus-sourced packets are not acknowledged unless bit 31 in this register is set. See Table 4–26 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Physical request filter high															
Type	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Physical request filter high															
Type	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Physical request filter high**
Offset: 110h set register
114h clear register
Type: Read/Set/Clear
Default: 0000 0000h

Table 4–26. Physical Request Filter High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	physReqAllBusses	RSC	If this bit is set, then all asynchronous requests received by the TSB43AA22 device from nonlocal bus nodes are accepted.
30	physReqResource62	RSC	If this bit is set for local bus node number 62, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
29	physReqResource61	RSC	If this bit is set for local bus node number 61, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
28	physReqResource60	RSC	If this bit is set for local bus node number 60, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
27	physReqResource59	RSC	If this bit is set for local bus node number 59, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
26	physReqResource58	RSC	If this bit is set for local bus node number 58, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
25	physReqResource57	RSC	If this bit is set for local bus node number 57, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
24	physReqResource56	RSC	If this bit is set for local bus node number 56, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
23	physReqResource55	RSC	If this bit is set for local bus node number 55, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
22	physReqResource54	RSC	If this bit is set for local bus node number 54, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
21	physReqResource53	RSC	If this bit is set for local bus node number 53, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
20	physReqResource52	RSC	If this bit is set for local bus node number 52, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
19	physReqResource51	RSC	If this bit is set for local bus node number 51, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.

Table 4–26. Physical Request Filter High Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
18	physReqResource50	RSC	If this bit is set for local bus node number 50, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
17	physReqResource49	RSC	If this bit is set for local bus node number 49, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
16	physReqResource48	RSC	If this bit is set for local bus node number 48, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
15	physReqResource47	RSC	If this bit is set for local bus node number 47, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
14	physReqResource46	RSC	If this bit is set for local bus node number 46, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
13	physReqResource45	RSC	If this bit is set for local bus node number 45, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
12	physReqResource44	RSC	If this bit is set for local bus node number 44, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
11	physReqResource43	RSC	If this bit is set for local bus node number 43, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
10	physReqResource42	RSC	If this bit is set for local bus node number 42, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
9	physReqResource41	RSC	If this bit is set for local bus node number 41, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
8	physReqResource40	RSC	If this bit is set for local bus node number 40, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
7	physReqResource39	RSC	If this bit is set for local bus node number 39, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
6	physReqResource38	RSC	If this bit is set for local bus node number 38, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
5	physReqResource37	RSC	If this bit is set for local bus node number 37, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
4	physReqResource36	RSC	If this bit is set for local bus node number 36, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
3	physReqResource35	RSC	If this bit is set for local bus node number 35, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
2	physReqResource34	RSC	If this bit is set for local bus node number 34, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
1	physReqResource33	RSC	If this bit is set for local bus node number 33, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
0	physReqResource32	RSC	If this bit is set for local bus node number 32, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.

4.35 Physical Request Filter Low Register

The physical request filter low set/clear register is used to enable physical receive requests on a per-node basis and handles the lower node IDs. When a packet is destined for the physical request context and the node ID has been compared against the asynchronous request filter registers, then the node ID comparison is done again with this register. If the bit corresponding to the node ID is not set in this register, then the request is handled by the asynchronous request context instead of the physical request context. See Table 4–27 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Physical request filter low															
Type	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Physical request filter low															
Type	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Physical request filter low**
Offset: 118h set register
11Ch clear register
Type: Read/Set/Clear
Default: 0000 0000h

Table 4–27. Physical Request Filter Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	physReqResource31	RSC	If this bit is set for local bus node number 31, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
30	physReqResource30	RSC	If this bit is set for local bus node number 30, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
⋮	⋮	⋮	Bits 29 through 2 follow the same pattern.
1	physReqResource1	RSC	If this bit is set for local bus node number 1, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.
0	physReqResource0	RSC	If this bit is set for local bus node number 0, then physical requests received by the TSB43AA22 device from that node are handled through the physical request context.

4.36 Physical Upper Bound Register (Optional Register)

The physical upper bound register is an optional register and is not implemented. It returns all 0s when read.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Physical upper bound															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Physical upper bound															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Physical upper bound**
Offset: 120h
Type: Read-only
Default: 0000 0000h

4.37 Asynchronous Context Control Register

The asynchronous context control set/clear register controls the state and indicates status of the DMA context. See Table 4–28 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Asynchronous context control															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Asynchronous context control															
Type	RSCU	R	R	RSU	RU	RU	R	R	RU	RU	RU	RU	RU	RU	RU	RU
Default	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

Register: **Asynchronous context control**
Offset: 180h set register [ATRQ]
184h clear register [ATRQ]
1A0h set register [ATRS]
1A4h clear register [ATRS]
1C0h set register [ARRQ]
1C4h clear register [ARRQ]
1E0h set register [ARRS]
1E4h clear register [ARRS]
Type: Read/Set/Clear/Update, Read/Set/Update, Read/Update, Read-only
Default: 0000 X0XXh

Table 4–28. Asynchronous Context Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	RSVD	R	Reserved. Bits 31–16 return 0s when read.
15	run	RSCU	This bit is set by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The TSB43AA22 device changes this bit only on a hardware or software reset.
14–13	RSVD	R	Reserved. Bits 14–13 return 0s when read.
12	wake	RSU	Software sets this bit to cause the TSB43AA22 device to continue or resume descriptor processing. The TSB43AA22 device clears this bit on every descriptor fetch.
11	dead	RU	The TSB43AA22 device sets this bit when it encounters a fatal error and clears the bit when software resets bit 15 (run).
10	active	RU	The TSB43AA22 device sets this bit to 1 when it is processing descriptors.
9–8	RSVD	R	Reserved. Bits 9–8 return 0s when read.
7–5	spd	RU	This field indicates the speed at which a packet was received or transmitted, and only contains meaningful information for receive contexts. This field is encoded as: 000 = 100 Mbits/sec 001 = 200 Mbits/sec 010 = 400 Mbits/sec All other values are reserved.
4–0	eventcode	RU	This field holds the acknowledge sent by the link core for this packet, or holds an internally generated error code if the packet was not transferred successfully.

4.38 Asynchronous Context Command Pointer Register

The asynchronous context command pointer register contains a pointer to the address of the first descriptor block that the TSB43AA22 device accesses when software enables the context by setting bit 15 (run) of the asynchronous context control register (see Section 4.37). See Table 4–29 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Asynchronous context command pointer															
Type	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Asynchronous context command pointer															
Type	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU	RWU
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Register: **Asynchronous context command pointer**
Offset: 18Ch [ATRQ]
1ACh [ATRS]
1CCh [ARRQ]
1ECh [ARRS]
Type: Read/Write/Update
Default: XXXX XXXXh

Table 4–29. Asynchronous Context Command Pointer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–4	descriptorAddress	RWU	Contains the upper 28 bits of the address of a 16-byte-aligned descriptor block.
3–0	Z	RWU	Indicates the number of contiguous descriptors at the address pointed to by the descriptor address. If Z is 0, then it indicates that the descriptorAddress field (bits 31–4) is not valid.

4.39 Isochronous Transmit Context Control Register

The isochronous transmit context control set/clear register controls options, state, and status for the isochronous transmit DMA contexts. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3, …, 7). See Table 4–30 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Isochronous transmit context control															
Type	RSCU	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC	RSC
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Isochronous transmit context control															
Type	RSC	R	R	RSU	RU	RU	R	R	RU	RU	RU	RU	RU	RU	RU	RU
Default	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

Register: **Isochronous transmit context control**
Offset: 200h + (16 * n) set register
204h + (16 * n) clear register
Type: Read/Set/Clear/Update, Read/Set/Clear, Read/Set/Update, Read/Update, Read-only
Default: XXXX X0XXh

Table 4–30. Isochronous Transmit Context Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	cycleMatchEnable	RSCU	When this bit is set to 1, processing occurs such that the packet described by the context first descriptor block is transmitted in the cycle whose number is specified in the cycleMatch field (bits 30–16). The cycleMatch field (bits 30–16) must match the low-order two bits of cycleSeconds and the 13-bit cycleCount field in the cycle start packet that is sent or received immediately before isochronous transmission begins. Since the isochronous transmit DMA controller may work ahead, the processing of the first descriptor block may begin slightly in advance of the actual cycle in which the first packet is transmitted. The effects of this bit, however, are impacted by the values of other bits in this register and are explained in the *1394 Open Host Controller Interface Specification.* Once the context has become active, hardware clears this bit.
30–16	cycleMatch	RSC	This field contains a 15-bit value, corresponding to the low-order two bits of the bus isochronous cycle timer register (OHCI offset F0h, see Section 4.31) cycleSeconds field (bits 31–25) and the cycleCount field (bits 24–12). If bit 31 (cycleMatchEnable) is set, then this isochronous transmit DMA context becomes enabled for transmits when the low-order two bits of the isochronous cycle timer register cycleSeconds field (bits 31–25) and the cycleCount field (bits 24–12) value equal this field (cycleMatch) value.
15	run	RSC	This bit is set by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The TSB43AA22 device changes this bit only on a hardware or software reset.
14–13	RSVD	R	Reserved. Bits 14–13 return 0s when read.
12	wake	RSU	Software sets this bit to cause the TSB43AA22 device to continue or resume descriptor processing. The TSB43AA22 device clears this bit on every descriptor fetch.
11	dead	RU	The TSB43AA22 device sets this bit when it encounters a fatal error and clears the bit when software resets bit 15 (run).
10	active	RU	The TSB43AA22 device sets this bit to 1 when it is processing descriptors.
9–8	RSVD	R	Reserved. Bits 9–8 return 0s when read.
7–5	spd	RU	This field in not meaningful for isochronous transmit contexts.
4–0	event code	RU	Following an OUTPUT_LAST* command, the error code is indicated in this field. Possible values are: ack_complete, evt_descriptor_read, evt_data_read, and evt_unknown.

4.40 Isochronous Transmit Context Command Pointer Register

The isochronous transmit context command pointer register contains a pointer to the address of the first descriptor block that the TSB43AA22 device accesses when software enables an isochronous transmit context by setting bit 15 (run) of the isochronous transmit context control register (see Section 4.39). The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3, …, 7).

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Isochronous transmit context command pointer															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Isochronous transmit context command pointer															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Register: **Isochronous transmit context command pointer**
Offset: 20Ch + (16 * n)
Type: Read-only
Default: XXXX XXXXh

4.41 Isochronous Receive Context Control Register

The isochronous receive context control set/clear register controls options, state, and status for the isochronous receive DMA contexts. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3). See Table 4–31 for a complete description of the register contents.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Isochronous receive context control															
Type	RSC	RSC	RSCU	RSC	R	R	R	R	R	R	R	R	R	R	R	R
Default	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Isochronous receive context control															
Type	RSCU	R	R	RSU	RU	RU	R	R	RU	RU	RU	RU	RU	RU	RU	RU
Default	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

Register: **Isochronous receive context control**
Offset: 400h + (32 * n) set register
404h + (32 * n) clear register
Type: Read/Set/Clear/Update, Read/Set/Clear, Read/Set/Update, Read/Update, Read-only
Default: X000 X0XXh

Table 4–31. Isochronous Receive Context Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	bufferFill	RSC	When this bit is set, received packets are placed back-to-back to completely fill each receive buffer. When this bit is cleared, each received packet is placed in a single buffer. If bit 28 (multiChanMode) is set to 1, then this bit must also be set to 1. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set.
30	isochHeader	RSC	When this bit is 1, received isochronous packets include the complete 4-byte isochronous packet header seen by the link layer. The end of the packet is marked with a xferStatus in the first doublet, and a 16-bit timeStamp indicating the time of the most recently received (or sent) cycleStart packet. When this bit is cleared, the packet header is stripped from received isochronous packets. The packet header, if received, immediately precedes the packet payload. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set.

Table 4–31. Isochronous Receive Context Control Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
29	cycleMatchEnable	RSCU	When this bit is set, the context begins running only when the 13-bit cycleMatch field (bits 24–12) in the isochronous receive context match register (See Section 4.43) matches the 13-bit cycleCount field in the cycleStart packet. The effects of this bit, however, are impacted by the values of other bits in this register. Once the context has become active, hardware clears this bit. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set.
28	multiChanMode	RSC	When this bit is set, the corresponding isochronous receive DMA context receives packets for all isochronous channels enabled in the isochronous receive channel mask high (OHCI offset 70h/74h, see Section 4.19) and isochronous receive channel mask low (OHCI offset 78h/7Ch, see Section 4.20) registers. The isochronous channel number specified in the isochronous receive context match register (see Section 4.43) is ignored. When this bit is cleared, the isochronous receive DMA context receives packets for the single channel specified in the isochronous receive context match register (see Section 4.43). Only one isochronous receive DMA context may use the isochronous receive channel mask registers (see Sections 4.19 and 4.20). If more than one isochronous receive context control register has this bit set, then results are undefined. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1.
27–16	RSVD	R	Reserved. Bits 27–16 return 0s when read.
15	run	RSCU	This bit is set by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The TSB43AA22 device changes this bit only on a hardware or software reset.
14–13	RSVD	R	Reserved. Bits 14–13 return 0s when read.
12	wake	RSU	Software sets this bit to cause the TSB43AA22 device to continue or resume descriptor processing. The TSB43AA22 device clears this bit on every descriptor fetch.
11	dead	RU	The TSB43AA22 device sets this bit when it encounters a fatal error and clears the bit when software resets bit 15 (run).
10	active	RU	The TSB43AA22 device sets this bit to 1 when it is processing descriptors.
9–8	RSVD	R	Reserved. Bits 9–8 return 0s when read.
7–5	spd	RU	This field indicates the speed at which the packet was received. 000 = 100 Mbits/sec 001 = 200 Mbits/sec 010 = 400 Mbits/sec All other values are reserved.
4–0	event code	RU	For bufferFill mode, possible values are: ack_complete, evt_descriptor_read, evt_data_write, and evt_unknown. Packets with data errors (either dataLength mismatches or dataCRC errors) and packets for which a FIFO overrun occurred are backed out. For packet-per-buffer mode, possible values are: ack_complete, ack_data_error, evt_long_packet, evt_overrun, evt_descriptor_read, evt_data_write, and evt_unknown.

4.42 Isochronous Receive Context Command Pointer Register

The isochronous receive context command pointer register contains a pointer to the address of the first descriptor block that the TSB43AA22 device accesses when software enables an isochronous receive context by setting bit 15 (run) of the isochronous receive context control register (see Section 4.41). The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3).

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Isochronous receive context command pointer															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Isochronous receive context command pointer															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Register: **Isochronous receive context command pointer**
Offset: 40Ch + (32 * n)
Type: Read-only
Default: XXXX XXXXh

4.43 Isochronous Receive Context Match Register

The isochronous receive context match register is used to start an isochronous receive context running on a specified cycle number, to filter incoming isochronous packets based on tag values, and to wait for packets with a specified sync value. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3). See Table 4–32 for a complete description of the register contents.

Bit	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Name	Isochronous receive context match															
Type	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	0	0	0	X	X	X	X	X	X	X	X	X
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Isochronous receive context match															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X

Register: **Isochronous receive context match**
Offset: 410Ch + (32 * n)
Type: Read/Write, Read-only
Default: XXXX XXXXh

Table 4–32. Isochronous Receive Context Match Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	tag3	R/W	If this bit is set, then this context matches on iso receive packets with a tag field of 11b.
30	tag2	R/W	If this bit is set, then this context matches on iso receive packets with a tag field of 10b.
29	tag1	R/W	If this bit is set, then this context matches on iso receive packets with a tag field of 01b.
28	tag0	R/W	If this bit is set, then this context matches on iso receive packets with a tag field of 00b.
27	RSVD	R	Reserved. Bit 27 returns a 0 when read.
26–12	cycleMatch	R/W	Contains a 15-bit value, corresponding to the two low-order bits of cycleSeconds and the 13-bit cycleCount field in the cycleStart packet. If cycleMatchEnable (bit 29) of the isochronous receive context control register (see Section 4.41) is set, then this context is enabled for receives when the two low-order bits of the isochronous cycle timer register (OHCI offset F0h, see Section 4.31) cycleSeconds field (bits 31–25) and cycleCount field (bits 24–12) value equal this (cycleMatch) field value.
11–8	sync	R/W	This field contains the four-bit field which is compared to the sync field of each iso packet for this channel when the command descriptor w field is set to 11b.
7	RSVD	R	Reserved. Bit 7 returns 0 when read.
6	tag1SyncFilter	R/W	If this bit and bit 29 (tag1) are set , then packets with tag 01b are accepted into the context if the two most significant bits of the packet sync field are 00b. Packets with tag values other than 01b are filtered according to tag0, tag2, and tag3 (bits 28, 30, and 31, respectively) without any additional restrictions. If this bit is cleared, then this context matches on isochronous receive packets as specified in bits 28–31 (tag0–tag3) with no additional restrictions.
5–0	channelNumber	R/W	This 6-bit field indicates the isochronous channel number for which this isochronous receive DMA context accepts packets.

5 Serial ROM Interface

The TSB43AA22 device provides a serial bus interface to initialize the GUID registers and a few PCI configuration registers through a serial ROM. The TSB43AA22 device communicates with the serial ROM via the 2-wire serial interface.

After power-up the serial interface initializes the locations listed in Table 5–1. While the TSB43AA22 device is accessing the serial ROM, all incoming PCI slave accesses are terminated with retry status. Table 5–2 shows the serial ROM memory map required for initializing the TSB43AA22 registers.

NOTE: If a ROM is implemented in the design, it must be programmed. An unprogrammed ROM defaults to all 1s, which will adversely impact device operation.

Table 5–1. Registers and Bits Loadable Through Serial ROM

ROM OFFSET	OHCI/PCI OFFSET	REGISTER	BITS LOADED FROM EEPROM
00h	PCI register (3Eh)	PCI maximum latency, PCI minimum grant	15–0
01h	PCI register (2Dh)	Vendor identification	15–0
03h	PCI register (2Ch)	Subsystem identification	15–0
05h (bit 6)	OHCI register (50h)	Host controller control	23
05h	PCI register (F4h)	Link enhancement control	7, 2, 1
06h–0Ah	OHCI register (24h)	GUID high	31–0
0Bh–0Eh	OHCI register(28h)	GUID low	31–0
10h	PCI register (F4h)	Link enhancement control	13, 12
11h–12h	PCI register (F0h)	Miscellaneous configuration	15, 13, 10, 4–0
13h	PCI register (40h)	OHCI control	0
14h	N/A	CNA enable	3

Table 5–2. Serial ROM Map

BYTE ADDRESS	BYTE DESCRIPTION							
00	PCI maximum latency (0h)				PCI_minimum grant (0h)			
01	PCI vendor ID							
02	PCI vendor ID (msbyte)							
03	PCI subsystem ID (lsbyte)							
04	PCI subsystem ID							
05	[7] Link_enhancement-Control.enab_unfair	[6] HCControl. ProgramPhy Enable	[5] RSVD	[4] RSVD	[3] RSVD	[2] Link_enhancement-Control.enab_ insert_idle	[1] Link_enhancement-Control.enab_accel	[0] RSVD
06	Mini ROM address							
07	GUID high (lsbyte 0)							
08	GUID high (byte 1)							
09	GUID high (byte 2)							
0A	GUID high (msbyte 3)							
0B	GUID low (lsbyte 0)							
0C	GUID low (byte 1)							
0D	GUID low (byte 2)							
0E	GUID low (msbyte 3)							
0F	Checksum							
10	[15] RSVD	[14] RSVD	[13–12] AT threshold		[11] RSVD	[10] RSVD	[9] RSVD	[8] RSVD
11	[7] RSVD	[6] RSVD	[5] RSVD	[4] Disable Target Abort	[3] GP2IIC	[2] Disable SCLK gate	[1] Disable PCI gate	[0] Keep PCI
12	[15] PME D3 Cold	[14] RSVD	[13] PME Support D2	[12] RSVD	[11] RSVD	[10] D2 support	[9] RSVD	[8] RSVD
13	[7] RSVD	[6] RSVD	[5] RSVD	[4] RSVD	[3] RSVD	[2] RSVD	[1] RSVD	[0] Global swap
14	[7] RSVD	[6] RSVD	[5] RSVD	[4] RSVD	[3] CNA Enable	[2] RSVD	[1] RSVD	[0] RSVD
15–1F	RSVD							

6 PHY Register Configuration

There are 16 accessible internal registers in the TSB43AA22 device. The configuration of the registers at addresses 0h through 7h (the base registers) is fixed, whereas the configuration of the registers at addresses 8h through Fh (the paged registers) is dependent upon which 1 of 8 pages, numbered 0h through 7h, is currently selected. The selected page is set in base register 7h.

6.1 Base Registers

Table 6–1 shows the configuration of the base registers, and Table 6–2 shows the corresponding field descriptions. The base register field definitions are unaffected by the selected page number.

A reserved register or register field (marked as Reserved in the following register configuration tables) is read as 0, but is subject to future usage. All registers in address pages 2 through 6 are reserved.

Table 6–1. Base Register Configuration

ADDRESS	BIT POSITION							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0000	Physical ID						R	CPS
0001	RHB	IBR	Gap_Count					
0010	Extended (111b)			Reserved	Num_Ports (0010b)			
0011	PHY_Speed (010b)			Reserved	Delay (0000b)			
0100	LCtrl	C	Jitter (000b)			Pwr_Class		
0101	RPIE	ISBR	CTOI	CPSI	STOI	PEI	EAA	EMC
0110	Reserved							
0111	Page_Select			Reserved	Port_Select			

Table 6–2. Base Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Physical ID	6	R	This field contains the physical address ID of this node determined during self-ID. The physical ID is invalid after a bus reset until self-ID has completed as indicated by an unsolicited register-0 status transfer.
R	1	R	Root. This bit indicates that this node is the root node. The R bit is cleared to 0 by bus reset, and is set to 1 during tree-ID if this node becomes root.
CPS	1	R	Cable-power-status. This bit indicates the state of the CPS input terminal. The CPS terminal is normally tied to serial bus cable power through a 400-kΩ resistor. A 0 in this bit indicates that the cable power voltage has dropped below its threshold for ensured reliable operation.
RHB	1	R/W	Root-holdoff bit. This bit instructs the PHY device to attempt to become root after the next bus reset. The RHB bit is cleared to 0 by a hardware reset, and is unaffected by a bus reset.
IBR	1	R/W	Initiate bus reset. This bit instructs the PHY device to initiate a long (166 μs) bus reset at the next opportunity. Any receive or transmit operation in progress when this bit is set will complete before the bus reset is initiated. The IBR bit is cleared to 0 after a hardware reset or a bus reset.
Gap_Count	6	R/W	Arbitration gap count. This value is used to set the subaction (fair) gap, arb-reset gap, and arb-delay times. The gap count can be set either by a write to the register, or by reception or transmission of a PHY_CONFIG packet. The gap count is reset to 3Fh by hardware reset or after two consecutive bus resets without an intervening write to the gap count register (either by a write to the PHY register or by a PHY_CONFIG packet).
Extended	3	R	Extended register definition. For the TSB43AA22 device, this field is 111b, indicating that the extended register set is implemented.
Num_Ports	4	R	Number of ports. This field indicates the number of ports implemented in the PHY device. For the TSB43AA22 device this field is 2.
PHY_Speed	3	R	PHY speed capability. For the TSB43AA22 PHY device this field is 010b, indicating S400 speed capability.
Delay	4	R	PHY repeater data delay. This field indicates the worst case repeater data delay of the PHY device, expressed as 144+(delay × 20) ns. For the TSB43AA22 device this field is 0.
LCtrl	1	R/W	Link-active status control. This bit is used to control active status of the LLC as indicated during self-ID. The logical AND of this bit and the LPS active status is replicated in the L field (bit 9) of the self-ID packet. The LLC is considered active only if both the LPS input is active and the LCtrl bit is set. The LCtrl bit provides a software controllable means to indicate the LLC active/status in lieu of using the LPS input. The LCtrl bit is set to 1 by a hardware reset and is unaffected by a bus reset. NOTE: The state of the PHY-LLC interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit. If the PHY-LLC interface is operational as determined by the LPS input being active, then received packets and status information will continue to be presented on the interface, and any requests indicated on the LREQ input will be processed, even if the LCtrl bit is cleared to 0.
C	1	R/W	Contender status. This bit indicates that this node is a contender for the bus or isochronous resource manager. This bit is replicated in the c field (bit 20) of the self-ID packet.
Jitter	3	R	PHY repeater jitter. This field indicates the worst case difference between the fastest and slowest repeater data delay, expressed as (Jitter+1) × 20 ns. For the TSB43AA22 device, this field is 0.
Pwr_Class	3	R/W	Node power class. This field indicates this node power consumption and source characteristics and is replicated in the pwr field (bits 21–23) of the self-ID packet. This field is reset to the state specified by the PC0–PC2 input terminals upon a hardware reset, and is unaffected by a bus reset. See Table 6–9.
RPIE	1	R/W	Resuming port interrupt enable. This bit, if set to 1, enables the port event interrupt (PEI) bit to be set whenever resume operations begin on any port. This bit is cleared to 0 by hardware reset and is unaffected by bus reset.

Table 6–2. Base Register Field Descriptions (Continued)

FIELD	SIZE	TYPE	DESCRIPTION
ISBR	1	R/W	Initiate short arbitrated bus reset. This bit, if set to 1, instructs the PHY device to initiate a short (1.3 μs) arbitrated bus reset at the next opportunity. This bit is cleared to 0 by a bus reset. NOTE: Legacy IEEE Std 1394-1995 compliant PHY devices can not be capable of performing short bus resets. Therefore, initiation of a short bus reset in a network that contains such a legacy device results in a long bus reset being performed.
CTOI	1	R/W	Configuration time-out interrupt. This bit is set to 1 when the arbitration controller times out during tree-ID start, and may indicate that the bus is configured in a loop. This bit is cleared to 0 by hardware reset, or by writing a 1 to this register bit. If the CTOI and RPIE bits are both set and the LLC is or becomes inactive, the PHY device will activate the LLC to service the interrupt. NOTE: If the network is configured in a loop, only those nodes which are part of the loop will generate a configuration-timeout interrupt. All other nodes will instead time out waiting for the tree-ID and/or self-ID process to complete and then generate a state time-out interrupt and bus-reset.
CPSI	1	R/W	Cable power status interrupt. This bit is set to 1 whenever the CPS input transitions from high to low indicating that cable power may be too low for reliable operation. This bit is cleared to 0 by hardware reset, or by writing a 1 to this register bit.
STOI	1	R/W	State time-out interrupt. This bit indicates that a state time-out has occurred (which also causes a bus reset to occur). This bit is cleared to 0 by hardware reset, or by writing a 1 to this register bit.
PEI	1	R/W	Port event interrupt. This bit is set to 1 upon a change in the bias (unless disabled) connected, disabled, or fault bits for any port for which the port interrupt enable (PIE) bit is set. Additionally, if the resuming port interrupt enable (RPIE) bit is set, the PEI bit is set to 1 at the start of resume operations on any port. This bit is cleared to 0 by hardware reset, or by writing a 1 to this register bit.
EAA	1	R/W	Enable accelerated arbitration. This bit enables the PHY device to perform the various arbitration acceleration enhancements defined in IEEE 1394a-2000 (ACK-accelerated arbitration, asynchronous fly-by concatenation, and isochronous fly-by concatenation). This bit is cleared to 0 by hardware reset and is unaffected by bus reset.
EMC	1	R/W	Enable multispeed concatenated packets. This bit enables the PHY device to transmit concatenated packets of differing speeds in accordance with the protocols defined in IEEE 1394a-2000. This bit is cleared to 0 by hardware reset and is unaffected by bus reset.
Page_Select	3	R/W	Page_Select. This field selects the register page to use when accessing register addresses 8 through 15. This field is cleared to 0 by a hardware reset and is unaffected by bus reset.
Port_Select	4	R/W	Port_Select. This field selects the port when accessing per-port status or control (for example, when one of the port status/control registers is accessed in page 0). Ports are numbered starting at 0. This field is cleared to 0 by hardware reset and is unaffected by bus reset.

6.2 Port Status Register

The port status page provides access to configuration and status information for each of the ports. The port is selected by writing 0 to the Page_Select field and the desired port number to the Port_Select field in base register 7. Table 6–3 shows the configuration of the port status page registers and Table 6–4 shows the corresponding field descriptions. If the selected port is not implemented, then all registers in the port status page are read as 0.

Table 6–3. Page 0 (Port Status) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	AStat		BStat		Ch	Con	Bias	Dis
1001	Peer_Speed			PIE	Fault	Reserved		
1010	Reserved							
1011	Reserved							
1100	Reserved							
1101	Reserved							
1110	Reserved							
1111	Reserved							

Table 6–4. Page 0 (Port Status) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
AStat	2	R	TPA line state. This field indicates the TPA line state of the selected port, encoded as follows: Code — Arb Value 11 — Z 10 — 0 01 — 1 00 — invalid
BStat	2	R	TPB line state. This field indicates the TPB line state of the selected port. This field has the same encoding as the AStat field.
Ch	1	R	Child/parent status. A 1 indicates that the selected port is a child port. A 0 indicates that the selected port is the parent port. A disconnected, disabled, or suspended port is reported as a child port. The Ch bit is invalid after a bus reset until tree-ID has completed.
Con	1	R	Debounced port connection status. This bit indicates that the selected port is connected. The connection must be stable for the debounce time of approximately 341 ms for the Con bit to be set to 1. The Con bit is cleared to 0 by hardware reset and is unaffected by bus reset. NOTE: The Con bit indicates that the port is physically connected to a peer PHY device, but the port is not necessarily active.
Bias	1	R	Debounced incoming cable bias status. A 1 indicates that the selected port is detecting incoming cable bias. The incoming cable bias must be stable for the debounce time of 52 μs for the Bias bit to be set to 1.
Dis	1	R/W	Port disabled control. If 1, the selected port is disabled. The Dis bit is cleared to 0 by hardware reset (all ports are enabled for normal operation following hardware reset). The Dis bit is not affected by bus reset.
Peer_Speed	3	R	Port peer speed. This field indicates the highest speed capability of the peer PHY device connected to the selected port, encoded as follows: Code — Peer Speed 000 — S100 001 — S200 010 — S400 011–111 — invalid The Peer_Speed field is invalid after a bus reset until self-ID has completed. NOTE: Peer speed codes higher than 010b (S400) are defined in IEEE 1394a-2000. However, the TSB43AA22 device is only capable of detecting peer speeds up to S400.

Table 6–4. Page 0 (Port Status) Register Field Descriptions (Continued)

FIELD	SIZE	TYPE	DESCRIPTION
PIE	1	R/W	Port event interrupt enable. When set to 1, a port event on the selected port will set the port event interrupt (PEI) bit and notify the link. This bit is cleared to 0 by a hardware reset, and is unaffected by bus reset.
Fault	1	R/W	Fault. This bit indicates that a resume-fault or suspend-fault has occurred on the selected port, and that the port is in the suspended state. A resume-fault occurs when a resuming port fails to detect incoming cable bias from its attached peer. A suspend-fault occurs when a suspending port continues to detect incoming cable bias from its attached peer. Writing 1 to this bit clears the fault bit to 0. This bit is cleared to 0 by hardware reset and is unaffected by bus reset.

6.3 Vendor Identification Register

The vendor identification page is used to identify the vendor/manufacturer and compliance level. The page is selected by writing 1 to the Page_Select field in base register 7. Table 6–5 shows the configuration of the vendor identification page, and Table 6–6 shows the corresponding field descriptions.

Table 6–5. Page 1 (Vendor ID) Register Configuration

	BIT POSITION							
ADDRESS	0	1	2	3	4	5	6	7
1000	Compliance							
1001	Reserved							
1010	Vendor_ID[0]							
1011	Vendor_ID[1]							
1100	Vendor_ID[2]							
1101	Product_ID[0]							
1110	Product_ID[1]							
1111	Product_ID[2]							

Table 6–6. Page 1 (Vendor ID) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Compliance	8	R	Compliance level. For the TSB43AA22 device this field is 01h, indicating compliance with the IEEE 1394a-2000 specification.
Vendor_ID	24	R	Manufacturer's organizationally unique identifier (OUI). For the TSB43AA22 device this field is 08 0028h (Texas Instruments) (the MSB is at register address 1010b).
Product_ID	24	R	Product identifier. For the TSB43AA22 device this field is 00 0000h (the MSB is at register address 1101b).

6.4 Vendor-Dependent Register

The vendor-dependent page provides access to the special control features of the TSB43AA22 device, as well as configuration and status information used in manufacturing test and debug. This page is selected by writing 7 to the Page_Select field in base register 7. Table 6–7 shows the configuration of the vendor-dependent page and Table 6–8 shows the corresponding field descriptions.

Table 6–7. Page 7 (Vendor-Dependent) Register Configuration

	BIT POSITION							
ADDRESS	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
1000	NPA	Reserved					Link_Speed	
1001	Reserved for test							
1010	Reserved for test							
1011	Reserved for test							
1100	Reserved for test							
1101	Reserved for test							
1110	Reserved for test							
1111	Reserved for test							

Table 6–8. Page 7 (Vendor-Dependent) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
NPA	1	R/W	Null-packet actions flag. This bit instructs the PHY device to not clear fair and priority requests when a null packet is received with arbitration acceleration enabled. If this bit is 1, then fair and priority requests are cleared only when a packet of more than 8 bits is received; ACK packets (exactly 8 data bits), null packets (no data bits), and malformed packets (less than 8 data bits) will not clear fair and priority requests. If this bit is 0, then fair and priority requests are cleared when any non-ACK packet is received, including null packets or malformed packets of less than 8 bits. This bit is cleared to 0 by hardware reset and is unaffected by bus reset.
Link_Speed	2	R/W	Link speed. This field indicates the top speed capability of the attached LLC. Encoding is as follows: Code Speed 00 S100 01 S200 10 S400 11 illegal This field is replicated in the sp field of the self-ID packet to indicate the speed capability of the node (PHY and LLC in combination). However, this field does not affect the PHY speed capability indicated to peer PHYs during self-ID; the TSB43AA22 PHY device identifies itself as S400 capable to its peers regardless of the value in this field. This field is set to 10b (S400) by hardware reset and is unaffected by bus-reset.

6.5 Power-Class Programming

The PC0–PC2 terminals are programmed to set the default value of the power-class indicated in the pwr field (bits 21–23) of the transmitted self-ID packet. Table 6–9 shows the descriptions of the various power classes. The default power-class value is loaded following a hardware reset, but is overridden by any value subsequently loaded into the Pwr_Class field in register 4.

Table 6–9. Power Class Descriptions

PC0–PC2	DESCRIPTION
000	Node does not need power and does not repeat power.
001	Node is self-powered and provides a minimum of 15 W to the bus.
010	Node is self-powered and provides a minimum of 30 W to the bus.
011	Node is self-powered and provides a minimum of 45 W to the bus.
100	Node may be powered from the bus and is using up to 3 W.
101	Node is powered from the bus and uses up to 3 W. No additional power is needed to enable the link.
110	Node is powered from the bus and uses up to 3 W. An additional 3 W is needed to enable the link.
111	Node is powered from the bus and uses up to 3 W. An additional 7 W is needed to enable the link.

7 GPIO Interface

The general-purpose input/output (GPIO) interface consists of two GPIO ports. GPIO2 and GPIO3 power up as general-purpose inputs and are programmable via the GPIO control register. Figure 7–1 shows the logic diagram for GPIO2 and GPIO3 implementation.

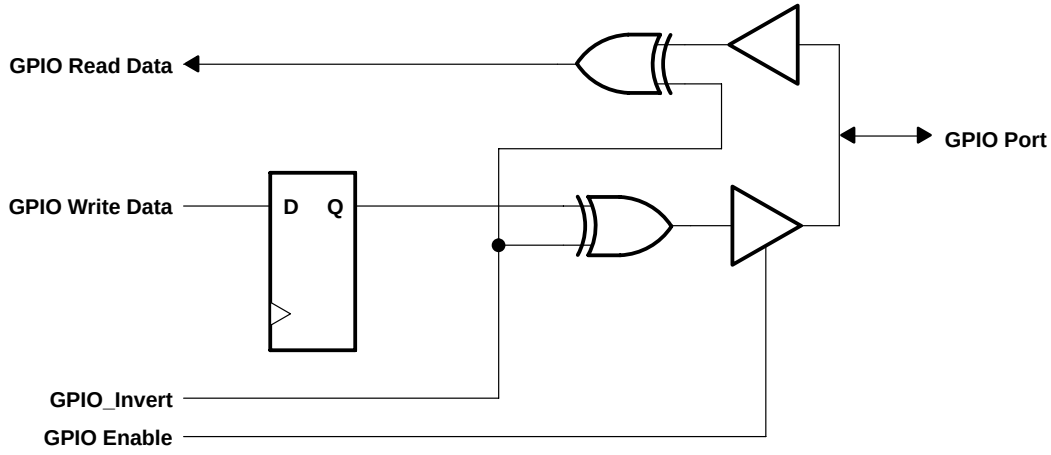
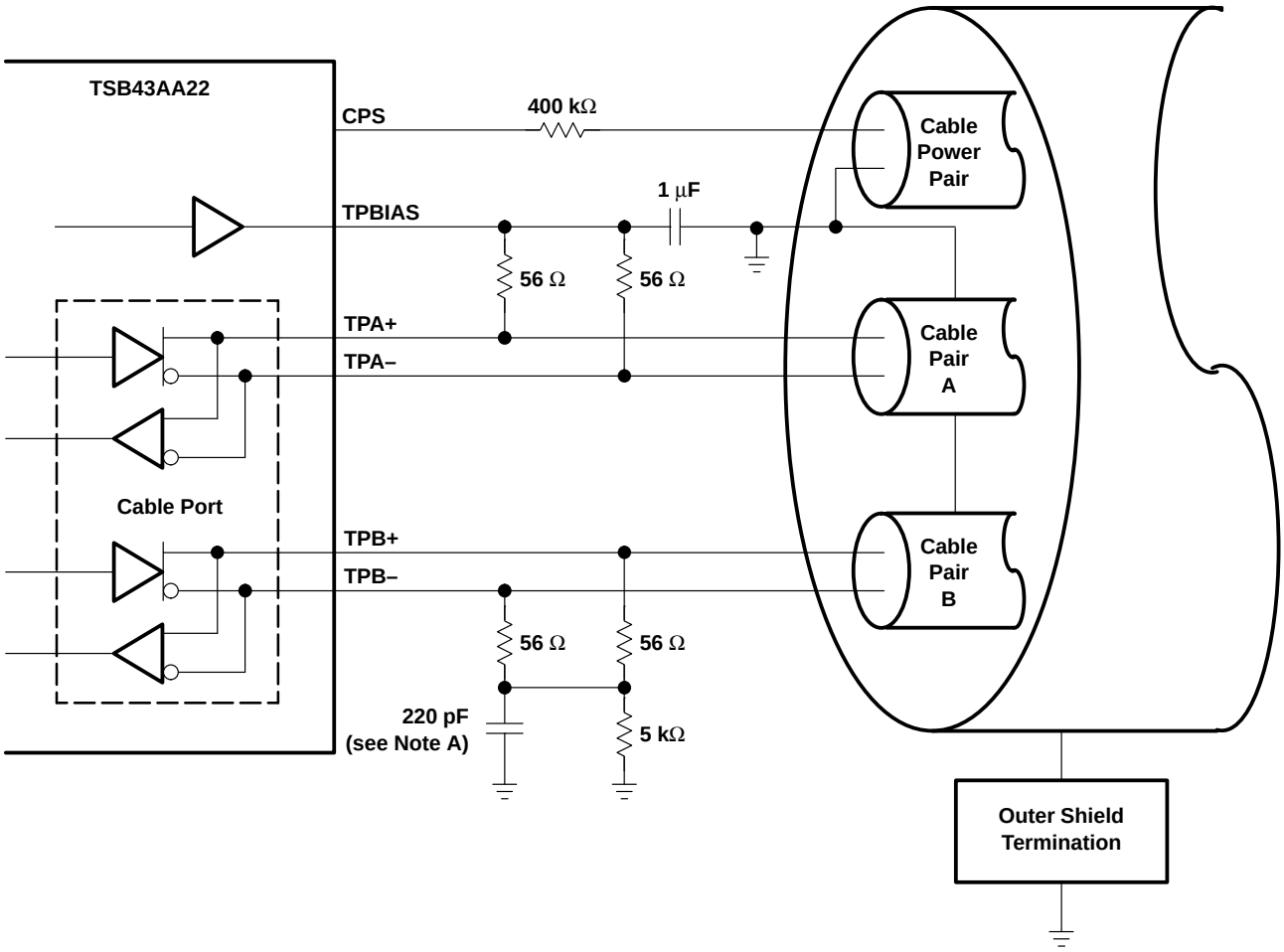


Figure 7–1. GPIO2 and GPIO3 Logic Diagram

8 Application Information

8.1 PHY Port Cable Connection



NOTE A: The IEEE 1394-1995 standard calls for a 250-pF capacitor, which is a nonstandard component value. A 220-pF capacitor is recommended.

Figure 8–1. TP Cable Connections

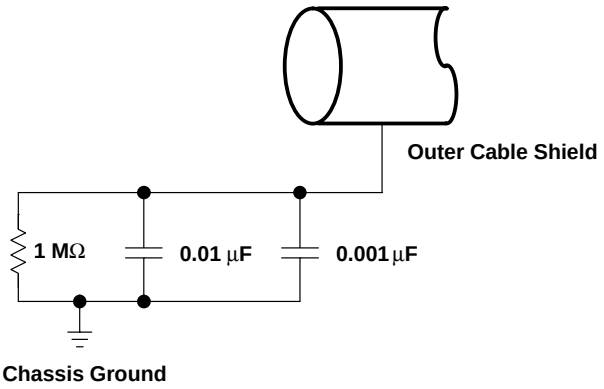


Figure 8–2. Typical Compliant DC Isolated Outer Shield Termination

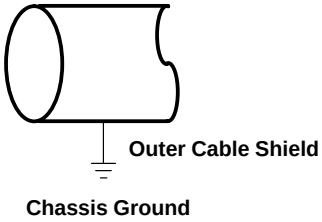


Figure 8–3. Non-DC Isolated Outer Shield Termination

8.2 Crystal Selection

The TSB43AA22 device is designed to use an external 24.576-MHz crystal connected between the XI and XO pins to provide the reference for an internal oscillator circuit. This oscillator in turn drives a PLL circuit that generates the various clocks required for transmission and resynchronization of data at the S100 through S400 media data rates.

A variation of less than ±100 ppm from nominal for the media data rates is required by IEEE 1394-1995. Adjacent PHYs may therefore have a difference of up to 200 ppm from each other in their internal clocks, and PHY devices must be able to compensate for this difference over the maximum packet length. Large clock variations may cause resynchronization overflows or underflows, resulting in corrupted packet data.

The following are some typical specifications for crystals used with the physical layers from TI in order to achieve the required frequency accuracy and stability:

- Crystal mode of operation: Fundamental
- Frequency tolerance @ 25°C: Total frequency variation for the complete circuit is ±100 ppm. A crystal with ±30 ppm frequency tolerance is recommended for adequate margin.
- Frequency stability (over temperature and age): A crystal with ±30 ppm frequency stability is recommended for adequate margin.

  NOTE: The total frequency variation must be kept below ±100 ppm from nominal with some allowance for error introduced by board and device variations. Trade-offs between frequency tolerance and stability may be made as long as the total frequency variation is less than ±100 ppm. For example, the frequency tolerance of the crystal may be specified at 50 ppm and the temperature tolerance may be specified at 30 ppm to give a total of 80 ppm possible variation due to the crystal alone. Crystal aging also contributes to the frequency variation.
- Load capacitance: For parallel resonant mode crystal circuits, the frequency of oscillation is dependent upon the load capacitance specified for the crystal. Total load capacitance (C_L) is a function of not only the discrete load capacitors, but also board layout and circuit. It is recommended that load capacitors with a maximum of ±5% tolerance be used.

As an example, for the TSB43AA22 evaluation module (EVM) which uses a crystal specified for 12 pF loading, load capacitors (C9 and C10 in Figure 8–4) of 16 pF each were appropriate for the layout of that particular board. The load specified for the crystal includes the load capacitors (C9, C10), the loading of the PHY pins (C_{PHY}), and the loading of the board itself (C_{BD}). The value of C_{PHY} is typically about 1 pF, and C_{BD} is typically 0.8 pF per centimeter of board etch; a *typical* board can have 3 pF to 6 pF or more. The load capacitors C9 and C10 combine as capacitors in series so that the total load capacitance is:

$$C_L = \frac{C9 \times C10}{C9 + C10} + C_{PHY} + C_{BD}$$

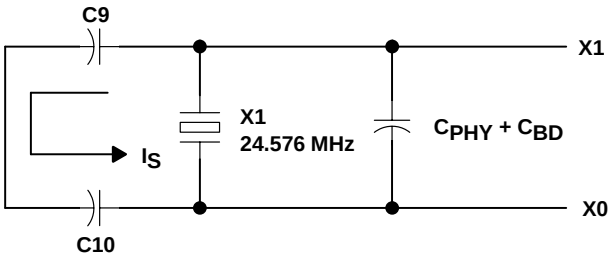
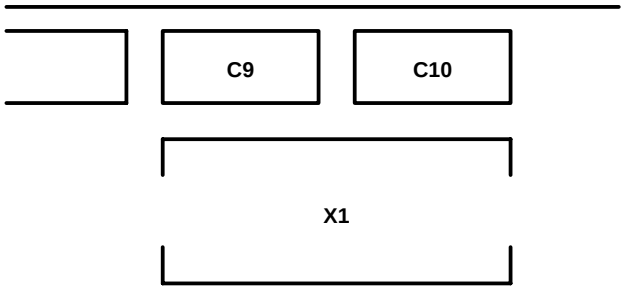


Figure 8–4. Load Capacitance for the TSB43AA22 PHY

The layout of the crystal portion of the PHY circuit is important for obtaining the correct frequency, minimizing noise introduced into the PHY phase-lock loop, and minimizing any emissions from the circuit. The crystal and two load capacitors should be considered as a unit during layout. The crystal and the load capacitors should be placed as close as possible to one another while minimizing the loop area created by the combination of the three components. Varying the size of the capacitors may help in this. Minimizing the loop area minimizes the effect of the resonant current (Is) that flows in this resonant circuit. This layout unit (crystal and load capacitors) should then be placed as close as possible to the PHY X1 and X0 pins to minimize etch lengths, as shown in Figure 8–5.



For more details on crystal selection, see application report SLLA051.

Figure 8–5. Recommended Crystal and Capacitor Layout

8.3 Bus Reset

In the TSB43AA22 device, the initiate bus reset (IBR) bit may be set to 1 in order to initiate a bus reset and initialization sequence. The IBR bit is located in PHY register 1, along with the root-holdoff bit (RHB) and Gap_Count field, as required by IEEE 1394a-2000. Therefore, whenever the IBR bit is written, the RHB and Gap_Count are also written.

The RHB and Gap_Count may also be updated by PHY-config packets. The TSB43AA22 device is IEEE 1394a-2000 compliant, and therefore both the reception and transmission of PHY-config packets cause the RHB and Gap_Count to be loaded, unlike older IEEE 1394-1995 compliant PHY devices which decode only received PHY-config packets.

The gap-count will be set to the maximum value of 63 after 2 consecutive bus resets without an intervening write to the Gap_Count, either by a write to PHY register 1 or by a PHY-config packet. This mechanism allows a PHY-config packet to be transmitted and then a bus reset initiated so as to verify that all nodes on the bus have updated their RHBs and Gap_Count values, without having the Gap_Count set back to 63 by the bus reset. The subsequent

connection of a new node to the bus, which initiates a bus reset, will then cause the Gap_Count of each node to be set to 63. Note, however, that if a subsequent bus reset is instead initiated by a write to register 1 to set the IBR bit, all other nodes on the bus will have their Gap_Count values set to 63, while this node Gap_Count remains set to the value just loaded by the write to PHY register 1.

Therefore, in order to maintain consistent gap-counts throughout the bus, the following rules apply to the use of the IBR bit, RHB, and Gap_Count in PHY register 1:

- Following the transmission of a PHY-config packet, a bus reset must be initiated in order to verify that all nodes have correctly updated their RHBs and Gap_Count values, and to ensure that a subsequent new connection to the bus will cause the Gap_Count to be set to 63 on all nodes in the bus. If this bus reset is initiated by setting the IBR bit to 1, the RHB and Gap_Count field must also be loaded with the correct values consistent with the just transmitted PHY-config packet. In the TSB43AA22 device, the RHB and Gap_Count will have been updated to their correct values upon the transmission of the PHY-config packet, and so these values may first be read from register 1 and then rewritten.
- Other than to initiate the bus reset which must follow the transmission of a PHY-config packet, whenever the IBR bit is set to 1 in order to initiate a bus reset, the Gap_Count value must also be set to 63 so as to be consistent with other nodes on the bus, and the RHB should be maintained with its current value.
- The PHY register 1 should not be written to except to set the IBR bit. The RHB and Gap_Count should not be written without also setting the IBR bit to 1.

9 Electrical Characteristics

9.1 Absolute Maximum Ratings Over Operating Temperature Ranges†

Supply voltage range: AV_{DD} . . . . . –0.5 V to 3.6 V
DV_{DD} . . . . . –0.5 V to 3.6 V
$PLLV_{DD}$ . . . . . –0.5 V to 3.6 V
V_{DDP} . . . . . –0.5 V to 5.5 V
Input voltage range for PCI, V_I, PHY, and Miscellaneous . . . . . –0.5 to DV_{DD} + 0.5 V
Output voltage range for PCI, V_O, PHY, and Miscellaneous . . . . . –0.5 to DV_{DD} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) (see Note 2) . . . . . ±20 mA
Storage temperature range . . . . . –65°C to 150°C
Electrostatic discharge (see Note 3) . . . . . HBM:2 kV, MM:200 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Applies to external input and bidirectional buffers. For 5-V tolerant use $V_I > V_{DDI}$. For PCI use $V_I > V_{DDP}$.
2. Applies to external output and bidirectional buffers. For 5-V tolerant use $V_O > V_{DDI}$. For PCI use $V_O > V_{DDP}$.
3. HBM is human body model, MM is machine model.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR§ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
PDT‡	2.33 W	0.023 W/°C	1.28 W
PDT§	1.54 W	0.015 W/°C	0.95 W

‡ Standard JEDEC high-K board
§ Standard JEDEC low-K board

9.2 Recommended Operating Conditions

			OPERATION	MIN	NOM	MAX	UNIT
Core voltage, AV_{DD}		Commercial	3.3 V	3	3.3	3.6	V
Core voltage, DV_{DD}		Commercial	3.3 V	3	3.3	3.6	V
Core voltage, $PLLV_{DD}$		Commercial	3.3 V	2.7	3	3.6	V
PCI I/O clamping voltage, V_{DDP}		Commercial	3.3 V	3	3.3	3.6	V
			5 V	4.5	5	5.5	
High-level input voltage, V_{IH}†		PCI	3.3 V	0.475 V_{DDP}		V_{DDP}	V
			5 V	2		V_{DDP}	
		PC0, PC1, PC2		0.7V_{DD}		DV_{DD}	
		$\overline{G\_RST}$		0.6V_{DD}		DV_{DD}	
		Miscellaneous‡		2		V_{DDP}	
Low-level input voltage, V_{IL}†		PCI	3.3 V	0		0.325 V_{DDP}	V
			5 V	0		0.8	
		PC0, PC1, PC2		0		0.2V_{DD}	
		$\overline{G\_RST}$		0		0.3V_{DD}	
		Miscellaneous‡		0		0.8	
Input voltage, V_I		PCI	3.3 V	0		V_{DDP}	V
		Miscellaneous‡		0		V_{DDP}	
Output voltage, V_O§		PCI	3.3 V	0		DV_{DD}	V
		Miscellaneous‡		0		DV_{DD}	
Input transition time (t_r and t_f), t_t		PCI		0		6	ns
Operating ambient temperature, T_A				0	25	70	°C
Virtual junction temperature, T_J¶				0	25	115	°C
Output current, I_O	TPBIAS outputs			−5.6		1.3	mA
Differential input voltage, V_{ID}	Cable inputs, during data reception			118		260	mV
	Cable inputs, during arbitration			168		265	
Common-mode input voltage, V_{IC}	TPB cable inputs, Source power node			0.4706		2.515	V
	TPB cable inputs, Nonsource power node			0.4706		2.015#	
Maximum junction temperature, T_J ($R\theta_{JA}$ values listed in thermal characteristic table)	128-PDT high-K JEDEC board $R\theta_{JA}$ = 42.96°C/W T_A = 70°C Pd = 0.8 W					112.96	°C
	128-PDT low-K JEDEC board $R\theta_{JA}$ = 60.97°C/W T_A = 70°C Pd = 0.8 W					134.86	
Power up reset time, t_{pu}	$\overline{G\_RST}$ input			2			ms
Receive input jitter	TPA, TPB cable inputs, S100 operation					±1.08	ns
	TPA, TPB cable inputs, S200 operation					±0.5	
	TPA, TPB cable inputs, S400 operation					±0.315	

† Applies to external inputs and bidirectional buffers without hysteresis.
‡ Miscellaneous pins are: GPIO2, GPIO3, SDA, SCL.
§ Applies to external output buffers.
¶ The junction temperatures reflect simulation conditions. Customer is responsible for verifying junction temperature.
# For a node that does not source power; see Section 4.2.2.2 in IEEE 1394a-2000.

Recommended Operating Conditions (Continued)

		OPERATION	MIN	NOM	MAX	UNIT
Receive input skew	Between TPA and TPB cable inputs, S100 operation				±0.8	ns
	Between TPA and TPB cable inputs, S200 operation				±0.55	
	Between TPA and TPB cable inputs, S400 operation				±0.5	

9.3 Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER			OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	PCI		I_{OH} = –0.5 mA	0.9 V_{DD}		V
				I_{OH} = –2 mA	2.4		
		Miscellaneous‡		I_{OH} = –4 mA	V_{DD}–0.6		
V_{OL}	Low-level output voltage	PCI		I_{OL} = 1.5 mA		0.1 V_{DD}	V
				I_{OL} = 6 mA		0.55	
		Miscellaneous‡		I_{OL} = 4 mA		0.5	
I_{OZ}	3-state output high-impedance	Output pins	3.6 V	V_O = V_{DD} or GND		±20	µA
I_{IL}	Low-level input current	Input pins	3.6 V	V_I = GND		±20	µA
		I/O pins†	3.6 V	V_I = GND	±20		
I_{IH}	High-level input current	PCI†	3.6 V	V_I = V_{DD}		±20	µA
		Others†	3.6 V	V_I = V_{DD}	±20		

† For I/O pins, input leakage (I_{IL} and I_{IH}) includes I_{OZ} of the disabled output.
‡ Miscellaneous pins are: GPIO2, GPIO3, SDA, SCL.

9.4 Switching Characteristics for PCI Interface§

PARAMETER		MEASURED	MIN	TYP	MAX	UNIT
t_{su}	Setup time before PCLK	–50% to 50%	7			ns
t_h	Hold time before PCLK	–50% to 50%	0			ns

§ These parameters are ensured by design.

9.5 Switching Characteristics for PHY Port Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Jitter, transmit	Between TPA and TPB			±0.15	ns
	Skew, transmit	Between TPA and TPB			±0.10	ns
t_r	TP differential rise time, transmit	10% to 90%, At 1394 connector	0.5		1.2	ns
t_f	TP differential fall time, transmit	90% to 10%, At 1394 connector	0.5		1.2	ns

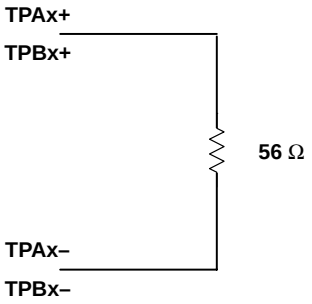


Figure 9–1. Test Load Diagram

9.6 Electrical Characteristics Over Recommended Ranges of Operating Conditions (unless otherwise noted)

9.6.1 Driver

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OD}	Differential output voltage	56 Ω, See Figure 9–1	172	265	mV
	Driver difference current, TPA+, TPA–, TPB+, TPB–	Drivers enabled, speed signaling off.	–1.05†	1.05†	mA
	Common-mode speed signaling current, TPB+, TPB–	S200 speed signaling enabled	–4.84‡	–2.53‡	mA
	Common-mode speed signaling current, TPB+, TPB–	S400 speed signaling enabled	–12.4‡	–8.10‡	mA
	Off state differential voltage	Drivers disabled, See Figure 9–1		20	mV

† Limits defined as algebraic sum of TPA+ and TPA– driver currents. Limits also apply to TPB+ and TPB– algebraic sum of driver currents.
‡ Limits defined as absolute limit of each of TPB+ and TPB– driver currents.

9.6.2 Receiver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{ID}	Differential impedance	Drivers disabled	10	14		kΩ
					4	pF
Z_{IC}	Common-mode impedance	Drivers disabled	20			kΩ
					24	pF
V_{TH-R}	Receiver input threshold voltage	Drivers disabled	–30		30	mV
V_{TH-CB}	Cable bias detect threshold, TPBx cable inputs	Drivers disabled	0.6		1.0	V
V_{TH+}	Positive arbitration comparator threshold voltage	Drivers disabled	89		168	mV
V_{TH-}	Negative arbitration comparator threshold voltage	Drivers disabled	–168		–89	mV
$V_{TH–SP200}$	Speed signal threshold	TPBIAS–TPA common mode voltage, drivers disabled	49		131	mV
$V_{TH–SP\ 400}$	Speed signal threshold	TPBIAS–TPA common mode voltage, drivers disabled	314		396	mV

9.6.3 Device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	See Note 4		217		mA
		See Note 5		214		
		See Note 6		77		
$I_{DD(ULP)}$	Supply current	Ports disabled DV_{DD} = 3.3 V LPD = off T_A = 25°C, D state = D0 PCI_CLK disabled, i.e., $\overline{\text{CLKRUN}}$ asserted		450		µA
V_{TH}	Power status threshold, CPS input†	400-kΩ resistor†	4.7		7.5	V
V_O	TPBIAS output voltage	At rated I_O current	1.665		2.015	V
I_I	Input current (PC0–PC2 inputs)	V_{DD} = 3.6 V			5	µA
I_{IRST}	Pullup current ($\overline{\text{G\_RST}}$ input)	V_I = 1.5 V	–90		–20	µA
		V_I = 0 V	–90		–20	

† Measured at cable power side of resistor.

NOTES: 4. Transmit (all ports transmit, 100% bandwidth, S400), V_{DD} = 3.3 V, T_A = 25°C
5. Repeat (receive on one port, transmit on other port, full ISO payload of 84 µs, S400, data value of CCCC CCCCh), V_{DD} = 3.3 V, T_A = 25°C
6. Idle (receive cycle start on one port, transmit cycle start on other port), V_{DD} = 3.3 V, T_A = 25°C

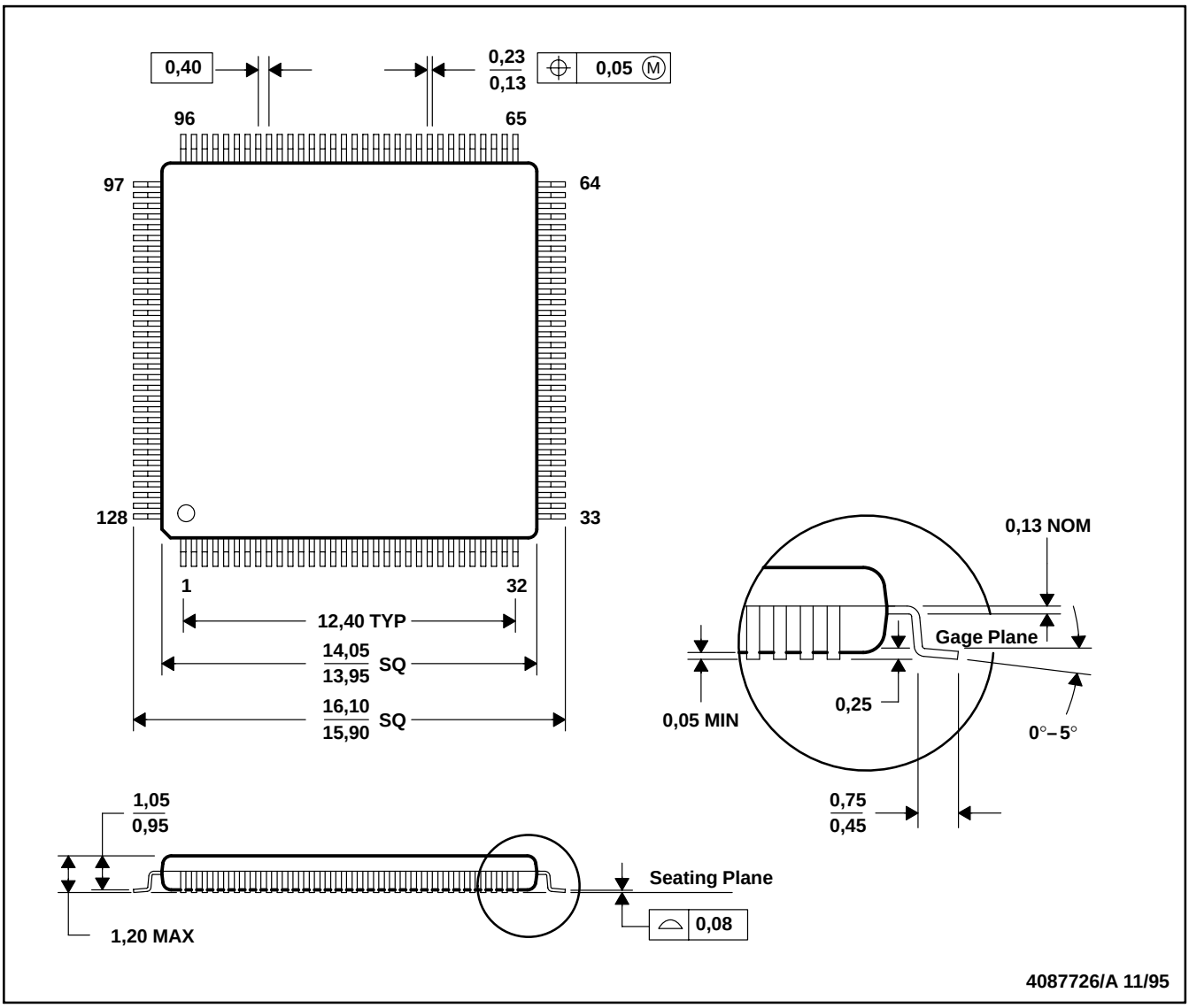
9.7 Thermal Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
128-PDT	$R\theta_{JA,}$ high-K board	Board mounted, no air flow, JEDEC test board			42.96	°C/W
128-PDT	$R\theta_{JA,}$ low-K board				60.97	°C/W
128-PDT	$R\theta_{JC}$				10.77	°C/W

10 Mechanical Information

The TSB43AA22 device is packaged in a 128-terminal PDT package. The following shows the mechanical dimensions for the PDT package.

PDT (S-PQFP-G128) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136