PDA ANALOG INTERFACE CIRCUIT
SILICON ERRATA

This document identifies an error in the control logic that affects parts TSC2000, TSC2200, TSC2300, TSC2301, and TSC2302. This error can cause incorrect operation in certain scenarios when a user is writing to the ADC Control Register (page 1, register 00). This error occurs when the user attempts to put the part into a self-control mode and the internal oscillator is not running. It is possible that the register write may not actually be latched and used by the part in this situation. However, this problem can be circumvented easily by following the sequence described below.

Advisory	*Control Logic*

Details:

This sequence avoids the logic error by first, stopping any conversions that are presently in progress, then it starts a host-controlled conversion (such as X, Y, Z1Z2, XY or XYZ) with settings that causes the internal oscillator to turn on and stay on for a specific time. While this host-controlled conversion is completing (with the internal oscillator running), the desired register setting is written to the ADC Control Register. The long host-controlled conversion forces the internal oscillator to start and stay on long enough for the user to write the desired setting into the register, thus avoiding the logic error.

Workaround :

When the user wants to write the ADC Control Register at any point and put the part into self-control mode (this applies when converting X, Y, Z1Z2, XY, or XYZ), the user should follow the sequence shown below:

1. Write a 1 in bit 15 (the STS bit) in the ADC Control Register, to stop any conversion that may be presently in progress.

2. Write the ADC Control Register to initiate a host-controlled conversion, such as an XY or XYZ conversion. This entails writing a 0 to the PSM bit, writing a 0 to the STP bit, and the appropriate code to the A/D3–0 bits to convert the desired coordinate(s). It is recommended that the user write to convert the same coordinates they intend to be converted in step 3, whether, X, Y, Z, XY, or XYZ. The remaining bits in this register should be written such that the resulting conversion takes a sufficiently long time to complete, that the desired register settings can be written before this conversion completes. This is accomplished by using the maximum number of averages (16 data averages), the slowest clock speed (1 MHz setting), the highest converter resolution (12 bits), and the longest panel voltage stabilization timing (100 msec).

3. While the conversion in step 2 is in progress, write the desired setting into the ADC Control Register. This must be done while the previous conversion is in progress, to ensure that the internal oscillator is running while the register is being written.

Following this sequence ensures that, when the desired setting is written into the ADC Control Register, it is actually latched and used by the control logic within the device.

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