June 1999
Revised March 2000

FSTU32160A
16-Bit to 32-Bit Multiplexer/Demultiplexer Bus Switch with −2V Undershoot Protection

General Description

The Fairchild Switch FSTU32160A is a 16-bit to 32-bit high-speed CMOS TTL-compatible multiplexer/demulti-plexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device can be used in applications where two buses need to be addressed simultaneously. The FSTU32160A is designed so that the A Port demultiplexes into B_1 or B_2 or both. The A and B Ports are "undershoot hardened" with UHC™ protection to support an extended range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit, UHC senses undershoot at the I/O's, and responds by preventing voltage differentials from developing and turning on the switch.

Two select (SEL_1, SEL_2) inputs provide switch enable con-trol. When SEL_1, SEL_2 are HIGH, the device precharges the B Port to a selectable bias voltage (Bias V) to minimize live insertion noise.

Features

■ Undershoot hardened to −2V (A and B Ports).

■ 4Ω switch connection between two ports.

■ Minimal propagation delay through the switch.

■ Low I_{CC}.

■ Zero bounce in flow-through mode.

■ Control inputs compatible with TTL level.

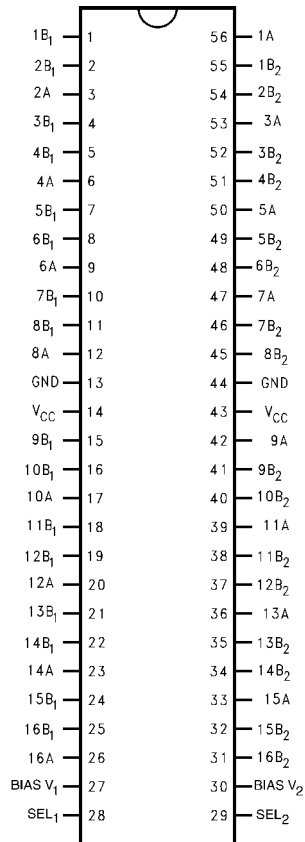■ See Applications Note AN-5008 for details

Ordering Code:

Order Number	Package Number	Package Description
FSTU32160AMTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

UHC™ is a trademark of Fairchild Semiconductor Corporation.

www.fairchildsemi.com

FSTU32160A

Connection Diagram

1B$_1$	1	56	1A
2B$_1$	2	55	1B$_2$
2A	3	54	2B$_2$
3B$_1$	4	53	3A
4B$_1$	5	52	3B$_2$
4A	6	51	4B$_2$
5B$_1$	7	50	5A
6B$_1$	8	49	5B$_2$
6A	9	48	6B$_2$
7B$_1$	10	47	7A
8B$_1$	11	46	7B$_2$
8A	12	45	8B$_2$
GND	13	44	GND
V$_{CC}$	14	43	V$_{CC}$
9B$_1$	15	42	9A
10B$_1$	16	41	9B$_2$
10A	17	40	10B$_2$
11B$_1$	18	39	11A
12B$_1$	19	38	11B$_2$
12A	20	37	12B$_2$
13B$_1$	21	36	13A
14B$_1$	22	35	13B$_2$
14A	23	34	14B$_2$
15B$_1$	24	33	15A
16B$_1$	25	32	15B$_2$
16A	26	31	16B$_2$
BIAS V$_1$	27	30	BIAS V$_2$
SEL$_1$	28	29	SEL$_2$

Pin Descriptions

Pin Name	Description
SEL$_1$, SEL$_2$	Select Inputs
A	Bus A
B$_1$, B$_2$	Bus B

Truth Table

Inputs		Function
SEL$_1$	SEL$_2$	
L	H	x A = x B$_1$
H	L	x A = x B$_2$
L	L	x A = x B$_1$ and x B$_2$
H	H	x B$_1$, x B$_2$ = BiasV

Logic Diagram
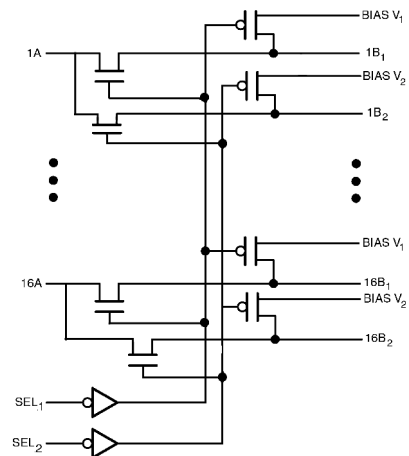
Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S) (Note 2)	−2.0V to +7.0V
BiasV Voltage Range	−0.5V to +7.0V
DC Input Control Pin Voltage	
(V_{IN}) (Note 3)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) $V_{IN} < 0V$	−50 mA
DC Output Current (I_{OUT})	128 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100 mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 4)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Precharge Supply (BiasV)	1.5 to V_{CC}
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	−40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: V_S is the voltage observed/applied at either the A or B Ports across the switch.

Note 3: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 4: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = -40 °C$ to $+85 °C$			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	$I_{IN} = -18mA$
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	μA	$0 \leq V_{IN} \leq 5.5V$
		0			10	μA	$V_{IN} = 5.5V$
I_O	Output Current	4.5	0.25			mA	BiasV = 2.4V $B_X = 0$
I_{OZH}, I_{OZL}	OFF-STATE Leakage Current	5.5			±1.0	μA	$0 \leq A \leq V_{CC}$, V $BiasV_1 = BiasV_2 = 5.5V$
I_{OZH}, I_{OZL}	OFF-STATE Leakage Current	5.5			±1.0	μA	$0 \leq B \leq V_{CC}$, V $BiasV_1 = BiasV_2 = Floating$
R_{ON}	Switch On Resistance (Note 6)	4.5		4	7	Ω	$V_{IN} = 0V$, $I_{IN} = 64$ mA
		4.5		4	7	Ω	$V_{IN} = 0V$, $I_{IN} = 30$ mA
		4.5		8	14	Ω	$V_{IN} = 2.4V$, $I_{IN} = 15$ mA
		4.0		11	20	Ω	$V_{IN} = 2.4V$, $I_{IN} = 15$ mA
I_{CC}	Quiescent Supply Current	5.5			3	μA	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND
I_{BIAS}	Bias Pin Leakage Current	5.5			±1.0	μA	SEL_1, $SEL_2 = 0V$ $B_X = 0V$, $BiasV_X = 5.5V$
V_{IKU}	Voltage Undershoot	5.5			−2.0	V	0.0 mA $\geq I_{IN} \geq -50$ mA SEL_1, $SEL_2 = 5.5V$

Note 5: Typical values are at $V_{CC} = 5.0V$ and $T_A = +25°C$

Note 6: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

| Symbol | Parameter | $T_A = -40\ °C$ to $+85\ °C$, $C_L = 50$ pF, RU= RD = 500Ω | | | | Units | Conditions | Figure No. |
| | | $V_{CC} = 4.5 - 5.5V$ | | $V_{CC} = 4.0V$ | | | | |
		Min	Max	Min	Max			
t_{PHL}, t_{PLH}	A or B, to B or A (Note 7)		0.25		0.25	ns	V_I = OPEN	Figure 2 Figure 3
t_{PZH}	Output Enable Time, SEL to A, B	0.5	4.0		4.5	ns	V_I = OPEN for t_{PZH} BiasV = GND	Figure 2 Figure 3
t_{PZL}	Output Enable Time, SEL to A, B	1.0	4.8		5.5	ns	V_I = 7V for t_{PZL} BiasV = 3V	Figure 2 Figure 3
t_{PHZ}	Output Disable Time, SEL to A, B	1.0	5.9		6.9	ns	V_I = Open for t_{PHZ} BiasV = GND	Figure 2 Figure 3
t_{PLZ}	Output Disable Time, SEL to A, B	1.0	7.4		7.0	ns	V_I = 7V for t_{PLZ} BiasV = 3V	Figure 2 Figure 3

Note 7: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 8)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	4		pF	V_{CC} = 5.0V
$C_{I/O\ OFF}$	Input/Output Capacitance "OFF State"	8		pF	V_{CC} = 5.0V, Switch OFF

Note 8: T_A = +25°C, f = 1 Mhz, Capacitance is characterized but not tested.

Undershoot Characteristic (Note 9)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OUTU}	Output Voltage During Undershoot	2.5	$V_{OH} - 0.3$		V	Figure 1

Note 9: This is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.
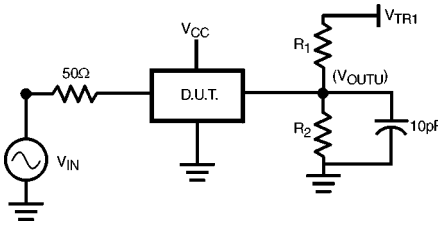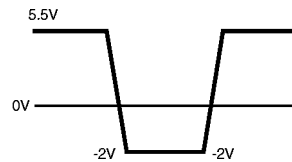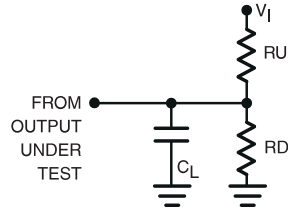

FIGURE 1.

Device Test Conditions

Parameter	Value	Units
V_{IN}	See Waveform	V
R_1 - R_2	100K	Ω
V_{TRI}	11.0	V
V_{CC}	5.5	V

Transient
Input Voltage (V_{IN}) Waveform

AC Loading and Waveforms

Note: Input driven by 50Ω source terminated in 50Ω

Note: C_L includes load and stray capacitance, C_L = 50 pF

Note: Input PRR = 1.0 MHz, t_W = 500 ns
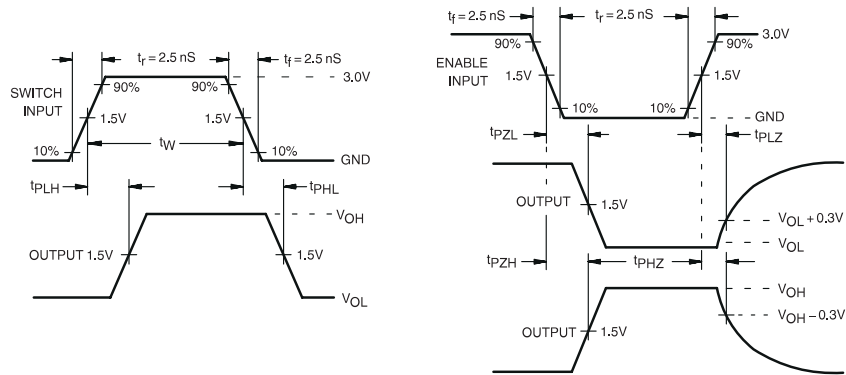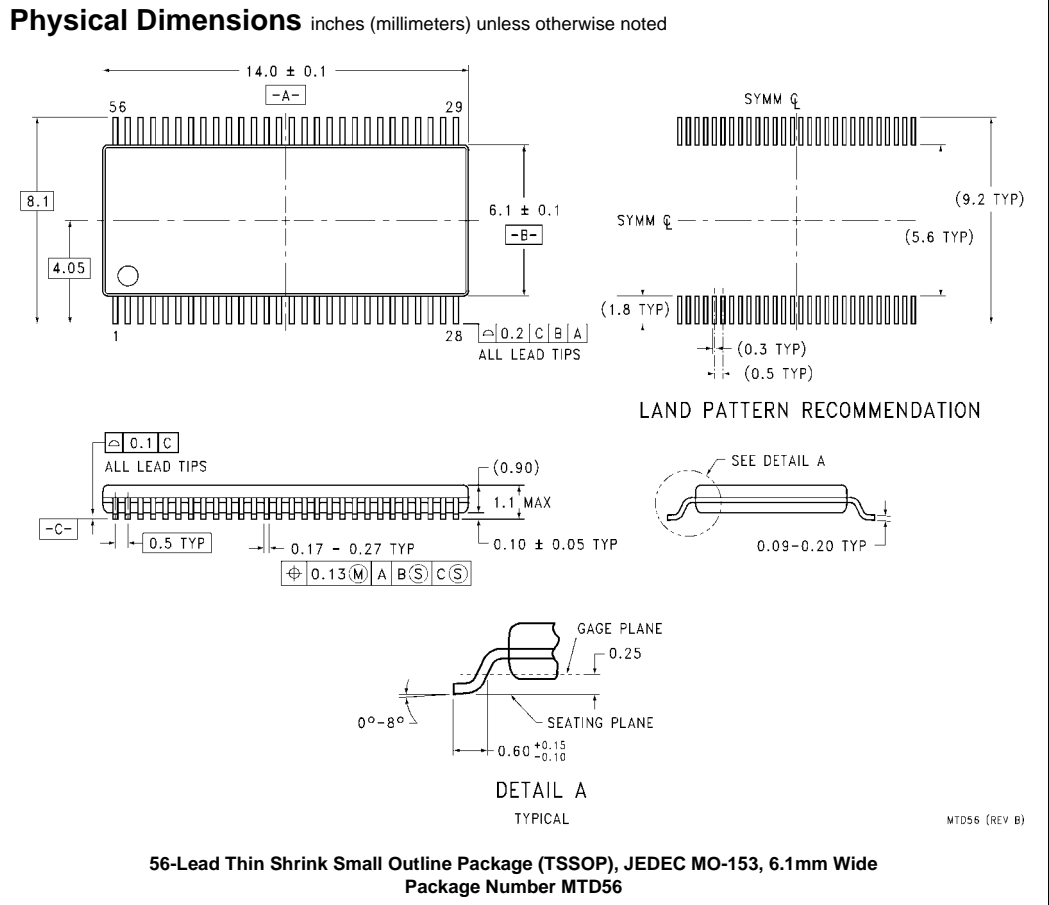
FIGURE 2. AC Test Circuit

FIGURE 3. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.