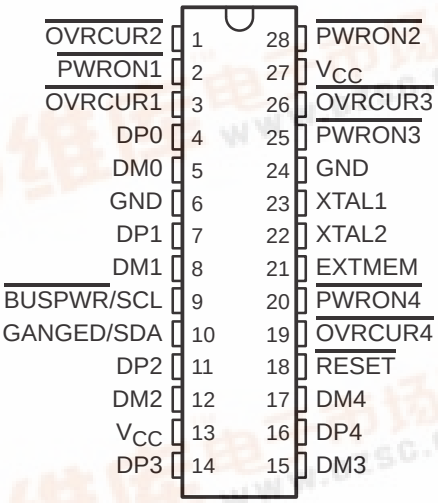
# TUSB2040A
# 4-PORT HUB FOR THE UNIVERSAL SERIAL BUS WITH OPTIONAL SERIAL EEPROM INTERFACE

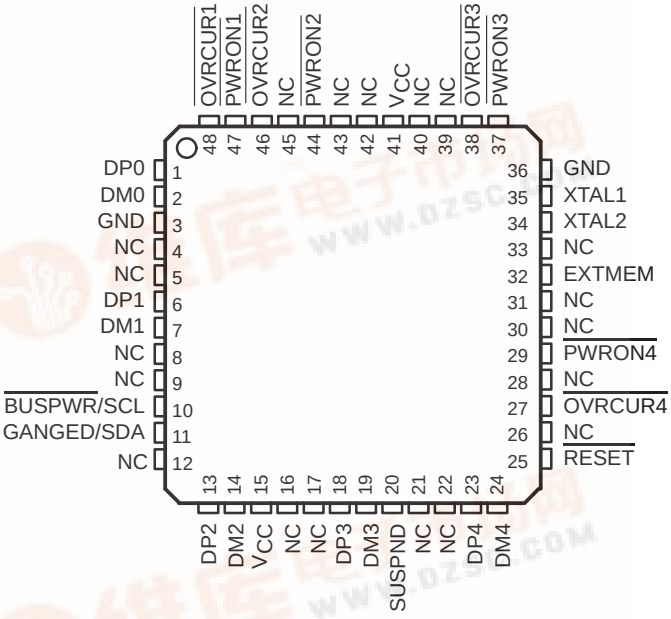
SLLS288B – FEBRUARY 1998 – REVISED MARCH 1998

- **Universal Serial Bus (USB) Version 1.0 Compliant**
- **Integrated USB Transceivers**
- **Four Downstream Ports**
- **Two Power Source Modes**
  - **Self-Powered Mode**
  - **Bus-Powered Mode**
- **Power Switching and Overcurrent Reporting is Provided Ganged or Per Port**
- **All Downstream Ports Support Full-Speed and Low-Speed Operations**
- **Supports Suspend and Resume Operations**
- **Pin-to-Pin Compatible with the TUSB2040 Device when EXTMEM Pin is Low**
- **Supports Programmable Vendor ID and Product ID With External Serial EEPROM**
- **Tri-State EEPROM Interface Allows EEPROM Sharing**
- **Available in 28-Pin DIP and 48-Pin TQFP Packages**
- **3.3-V Operation**

**N PACKAGE**
**(TOP VIEW)**




**PT PACKAGE**
**(TOP VIEW)**




† JEDEC descriptor S–PQFP–G for thin quad flatpack (TQFP)

## description

The TUSB2040A hub is a 3.3-V CMOS device that provides up to four downstream ports in compliance with the USB specification 1.0 version. Pin 21 (EXTMEM) enables or disables the EEPROM interface. When EXTMEM is low, the TUSB2040A is functionally equivalent to the TUSB2040 hub and the product ID (PID) displayed during enumeration is General Purpose USB Hub. For this configuration, pins 9 and 10 are the $\overline{\text{BUSPWR}}$ and GANGED input pins, respectively.

If programmable vendor ID(VID) and product ID(PID) descriptors are desired, pin 21 must be high (EXTMEM = 1) and a SGS Thompson M93C46 or equivalent EEPROM must be connected to pins 9 and 10. For this configuration, the values for $\overline{\text{BUSPWR}}$ and GANGED are stored in the EEPROM and pins 9 and 10 become the EEPROM interface.

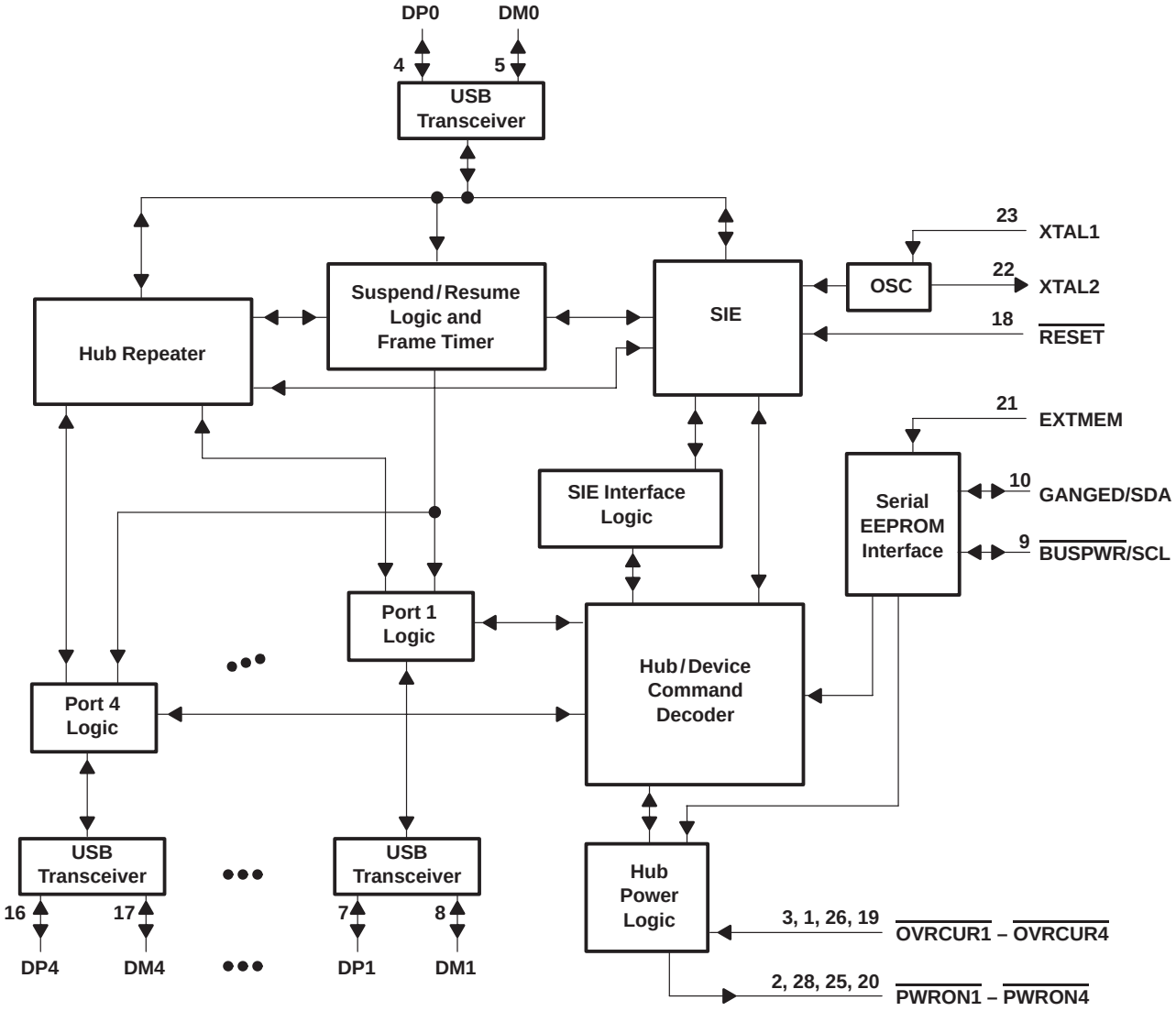
## description (continued)

The TUSB2040A supports bus-power and self-power modes. The power switching to the downstream ports can either be controlled individually or ganged using external devices to switch power and to detect overcurrent conditions. Outputs from the external power devices provide overcurrent inputs to the TUSB2040A $\overline{\text{OVRCUR}}$ pins and in the case of an overcurrent condition, the corresponding $\overline{\text{PWRON}}$ pins will be disabled by the TUSB2040A. In the GANGED operation, all $\overline{\text{PWRON}}$ signals transition simultaneously, and any $\overline{\text{OVRCUR}}$ input can be used.

The hub requires a 48-MHz clock signal to sample data from the upstream port and generate a synchronized 12-MHz USB clock signal. The hub supports the flexibility to use any device that generates a 48-MHz clock. Because the majority of oscillators are active devices, the low power suspend mode of the TUSB2040A will not function because there is no way to stop the oscillator from driving the internal clock. An oscillator with a TTL output not exceeding 3.6 V can be used by connecting its output to the XTAL1 terminal and leaving the XTAL2 terminal open. For crystal or resonator implementations, use the XTAL1 terminal as the input and the XTAL2 terminal as the feedback path. Because the crystal is required to resonate at 48 MHz, a tuning circuit as shown in Figure 8 may be required.

The upstream port and all downstream ports are USB-compliant transceivers. Every downstream port supports both full-speed and low-speed connections by automatically setting the slew rate according to the speed of the device attached to the port.

## functional block diagram




NOTE: Terminal numbers shown are for the N package.

## Terminal Functions

| TERMINAL NAME | TERMINAL N | TERMINAL PT | I/O | DESCRIPTION |
|---|---|---|---|---|
| $\overline{\text{BUSPWR}}$/SCL | 9 | 10 | I/O | Power source input/EEPROM serial clock. When EXTMEM is low, $\overline{\text{BUSPWR}}$/SCL is an active low input that indicates whether the ports and the hub derive power from the bus or the local supply. When EXTMEM is high, $\overline{\text{BUSPWR}}$/SCL acts as a tri-state serial clock output to the EEPROM with a 100 μA internal pulldown. This standard TTL input must not change dynamically during operation. |
| DM0 | 5 | 2 | I/O | Root port USB differential data minus. DM0 paired with DP0 constitutes the upstream USB port. |
| DM1 – DM4 | 8, 12, 15, 17 | 7, 14, 19, 24 | I/O | USB differential data minus. DM1 – DM4 paired with DP1 – DP4 support up to four downstream USB ports. |
| DP0 | 4 | 1 | I/O | Root port USB differential data plus. DP0 paired with DM0 constitutes the upstream USB port. |
| DP1 – DP4 | 7, 11, 14, 16 | 6, 13, 18, 23 | I/O | USB differential data plus. DP1 – DP4 paired with DM1 – DM4 support up to four downstream USB ports. |
| GANGED/SDA | 10 | 11 | I/O | Power switching and overcurrent detection mode/EEPROM serial data I/O. When EXTMEM is low, GANGED/SDA selects between gang or per port switching for the overcurrent detection of the downstream ports. When EXTMEM is high, GANGED/SDA acts as a tri-state serial data I/O to and from the EEPROM with a 100 μA internal pull-down. This standard TTL input must not change dynamically during operation. |
| GND | 6, 24 | 3, 36 | | Ground. GND terminals must be tied to ground for proper operation. |
| EXTMEM | 21 | 32 | I | EEPROM read enable. When EXTMEM is low, it disables the serial EEPROM interface of the device. Pins 9 and 10 are configured as $\overline{\text{BUSPWR}}$ and GANGED, respectively. When EXTMEM is high, it enables the serial EEPROM interface and pins 9 and 10 are configured as SCL and SDA, respectively. |
| $\overline{\text{OVRCUR1}}$ – $\overline{\text{OVRCUR4}}$ | 3, 1, 26, 19 | 48, 46, 38, 27 | I | Overcurrent indicators. $\overline{\text{OVRCUR1}}$ – $\overline{\text{OVRCUR4}}$ are active low, standard TTL inputs. One overcurrent indicator is available for each of the four downstream ports. In GANGED mode, one implementation is to tie these inputs together. Alternatively, one $\overline{\text{OVRCUR}}$ input pin may be used with the remaining $\overline{\text{OVRCUR}}$ pins tied to $V_{CC}$. |
| $\overline{\text{PWRON1}}$ – $\overline{\text{PWRON4}}$ | 2, 28, 25, 20 | 47, 44, 37, 29 | O | Power-on/-off control signals. $\overline{\text{PWRON1}}$ – $\overline{\text{PWRON4}}$ are active low, open-drain outputs. One power-on/-off control switch is used for each of the four downstream ports. In GANGED mode, all outputs are switched together. |
| $\overline{\text{RESET}}$ | 18 | 25 | I | Reset. $\overline{\text{RESET}}$ is an active low TTL input with hysteresis and must be asserted at power up. When $\overline{\text{RESET}}$ is asserted, it initializes all logic. |
| SUSPND | | 20 | O | Suspend status. SUSPND is an active high output that is available for external logic power down operations. During the SUSPEND mode, SUSPND is high. SUSPND is low for normal operation. |
| $V_{CC}$ | 13, 27 | 15, 41 | | 3.3-V supply voltage |
| XTAL1 | 23 | 35 | I | Crystal 1. XTAL1 is a 48-MHz crystal input with 50% duty cycle. Operation at 48-MHz is four times the USB full-speed bit rate of 12 Mbps. |
| XTAL2 | 22 | 34 | O | Crystal 2. XTAL2 is a 48-MHz crystal output. Operation at 48-MHz is four times the USB full-speed bit rate of 12 Mbps. This terminal is left open when using an oscillator. |

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . –0.5 V to 3.8 V
Input voltage range, $V_I$ . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$, ($V_I$ < 0 V or $V_I$ > $V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$, ($V_O$ < 0 V or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to GND.

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 3 | 3.3 | 3.6 | V |
| Input voltage, TTL/LVCMOS, $V_I$ | 0 | | $V_{CC}$ | V |
| Output voltage, TTL/LVCMOS, $V_O$ | 0 | | $V_{CC}$ | V |
| High-level input voltage, signal-ended receiver, $V_{IH(REC)}$ | 2 | | $V_{CC}$ | V |
| Low-level input voltage, signal-ended receiver, $V_{IL(REC)}$ | | | 0.8 | V |
| High-level input voltage, TTL/LVCMOS, $V_{IH(TTL)}$ | 2 | | $V_{CC}$ | V |
| Low-level input voltage, TTL/LVCMOS, $V_{IL(TTL)}$ | | | 0.8 | V |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |
| External series, differential driver resistor, $R_{(DRV)}$ | 22 (–5%) | | 22 (+5%) | Ω |
| Operating (dc differential driver) high speed mode, $f_{(OPRH)}$ | | | 12 | Mb/s |
| Operating (dc differential driver) low speed mode, $f_{(OPRL)}$ | | | 1.5 | Mb/s |
| Common mode, input range, differential receiver, $V_{(ICR)}$ | 0.8 | | 2.5 | V |
| Input transition times, $t_t$, TTL/LVCMOS | 0 | | 6 | ns |

## electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | USB data lines | $R_{(DRV)}$ = 15 kΩ, to GND | 2.8 | 3.6 | V |
| | | | $I_{OH}$ = –12 mA (without $R_{(DRV)}$) | $V_{CC}$ – 0.5 | | |
| $V_{OL}$ | Low-level output voltage | TTL/LVCMOS | $I_{OL}$ = 4 mA | | 0.5 | V |
| | | USB data lines | $R_{(DRV)}$ = 1.5 k Ω to 3.6 V | | 0.3 | |
| | | | $I_{OL}$ = 12 mA (without $R_{(DRV)}$) | | 0.5 | |
| $V_{IT+}$ | Positive input threshold voltage | TTL/LVCMOS | | | 2 | V |
| | | Single-ended | 0.8 V ≤ $V_{ICR}$ ≤ 2.5 V | | 1.8 | V |
| $V_{IT–}$ | Negative-input threshold voltage | TTL/LVCMOS | | 0.8 | | V |
| | | Single-ended | 0.8 V ≤ $V_{ICR}$ ≤ 2.5 V | 1 | | V |
| $V_{hys}$ | Input hysteresis† ($V_{T+} – V_{T–}$) | TTL/LVCMOS | | 0.25 | 0.7 | V |
| | | Single-ended | 0.8 V ≤ $V_{ICR}$ ≤ 2.5 V | 300 | 500 | mV |
| $I_{OZ}$ | High-impedance output current | TTL/LVCMOS | V = $V_{CC}$ or GND‡ | | ±10 | µA |
| | | USB data lines | 0 V ≤ $V_O$ ≤ $V_{CC}$ | | ±10 | µA |
| $I_{IL}$ | Low-level input current | TTL/LVCMOS | $V_I$ = GND | | –1 | µA |
| $I_{IH}$ | High-level input current | TTL/LVCMOS | $V_I$ = $V_{CC}$ | | 1 | µA |
| $z_{o(DRV)}$ | Driver output impedance | USB data lines | Static $V_{OH}$ or $V_{OL}$ | 7.1 | 19.9 | Ω |
| $V_{ID}$ | Differential input voltage | USB data lines | 0.8 V ≤ $V_{ICR}$ ≤ 2.5 V | 0.2 | | V |
| $I_{CC}$ | Input supply current | | Normal operation | | 100 | mA |
| | | | Suspend mode | | 1 | µA |

† Applies for input buffers with hysteresis
‡ Applies for open drain buffers

**differential driver switching characteristics over recommended ranges of operating free-air temperature and supply voltage, $C_L$ = 50 pF unless otherwise noted (see Figures 1 and 2)**

**full speed mode**

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_r$ | Transition rise time for DP or DM | See Figure 1 and Figure 2 | 4 | 20 | ns |
| $t_f$ | Transition fall time for DP or DM | See Figure 1 and Figure 2 | 4 | 20 | ns |
| $t_{(RFM)}$ | Rise/fall time matching | ($t_r$/$t_f$) x 100 | 90 | 110 | % |
| $V_{O(CRS)}$ | Signal crossover output voltage | | 1.3 | 2.0 | V |

**low speed mode**

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_r$ | Transition rise time for DP to DM | $C_L$ = 50 pF to 350 pF, | See Figure 1 and Figure 2 | 75 | 300 | ns |
| $t_f$ | Transition fall time for DP to DM | $C_L$ = 50 pF to 350 pF, | See Figure 1 and Figure 2 | 75 | 300 | ns |
| $t_{(RFM)}$ | Rise/fall time matching | ($t_r$/$t_f$) x 100 | | 80 | 120 | % |
| $V_{O(CRS)}$ | Signal crossover output voltage | $C_L$ = 50 pF to 350 pF | | 1.3 | 2.0 | V |

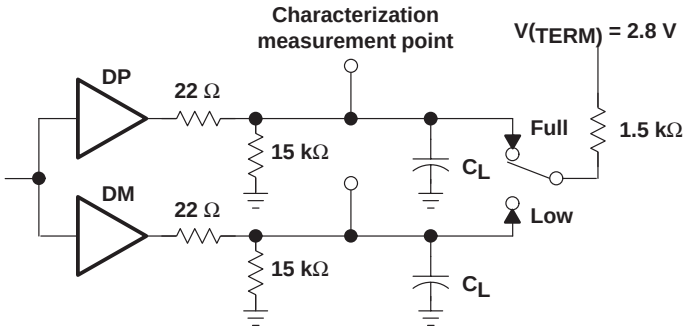



**Figure 1. Differential Driver Switching Load**

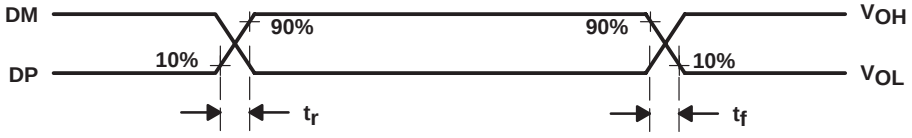



**Figure 2. Differential Driver Timing Waveforms**

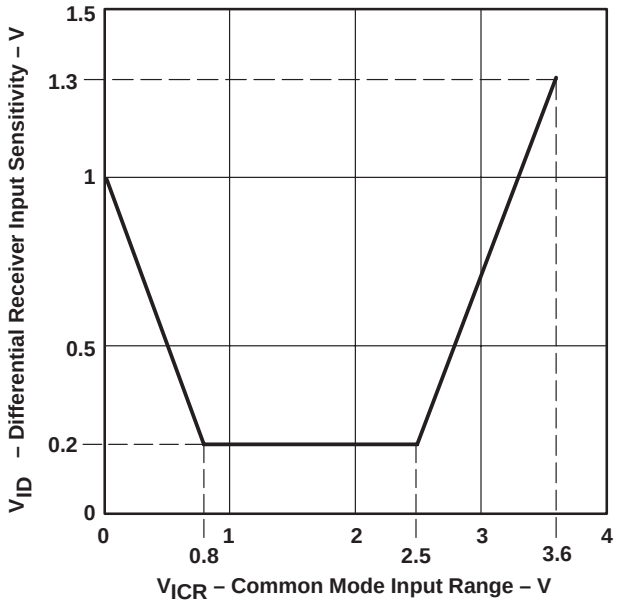



**Figure 3. Differential Receiver Input Sensitivity vs. Common Mode Input Range**

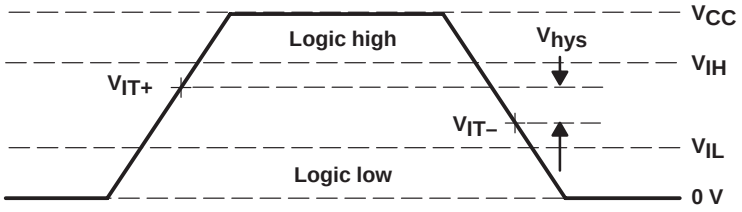



**Figure 4. Single-Ended Receiver Input Signal Parameter Definitions**

## APPLICATION INFORMATION

A major advantage of USB is the ability to connect 127 functions configured in up to six logical layers (tiers) to a single personal computer (see Figure 5).

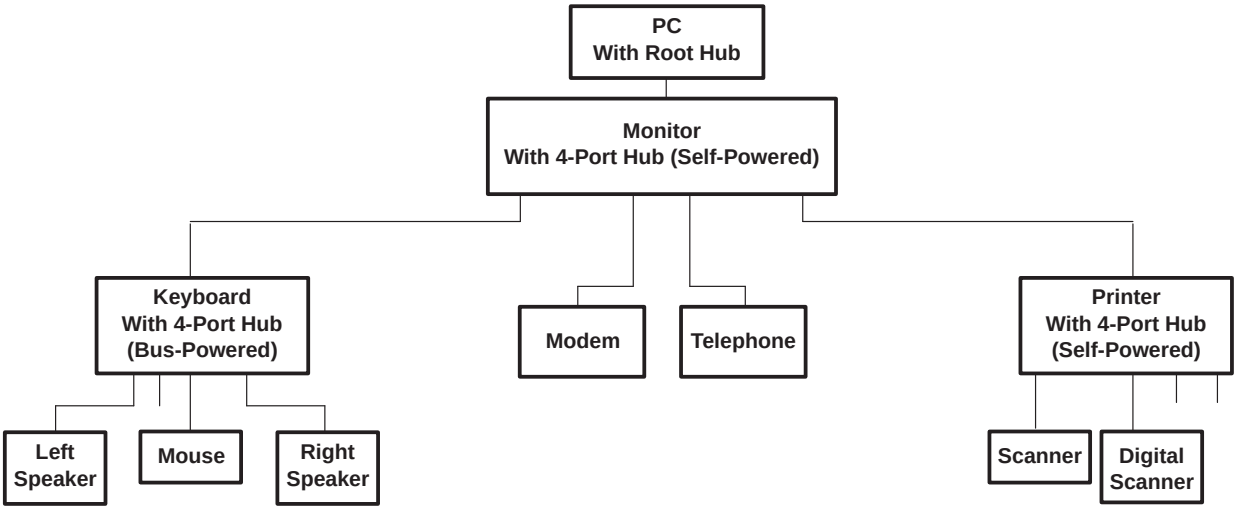



**Figure 5. USB Tiered Configuration Example**

Another advantage of USB is that all peripherals are connected using a standardized four wire cable that provides both communication and power distribution. The three power configurations are bus-powered, self-powered and high-powered modes. For all three configurations, 100 mA is the maximum current that may be drawn from the USB 5-V line during power up. For the bus-powered mode, a hub can draw a maximum of 500 mA from the 5-V line of the USB cable. A bus-powered hub must always be connected downstream to a self-powered hub unless it is the only hub connected to the PC and there are no high-powered functions connected downstream. In the self-powered mode, the hub is connected to its own power supply and can supply up to 500 mA to each downstream port. High-powered functions may draw a maximum of 500 mA and may only be connected downstream to self-powered hubs.

Both bus-powered and self-powered hubs require overcurrent protection for all downstream ports. The two types of protection are individual port management (individual port basis) or ganged port management (multiple port basis). Individual port management requires power management devices for each individual downstream port, but adds robustness to the USB system because, in the event of an overcurrent condition, the USB host powers down the port that has the condition. The ganged configuration uses fewer power management devices and thus has lower system costs, but in the event of an overcurrent condition on any of the downstream ports, all the ganged ports are disabled by the USB host.

Using a combination of the $\overline{\text{BUSPWR}}$ and GANGED inputs, the TUSB2040A supports four modes of power management: bus-powered hub with either individual port power management, or ganged port power management and the self-powered hub with either individual port power management, or ganged port power management. Texas Instruments supplies the complete hub solution because we offer this TUSB2040A, the TUSB2070 (7–port) and the TUSB2140A (4-port with $I^2C$) hubs along with the power management chips needed to implement a fully USB Specification 1.0 compliant system.

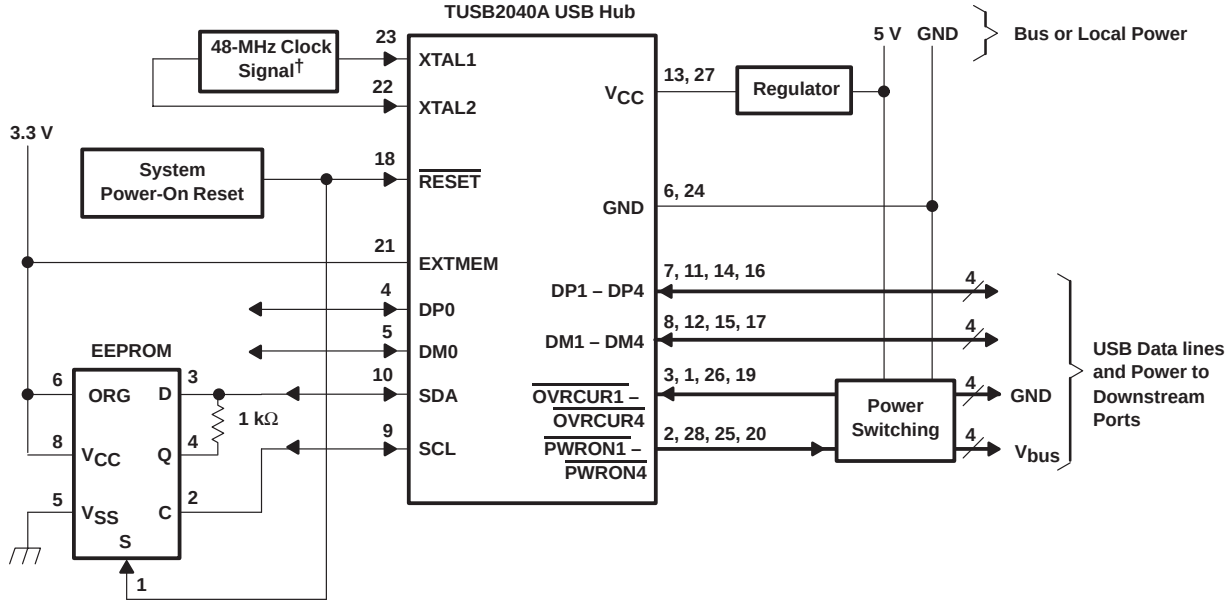
## APPLICATION INFORMATION

### USB design notes

The following sections provide block diagram examples of how to implement the TUSB2040A device. Please note, even though no resistors are shown, pull-up, pull-down and series resistors must still be used to properly implement this device. Figure 1 shows a few resistors that must be used for the USB lines, and for a general reference design, one is available on the TI USB web site.

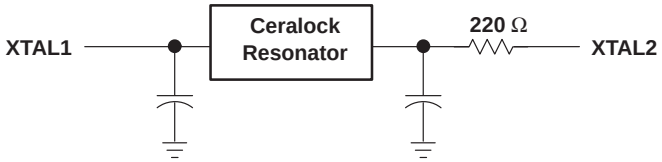
Figure 6 is a block diagram example of how to connect the external EEPROM if configurable Product ID and Vendor ID are desired. Please note that the pin numbers in Figure 6 are for the DIP package.

Figure 7 and 8 are examples of how to generate the 48-MHz clock signal. Figure 9 shows the EEPROM Read Operation Timing Diagram. Figures 10, 11 and 12 illustrate how to connect the TUSB2040A device for different power source and port power management combinations.




† Figures 7 and 8 are two examples of how to generate the 48-MHz clock signal.
‡ Pin numbers shown are for the N package.

**Figure 6. Typical Application of the TUSB2040 USB Hub**

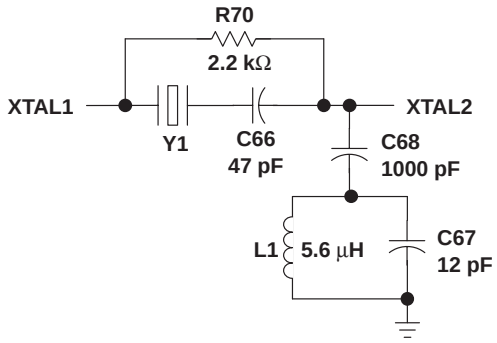



NOTE A: A simple way to achieve the required 48-MHz clock signal is to use a resonator such as the Ceralock™ resonator in Figure 7. MuRata Electronics, Inc. manufactures a surface mount version, P/N CSACV48.00MXJ040, and a dip version, P/N CSA48.00MXZ040. The 220 Ω resistor is used to tune the 48-MHz signal. The circuit functions properly without the capacitors, but in order to decrease EMI emissions, the capacitors are used to decrease the amplitude of the signal. The exact values of the capacitors are dependent on the capacitance of the board layout. Increasing the capacitance decreases the amplitude of the clock signal. For the 4-layer PCB tested, 22 pF capacitors were used. If the capacitors are too large, the amplitude of the clock signal will not be large enough for the successful numeration of the TUSB2040A by the USB host.

**Figure 7. Resonator Clock Circuit**

Ceralock is a trademark of MuRata Electronics Incorporated

## APPLICATION INFORMATION




NOTE B: This application shows a third harmonic 48-Mhz crystal, P/N HC-18/U 48-MHz, manufactured by US Crystal, Inc. Since the first harmonic of most crystals is not 48-MHz, a tuning circuit such as this must be used to tune the crystal to the required 48-MHz clock signal. When tuning the crystal (Y1) for different board implementations, the capacitor (C67) and the resistor (R70) are subject to change and the other components should remain the same.

**Figure 8. Crystal Tuning Circuit**

### programming the EEPROM

An SGS Thompson M93C46 EEPROM or equivalent is used for storing the programmable VID and PID. When the EEPROM interface is enabled (EXTMEM = 1), the SCL and SDA are internally pulled down (100 μA) inside the TUSB2040A. However, in low-power suspend mode, the $\overline{\text{BUSPWR}}$/SCL pin must be externally pulled down because the internal pulldowns are disabled. The internal pulldowns are also disabled when the EEPROM interface is disabled (EXTMEM = 0).

The EEPROM is programmed with the three 16-bit locations as shown in Table 1. Connecting pin 6 of the EEPROM high (ORG = 1) organizes the EEPROM memory into 64×16 bit words.

**Table 1. EEPROM Memory Map**

| ADDRESS | D15 | D14 | D13 | D12–D8 | D7–D0 |
|---|---|---|---|---|---|
| 00000 | 0 | GANGED | $\overline{\text{BUSPWR}}$ | 00000 | 00000000 |
| 00001 | VID High-byte | | | | VID Low-byte |
| 00010 | PID High-byte | | | | PID Low-byte |
| | XXXXXXXX | | | | |

The D and Q signals of the EEPROM must be tied together using a 1 kΩ resistor with the common I/O operations forming a single-wire bus. After system power-on reset, the TUSB2040A performs a one-time access read operation from the EEPROM if the EXTMEM pin is pulled high and the chip select of the EEPROM is connected to the system power-on reset. Initially, the SDA pin will be driven by the TUSB2040A to send a start bit (1) which is followed by the read instruction (10) and the starting-word address (00000). Once the read instruction is received, the instruction and address are decoded by the EEPROM, which then sends the data to the output shift register. At this point, the hub stops driving the SDA pin and the EEPROM starts driving. A dummy (0) bit is then output and the first three 16-bit words in the EEPROM are output with the most significant bit (MSB) first.

The output data changes are triggered by the rising edge of the clock provided by the TUSB2040A on the SCL pin. The *SGS-Thompson M936C46* EEPROM is recommended because it advances to the next memory location by automatically incrementing the address internally. Any EEPROM used must have the automatic internal address advance function. After reading the three words of data from the EEPROM, the TUSB2040A puts the EEPROM interface into a high-impedance condition (pulled down internally) to allow other logic to share the EEPROM. The EEPROM read operation is summarized in Figure 9. For more details on EEPROM operation, refer to *SGS-Thompson Microelectronics M93C46 Serial Microwire Bus EEPROM* data sheet.

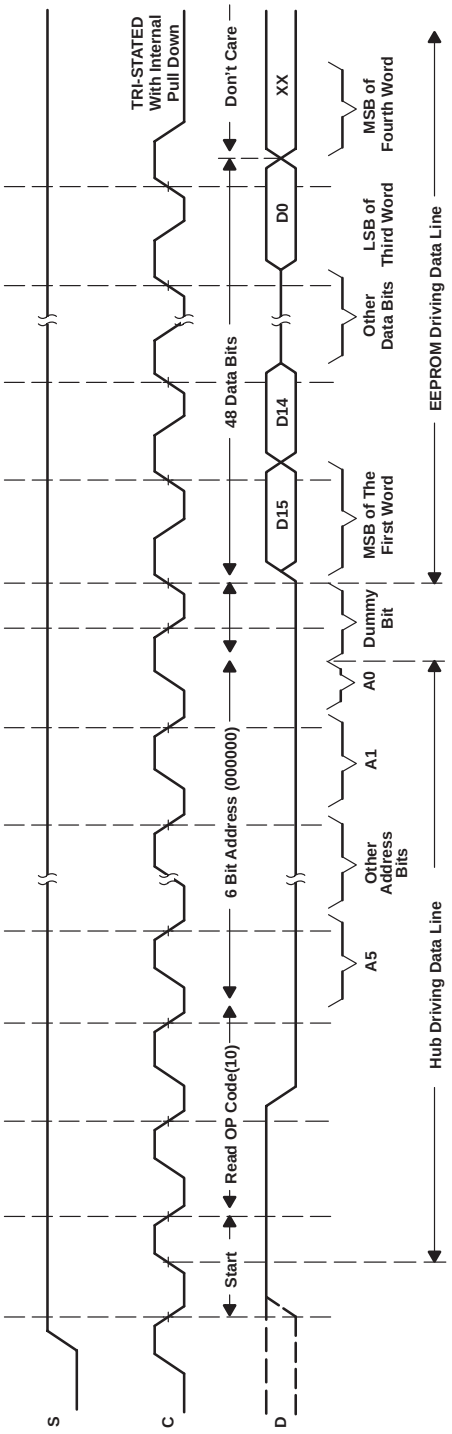
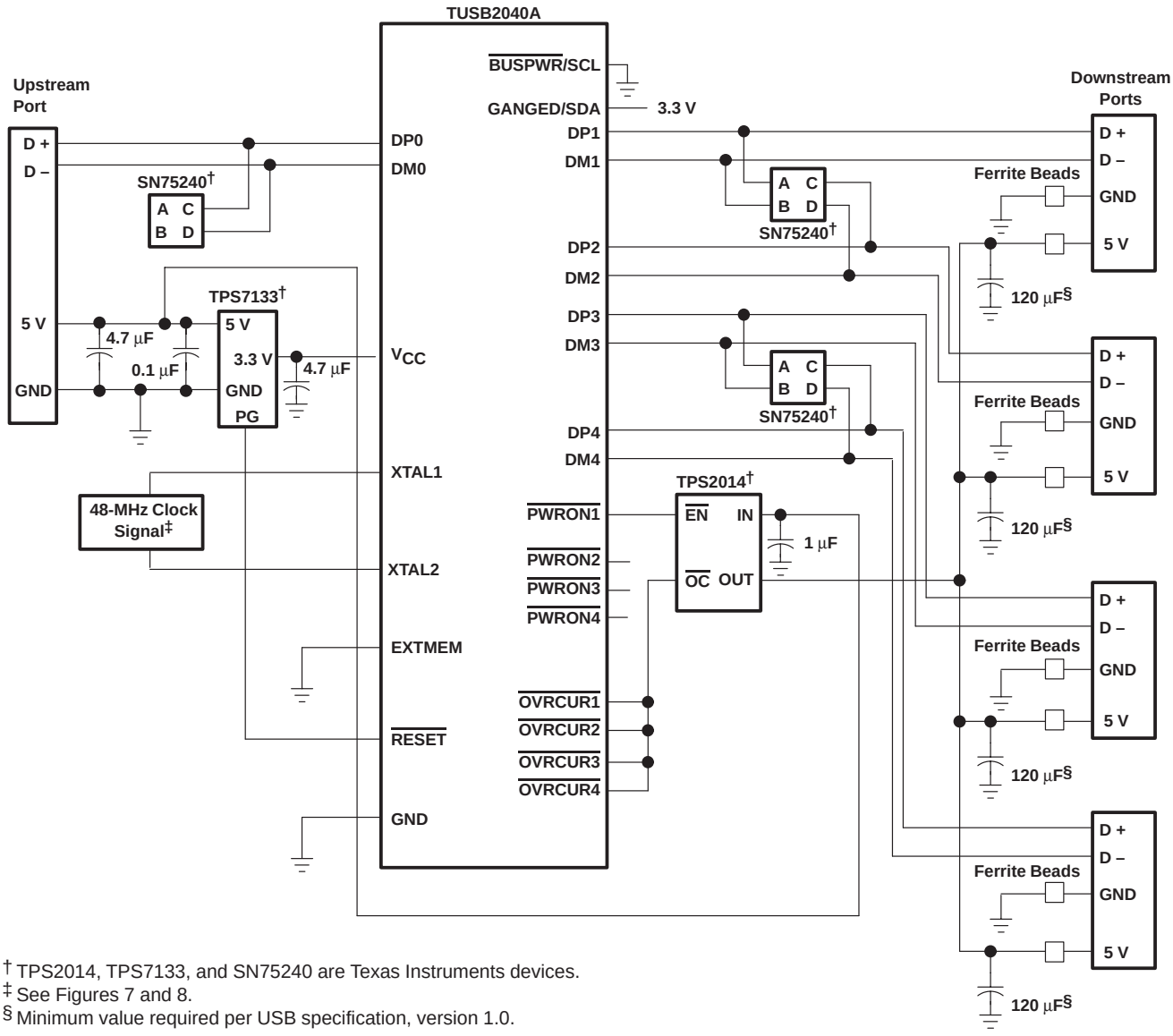



**Figure 9. EEPROM Read Operation Timing Diagram**

## APPLICATION INFORMATION

### bus-powered hub, ganged port power management

A bus-powered TUSB2040A supports up to four downstream ports and is capable of supplying 100 mA of current for low-power device class functions to each downstream port. Bus-powered hubs must implement power switching. Ganged power management (see Figure 10) utilizes the TPS2014 power switch device and provides overcurrent protection for downstream ports. Individual SN75240 transient suppressors reduce in-rush current and voltage spikes. The TPS7133 low-dropout voltage regulator provides a power good (PG) signal for reset at power up. $\overline{\text{OVRCUR1}}$ – $\overline{\text{OVRCUR4}}$ inputs can be tied together for ganged mode operation.



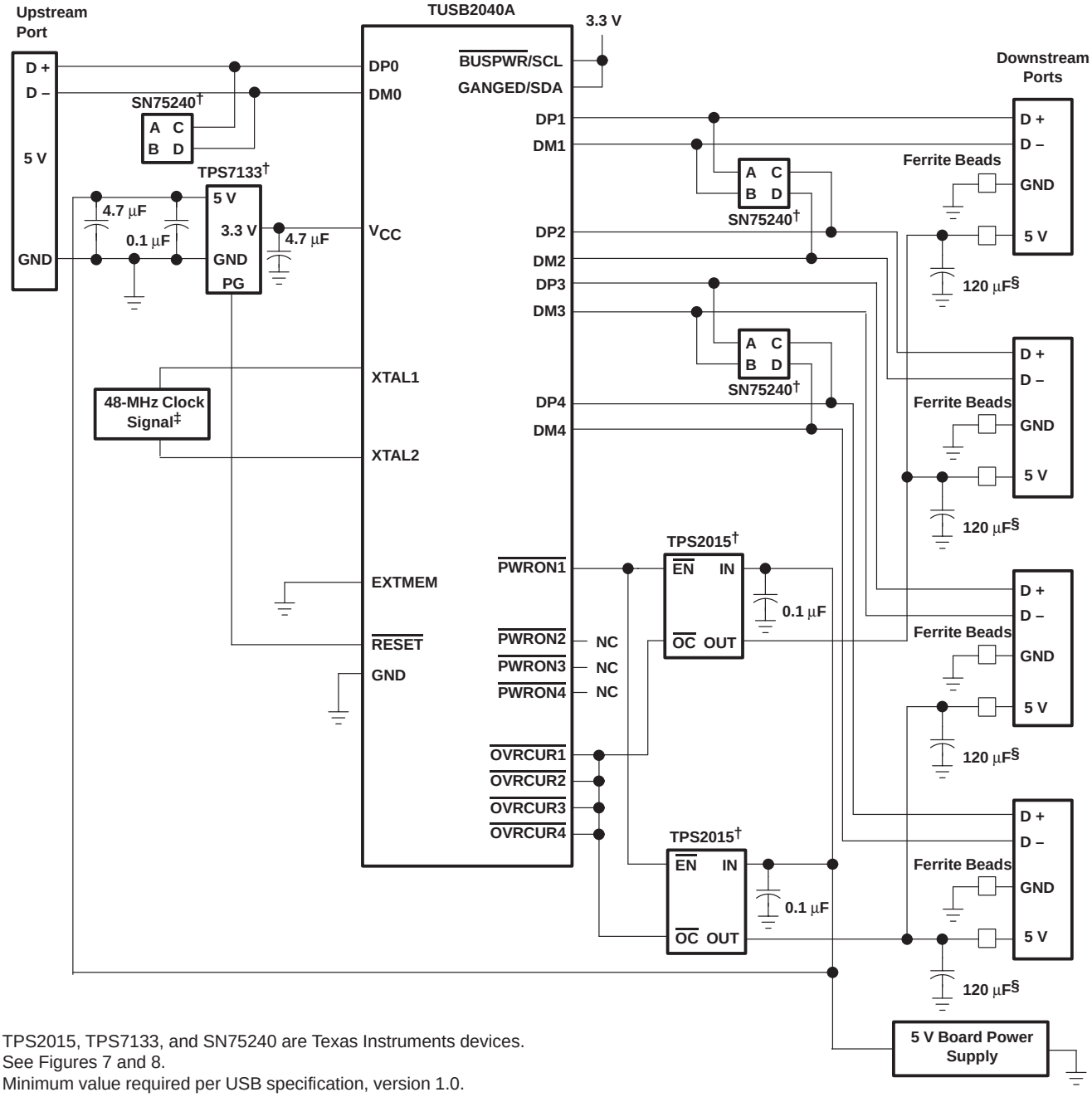

† TPS2014, TPS7133, and SN75240 are Texas Instruments devices.
‡ See Figures 7 and 8.
§ Minimum value required per USB specification, version 1.0.

**Figure 10. TUSB2040A Bus-Powered Hub, Ganged Port Power Management Application**

## APPLICATION INFORMATION

### self-powered hub, ganged port power management

A self-powered TUSB2040A can also be implemented using ganged port power management (see Figure 11). This implementation is similar to the individual power management except one TPS2015 provides power switching and overcurrent protection for two ports. Although this is a more economical solution, a fault on one downstream port causes power to be removed from both downstream ports.



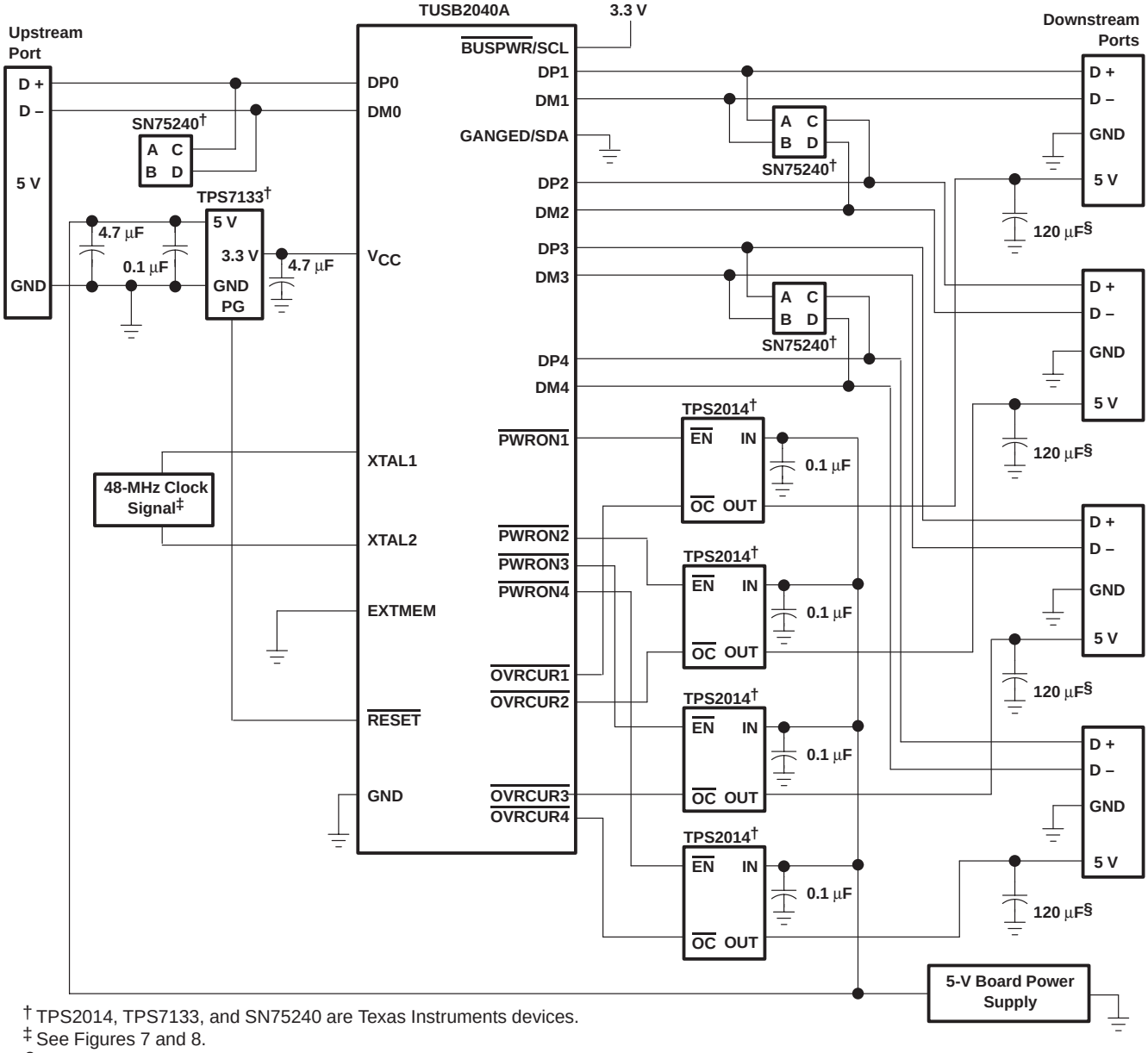

† TPS2015, TPS7133, and SN75240 are Texas Instruments devices.
‡ See Figures 7 and 8.
§ Minimum value required per USB specification, version 1.0.

**Figure 11. TUSB2040A Self-Powered Hub, Ganged Port Power Management**

## APPLICATION INFORMATION

### self-powered hub, individual port power management

A self-powered TUSB2040A is capable of supplying 500 mA of current for low-power or high-power device class functions to each downstream port. Self-powered hubs are required to implement overcurrent protection. Individual port-power management (see Figure 12) utilizes the TPS2014 power switching and overcurrent protection that provide maximum robustness to the hub system. When the hub detects a downstream port fault, power is removed from the faulty port only, thus allowing other ports to continue normal operation. Individual SN75240 transient suppressors reduce in-rush current and voltage spikes. The TPS7133 low-dropout regulator provides a power good (PG) signal for reset at power up.



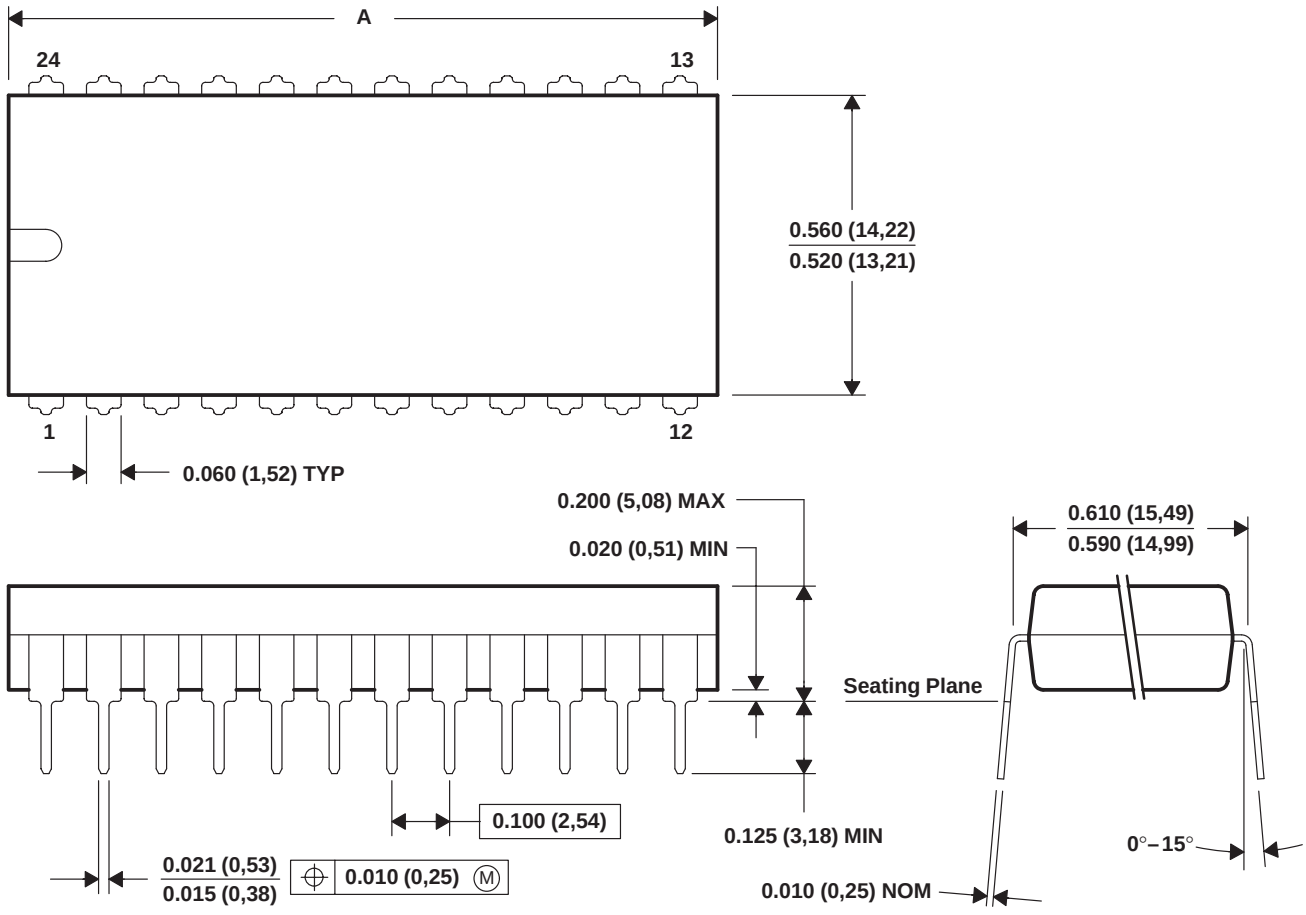

† TPS2014, TPS7133, and SN75240 are Texas Instruments devices.
‡ See Figures 7 and 8.
§ Minimum value required per USB specification, version 1.0.

**Figure 12. TUSB2040A Self-Powered Hub, Individual Port-Power Management Application**

## MECHANICAL DATA

**N (R-PDIP-T**)** **PLASTIC DUAL-IN-LINE PACKAGE**

**24 PIN SHOWN**



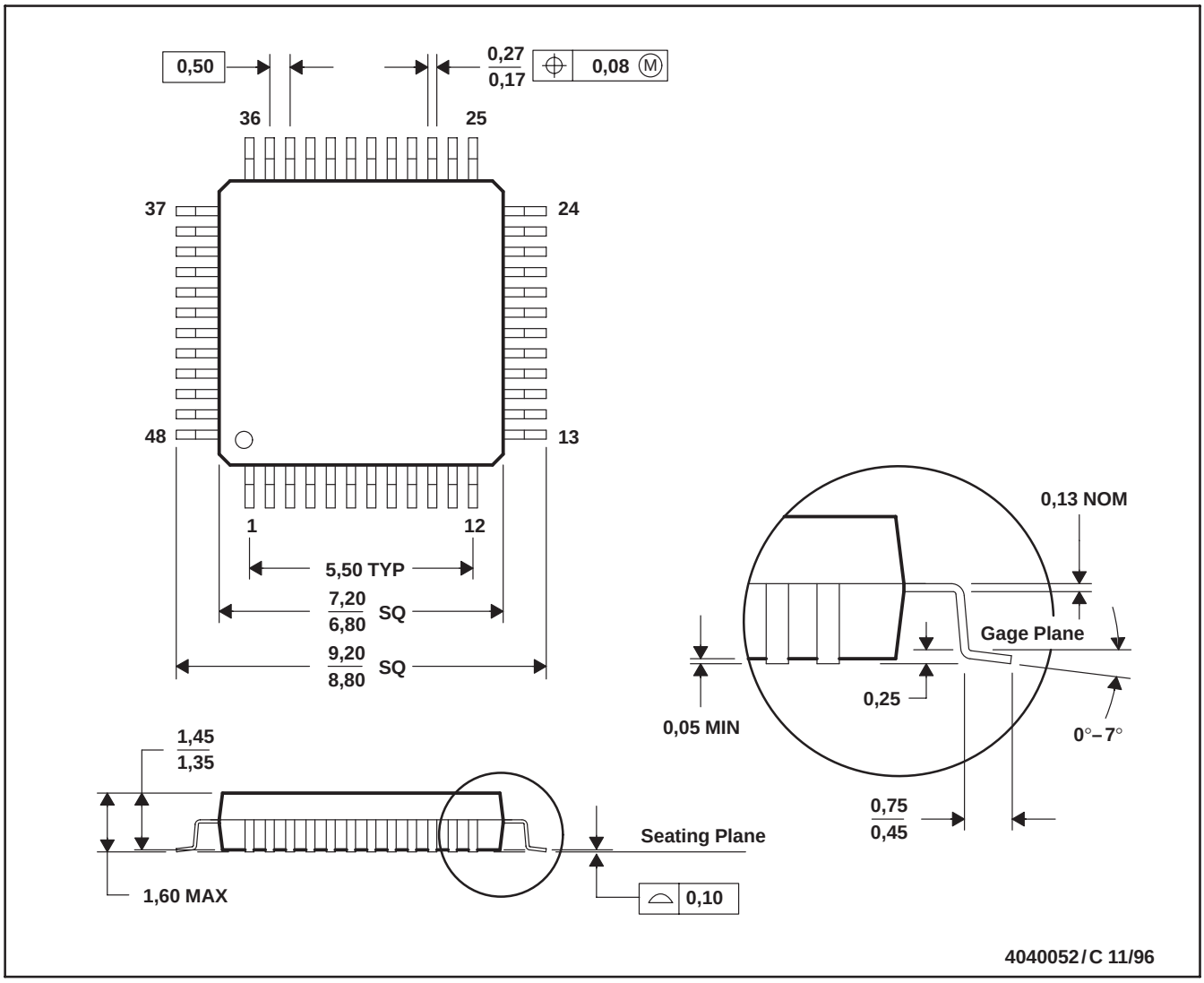

| DIM \ PINS ** | 24 | 28 | 32 | 40 | 48 | 52 |
|---|---|---|---|---|---|---|
| A MAX | 1.270 (32,26) | 1.450 (36,83) | 1.650 (41,91) | 2.090 (53,09) | 2.450 (62,23) | 2.650 (67,31) |
| A MIN | 1.230 (31,24) | 1.410 (35,81) | 1.610 (40,89) | 2.040 (51,82) | 2.390 (60,71) | 2.590 (65,79) |

**4040053/B 04/95**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32-pin only)

## MECHANICAL DATA

**PT (S-PQFP-G48)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

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