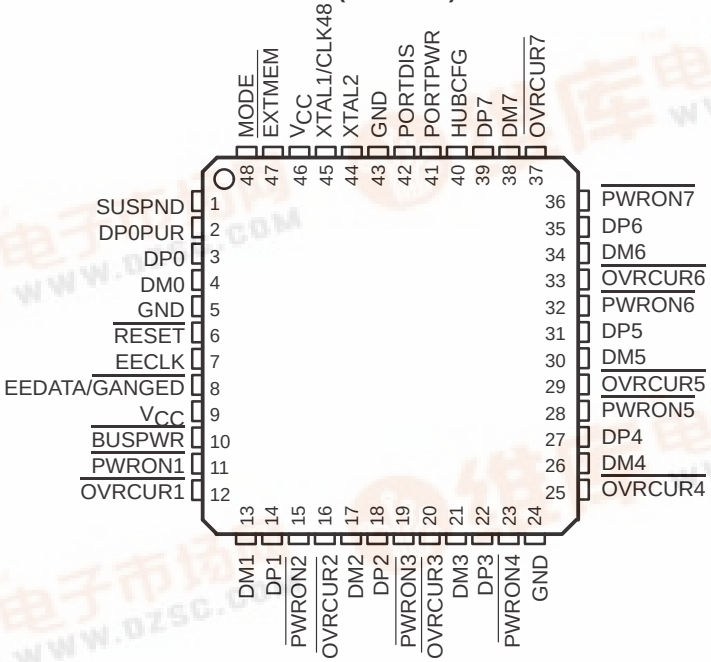
TUSB2077A
7-PORT HUB FOR THE UNIVERSAL SERIAL BUS WITH OPTIONAL SERIAL EEPROM INTERFACE

SLLS414 – MARCH 2000

- Universal Serial Bus (USB) Version 1.1 Compliant
- Integrated USB Transceivers
- 3.3-V Low Power ASIC Logic
- Two Power Source Modes
  - Self-powered Mode Supporting Seven Downstream Ports
  - Bus-powered Mode Supporting Four Downstream Ports
- All Downstream Ports Support Full-Speed and Low-Speed Operations
- Power Switching and Overcurrent Reporting is Provided Per Port or Ganged
- Supports Suspend and Resume Operations
- Suspend Status Terminal Avaliable for External Logic Power Down
- Supports Custom Vendor ID and Product ID With External Serial EEPROM
- 3-State EEPROM Interface to Allow EEPROM Sharing
- Push-Pull Outputs for $\overline{\text{PWRON}}$ Eliminate the Need for External Pullup Resistors
- Noise Filtering on $\overline{\text{OVRCUR}}$ Provides Immunity to Voltage Spikes
- Supports 6-MHz Operation Through Crystal Input or 48-MHz Input Clock
- New Functional Pins Introduced to Reduce the Board Material Cost
  - 3 LED Indicator Control Outputs Enable Visualized Monitoring of 6 Different Hub/Port Status (HUBCFG, PORTPWR, PORTDIS)
  - Output Pin Available to Disable External Pullup Resistor on DP0 for 15 ms After Reset or After Change on $\overline{\text{BUSPWR}}$ and Enable Easy Implementation of On-Board Bus/Self Power Dynamic Switching Circuitry
- Available in 48-Pin LQFP† Package

PT PACKAGE
(TOP VIEW)



NC – No internal connection

† JEDEC descriptor S–PQFP–G for low-profile quad flatpack (LQFP)

description

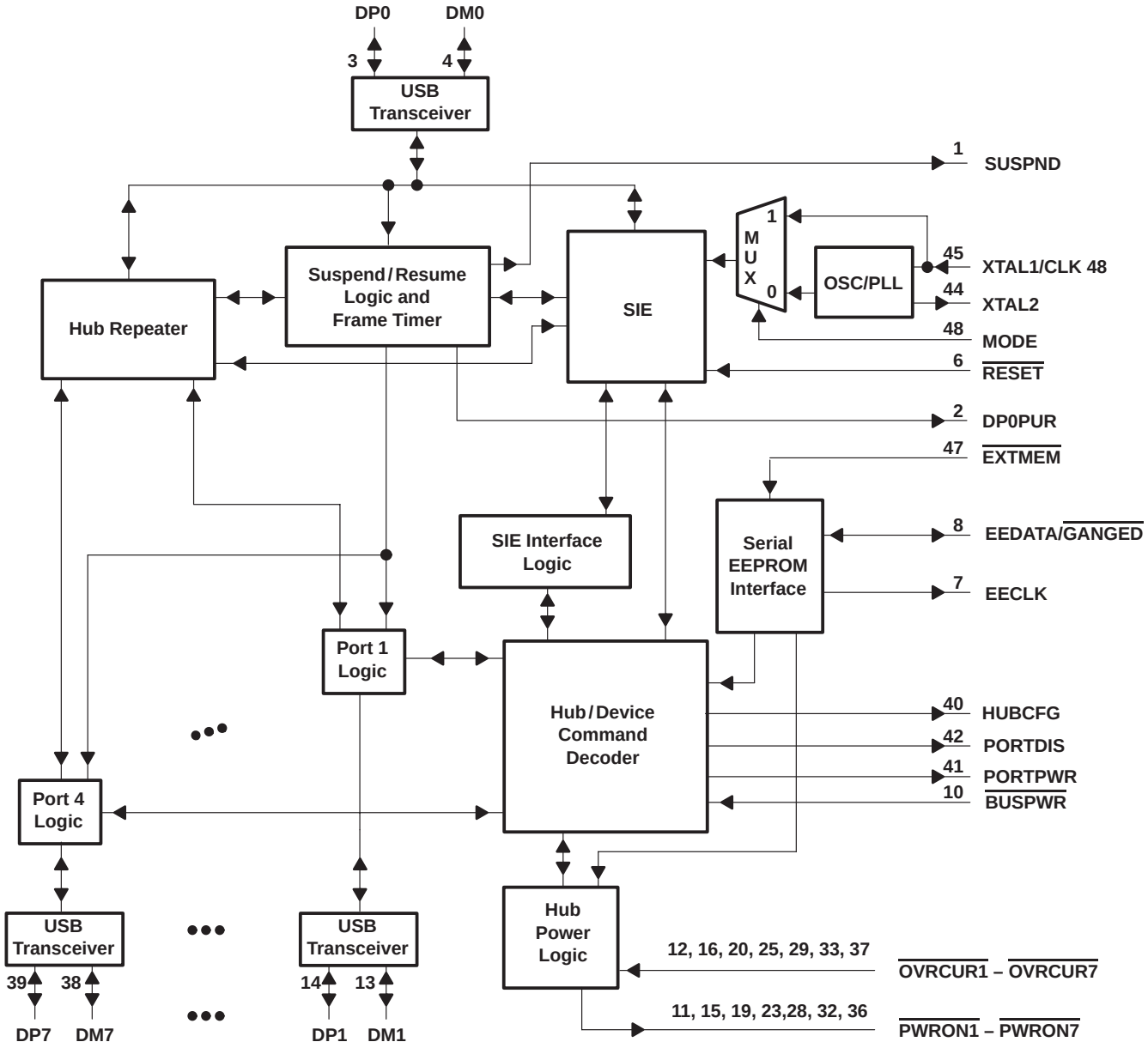
The TUSB2077A hub is a 3.3-V CMOS device that provides up to seven down stream ports in compliance with the USB version 1.1 specification. Because this device is implemented with a digital state machine instead of a microcontroller, no software programming is required. Fully compliant USB transceivers are integrated into the ASIC for all upstream and downstream ports. The downstream ports support both full-speed and low-speed devices by automatically setting the slew rate according to the speed of the device attached to the ports. The configuration of the $\overline{\text{BUSPWR}}$ terminal selects either the bus-powered or the self-powered mode. The introduction of the DP0 pull-up resistor disable pin, DP0PUR, makes it much easier to implement an on-board bus/self-power dynamic-switching circuitry. The three LED indicator control output pins also enable the implementation of visualized status monitoring of the hub and its downstream ports. With these new function pins, the end equipment vendor can considerably reduce the total board cost while adding additional product value.

The $\overline{\text{EXTMEM}}$ (Pin 47) enables or disables the optional EEPROM interface. When $\overline{\text{EXTMEM}}$ is high, the vendor and product IDs (VID and PID) use defaults, such that the message displayed during enumeration is *General Purpose USB Hub*. For this configuration, pin 8 functions as the $\overline{\text{GANGED}}$ input pin and the EECLK (Pin 7) is unused. If custom VID and PID descriptors are desired, the $\overline{\text{EXTMEM}}$ must be tied low ($\overline{\text{EXTMEM}}$ = 0) and a SGS Thompson M93C46 or equivalent EEPROM must be used to store the programmable VID, PID and $\overline{\text{GANGED}}$ value. For this configuration, pin 7 and pin 8 function as the EEPROM interface signals with pin 7 as EECLK and pin 8 as EEDATA respectively.

The TUSB2077A supports both bus-powered and self-powered modes. External power management devices such as the TPS2044 are required to control the 5 V-power source switching (on/off) to the downstream ports and detect over-current condition from the downstream ports individually or ganged. Outputs from external power devices provide over-current inputs to the TUSB2077A $\overline{\text{OVRCUR}}$ pins in case of an over-current condition, the corresponding $\overline{\text{PWRON}}$ pins will be disabled by the TUSB2077A. In the ganged mode, all $\overline{\text{PWRON}}$ signals transitions simultaneously, and any $\overline{\text{OVRCUR}}$ input can be used. In the nonganged mode, the $\overline{\text{PWROR}}$ outputs and $\overline{\text{OVRCUR}}$ inputs operate on a per port basis.

The TUSB2077A provides the flexibility of using either a 6-MHz or a 48-MHz clock. The logic level of the MODE terminal controls the selection of the clock source. When MODE is low, the output of the internal APLL circuitry is selected to drive the internal core of the chip. When MODE is high, the XTAL1 input is selected as the input clock source and the APLL circuitry is powered down and bypassed. The internal oscillator cell is also powered down while MODE is high. For 6-MHz operation, TUSB2077A requires a 6-MHz clock signal on XTAL1 pin (with XTAL2 for a crystal) from which its internal APLL circuitry generates a 48 MHz internal clock to sample the data from the upstream port. For 48-MHz operation, the clock cannot be generated with a crystal, using the XTAL2 output, since the internal oscillator cell only supports fundamental frequency. If low power suspend and resume are desired, a passive crystal or resonator must be used, although the hub supports the flexibility of using any device that generates a 6-MHz clock. Because most oscillators cannot be stopped while power is on, their use prohibits low-power suspend, which depends on disabling the clock. When the oscillator is used, by connecting its output to XTAL1 terminal and leaving XTAL2 terminal open, its TTL output level can not exceed 3.6 V. If a 6 MHz oscillator is used, it must be stopped at logic low whenever SUSPND is high. For crystal or resonator implementations, the XTAL1 terminal is the input and the XTAL2 terminal is used as the feedback path. A sample crystal tuning circuit is shown in Figure 7.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BUSPWR	10	I	Power source indicator. BUSPWR is an active low input that indicates whether the downstream ports source their power from the USB cable or a local power supply. For the bus-power mode, this pin should be pulled low, and for the self–powered mode, this pin should be pulled to 3.3 V. Input must not change dynamically during operation.
DM0	4	I/O	Root port USB differential data minus. DM0 paired with DP0 constitutes the upstream USB port.
DM1 – DM7	13, 17, 21, 26, 30, 34, 38	I/O	USB differential data minus. DM1 – DM7 paired with DP1 – DP7 support up to seven downstream USB ports.
DP0	3	I/O	Root port USB differential data plus. DP0 paired with DM0 constitutes the upstream USB port.
DP1 – DP7	14, 18, 22, 27, 31, 35, 39	I/O	USB differential data plus. DP1 – DP7 paired with DM1 – DM7 support up to seven downstream USB ports.
DP0PUR	2	O	Pull-up resistor connection. When a system reset happens (RESET being driven to low, but not USB reset) or any logic level change on BUSPWR terminal, DP0PUR output is inactive (floating) until the internal counter reaches a 15 ms time period. After the counter expires, DP0PUR is driven to the V_{CC} (3.3 V) level thereafter until the next system reset event occurs or there is a BUSPWR logic level change.
EECLK	7	O	EEPROM serial clock. When EXTMEM is high, the EEPROM interface is disabled. The EECLK pin is disabled and should be left floating (unconnected). When EXTMEM is low, EECLK acts as a 3-state serial clock output to the EEPROM with a 100 μA internal pulldown.
EEDATA/ GANGED	8	I/O	EEPROM serial data/power management mode indicator. When EXTMEM is low, EEDATA/ GANGED acts as a serial data I/O for the EEPROM and is internally pulled down with a 100 μA pulldown. When EXTMEM is high, EEDATA/GANGED selects between gang or per port power over–current detection for the downstream ports. This standard TTL input must not change dynamically during operation.
EXTMEM	47	I	EEPROM read enable. When EXTMEM is high, the serial EEPROM interface of the device is disabled. When EXTMEM is low, terminals 7 and 8 are configured as the clock and data pins of the serial EEPROM interface, respectively.
GND	5, 24, 43		Ground. GND terminals must be tied to ground for proper operation.
HUBCFG†	40	O	Hub configured. Used to control LED indicator. When the hub is configured, HUBCFG is high, which can be used to turn on a green LED. When the hub is not configured, HUBCFG is low, which can be used to turn on a red LED.
MODE	48	I	Mode select. When MODE is low, the APLL output clock is selected as the clock source to drive the internal core of the chip and 6-MHz crystal or oscillator can used. When MODE is high, the clock on XTAL1/CLK48 is selected as the clock source and 48-MHz oscillator or other on-board clock source can be used.
OVRCUR1 – OVRCUR7	12, 16, 20, 25, 29, 33, 37	I	Over-current input. OVRCUR1 – OVRCUR7 are active low. For per-port over current detection, one over-current input is available for each of the seven downstream ports. In the ganged mode, any OVRCUR input may be used and all OVRCUR pins should be tied together. OVRCUR pins have noise filtering logic.
PORTPWR†	41	O	Any port powered. Used to control LED indicator. When any port is powered on, PORTPWR is high, which can be used to turn on a green LED. When all ports are off, PORTPWR is low, which can be used to turn on a red LED.
PORTDIS†	42	O	No ports disabled. PORTDIS is used for LED indicator control. When no port is disabled, PORTDIS is high, which can be used to turn on a green LED. When any port is disabled, PORTDIS is low, which can be used to turn on a red LED.
PWRON1 – PWRON7	11, 15, 19, 23, 28, 32, 36	O	Power-on/-off control signals. PWRON1 – PWRON7 are active low, push-pull outputs that enables the external power switch device. Push-pull outputs eliminate the pull-up resistors which are required by for open-drain outputs. However, the external power switches that connect to these pins must be able to operate with 3.3-V inputs because these outputs cannot drive 5-V signals.
RESET	6	I	Reset. RESET is an active low TTL input with hysteresis and must be asserted at power up. When RESET is asserted, all logic is initialized. Generally, a reset with a pulse width between 100 μs and 1 ms is recommended after 3.3-V V_{CC} reaching its 90%. The clock signal must be active during the last 60 μs of the reset window.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
SUSPND	1	O	Suspend status. SUSPND is an active high output available for external logic power down operations. During the SUSPEND mode, SUSPND is high. SUSPND is low for normal operation.
V_{CC}	9, 46		3.3-V supply voltage.
XTAL1/CLK48	45	I	Crystal 1/48-MHz Clock Input. When MODE is low, XTAL1/CLK48 is a 6-MHz crystal input with 50% duty cycle. An internal APLL generates the 48-MHz and 12-MHz clocks used internally by the ASIC logic. When MODE is high, XTAL1/CLK48 acts as the input of the 48 MHz clock and the internal APLL logic is bypassed.
XTAL2	44	O	Crystal 2. XTAL2 is a 6-MHz crystal output. This terminal should be left open when using an oscillator.

† All LED control are 3-stated during low-power suspend.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 3.6 V
Input voltgage range, V_I . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK}, (V_I < 0 V or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK}, (V_O < 0 V or V_O > V_{CC}) . . . . . ±20 mA
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Operating free-air temperature range, T_A . . . . . 0°C to 70°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Input voltage, TTL/LVCMOS‡, V_I	0		V_{CC}	V
Output voltage, TTL/LVCMOS§, V_O	0		V_{CC}	V
High-level input voltage, signal-ended receiver, $V_{IH(REC)}$	2		V_{CC}	V
Low-level input voltage, signal-ended receiver, $V_{IL(REC)}$			0.8	V
High-level input voltage, TTL/LVCMOS‡, $V_{IH(TTL)}$	2		V_{CC}	V
Low-level input voltage, TTL/LVCMOS‡, $V_{IL(TTL)}$	0		0.8	V
Operating free-air temperature, T_A	0		70	°C
External series, differential driver resistor, $R_{(DRV)}$		22		Ω
Operating (DC differential driver) high speed mode, $f_{(OPRH)}$			12	Mb/s
Operating (DC differential driver) low speed mode, $f_{(OPRL)}$			1.5	Mb/s
Common mode, input range, differential receiver, $V_{(ICR)}$	0.8		2.5	V
Input transition times (t_r and t_f), TTL/LVCMOS‡	0		25	ns
Junction temperature range, T_J¶	0		115	°C

‡ Applies for input and bidirectional buffers
§ Applies for output and bidirectional buffers
¶ These junction temperatures reflect simulated conditions. Absolute maximum junction temperature is 150°C. The customer is responsible for verifying junction temperature.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL/LVCMOS	I_{OH} = –4 mA	V_{CC} – 0.5		V
		USB data lines	$R_{(DRV)}$ = 15 kΩ, to GND	2.8		
			I_{OH} = –12 mA (without $R_{(DRV)}$)	V_{CC} – 0.5		
V_{OL}	Low-level output voltage	TTL/LVCMOS	I_{OL} = 4 mA		0.5	V
		USB data lines	$R_{(DRV)}$ = 1.5 k Ω to 3.6 V		0.3	
			I_{OL} = 12 mA (without $R_{(DRV)}$)		0.5	
V_{IT+}	Positive input threshold voltage	TTL/LVCMOS			1.8	V
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V		1.8	V
$V_{IT–}$	Negative-input threshold voltage	TTL/LVCMOS		0.8		V
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V	1		V
V_{hys}	Input hysteresis† ($V_{T+} – V_{T–}$)	TTL/LVCMOS		0.3	0.7	V
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V	300	500	mV
I_{OZ}	High-impedance output current	TTL/LVCMOS	V = V_{CC} or GND‡		±10	µA
		USB data lines	0 V ≤ V_O ≤ V_{CC}		±10	µA
I_{IL}	Low-level input current	TTL/LVCMOS	V_I = GND		–1	µA
I_{IH}	High-level input current	TTL/LVCMOS	V_I = V_{CC}		1	µA
$z_{o(DRV)}$	Driver output impedance	USB data lines	Static V_{OH} or V_{OL}	7.1	19.9	Ω
V_{ID}	Differential input voltage	USB data lines	0.8 V ≤ V_{ICR} ≤ 2.5 V	0.2		V
I_{CC}	Input supply current		Normal operation		40	mA
			Suspend mode		1	µA

† Applies for input buffers with hysteresis
‡ Applies for open drain buffers

differential driver switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 50 pF (unless otherwise noted)

full speed mode

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_r	Transition rise time for DP or DM	See Figure 1 and Figure 2	4	20	ns
t_f	Transition fall time for DP or DM	See Figure 1 and Figure 2	4	20	ns
$t_{(RFM}$	Rise/fall time matching§	(t_r/t_f) × 100	90%	110%	
$V_{O(CRS)}$	Signal crossover output voltage§		1.3	2.0	V

§ Charicterized only. Limits are approved by design and are not production tested.

low speed mode

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_r	Transition rise time for DP or DM§	C_L = 200 pF to 600 pF,	See Figure 1 and Figure 2	75	300	ns
t_f	Transition fall time for DP or DM§	C_L = 200 pF to 600 pF,	See Figure 1 and Figure 2	75	300	ns
$t_{(RFM)}$	Rise/fall time matching§	(t_r/t_f) × 100		80%	120%	
$V_{O(CRS)}$	Signal crossover output voltage§	C_L = 200 pF to 600 pF		1.3	2.0	V

§ Charicterized only. Limits are approved by design and are not production tested.

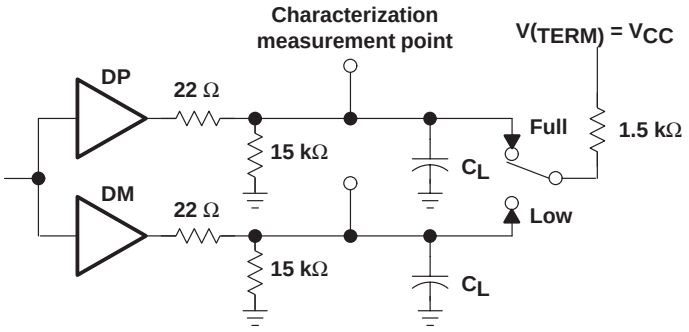
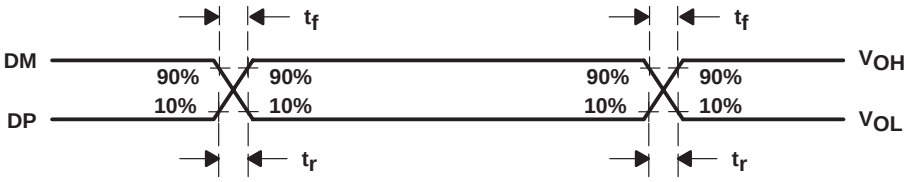


Figure 1. Differential Driver Switching Load



NOTE: The t_r/t_f ratio is measured as $t_{r(DP)}/t_{f(DM)}$ and $t_{r(DM)}/t_{f(DP)}$ at each crossover point.

Figure 2. Differential Driver Timing Waveforms

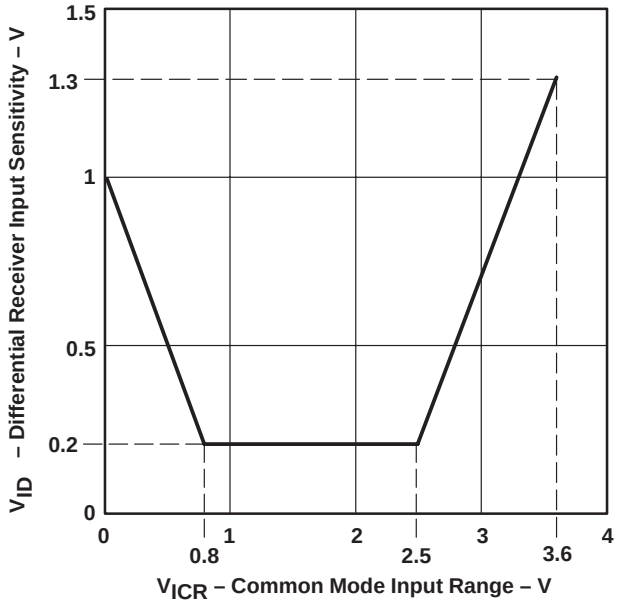


Figure 3. Differential Receiver Input Sensitivity vs. Common Mode Input Range

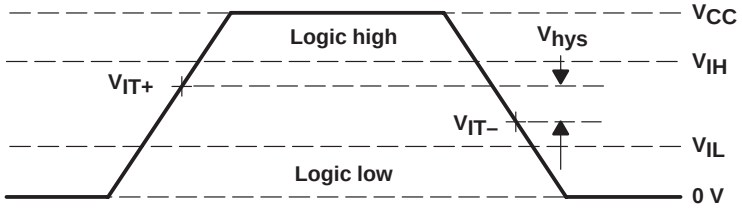


Figure 4. Single-Ended Receiver Input Signal Parameter Definitions

APPLICATION INFORMATION

A major advantage of USB is the ability to connect 127 functions configured in up to six logical layers (tiers) to a single personal computer (see Figure 5)

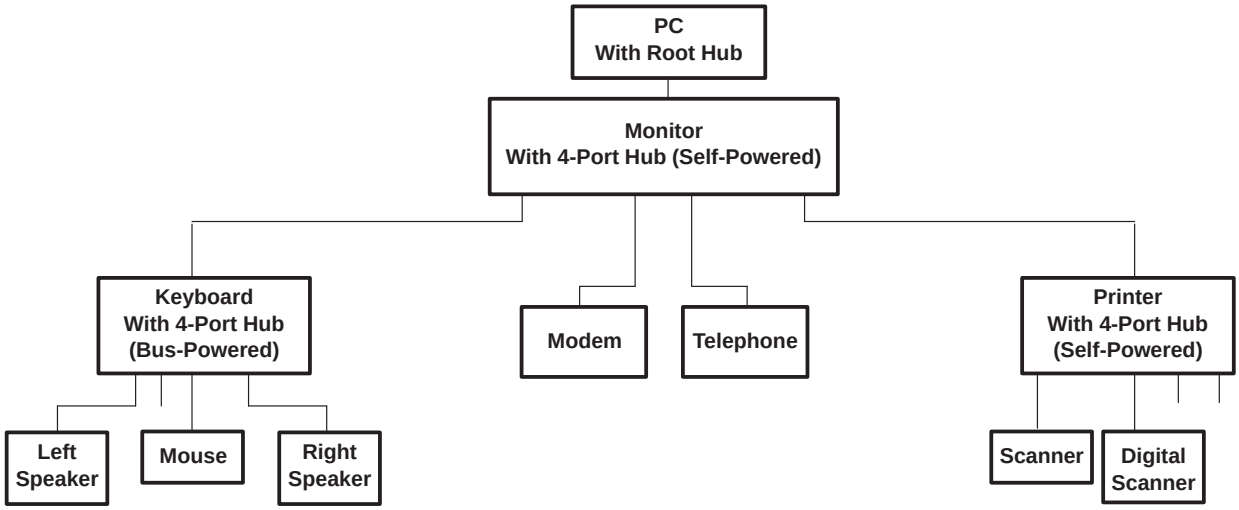


Figure 5. USB Tiered Configuration Example

Another advantage of USB is that all peripherals are connected using a standardized four wire cable that provides both communication and power distribution. The power configurations are bus-powered and self-powered modes. The maximum current that may be drawn from the USB 5-V line during power up is 100 mA. For the bus-powered mode, a hub can draw a maximum of 500 mA from the 5-V line of the USB cable. A bus-powered hub must always be connected downstream to a self-powered hub unless it is the only hub connected to the PC and there are no high-powered functions connected downstream. In the self-powered mode, the hub is connected to an external power supply and can supply up to 500 mA to each downstream port. High-powered functions may draw a maximum of 500 mA from each downstream port and may only be connected downstream to self-powered hubs. Per the USB specification, in the bus-powered mode, each downstream port can provide a maximum of 100 mA of current, and in the self-powered mode, each downstream port can provide a maximum of 500 mA of current.

Both bus-powered and self-powered hubs require over-current protection for all downstream ports. The two types of protection are individual port management (individual port basis) or ganged port management (multiple port basis). Individual port management requires power management devices for each individual downstream port, but adds robustness to the USB system because, in the event of an over-current condition, the USB host only powers down the port that has the condition. The ganged configuration uses fewer power management devices and thus has lower system costs, but in the event of an over-current condition on any of the downstream ports, all the ganged ports are disabled by the USB host.

Using a combination of the BUSPWR and EEDATA/$\overline{\text{GANGED}}$ inputs, the TUSB2077A supports four modes of power management: bus-powered hub with either individual port power management or ganged port power management, and the self-powered hub with either individual port power management or ganged port power management. Texas Instruments supplies the complete hub solution because we offer this TUSB2077A, the TUSB2046 (4-port) and the TUSB2140B (4-port with I^2C) hubs along with the power management chips needed to implement a fully USB Specification 1.1 compliant system.

APPLICATION INFORMATION

The following sections provide block diagram examples of how to implement the TUSB2077A device. Please note, even though no resistors are shown, pullup, pulldown and series resistors must still be used to properly implement this device.

Figure 6 is a block diagram example of how to connect the external EEPROM if a custom Product ID and Vendor ID are desired.

Figure 7 is an example of how to generate the 6-MHz clock signal. Figure 8 shows the EEPROM Read Operation Timing Diagram. Figures 9, 10, and 11 illustrate how to connect the TUSB2077A device for different power source and port power management combinations.

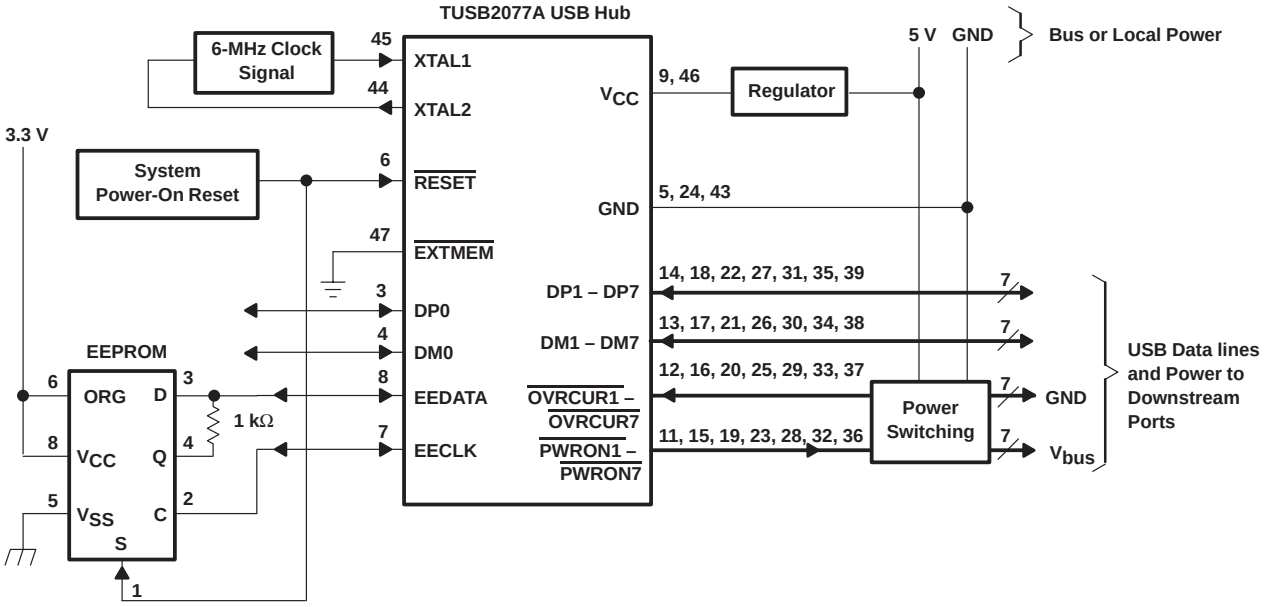
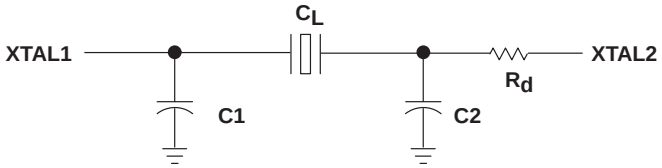


Figure 6. Typical Application of the TUSB2077A USB Hub



NOTE A: Figure 7 assumes a 6 MHz fundamental crystal that is parallel loaded. The component values of C1, C2 and R_d were determined using a crystal from Fox Electronics – part number HC49U–6.00MHz30\50\0 ±70\20 which means ±30 ppm at 25°C and 50 ppm from 0°C to 70°C. The characteristics for the crystal are load capacitance (C_L) of 20 pF, maximum shunt capacitance (C_0) of 7 pF and the maximum ESR of 50 Ω. In order to insure enough negative resistance, use C1 = C2 = 27 pF. The resistor R_d is used to trim the gain, and R_d = 1.5 kΩ is recommended.

Figure 7. Crystal Tuning Circuit

APPLICATION INFORMATION

programming the EEPROM

An SGS Thompson M93C46 EEPROM or equivalent is used for storing the programmable VID and PID. When the EEPROM interface is enabled ($\overline{\text{EXTMEM}}$ = 0), the EECLK and EEDATA are internally pulled down (100 μA) inside the TUSB2077A. The internal pulldowns are disabled when the EEPROM interface is disabled ($\overline{\text{EXTMEM}}$ = 1).

The EEPROM is programmed with the three 16-bit locations as shown in Table 1. Connecting pin 6 of the EEPROM high (ORG = 1) organizes the EEPROM memory into 64×16 bit words.

Table 1. EEPROM Memory Map

ADDRESS	D15	D14	D13	D12–D8	D7–D0
00000	0	$\overline{\text{GANGED}}$	00000	00000	00000000
00001	VID High-byte				VID Low-byte
00010	PID High-byte				PID Low-byte
	XXXXXXXX				

The D and Q signals of the EEPROM must be tied together using a 1 kΩ resistor with the common I/O operations forming a single-wire bus. After system power-on reset, the TUSB2077A performs a one-time access read operation from the EEPROM if the $\overline{\text{EXTMEM}}$ pin is pulled low and the chip select(s) of the EEPROM is connected to the system power-on reset. Initially, the EEDATA pin will be driven by the TUSB2077A to send a start bit (1) which is followed by the read instruction (10) and the starting-word address (00000). Once the read instruction is received, the instruction and address are decoded by the EEPROM, which then sends the data to the output shift register. At this point, the hub stops driving the EEDATA pin and the EEPROM starts driving. A dummy (0) bit is then output and the first three 16-bit words in the EEPROM are output with the most significant bit (MSB) first.

The output data changes are triggered by the rising edge of the clock provided by the TUSB2077A on the EECLK pin. The *SGS-Thompson M936C46* EEPROM is recommended because it advances to the next memory location by automatically incrementing the address internally. Any EEPROM used must have the automatic internal address advance function. After reading the three words of data from the EEPROM, the TUSB2077A puts the EEPROM interface into a high-impedance condition (pulled down internally) to allow other logic to share the EEPROM. The EEPROM read operation is summarized in Figure 8. For more details on EEPROM operation, refer to *SGS-Thompson Microelectronics M93C46 Serial Microwire Bus EEPROM* data sheet.

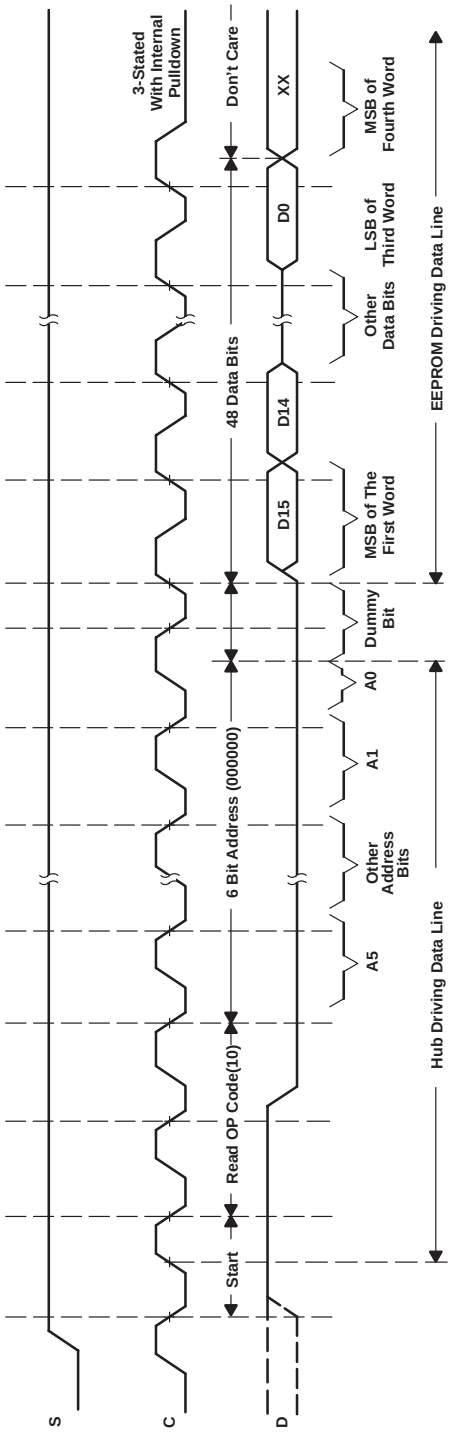
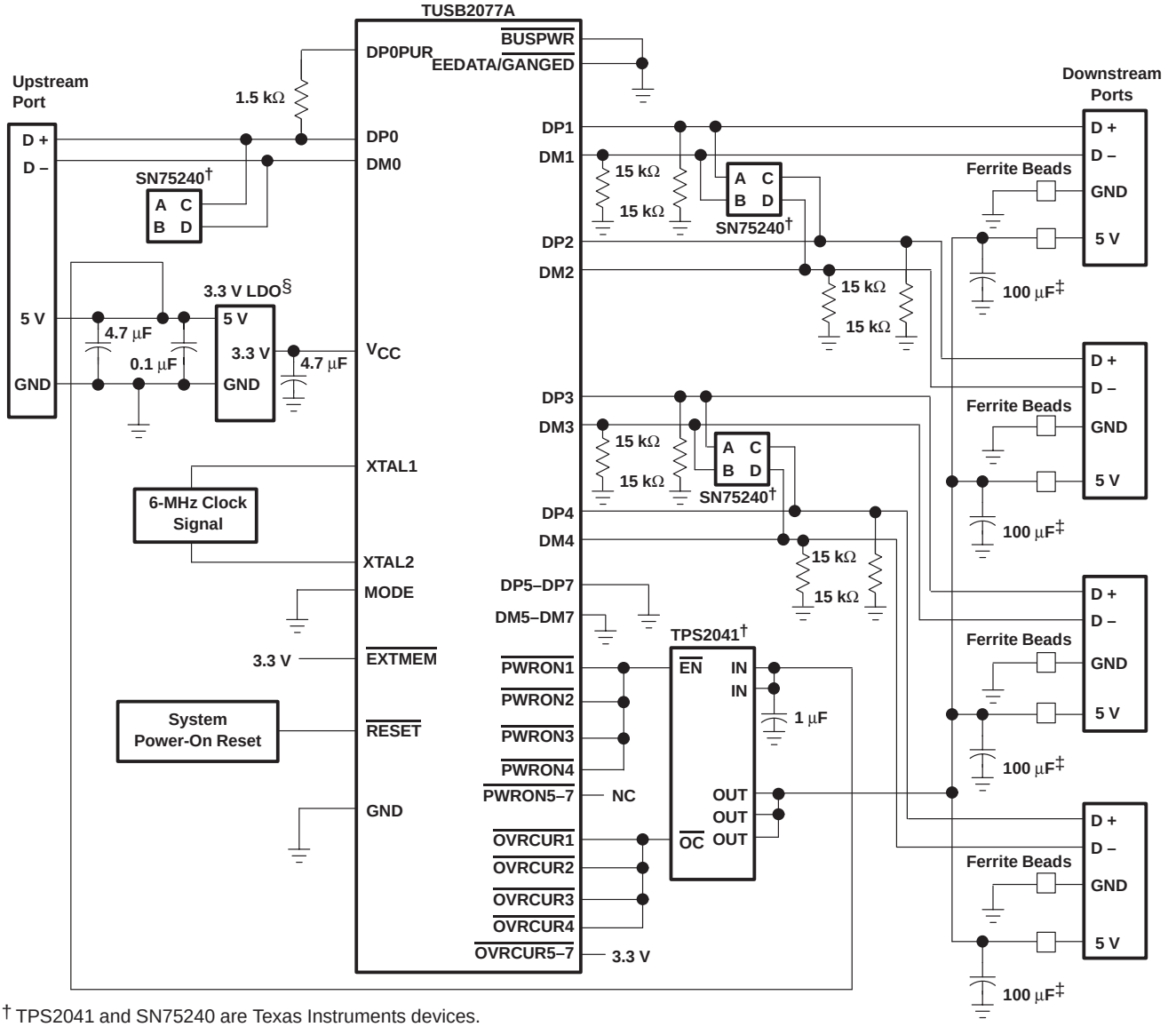


Figure 8. EEPROM Read Operation Timing Diagram

APPLICATION INFORMATION

bus-powered hub, ganged port power management

When used in bus-powered mode, the TUSB2077A supports up to four downstream ports by controlling a TPS2041 device which is capable of supplying 100 mA of current to each downstream port. Bus-powered hubs must implement power switching to ensure current demand is held below 100 mA when the hub is hot-plugged into the system. Utliizing the TPS2041 for ganged power management provides over-current protection for the downstream ports. The SN75240 transient suppressors reduce inrush current and voltage spikes on the data lines. The $\overline{\text{OVRCUR}}$ signals should be tied together for a ganged operation.



† TPS2041 and SN75240 are Texas Instruments devices.

‡ 120 µF per hub is the minimum required per the USB specification, version 1.1. However, TI recommends a 100 µF low ESR tantulum capacitor per port for immunity to voltage droop.

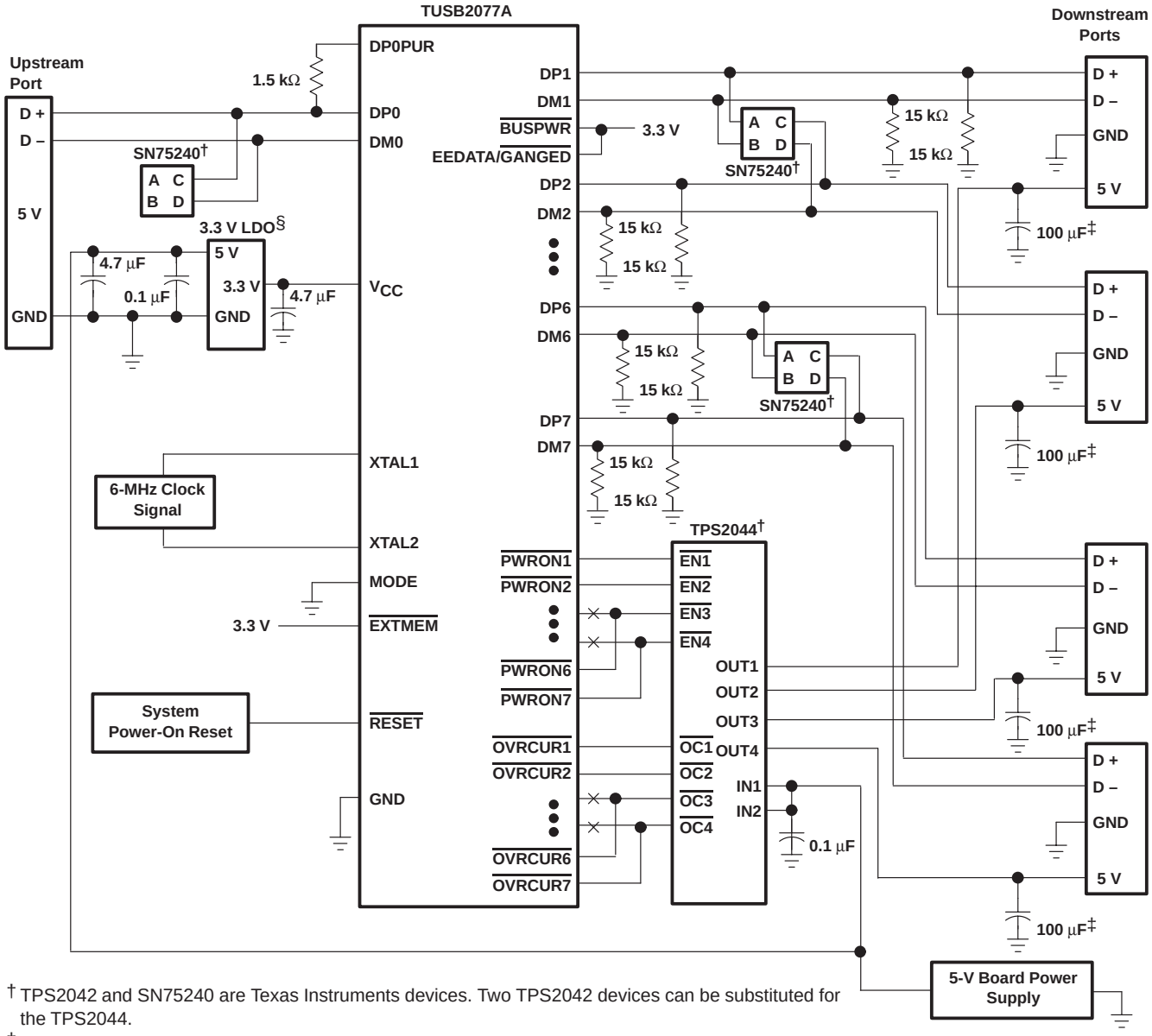
§ LDO is a 5 V to 3.3 V voltage regulator. TPS76333 from Texas Instruments can be used.

Figure 9. TUSB2077A Bus-Powered Hub, Ganged Port Power Management Application

APPLICATION INFORMATION

self-powered hub, individual port power management

In a self-powered configuration, the TUSB2077A can be implemented for individual port-power management when used with two TPS2044 because it is capable of supplying 500 mA of current to each downstream port and can provide current limiting on a per port basis. When the hub detects a fault on a downstream port, power is removed from only the port with the fault and the remaining ports continue to operate normally. Self-powered hubs are required to implement over-current protection and report overcurrent conditions. The SN75240 transient suppressors reduce inrush current and voltage spikes on the data lines.



† TPS2042 and SN75240 are Texas Instruments devices. Two TPS2042 devices can be substituted for the TPS2044.

‡ 120 µF per hub is the minimum required per the USB specification, version 1.1. However, TI recommends a 100 µF low ESR tantulum capacitor per port for immunity to voltage droop.

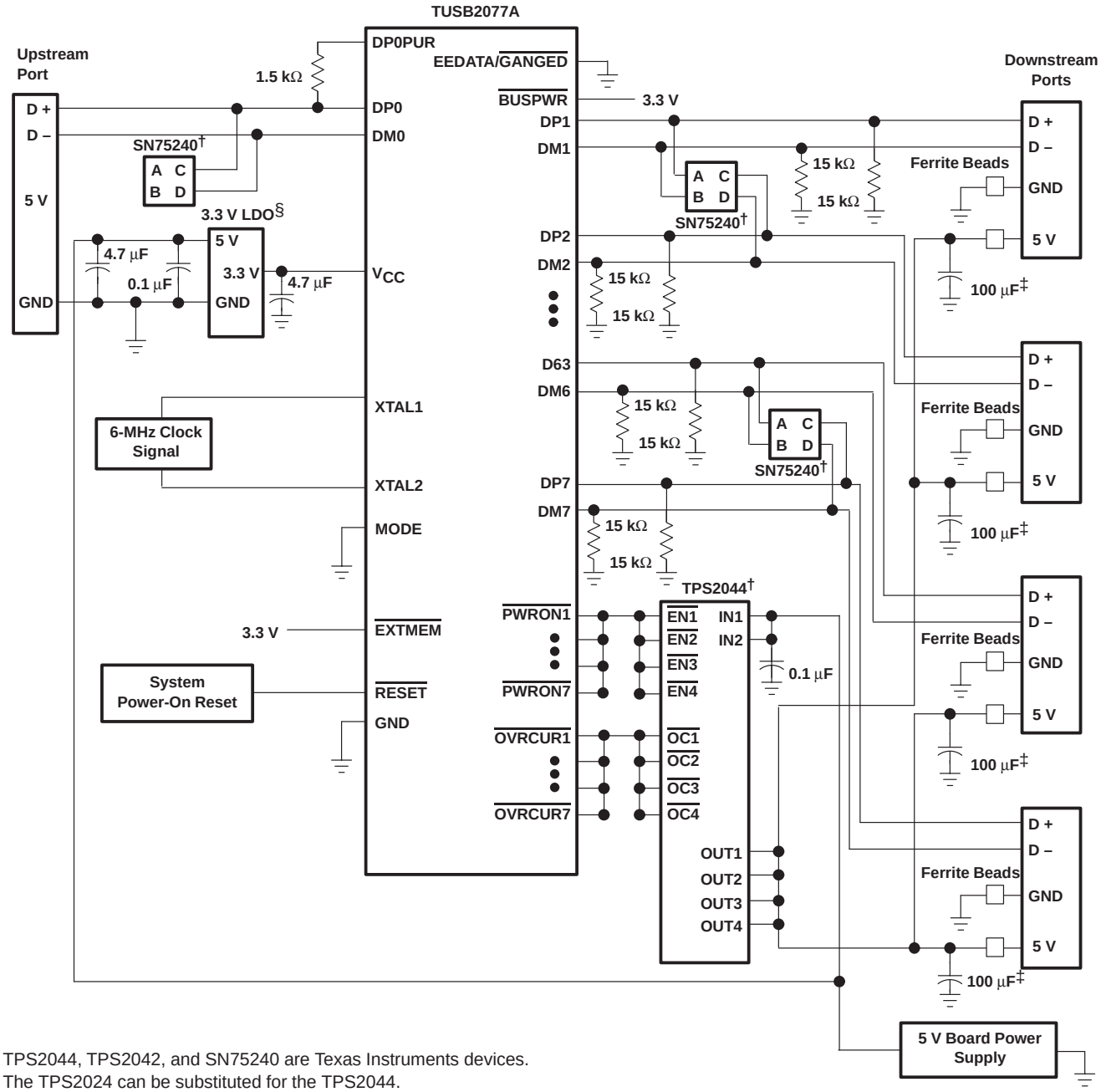
§ LDO is a 5 V to 3.3 V voltage regulator. TPS76333 from Texas Instruments can be used.

Figure 10. TUSB2077A Self-Powered Hub, Individual Port-Power Management Application

APPLICATION INFORMATION

self-powered hub, ganged port power management

The TUSB2077 can also be implemented for ganged port power management in a self-powered configuration. The implementation is very similar to the bus-powered example with the exception that a self-powered port supplies 500 mA of current to each downstream port. The over-current protection can be provided by a TPS2044 quad device or a TPS2024 single power switch.



† TPS2044, TPS2042, and SN75240 are Texas Instruments devices. The TPS2024 can be substituted for the TPS2044.

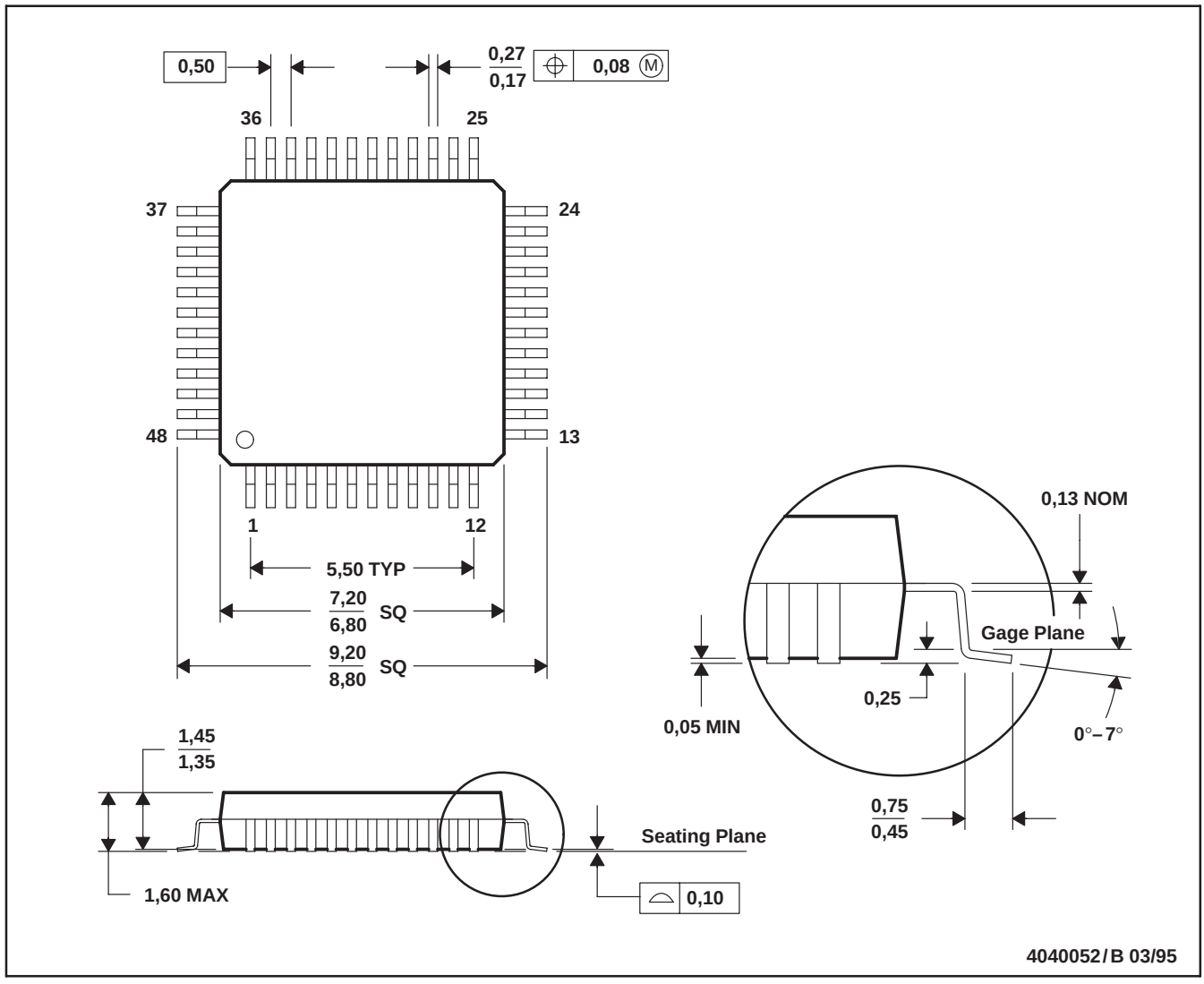
‡ 120 µF per hub is the minimum required per the USB specification, version 1.1. However, TI recommends a 100 µF low ESR tantulum capacitor per port for immunity to voltage droop.

§ LDO is a 5 V to 3.3 V voltage regulator. TPS76333 from Texas Instruments can be used.

Figure 11. TUSB2077A Self-Powered Hub, Ganged Port Power Management Application

MECHANICAL DATA

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136
D. This may also be a thermally enhanced plastic package with leads connected to the die pads.

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