TUSB2140
Data Manual

4-Port Hub With an Embedded Function for the Universal Serial Bus

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TEXAS INSTRUMENTS

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1 Introduction

The TUSB2140 is a compound USB device that provides a 4-port hub and an embedded function. The TUSB2140 is fully compatible with the USB, version 1.0, specification and the embedded function is fully compatible with the USB display-device class specification.

The embedded function is virtually connected to a fifth full-speed downstream hub port. In addition, the embedded function includes a control endpoint and an interrupt endpoint to support USB data transfers. The FIFOs and control registers associated with the endpoints are fully integrated within the device. An Inter IC(I^2C), 2-wire serial interface is provided for a local micro-controller unit (MCU) to access the FIFOs and control registers.

The TUSB2140 hub supports power switching to the downstream ports for either individual or ganged power management modes. External devices are required to switch power and to detect overcurrent conditions. Please see the application notes in Section 6. The TUSB2140 provides the required outputs to control power switching and the inputs to monitor any overcurrent conditions. In the ganged mode, all $\overline{\text{PWRON}}$ signals switch simultaneously.In addition, in the ganged mode the $\overline{\text{OVRCUR}}$ inputs should be tied together and driven by the same signal.

The TUSB2140 requires a 48-MHz clock signal to sample data from the upstream port and to generate a synchronized 12-MHz USB clock signal. The hub supports the flexibility to use either a 48-MHz oscillator or a crystal tuned to 48-MHz. When an oscillator is used, the oscillator output must be connected to the XTAL1 terminal and the XTAL2 terminal should remain open. An oscillator with a TTL level output may be used if the output does not exceed 3.6-V maximum. For a crystal implementation, the XTAL1 terminal should be used as the input and the XTAL2 terminal should be used as the feedback path to the crystal. Because the crystal is required to resonate at 48-MHz, a tuning circuit may be required such as shown in Figure 6–3.

USB-compatible transceivers are provided for all upstream and downstream ports. All external downstream ports support both full- and low-speed connection by automatically setting the slew rate according to the speed of the device attached to the port.

1.1 Features

The main features of the TUSB2140 hub and embedded function are listed in the following sections.

1.1.1 Hub

- Universal Serial Bus (USB) Version 1.0 Compatible
- Includes Serial Interface Engine (SIE)
- All Four External Downstream Ports Support Full-Speed and Low-Speed Operations
- Integrated USB Transceivers
- Power Switching and Overcurrent Conditions are Reported for Per Port or Ganged Modes

1.1.2 Embedded Function

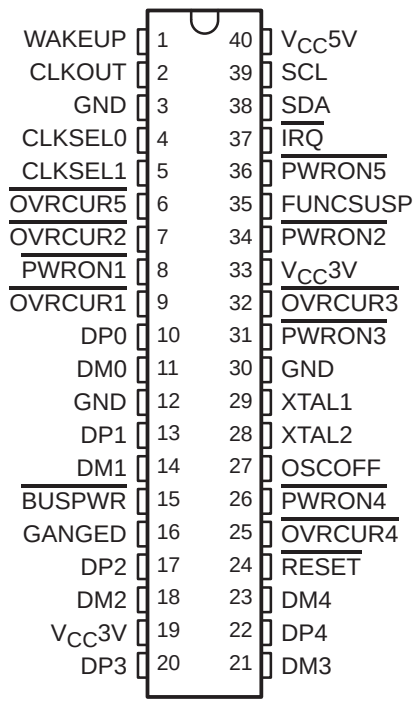
- USB Display Class Compatible
- Supports both Control and Interrupt Data Transfers
- Integrated FIFOs and Control/Status Registers
- Supports Interrupt Driven Operation to Minimize Local Micro-Controller Polling
- Supports USB Remote Wake-Up

1.1.3 General Characteristics

- Low-Power CMOS Technology
- Generates a Clock Output With a Frequency of 12 MHz, 8 MHz, 6 MHz, or 4 MHz
- Available in a 40-Pin Dip Package or a 64-Pin TQFP Package
- Requires a 48-MHz Crystal or Oscillator Input
- Uses a 3.3 V and 5 V Power Supply

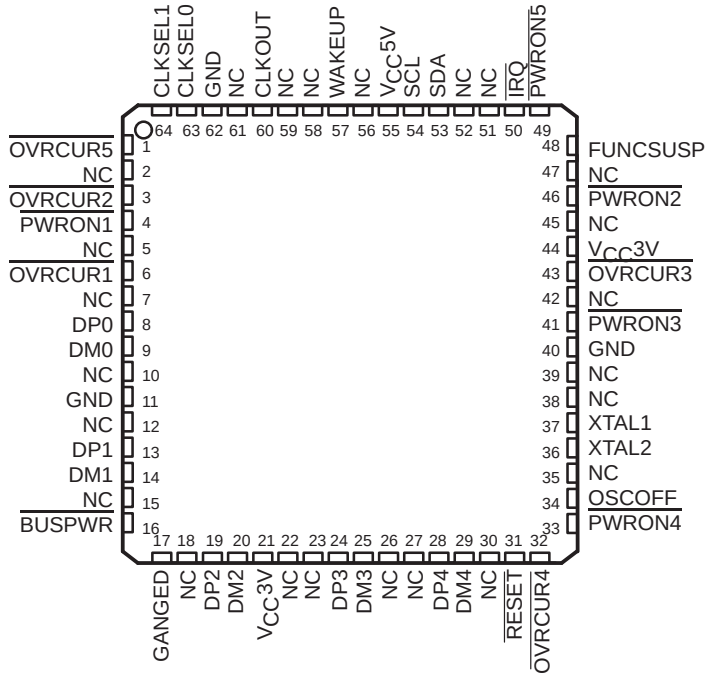
1.2 Terminal Assignments

N PACKAGE
(TOP VIEW)



NC – No internal connection

PAG PACKAGE
(TOP VIEW)



NC – No internal connection

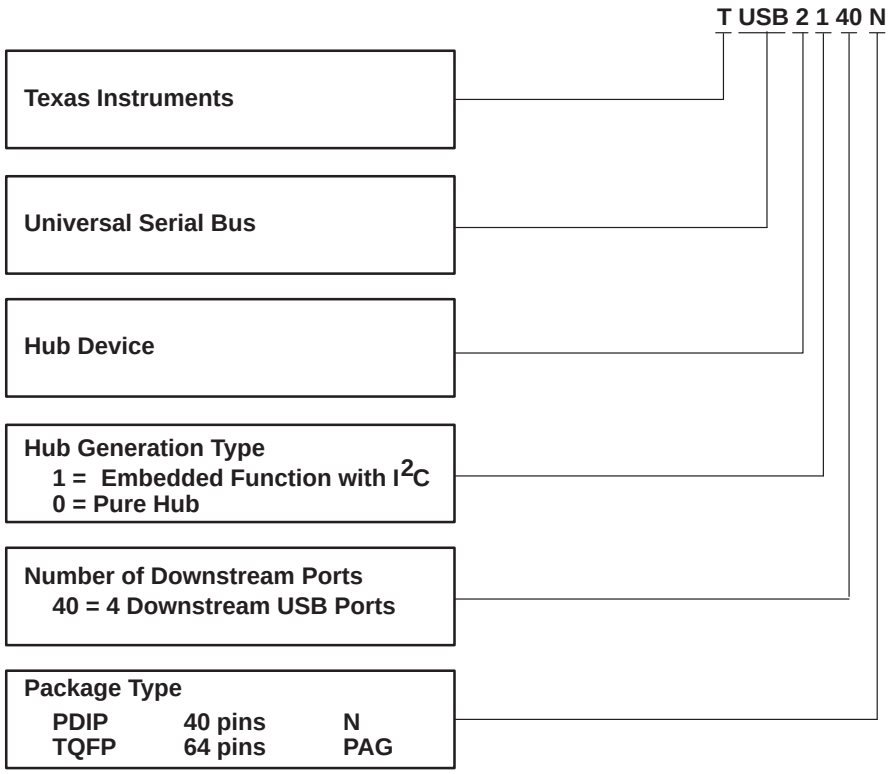
1.3 Terminal Functions

TERMINAL NAME	TERMINAL PAG NO.	TERMINAL N NO.	I/O	DESCRIPTION
$\overline{\text{BUSPWR}}$	16	15	I	Port power indicator. $\overline{\text{BUSPWR}}$ is an active low input that indicates whether the ports and the hub source power from the bus or are self-powered by the local power supply. This standard TTL input must not change dynamically during operation.
CLKOUT	60	2	O	Clock output. Depending on the configuation of CLKSEL0 and CLKSEL1, CLKOUT is a selected clock output of 12 MHz, 8 MHz, 6 MHz, or 4 MHz.
DM1 – DM4	14, 20, 25, 29	14, 18, 21, 23	I/O	Data minus USB differential data pairs. DM1 – DM4 support up to four negative-signal downstream USB ports.
DP1 – DP4	13, 19, 24, 28	13, 17, 20, 22	I/O	Data plus USB differential data pairs. DP1 – DP4 support up to four positive-signal downstream USB ports.
DM0	9	11	I/O	Data minus USB differential data. DM0 is used for the upstream USB port cable pair and negative signal.
DP0	8	10	I/O	Data plus USB differential data. DP0 is used for the upstream USB port cable pair and positive signal.
FUNCSUSP	48	35	O	Function port suspend. FUNCSUSP is an active high output that indicates if the port that connects to the embedded function has been selectively suspended.
GANGED	17	16	I	Power switch/overcurrent detection. GANGED selects between gang or per port switching for overcurrent detection of the downstream ports. The setting is dependent upon an external power control device. This standard TTL input must not change dynamically during operation.
GND	11, 40, 62	3, 12, 30		Ground. All terminals must be tied to ground for proper operation
$\overline{\text{IRQ}}$	50	37	O	Interrupt. $\overline{\text{IRQ}}$ is an active low output that indicates that an interrupt condition has occured.
OSCOFF	34	27	I	Oscillator off. OSCOFF disables the internal oscillator for quiescent current draw ($I_{CC}Q$) testing. OSCOFF must be tied low for operation.
$\overline{\text{OVRCUR1}}$ – $\overline{\text{OVRCUR5}}$	6, 3, 43, 32, 1	9, 7, 32, 25, 6	I	Overcurrent indicators. $\overline{\text{OVRCUR1}}$ – $\overline{\text{OVRCUR5}}$ are active low, standard TTL inputs. One overcurrent indicator is available for each of the four downstream ports. These inputs are internally gated when port power switching is ganged. The unused terminals must be tied high.
$\overline{\text{PWRON1}}$ – $\overline{\text{PWRON5}}$	4, 46, 41, 33, 49	8, 34, 31, 26, 36	O	Power on/off control switches. $\overline{\text{PWRON1}}$ – $\overline{\text{PWRON5}}$ are active low, open-drain outputs. One power on/off control switch is used for each of the four downstream ports. All outputs are switched together when the port power switching is ganged.
$\overline{\text{RESET}}$	31	24	I	Reset. $\overline{\text{RESET}}$ is a TTL input with hysteresis and must be asserted at power up for conformance to USB. When $\overline{\text{RESET}}$ is an active low, it initializes all logic.
SCL	54	39	I	Serial clock. SCL is the clock signal for the I^2C serial interface and is 5-V tolerant.
SDA	53	38	I/O	Serial data. SDA is the bidirectional data signal for the I^2C serial interface and is 5-V tolerant. SDA uses an open-drain output driver.
$V_{CC}3V$	21, 44	19, 33		3.3-V supply voltage
$V_{CC}5V$	55	40		5-V supply voltage

1.3 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL PAG NO.	TERMINAL N NO.	I/O	DESCRIPTION
WAKEUP	57	1	I	Function port remote wake-up. WAKEUP is an active high input used by the micro-controller to initiate a remote wake-up from a suspended mode. WAKEUP is 5-V tolerant.
XTAL1	37	29	I	Crystal 1. XTAL1 is a 48-MHz crystal or oscillator input. Operation at 48-MHz is four times the USB full-speed bit rate of 12 Mbps.
XTAL2	36	28	O	Crystal 2. XTAL2 is a 48-MHz crystal output. Operation at 48-MHz is four times the USB full-speed bit rate of 12 Mbps
CLKSEL0, CLKSEL1	63, 64	4, 5	I	Clock select inputs. CLKSEL0 and CLKSEL1 determine the CLKOUT frequency (See Table 4–2).

1.4 Device-Numbering Convention and Ordering Information



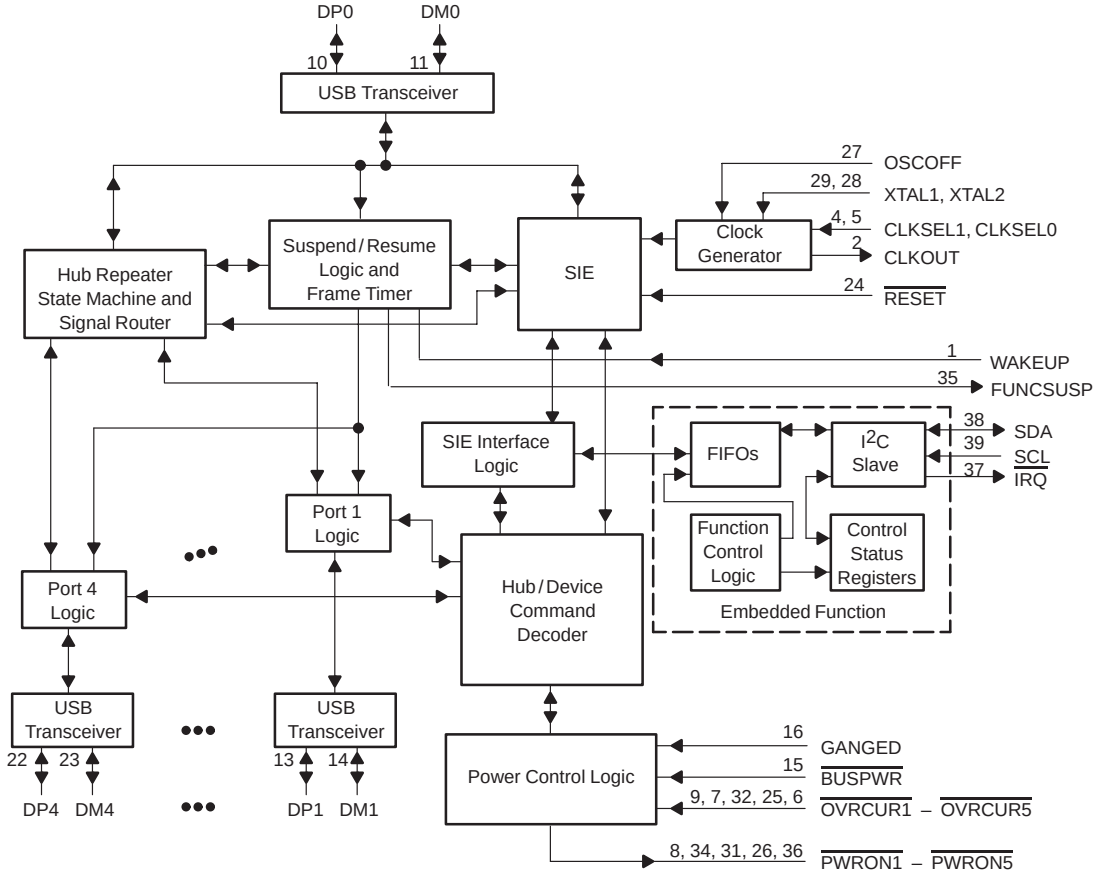
1.5 Related Documents Referenced

- Universal Serial Bus Specification version 1.0 dated January 19, 1996.
- Inter IC (I^2C) Specification

2 Functional Description

The functional block diagram for the TUSB2140 is shown in Section 2.1. The description for the function blocks follow Section 2.1. For additional information, including USB signaling specifications, packet protocol, and hub functionality, please refer to the Universal Serial Bus Specification version 1.0 dated January 19, 1996.

2.1 Functional Block Diagram



NOTE A: Terminal numbers shown are for the N package

2.2 USB Transceiver

The TUSB2140 provides integrated transceivers for all the USB ports. The transceivers include a differential output driver, a differential input receiver and two single ended inputs. The transceiver for each port connects to the appropriate DP and DM differential signal pair.

2.3 Clock Generator

Utilizing the 48-MHz input signal, the clock generator logic generates the CLKOUT output signal in addition to the various internal clock signals. The TUSB2140 internal clocks consist of the 48-MHz clock, a 12-MHz clock and a USB clock. The USB clock also has a frequency of 12-MHz. The USB clock is the same as the 12-MHz clock when the TUSB2140 is transmitting data and is derived from the data when the TUSB2140 is receiving data.

2.4 Serial Interface Engine (SIE)

The serial interface engine logic manages the USB packet protocol requirements for the packets being received and transmitted by the TUSB2140. For packets being received, the SIE decodes the packet identifier field (PID) to determine the type of packet being received and ensures the PID is valid. For token packets and data packets being received, the SIE calculates the packet CRC and compares the value to the CRC contained in the packet to verify that the packet was not corrupted during transmission. For token packets and data packets being transmitted, the SIE generates the CRC that is transmitted with the packet. For packets being transmitted, the SIE also generates the synchronization field (SYNC) which is the eight bit field at the beginning of each packet. In addition, the SIE generates the correct PID for all packets being transmitted. Another major function of the SIE is the overall serial-to-parallel conversion of the data packets being received and the parallel-to-serial conversion of the data packets being transmitted.

2.5 SIE Interface Logic

The SIE interface logic provides the control logic that interfaces the SIE to the hub control logic and the embedded function control logic. One of the major functions of the SIE interface logic is to decode the function address from the SIE to determine if either the hub or embedded function is being addressed. In addition, the endpoint address field is decoded to determine which particular endpoint of the hub or embedded function is being addressed. The SIE interface logic also managers the multiplexing of the byte-wide transmit data signals and other control signals, from the hub control logic and embedded function control logic.

2.6 Hub Command Decoder

The hub command decoder logic manages the overall control of the hub including the decode and execution of host initiated control commands, as well as the status change endpoint. During USB interrupt transfers, the USB host uses the status change endpoint to aquire hub status and port status change information.

2.7 Frame Timer

The frame timer logic generates the End of Frame (EOF) signal which is used mainly to ensure that all downstream traffic is completed during each frame period. In addition, since the frame timer counts 1.0 ms periods, the EOF signal is used by other logic that needs to time events based on multiples of 1.0 ms periods. The hub frame timer logic is locked to the host frame timer logic by the host generated Start of Frame (SOF) packets.

2.8 Suspend/Resume Logic

The suspend/resume logic is used to detect the suspend/resume states and to generate the signals used to control the overall device during the suspend/resume states.

2.9 Hub Repeater

The hub repeater logic manages the connectivity of the root port and the downstream ports on a per-packet basis. The data flow of the USB packets through the TUSB2140 from the root port to the downstream ports and vice-a-versa is totally asynchronous.

2.10 Port Logic

The port logic manages the overall state of a particular downstream port. Each of the downstream ports has unique port logic which controls the connect/disconnect, enable/disable, suspend/resume and reset states of the port.

2.11 Power Control Logic

The power control logic generates the $\overline{\text{PWRON1}}$ thru $\overline{\text{PWRON5}}$ output signals based on the GANGED, $\overline{\text{BUSPWR}}$, and $\overline{\text{OVRCUR}}$ input signals.

2.12 Embedded Function Control Logic

The Function Control Logic (FCL) manages communication between the local Micro-Controller Unit (MCU) and the Serial Interface Engine (SIE). The local MCU directs the operation of the FCL through the control and status registers. One of the major functions performed by the FCL is to move data to and from the internal FIFOs during the control and interrupt endpoint transfer operations.

2.13 Embedded Function Control/Status Registers

The control and status registers allow the local MCU to control and monitor transfer operations done by the TUSB2140. A separate set of registers is used to control the transmit and receive operations for the control endpoint which is endpoint 0. In addition, a seperate set of registers are provided for the interrupt endpoint transmit operations, which is endpoint 1. Also, an interrupt and interrupt mask register is provided to control the conditions that generate the $\overline{\text{IRQ}}$ output signal.

2.14 Embedded Function FIFOs

The TUSB2140 internal FIFOs provide a buffer between the SIE and the local MCU. There are three 8-byte by 8-bit FIFOs provided. There is a separate transmit and receive FIFO provided for the control endpoint, which is endpoint 0. In addition, there is a transmit FIFO provided for the interrupt endpoint, which is endpoint 1.

2.15 Embedded Function I^2C Interface

The I^2C Interface logic provides a two-wire serial interface that is used by a local MCU or device needing serial access to the TUSB2140 control/status registers and FIFOs. The interface allows single byte read and writes to the registers and multiple byte read and writes to the FIFOs. Note that the transmit FIFOs are write only and the receive FIFOs are read only from the local MCU side.

3 Internal Registers

The TUSB2140 provides a set of control and status registers to be used by the local micro–controller unit to control the overall operation of the embedded function. The control and status registers allow the local MCU to control and monitor USB transfers to both the control endpoint and the interrupt endpoint of the embedded function. There is a separate set of registers provided for the control endpoint transmit and receive operations. In addition, there is a separate set of registers provided for the transmit operations of the interrupt endpoint. Also, an interrupt and interrupt mask register is provided to control the conditions that generate the $\overline{\text{IRQ}}$ output signal.

3.1 Address Map

ADDRESS	MSB							LSB	NAME
	7	6	5	4	3	2	1	0	
00h				FSUSP	FRST	EP1TX	EP0RX	EP0TX	Interrupt Register
01h				FSUSP	FRST	EP1TX	EP0RX	EP0TX	Interrupt Mask Register
02h	FEN	FA6	FA5	FA4	FA3	FA2	FA1	FA0	Function Address Register
03h									
04h	D7	D6	D5	D4	D3	D2	D1	D0	EP0 TX FIFO
05h					BCNT3	BCNT2	BCNT1	BCNT0	EP0 TX Byte Count Register
06h	TXCLR				TXSTL		TXFEN	TXEN	EP0 TX Control Register
07h	TXSEQ			STSGE	STALL	NACK	ERROR	ACK	EP0 TX Status Register
08h					EMPT	FULL	UNDR	OVRR	EP0 TX FIFO Flags Register
09h	D7	D6	D5	D4	D3	D2	D1	D0	EP0 RX FIFO
0Ah					BCNT3	BCNT2	BCNT1	BCNT0	EP0 RX Byte Count Register
0Bh	RXCLR				RXSTL		RXFEN	RXEN	EP0 RX Control Register
0Ch	RXSEQ	SETUP	RXFSW	STSGE	STALL	NACK	ERROR	ACK	EP0 RX Status Register
0Dh					EMPT	FULL	UNDR	OVRR	EP0 RX FIFO Flags Register
0Eh									
0Fh									
10h	D7	D6	D5	D4	D3	D2	D1	D0	EP1 TX FIFO
11h					BCNT3	BCNT2	BCNT1	BCNT0	EP1 TX Byte Count Register
12h	TXCLR	TXSOW			TXSTL		TXFEN	TXEN	EP1 TX Control Register
13h	TXSEQ				STALL	NACK	ERROR	ACK	EP1 TX Status Register
14h					EMPT	FULL	UNDR	OVRR	EP1 TX FIFO Flags Register
15h									
16h									
17h									
18h									
19h									

3.1 Address Map (continued)

ADDRESS	MSB							LSB	NAME
	7	6	5	4	3	2	1	0	
1Ah									
1Bh									
1Ch									
1Dh									
1Eh									
1Fh									

3.2 Register Functional Description

The following sections contain the functional descriptions for each register and the individual register bits. Note that firmware should write a “0” to reserved bits and ignore any value read from reserved bits.

3.2.1 Interrupt Register

The interrupt register bits are used to indicate when an interrupt condition is pending. If one or more of the interrupt bits are set, the TUSB2140 interrupt output signal ($\overline{IRQ}$) will be asserted until the interrupt condition(s) is cleared. One or more of the interrupt bits can be masked by setting the corresponding bit in the interrupt mask register. If the interrupt mask bit is set, the corresponding interrupt bit will still be set when an interrupt condition occurs. However, the $\overline{IRQ}$ output signal will not be asserted. This feature is provided for systems that detect pending interrupt conditions with a polling scheme rather than by monitoring the $\overline{IRQ}$ output signal.

7							0
–	–	–	FSUSP	FRST	EP1TX	EP0RX	EP0TX

BIT	MNEMONIC	NAME	DESCRIPTION
7:5	–	Reserved	Reserved for future use.
4	FSUSP	Function suspend	The function suspend interrupt bit is set in response to the hub suspend logic detecting a global suspend condition or a selective suspend condition for the embedded function. To enable the TUSB2140 to enter a low–power suspend state which includes disabling the clocks, this bit must be cleared by the local MCU. This bit is cleared by writing a “1” to this register. This bit is read/write and is cleared by power-on reset.
3	FRST	Function reset	The function reset interrupt bit is set in response to the host initiating a port reset on the function port. When a function reset occurs, all of the Function Interface logic within the TUSB2140 will be reset except the endpoint 0 receive enable bit (RXEN), the endpoint 0 transmit enable bit (TXEN), the function reset interrupt bit (FRST) and all of the interrupt mask bits. This bit is cleared by writing a ”1” to this register. This bit is read/write and is cleared by power-on reset.
2	EP1TX	Endpoint 1 transmit interrupt	The endpoint 1 transmit interrupt bit is set in response to the endpoint 1 transmit acknowledge status bit (ACK), the endpoint 1 transmit FIFO over-run flag bit (OVRR), or the endpoint 1 transmit FIFO under-run flag bit (UNDR) being set. This bit is cleared by clearing the corresponding status or FIFO flag bit that caused the interrupt. This bit is read-only and is cleared by power-on reset.
1	EP0RX	Endpoint 0 receive interrupt	The endpoint 0 receive interrupt bit is set in response to the endpoint 0 receive acknowledge status bit (ACK), the endpoint 0 receive FIFO over-run flag bit (OVRR), or the endpoint 0 receive FIFO under-run flag bit (UNDR) being set. This bit is cleared by clearing the corresponding status or FIFO flag bit that caused the interrupt. This bit is read-only and is cleared by power-on reset.
0	EP0TX	Endpoint 0 transmit interrupt	The endpoint 0 transmit interrupt bit is set in response to the endpoint 0 transmit acknowledge status bit (ACK), the endpoint 0 transmit FIFO over-run flag bit (OVRR), or the endpoint 0 transmit FIFO under-run flag bit (UNDR) being set. This bit is cleared by clearing the corresponding status or FIFO flag bit that caused the interrupt. This bit is read-only and is cleared by power-on reset.

3.2.2 Interrupt Mask Register

The interrupt mask register bits are used to mask the corresponding interrupt bits.

7							0
–	–	–	FSUSP	FRST	EP1TX	EP0RX	EP0TX

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	–	Reserved	Reserved for future use.
4	FSUSP	Function suspend interrupt mask	The function suspend interrupt mask bit is set to enable the function suspend interrupt bit. This bit is read/write and is cleared by power–on reset.
3	FRST	Function reset interrupt mask	The function reset interrupt mask bit is set to enable the function reset interrupt bit. This bit is read/write and is cleared by power-on reset.
2	EP1TX	Endpoint 1 transmit interrupt mask	The endpoint 1 transmit interrupt mask bit is set to enable the endpoint 1 transmit interrupt bit. This bit is read/write and is cleared by power-on reset.
1	EP0RX	Endpoint 0 receive interrupt mask	The endpoint 0 receive interrupt mask bit is set to enable the endpoint 0 receive interrupt bit. This bit is read/write and is cleared by power-on reset.
0	EP0TX	Endpoint 0 transmit interrupt mask	The endpoint 0 transmit interrupt mask bit is set to enable the endpoint 0 transmit interrupt bit. This bit is read/write and is cleared by power-on reset.

3.2.3 Function Address Register

The function address register contains the current setting of the USB device address assigned to the function. During enumeration of the function, the function address is loaded into this register automatically by the TUSB2140 Function Control Logic when a Set Address request is received from the USB host. This register is read only and is used only for diagnostic purposes.

7							0
FEN	FA6	FA5	FA4	FA3	FA2	FA1	FA0

BIT	MNEMONIC	NAME	DESCRIPTION
7	FEN	Function enabled	The function enabled bit is set when the embedded function port has been enabled by the host with a set port feature request. This bit is read-only and is cleared by power-on reset.
6:0	FA(6:0)	Function address	The function register value is set to the current device address assigned to the function. These bits are read-only and are cleared by power-on reset.

3.2.4 Endpoint 0 Transmit FIFO

7							0
D7	D6	D5	D4	D3	D2	D1	D0

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	D(7:0)	Transmit FIFO data	Endpoint 0 transmit FIFO data is written to the transmit FIFO on a byte-to-byte basis. These bits are write-only.

3.2.5 Endpoint 0 Transmit Byte Count Register

7							0
–	–	–	–	BCNT3	BCNT2	BCNT1	BCNT0

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	–	Reserved	Reserved for future use.
3:0	BCNT(3:0)	Transmit byte count	The transmit byte count register should be loaded with the number of bytes to be transmitted. The byte count should be the number of bytes in the data packet that was loaded into the transmit FIFO. When the local MCU writes to the byte count register, the EP0 transmit FIFO enable bit (TXFEN) will automatically be set. Also, the byte count register does not decrement as data is transmitted. These bits are read/write and are cleared by power-on reset.

3.2.6 Endpoint 0 Transmit Control Register

The transmit control register is used to store bits which control various functions and operating modes of the Function Interface Logic within the TUSB2140.

7							0
TXCLR	–	–	–	TXSTL	–	TXFEN	TXEN

BIT	MNEMONIC	NAME	DESCRIPTION
7	TXCLR	Transmit clear	The transmit clear bit is set to reset the transmit FIFO pointers and flags. This bit should be set in response to a transmit FIFO over–run or under-run condition. After the FIFO pointers are reset, this bit will be automatically cleared. In addition, the FIFO empty flag will be set and the other FIFO flags will be cleared upon completion of the FIFO reset. This bit is read/write and is cleared by power-on reset.
6	–	Reserved	Reserved for future use.
5	–	Reserved	Reserved for future use.
4	–	Reserved	Reserved for future use.
3	TXSTL	Transmit stall	The transmit stall bit is set to enable a STALL handshake to be returned in response to the next valid In Transaction. This bit is automatically cleared if a new Setup Stage Transaction is successfully received. This bit is read/write and is cleared by power-on reset.
2	–	Reserved	Reserved for future use.
1	TXFEN	Transmit FIFO enable	The transmit FIFO enable bit is set to enable the transmission of data in the transmit FIFO when the next valid In Transaction occurs. This bit is automatically set when the local MCU writes to the EP0 transmit byte count register and is automatically cleared when the EP0 transmit acknowledge status bit (ACK) is set. This bit is also automatically cleared if a new Setup Stage Transaction is successfully received or the EP0 transmit clear bit (TXCLR) is set. If the transmit enable bit is not set, the device returns a NACK handshake. If the transmit stall control bit (TXSTL) is set, a STALL handshake is returned instead of a NACK handshake. This bit is read/write and is cleared by power-on reset.
0	TXEN	Transmit enable	The transmit enable bit is set to enable the transmit endpoint. For endpoint 0, the Control Endpoint, both a receive and transmit endpoint are required. Therefore, the transmit enable and receive enable bits must both be set before the device will be enumerated. If either of these bits are not set, the function port will remain in the disconnected state. This bit is read/write and is cleared by power-on reset.

3.2.7 Endpoint 0 Transmit Status Register

The transmit status register is used to store bits which report status information about the operating conditions of the Function Control Logic within the TUSB2140.

7							0
TXSEQ	–	–	STSGE	STALL	NACK	ERROR	ACK

BIT	MNEMONIC	NAME	DESCRIPTION
7	TXSEQ	Transmit sequence	The transmit sequence bit value determines the data packet PID to be used for the next data packet to be transmitted for the next In Data Stage Transaction. This bit is automatically set at the end of a successful Setup Stage Transaction and is automatically toggled at the end of each successful In Data Stage Transaction. If this bit is a '0', a DATA0 PID is sent in the data packet. If this bit is a'1', a DATA1 PID is sent in the data packet. This bit is read only and is cleared by power-on reset.
6	–	Reserved	Reserved for future use.
5	–	Reserved	Reserved for future use.
4	STSGE	In status stage	The in status stage bit is set when the Function Control Logic detects the Status Stage Transaction of a Control Transfer. This bit will be automatically cleared at the beginning of the next Setup Stage Transaction. This bit is read-only and is cleared by power-on reset.
3	STALL	Stall	The stall status bit is set at the end of an In Transaction if a STALL handshake packet is returned to the host instead of a data packet. The Function Control Logic will automatically return a STALL handshake to the host if a valid In Transaction is received and the transmit stall control bit is set. This stall status bit will be automatically updated at the end of the next valid In Transaction. This bit is read-only and is cleared by power-on reset.
2	NACK	No acknowledge	The no acknowledge status bit is set at the end of an In Transaction if a NACK handshake packet is returned to the host instead of a data packet. The Function Control Logic will automatically return a NACK handshake to the host if a valid In Transaction is received and there is not a data packet in the transmit FIFO ready to be transmitted. This bit will be automatically updated at the end of the next valid In Transaction. This bit is read-only and is cleared by power-on reset.
1	ERROR	Error	The error status bit is set at the end of an In Transaction if a timeout, bit-stuff, CRC, force transmit or other errors occur. This bit will be automatically updated at the end of the next valid In Transaction. This bit is read-only and is cleared by power-on reset.
0	ACK	Acknowledge	The acknowledge status bit is set at the end of an In Transaction if the data packet in the transmit FIFO was sent successfully and an acknowledge handshake was received from the host. When this bit is set, the endpoint 0 transmit interrupt bit is also set. The acknowledge status bit should be cleared by the local MCU in order to clear the interrupt condition. This bit will be automatically cleared at the beginning of the next Setup Stage Transaction. This bit is read/write and is cleared by power-on reset.

3.2.8 Endpoint 0 Transmit FIFO Flags Register

The transmit FIFO flags register is used to store bits which report status information about the transmit FIFO operating condition.

7							0
–	–	–	–	EMPT	FULL	UNDR	OVRR

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	–	Reserved	Reserved for future use.
3	EMPT	Transmit FIFO empty	The transmit FIFO empty flag is set when the transmit FIFO is empty. This bit is cleared when the FIFO is no longer empty. This bit is read-only and is set by power-on reset.
2	FULL	Transmit FIFO full	The transmit FIFO full flag is set when the transmit FIFO is full. This bit is cleared when the FIFO is no longer full. This bit is read-only and is cleared by power-on reset.
1	UNDR	Transmit FIFO under-run	The transmit FIFO under-run flag is set when the transmit FIFO is empty and the Function Control Logic attempts to read another byte from the FIFO. This will happen if the number of bytes actually written to the transmit FIFO is less than the value loaded into the transmit byte count register. When this bit is set, the endpoint 0 transmit interrupt bit is also set. To clear the FIFO under-run condition, the transmit FIFO clear control bit should be set. After the FIFO has been cleared, this bit and the endpoint 0 transmit interrupt bit will be automatically cleared. This bit is read-only and is cleared by power-on reset.
0	OVRR	Transmit FIFO over-run	The transmit FIFO over-run flag is set when the transmit FIFO is full and the local MCU attempts to write another byte to the FIFO. When this bit is set, the endpoint 0 transmit interrupt bit is also set. To clear the FIFO over-run condition, the transmit FIFO clear control bit should be set. After the FIFO has been cleared, this bit and the endpoint 0 transmit interrupt bit will be automatically cleared. This bit is read-only and is cleared by power-on reset.

3.2.9 Endpoint 0 Receive FIFO

7							0
D7	D6	D5	D4	D3	D2	D1	D0

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	D(7:0)	Receive FIFO data	Endpoint 0 receive FIFO data is read from the receive FIFO on a byte-to-byte basis. These bits are read-only.

3.2.10 Endpoint 0 Receive Byte Count Register

7							0
–	–	–	–	BCNT3	BCNT2	BCNT1	BCNT0

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	–	Reserved	Reserved for future use.
3:0	BCNT(3:0)	Receive byte count	The receive byte count register is loaded with the number of bytes in the data packet received into the endpoint 0 receive FIFO for a valid Setup Stage transaction or OUT Transaction. The receive FIFO byte count register does not decrement as data is read from the FIFO. These bits are read-only and are cleared by power-on reset.

3.2.11 Endpoint 0 Receive Control Register

The receive control register is used to store bits which control various functions and operating modes of the Function Interface Logic within the TUSB2140 device.

7							0
RXCLR	–	–	–	RXSTL	–	RXFEN	RXEN

BIT	MNEMONIC	NAME	DESCRIPTION
7	RXCLR	Receive clear	The receive clear bit is set to reset the receive FIFO pointers and flags. This bit should be set in response to a receive FIFO over–run or under-run condition. After the FIFO pointers are reset, this bit will be automatically cleared. In addition, the FIFO empty flag will be set and the other FIFO flags will be cleared upon completion of the FIFO reset. This bit is read/write and is cleared by power-on reset.
6	–	Reserved	Reserved for future use.
5	–	Reserved	Reserved for future use.
4	–	Reserved	Reserved for future use.
3	RXSTL	Receive stall	The receive stall bit is set to enable a STALL handshake to be returned in response to the next valid OUT Transaction. This bit does not effect a Setup Stage Transaction. The Setup Stage Transaction must always be accepted, unless there is a data packet error or a time out error, so that a Clear Feature Endpoint Stall request can be received from the host. This bit is automatically cleared if a new Setup Stage Transaction is successfully received. This bit is read/write and is cleared by power-on reset.
2	–	Reserved	Reserved for future use.
1	RXFEN	Receive FIFO enable	The receive FIFO enable bit is set to enable the reception of data into the receive FIFO when the next valid OUT Transaction occurs. This bit is automatically cleared when the local EP0 receive acknowledge status bit (ACK) is set. This bit is also automatically cleared if a new Setup Stage Transaction is successfully received or the EP0 receive clear bit (RXCLR) is set. If the receive enable bit is not set, the device returns a NACK handshake. If the receive stall control bit (RXSTL) is set, a STALL handshake is returned instead of a NACK handshake. This bit does not effect a Setup Stage Transaction. The Setup Stage Transaction must always be accepted, unless there is a data packet error or a time-out error. This bit is read/write and is cleared by power-on reset.
0	RXEN	Receive enable	The receive enable bit is set to enable the receive endpoint. For endpoint 0, the Control Endpoint, both a receive and transmit endpoint are required. Therefore, the transmit enable and receive enable bits must both be set before the device will be enumerated. If either of these bits are not set, the function port will remain in the disconnected state. This bit is read/write and is cleared by power-on reset.

3.2.12 Endpoint 0 Receive Status Register

The receive status register is used to store bits which report status information about the operating conditions of the Function Control Logic within the TUSB2140 device.

7							0
RXSEQ	SETUP	RXFSW	STSGE	STALL	NACK	ERROR	ACK

BIT	MNEMONIC	NAME	DESCRIPTION
7	RXSEQ	Receive sequence	The receive sequence bit is toggled by the Function Control Logic at the end of an Out Data Stage Transaction if a valid data packet is received and the data packet PID matches the expected PID. The receive sequence bit is initialized to a '1' at the end of a successful Setup Stage Transaction. This bit is read-only and is cleared by power-on reset.
6	SETUP	Setup stage transaction	The setup stage transaction bit is set at the end of a successful Setup Stage Transaction to indicate that the data packet in the receive FIFO is a Setup Stage Transaction data packet. This bit is cleared by writing a "1" to this register. To read the receive FIFO, the local MCU must first clear the Setup Stage Transaction bit (SETUP). This bit is read/write and is cleared by power-on reset.
5	RXFSW	Receive FIFO setup stage transaction data packet write	The receive FIFO Setup Stage Transaction data packet write bit is set at the beginning of a Setup Stage Transaction and is cleared at the end of Setup Stage Transaction. This bit indicates that the receive FIFO is being over-written with data from the Setup Stage Transaction data packet. This bit, in conjunction with the setup stage bit (SETUP), is used to indicate when a new Setup Stage Transaction has occurred and data in the receive FIFO from a previous Out Data Stage Transaction may have been over-written. This bit is read-only and is cleared by power-on reset.
4	STSGE	In status stage	The in status stage bit is set when the Function Control Logic detects the Status Stage Transaction of a Control Transfer. This bit will be automatically cleared at the beginning of the next Setup Stage Transaction. This bit is read-only and is cleared by power-on reset.
3	STALL	Stall	The stall status bit is set at the end of an Out Transaction if a STALL handshake packet is returned to the host. The Function Control Logic will automatically return a STALL handshake to the host if a valid Out Transaction is received and the receive stall control bit is set. This stall status bit will automatically be updated at the end of the next valid Out Transaction. This bit is read-only and is cleared by power-on reset.
2	NACK	No acknowledge	The no acknowledge status bit is set at the end of an Out Transaction if a NACK handshake packet is returned to the host. The Function Control Logic will automatically return a NACK handshake to the host if a valid Out Transaction is received and the receive FIFO enable bit has not been set. This bit will be automatically updated at the end of the next valid Out Transaction. This bit is read-only and is cleared by power-on reset.
1	ERROR	Error	The error status bit is set at the end of an Out Transaction if a timeout, bit-stuff, CRC, force receive or other errors occur. This bit will be automatically updated at the end of the next valid Out Transaction. This bit is read-only and is cleared by power-on reset.
0	ACK	Acknowledge	The acknowledge status bit is set at the end of an Out Transaction if the data packet was received successfully and an acknowledge handshake was sent to the host. When this bit is set, the endpoint 0 receive interrupt bit is also set. The acknowledge status bit should be cleared by the local MCU in order to clear the interrupt condition. This bit will be automatically cleared at the beginning of the next Setup Stage Transaction. This bit is read/write and is cleared by power-on reset.

3.2.13 Endpoint 0 Receive FIFO Flags Register

The receive FIFO flags register is used to store bits which report status information about the receive FIFO operating condition.

7							0
–	–	–	–	EMPT	FULL	UNDR	OVRR

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	–	Reserved	Reserved for future use.
3	EMPT	Receive FIFO empty	The receive FIFO empty flag is set when the receive FIFO is empty. This bit is cleared when the FIFO is no longer empty. This bit is read-only and is set by power-on reset.
2	FULL	Receive FIFO full	The receive FIFO full flag is set when the receive FIFO is full. This bit is cleared when the FIFO is no longer full. This bit is read-only and is cleared by power-on reset.
1	UNDR	Receive FIFO under-run	The receive FIFO under-run flag is set when the receive FIFO is empty and when the local MCU attempts to read a byte from the FIFO. When this bit is set, the endpoint 0 receive interrupt bit is also set. To clear the FIFO under-run condition, the receive FIFO clear control bit should be set. After the FIFO has been cleared, this bit and the endpoint 0 receive interrupt bit will be automatically cleared. This bit is read-only and is cleared by power-on reset.
0	OVRR	Receive FIFO over-run	The receive FIFO over-run flag is set when the receive FIFO is full and the Function Control Logic attempts to write another byte to the FIFO. When this bit is set, the endpoint 0 receive interrupt bit is also set. To clear the FIFO over-run condition, the receive FIFO clear control bit should be set. After the FIFO has been cleared, this bit and the endpoint 0 receive interrupt bit will be automatically cleared. This bit is read-only and is cleared by power-on reset.

3.2.14 Endpoint 1 Transmit FIFO

7							0
D7	D6	D5	D4	D3	D2	D1	D0

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	D(7:0)	Transmit FIFO data	Endpoint 1 transmit FIFO data is written to the transmit FIFO on a byte-to-byte basis. These bits are write-only.

3.2.15 Endpoint 1 Transmit Byte Count Register

7							0
–	–	–	–	BCNT3	BCNT2	BCNT1	BCNT0

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	–	Reserved	Reserved for future use.
3:0	BCNT(3:0)	Transmit byte count	The transmit byte count register should be loaded with the number of bytes to be transmitted. The byte count should be the number of bytes in the data packet that was loaded into the transmit FIFO. When the local MCU writes to the byte count register, the EP1 transmit FIFO enable bit (TXFEN) will automatically be set. Also, the byte count register does not decrement as data is transmitted. These bits are read/write and are cleared by power-on reset.

3.2.16 Endpoint 1 Transmit Control Register

The transmit control register is used to store bits which control various functions and operating modes of the Function Interface Logic within the TUSB2140 device.

7							0
TXCLR	TXSOW	–	–	TXSTL	–	TXFEN	TXEN

BIT	MNEMONIC	NAME	DESCRIPTION
7	TXCLR	Transmit clear	The transmit clear bit is set to reset the transmit FIFO pointers and flags. This bit should be set in response to a transmit FIFO over–run or under-run condition. After the FIFO pointers are reset, this bit will be automatically cleared. In addition, the FIFO empty flag will be set and the other FIFO flags will be cleared upon completion of the FIFO reset. This bit is read/write and is cleared by power-on reset.
6	TXSOW	Transmit sequence bit over-write	The transmit sequence bit over-write bit is set to enable the local MCU to write to the transmit sequence bit (TXSEQ). See the EP1TX Transmit Status Register. This bit is read/write and is cleared by power-on reset.
5	–	Reserved	Reserved for future use.
4	–	Reserved	Reserved for future use.
3	TXSTL	Transmit stall	The transmit stall bit is set to enable a STALL handshake to be returned in response to the next valid In Transaction. This bit is read/write and is cleared by power-on reset.
2	–	Reserved	Reserved for future use.
1	TXFEN	Transmit FIFO enable	The transmit FIFO enable bit is set to enable the transmission of data in the transmit FIFO when the next valid In Transaction occurs. This bit is automatically set when the local MCU writes to the EP1 transmit byte count register and is automatically cleared when the EP1 transmit acknowledge status bit (ACK) is set. This bit is also automatically cleared if the EP1 transmit clear bit (TXCLR) is set. If the transmit enable bit is not set, the device returns a NACK handshake. If the transmit stall control bit (TXSTL) is set, a STALL handshake is returned instead of a NACK handshake. This bit is read/write and is cleared by power-on reset.
0	TXEN	Transmit enable	The transmit enable bit is set to enable the transmit endpoint. This bit is read/write and is cleared by power-on reset.

3.2.17 Endpoint 1 Transmit Status Register

The transmit status register is used to store bits which report status information about the operating conditions of the Function Control Logic within the TUSB2140 device.

7							0
TXSEQ	–	–	–	STALL	NACK	ERROR	ACK

BIT	MNEMONIC	NAME	DESCRIPTION
7	TXSEQ	Transmit sequence	The transmit sequence bit value determines the data packet PID to be used for the next data packet to be transmitted during the next In Data Stage Transaction. This bit is automatically toggled at the end of a successful In Transaction. If this bit is a '0', a DATA0 PID is sent in the data packet. If this bit is a '1', a DATA1 PID is sent in the data packet. The local MCU can write to this bit if the transmit sequence bit over-write (TXSOW) is set. This bit is read/write and is cleared by power-on reset.
6	–	Reserved	Reserved for future use.
5	–	Reserved	Reserved for future use.
4	–	Reserved	Reserved for future use.
3	STALL	Stall	The stall status bit is set at the end of an In Transaction if a STALL handshake packet is returned to the host instead of a data packet. The Function Control Logic will automatically return a STALL handshake to the host if a valid In Transaction is received and the transmit stall control bit is set. This stall status bit will be automatically updated at the end of the next valid In Transaction. This bit is read-only and is cleared by power-on reset.
2	NACK	No acknowledge	The no acknowledge status bit is set at the end of an In Transaction if a NACK handshake packet is returned to the host instead of a data packet. The Function Control Logic will automatically return a NACK handshake to the host if a valid In Transaction is received and there is not a data packet in the transmit FIFO ready to be transmitted. This bit will be automatically updated at the end of the next valid In Transaction. This bit is read-only and is cleared by power-on reset.
1	ERROR	Error	The error status bit is set at the end of an In Transaction if a timeout, bit-stuff, CRC, force transmit or other errors occur. This bit will be automatically updated at the end of the next valid In Transaction. This bit is read-only and is cleared by power-on reset.
0	ACK	Acknowledge	The acknowledge status bit is set at the end of an In Transaction if the data packet in the transmit FIFO was sent successfully and an acknowledge handshake was received from the host. When this bit is set, the endpoint 1 transmit interrupt bit is also set. The acknowledge status bit should be cleared by the local MCU in order to clear the interrupt condition. This bit is read/write and is cleared by power-on reset.

3.2.18 Endpoint 1 Transmit FIFO Flags Register

The transmit FIFO flags register is used to store bits which report status information about the transmit FIFO operating condition.

7							0
–	–	–	–	EMPT	FULL	UNDR	OVRR

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	–	Reserved	Reserved for future use.
3	EMPT	Transmit FIFO empty	The transmit FIFO empty flag is set when the transmit FIFO is empty. This bit is cleared when the FIFO is no longer empty. This bit is read-only and is set by power-on reset.
2	FULL	Transmit FIFO full	The transmit FIFO full flag is set when the transmit FIFO is full. This bit is cleared when the FIFO is no longer full. This bit is read-only and is cleared by power-on reset.
1	UNDR	Transmit FIFO under-run	The transmit FIFO under-run flag is set when the transmit FIFO is empty and the Function Control Logic attempts to read another byte from the FIFO. This will happen if the number of bytes actually written to the transmit FIFO is less than the value loaded into the transmit byte count register. When this bit is set, the endpoint 1 transmit interrupt bit is also set. To clear the FIFO under-run condition, the transmit FIFO clear control bit should be set. After the FIFO has been cleared, this bit and the endpoint 1 transmit interrupt bit will be automatically cleared. This bit is read-only and is cleared by power-on reset.
0	OVRR	Transmit FIFO over-run	The transmit FIFO over-run flag is set when the transmit FIFO is full and the local MCU attempts to write another byte to the FIFO. When this bit is set, the endpoint 1 transmit interrupt bit is also set. To clear the FIFO over-run condition, the transmit FIFO clear control bit should be set. After the FIFO has been cleared, this bit and the endpoint 1 transmit interrupt bit will be automatically cleared. This bit is read-only and is cleared by power-on reset.

4 Device Operation

The operation of the TUSB2140 is explained in the following sections. For additional information on USB, please refer to the Universal Serial Bus Specification version 1.0 dated January 19, 1996. Chapter 11 of the specification contains very detailed information on the hub operations.

4.1 Device Initialization

When a power-on reset is applied to the TUSB2140, the device is automatically configured as a stand-alone hub with five downstream ports. In addition, all of the registers associated with the embedded function are initialized as defined in Section 3.2, Register Functional Descriptions. Both the hub and the embedded function power-up with a default function address of zero, and the embedded function is disconnected. To connect the embedded function to the downstream port 5 of the hub, the MCU must set the receive enable bit (RXEN) to 1 and the transmit enable bit (TXEN) to a 1.

4.2 Hub

The hub within the TUSB2140 supports a maximum of 4 external downstream ports and the embedded function. If the embedded function is not connected to downstream port 5, then the hub functions as a four port stand-alone device. The hub is a separate logical device and contains a seperate control endpoint and interrupt endpoint from the embedded function. The hub automatically handles all USB standard device commands addressed to the hub function address. Because the hub is a state machine approach instead of being based on a micro-controller, the only software required to support the hub function is the generic USB driver, on the host side, that supports the hub-class.

4.3 Embedded Function

The embedded function within the TUSB2140 supports USB control and interrupt data transfers by providing FIFOs, control/status registers, and the USB bus interface to be used by a local MCU. The embedded function is a separate logical device, and therefore, the embedded function requires a unique function address. To enumerate the embedded function, the TUSB2140 hub must first be enumerated and configured. In additon, the embedded function must be connected to downstream port 5 of the hub, which is accomplished by setting the embedded function endpoint 0 receive enable bit (RXEN) and transmit enable bit (TXEN) to a 1.

4.3.1 Interrupt Handler

The interrupt handler monitors the various conditions that can cause interrupts and asserts the appropriate interrupt bit when an interrupt condition is pending. If one or more of the interrupt bits are set, the TUSB2140 interrupt output signal ($\overline{IRQ}$) will be asserted until the interrupt condition(s) is cleared. The interrupt bits are enabled by setting the corresponding bit in the interrupt mask register. If the interrupt mask bit is cleared, the corresponding interrupt bit will still be set when an interrupt condition occurs. However, the $\overline{IRQ}$ output signal will not be asserted. This feature is provided for systems that detect pending interrupt conditions with a polling scheme rather than monitoring the $\overline{IRQ}$ output signal.

4.3.2 USB Reset

To reset the embedded function, the host initiates a port reset on the function port which sets the function reset interrupt bit. When a function reset occurs, all of the function interface logic within the TUSB2140 will be reset except the endpoint 0 receive enable bit (RXEN), the endpoint 0 transmit enable bit (TXEN), the function reset interrupt bit (FRST) and all of the interrupt mask bits. When a USB reset occurs, the local MCU should respond by setting the default configuration then clearing the FRST interrupt bit.

4.3.3 Enumeration

After enumeration of the hub and the connection of the embedded function, the host should enable, reset, and set the function address of the embedded function. To enable the port, the host should first power-on the port, which should result in the PWRON5 output signal being asserted. When the embedded function has been enabled, the function enabled bit (FEN), bit 7 of the function address register, will also be set. When the host initiates the port reset for the embedded function, the function reset bit (FRST), bit 3 of the interrupt register, will be set. If the corresponding mask bit is a 1, then the IRQ output signal will be asserted. The local MCU should respond to the FRST by setting the default configuration for the device and then clearing the FRST interrupt bit. To set the function address, the host should initiate the set address command. The embedded function will automatically decode the set address command and set the function address within the embedded function to the address requested by the host.

4.3.4 Control Transfers

Control transfers to the embedded function require multiple transactions which use both the embedded function endpoint 0 receive and transmit endpoints. The three types of control transfers are Control Write, Control Write with No-Data Stage and Control Read. All USB commands, except the set address command, are passed by the embedded function logic to the local MCU which does the decoding. The set address command is handled completely by the embedded function. After the set address command is complete, the function address can be read by the local MCU from the function address register (see *Firmware Development Flow Diagram* in Appendix A).

4.3.4.1 Control Read Transfers

A Control Read Transfer is used by the host to read data from the embedded function. A Control Read Transfer requires a Setup Stage Transaction, at least one In Data Stage Transaction, and an Out Status Stage Transaction. As a result, the Setup Stage Transaction and the Out Status Stage Transaction use the endpoint 0 receive endpoint and the In Data Stage Transactions use the endpoint 0 transmit endpoint.

4.3.4.2 Control Write Transfers

A Control Write Transfer is used by the host to write data to the embedded function. A Control Write Transfer requires a Setup Stage Transaction, at least one Out Data Stage Transaction, and an In Status Stage Transaction. As a result, the Setup Stage Transaction and the Out Data Stage Transactions use the endpoint 0 receive endpoint and the In Status Stage Transaction uses the endpoint 0 transmit endpoint.

4.3.4.3 Control Write Transfers with No-Data Stages

A Control Write Transfer with No-Data Stages is used by the host to write data to the embedded function. A Control Write Transfer with No-Data Stages requires a Setup Stage Transaction, no Data Stage Transactions, and an In Status Stage Transaction. As a result, the Setup Stage Transaction uses the endpoint 0 receive endpoint and the In Status Stage Transaction uses the endpoint 0 transmit endpoint. The data written to the function by the host is contained in the Setup Stage Transaction data packet and is limited to two bytes.

4.3.5 Interrupt Transfers

The transfer of interrupt type data is accomplished by the TUSB2140 using the interrupt endpoint, which is transmit endpoint 1. In addition to the endpoint 1 transmit FIFO, the operation of transmit endpoint 1 requires the use of 4 registers, which are the endpoint 1 TX byte count register, TX control register, TX status register and TX FIFO flags register.

The steps to be followed to transfer interrupt data are as follows:

1. The local MCU loads the data packet to be transmitted into the endpoint 1 transmit FIFO. The endpoint 1 transmit FIFO is 8 bytes deep, and therefore, the maximum data packet size is 8 bytes. If a FIFO over-run occurs while loading the data packet, the MCU sets the FIFO clear bit (TXCLR) to clear the FIFO. After the over-run condition is cleared, the MCU loads the data packet into the

FIFO again. The FIFO over-run condition results in the FIFO over-run bit (OVRR) being set and the endpoint 1 transmit interrupt bit (EP1TX) being set. The FIFO clear bit (TXCLR) is cleared automatically after the FIFO clear is complete. The MCU should poll the FIFO clear bit to determine when the FIFO clear is complete. After the FIFO clear is complete, the MCU should clear the FIFO over-run bit (OVRR), which automatically clears the endpoint 1 transmit interrupt bit (EP1TX).

2. Next, the local MCU loads the data packet byte count into the endpoint 1 transmit byte count register. Writing the byte count automatically sets the transmit FIFO enable bit (TXFEN) to enable the FCL to send the data packet when the next endpoint 1 In Transaction occurs.

3. At the end of the In Transaction, if the data packet was sent successfully and an acknowledge (ACK) handshake was received from the host, the acknowledge status bit (ACK) and the endpoint 1 transmit interrupt bit (EP1TX) are set. First the interrupt register is read to determine that an endpoint 1 transmit interrupt (EP1TX) has occurred. Then the status register is read to determine that the source of the interrupt was the acknowledge bit (ACK). Note that the transmit FIFO enable bit (TXFEN) is automatically cleared when the ACK bit is set. Finally, the MCU clears the acknowledge status bit (ACK), which automatically clears the interrupt bit (EP1TX).

4.3.6 Suspend and Remote Wake-up

The TUSB2140 embedded function supports both suspend and remote wake-up. The ability to support remote wake-up should be reported by the function to the host in the configuration descriptor for the embedded function. In addition, the host should be able to enable and disable the remote wake-up feature using the Set Feature Device and Clear Feature Device commands.

The TUSB2140 will assert the function suspend interrupt bit (FSUSP) if either a global suspend of the entire bus or a selective suspend of the embedded function is detected by the hub. In order for the TUSB2140 to enter a low power suspend state, the local MCU must clear the FSUSP bit. In the low power suspend state, the power control logic within the TUSB2140 will assert the function suspend output signal, FUNCSUSP. In addition, to reduce power consumption to a minimum, the TUSB2140 will disable all clocks including the CLKOUT output signal. If the embedded function is not connected to the hub, the power control logic will enter the low power suspend state and will disable the clocks without interaction from the local MCU. The FUNCSUSP output signal will still be asserted when the low power suspend state is active to indicate a bus suspend.

The remote wake-up function allows the local MCU or other logic to initiate a wake-up telling the host to resume USB operations. To initiate the remote wake-up, the active high WAKEUP input signal to the TUSB2140 should be asserted as shown in Figure 5–12.

4.3.7 I^2C Interface

The TUSB2140 uses a bi-directional two-wire serial interface to access the internal registers and FIFOs used for the embedded function operations. This serial interface is compatible with the I^2C (Inter IC) bus protocol and supports both 100 kbps and 400 kbps data transfer rates. The TUSB2140 is a slave only device on the bus with an assigned I^2C device address as shown below in Table 4–1.

Table 4–1. I^2C Device Address

A6	A5	A4	A3	A2	A1	A0	R/W
0	1	0	1	1	1	0	

4.3.7.1 Data Transfers

The two-wire serial interface uses the serial clock signal, SCL, and the serial data signal, SDA. As stated above, the TUSB2140 is a slave only device, and therefore, the SCL signal is an input only. The SDA signal is a bi-directional signal that uses an open-drain output to allow the TUSB2140 to be wire-ORed with other devices that use open-drain or open-collector outputs.

All read and write data transfers on the serial bus are initiated by a master device. The master device is also responsible for generating the clock signal used by the TUSB2140 for all data transfers. The data is transferred on the bus serially one bit at a time. However, the protocol requires that the address and data information be transferred in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus.

The timing relationship between the SCL and SDA signals for each bit transferred on the bus is shown in Figure 5–5. As shown, the SDA signal must be stable while the SCL signal is high, which also means that the SDA signal can only change states while the SCL signal is low.

The timing relationship between the SCL and SDA signals for the start and stop conditions is shown in Figure 5–6. As shown, the start condition is defined as a high-to-low transition of the SDA signal while the SCL signal is high. Also, as shown, the stop condition is defined as a low-to-high transition of the SDA signal while the SCL signal is high.

When the TUSB2140 is the device receiving address or data information, the TUSB2140 will acknowledge each byte received by driving the SDA signal low during the acknowledge SCL period. During the acknowledge SCL period, the master device must stop driving the SDA signal. If the TUSB2140 is unable to receive a byte, the SDA signal will not be driven low and should be pulled high external to the TUSB2140 device. A high during the SCL period indicates a not-acknowledge to the master device. After receiving a not-acknowledge from the TUSB2140, the master device should generate a stop condition. The output acknowledge timing is shown in Figure 5–7.

Read and write data transfers to the TUSB2140 internal registers are done using single byte data transfers. However, read and write data transfers to the TUSB2140 internal FIFOs can be done with either single or multiple byte data transfers.

4.3.7.2 Single Byte Write

As shown in Figure 5–8, a single byte data write transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit (refer to Table 4–1). The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit should be a 0. After receiving the correct I^2C device address and the read/write bit, the TUSB2140 should respond with an acknowledge bit. Next, the master device should transmit the address byte corresponding to the TUSB2140 internal register or FIFO being accessed (see Section 3.1). After receiving the address byte, the TUSB2140 should again respond with an acknowledge bit. Next, the master device should transmit the data byte to be written to the register or FIFO being addressed. After receiving the data byte, the TUSB2140 should again respond with an acknowledge bit. Finally, the master device should transmit a stop condition to complete the single byte data write transfer.

4.3.7.3 Multiple Byte Write

A multiple byte data write transfer is identical to a single byte data write transfer except that multiple data bytes are transmitted by the master device to the TUSB2140 as shown in Figure 5–9. After receiving each data byte, the TUSB2140 should respond with an acknowledge bit.

4.3.7.4 Single Byte Read

As shown in Figure 5–10, a single byte data read transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit (refer to Table 4–1). For the data read transfer, both a write and a read are actually done. Initially, a write is done to transfer the address byte of the internal register or FIFO to be read. As a result, the read/write bit should be a 0. After receiving the I^2C device address and the read/write bit the TUSB2140 should respond with an acknowledge bit. Also, after sending the address byte, the master device should transmit another start condition followed by the I^2C device address and the read/write bit again. This time the read/write bit should be a 1 indicating a read transfer. After receiving the I^2C device address and the read/write bit the TUSB2140 should again respond with an acknowledge bit. Next, the TUSB2140 should transmit the data byte from the register or FIFO being addressed. After receiving the data byte, the master device should transmit a not-acknowledge followed by a stop condition to complete the single byte data read transfer.

4.3.7.5 Multiple Byte Read

A multiple byte data read transfer is identical to a single byte data read transfer except that multiple data bytes are transmitted by the TUSB2140 to the master device as shown in Figure 5–11. Except for the last data byte, the master device should respond with an acknowledge bit after receiving each data byte.

4.4 Over-current Detection and Power Switching

The TUSB2140 provides an active low over-current input signal for each downstream port including the embedded function. External circuitry is required to detect an over-current condition for each port and to assert the appropriate over-current input. When an over-current input is asserted using individual port power management, the TUSB2140 will de-assert the power-on output signal corresponding to the over-current input. The external circuitry should remove power from the appropriate downstream port when the power-on output is de-asserted. In addition, the over-current condition will be reported to the host by the TUSB2140 hub controller. If the ganged port power management mode is used, the GANGED input to the TUSB2140 is set to a 1, then the power-on outputs are all de-asserted at the same time, when any of the over-current inputs are asserted.

4.5 Clock Output Generation

The TUSB2140 generates a clock output signal, CLKOUT, that is synchronous to the 48 MHz crystal input. The CLKOUT signal frequency is selected using the two clock select inputs, CLKSEL0 and CLKSEL1. As shown in Table 4–2, the CLKOUT frequency can be selected to be 12 MHz, 8 MHz, 6 MHz or 4 MHz.

Table 4–2. Clock Output Signal Frequency

CLKSEL1	CLKSEL0	CLKOUT FREQUENCY
0	0	12 Mhz
0	1	8 Mhz
1	0	6 Mhz
1	1	4 Mhz

4.6 Power Supply Sequencing

Turning power supplies on and off with a mixed 5-V/3.3-V system is an important consideration. To avoid possible damage to the TUSB2140 device, proper power sequencing is required. The basic turn on requirement is that the 5-V and 3.3-V power supplies should start ramping from 0 V and reach 95 percent of the final voltage values within 25 ms of each other. The turn-off requirement is that the 5-V and 3.3-V power supplies should start ramping from the steady-state voltage and reach 5 percent of these values with 25 ms of each other. In addition, the difference between the two voltages should never exceed 3.6 V while turning on or off. Normally, in a mixed voltage system, the 3.3-V supply is generated from a voltage regulator running from the 5-V supply. A voltage regulator, such as TI's TPS7133, can be used to meet these power sequencing requirements.

5 Electrical Specifications

5.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, V_{CC}3V (see Note 1) . . . . . –0.5 V to 3.8 V
Supply voltage range, V_{CC}5V (see Note 1) . . . . . –0.5 V to 5.5 V
Input voltage range, V_I: (3.3 V_{CC}3V) . . . . . –0.5 V to V_{CC}3V + 0.5 V
(5 V_{CC}5V) . . . . . –0.5 V to V_{CC}5V + 0.5 V
Output voltage range, V_O (3.3 V_{CC}3V) . . . . . –0.5 V to V_{CC}3V + 0.5 V
Input clamp current, I_{IK}, (V_I < 0 V or V_I > V_{CC}3V) . . . . . ±20 mA
Output clamp current, I_{OK}, (V_O < 0 V or V_O > V_{CC}3V) . . . . . ±20 mA
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Operating free-air temperature range, T_A . . . . . –40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to GND.

5.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}3V	3	3.3	3.6	V
Supply voltage, V_{CC}5V	4.75	5	5.25	V
Input voltage, TTL/LVCMOS, V_I	0		V_{CC}3V	V
Input voltage, 5-V tolerant TTL, V_I	0		V_{CC}5V	V
Output voltage, TTL/LVCMOS, V_O	0		V_{CC}3V	V
High-level input voltage, signal-ended receiver, $V_{IH(REC)}$	2		V_{CC}3V	V
Low-level input voltage, signal-ended receiver, $V_{IL(REC)}$	0		0.8	V
High-level input voltage, TTL/LVCMOS, $V_{IH(TTL)}$	2		V_{CC}3V	V
High-level input voltage, 5-V tolerant TTL, $V_{IH(TTL)}$	2		V_{CC}5V	V
Low-level input voltage, TTL/LVCMOS, $V_{IL(TTL)}$	02		0.8	V
Low-level input voltage, 5-V tolerant TTL, $V_{IL(TTL)}$	0		0.8	V
Operating junction temperature, T_J	0		115	°C
External series, differential driver resistor, $R_{(DRV)}$	22 (–5%)		22 (+5%)	Ω
Operating (dc differential driver) high speed mode, $f_{(OPRH)}$			12	Mb/s
Operating (dc differential driver) low speed mode, $f_{(OPRL)}$			1.5	Mb/s
Common mode, input range, differential receiver, $V_{(ICR)}$	0.8		2.5	V
Input transition times, t_t, TTL/LVCMOS	0		6	ns

5.3 Electrical Characteristics Over Recommended Ranges of Operating Free-Air Temperature and Supply Voltage (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL/LVCMOS	I_{OH} = –4 mA	V_{CC}3V – 0.6	3.6	V
			I_{OH} = –0.1 mA	2.4		
		USB data lines	$R_{(DRV)}$ = 15 kΩ, to GND	2.8	3.6	
			I_{OH} = –12 mA (without $R_{(DRV)}$)	V_{CC} – 0.5		
V_{OL}	Low-level output voltage	TTL/LVCMOS	I_{OL} = 4 mA		0.5	V
		USB data lines	$R_{(DRV)}$ = 1.5 k Ω to 3.6 V		0.3	
			I_{OL} = 12 mA (without $R_{(DRV)}$)		0.5	
V_{IT+}	Positive input threshold voltage	TTL/LVCMOS			2	V
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V		1.8	V
$V_{IT–}$	Negative-input threshold voltage	TTL/LVCMOS		0.8		V
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V	1		V
V_{hys}	Input hysteresis† (V_{T+} – $V_{T–}$)	TTL/LVCMOS		0.25	0.7	V
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V	300	500	mV
I_{OZ}	High-impedance output current	TTL/LVCMOS	V = V_{CC} or GND‡		±10	µA
		USB data lines	0 V ≤ V_O ≤ V_{CC}		±10	µA
I_{OZH}	5–V tolerant, 3-state output, high-impedance state current		V_O = 5.5 V		85	µA
I_{IL}	Low-level input current	TTL/LVCMOS	V_I = GND		–1	µA
I_{IH}	High-level input current	TTL/LVCMOS	V_I = V_{CC}		1	µA
$z_{o(DRV)}$	Driver output impedance	USB data lines	Static V_{OH} or V_{OL}	7.1	19.9	Ω
V_{ID}	Differential input voltage	USB data lines	0.8 V ≤ V_{ICR} ≤ 2.5 V	0.2		V
I_{CC}	Input supply current		Normal operation		100	mA
			Suspend mode		1	µA

† Applies for input buffers with hysteresis
‡ Applies for open drain buffers

5.4 Timing Characteristics

5.4.1 Timing Characteristics for USB Transceivers

Full Speed Mode

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_r	Transition rise time for DP or DM	See Figure 5–1 and Figure 5–2	4	20	ns
t_f	Transition fall time for DP or DM	See Figure 5–1 and Figure 5–2	4	20	ns
$t_{(RFM)}$	Rise/fall time matching	(t_r/t_f) x 100	90	110	%
$V_{O(CRS)}$	Signal crossover output voltage		1.3	2.0	V

Low Speed Mode

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_r	Transition rise time for DP to DM	C_L = 50 pF to 350 pF, See Figure 1 and Figure 2	75	300	ns
t_f	Transition fall time for DP to DM	C_L = 50 pF to 350 pF, See Figure 1 and Figure 2	75	300	ns
$t_{(RFM)}$	Rise/fall time matching	(t_r/t_f) x 100	80	120	%
$V_{O(CRS)}$	Signal crossover output voltage	C_L = 50 pF to 350 pF	1.3	2.0	V

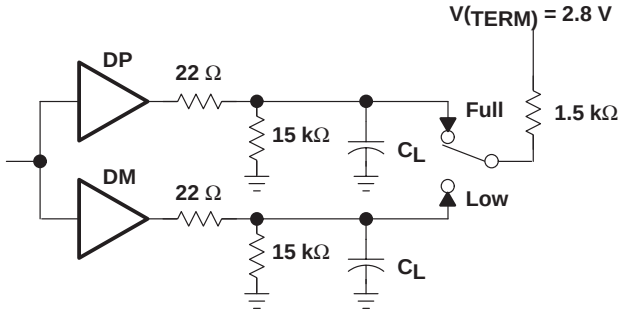


Figure 5–1. Differential Driver Switching Load

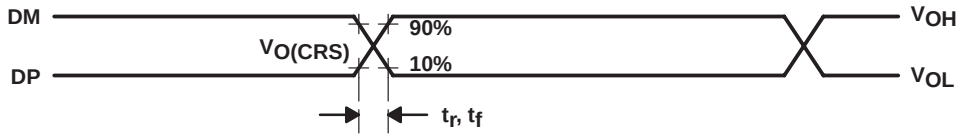


Figure 5–2. Differential Driver Timing Waveforms

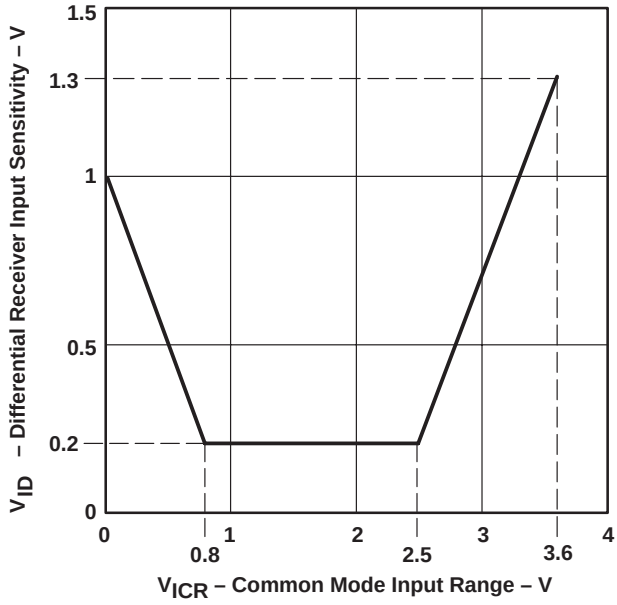


Figure 5–3. Differential Receiver Input Sensitivity vs. Common Mode Input Range

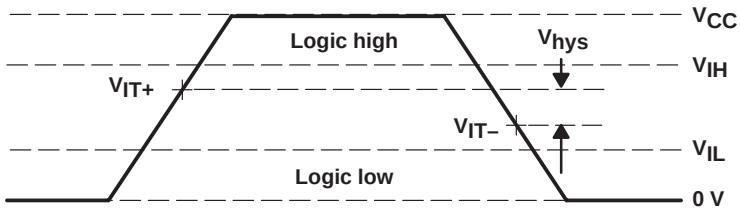


Figure 5–4. Single-Ended Receiver Input Signal Parameter Definitions

5.4.2 Timing Characteristics for I²C Interface

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNITS
			MIN	MAX	MIN	MAX	
f_{SCL}	Clock frequency, SCL		0	100	0	400	kHz
$t_{w(H)}$	Pulse duration, SCL high		4		0.6		µs
$t_{w(L)}$	Pulse duration, SCL low		4.7		1.3		µs
t_r	Rise time, SCL and SDA			1000		300	ns
t_f	Fall time, SCL and SDA			300		300	ns
t_{su1}	Setup time, SDA to SCL		250		100		ns
t_{h1}	Hold time, SCL to SDA		0		0		ns
t_{buf}	Bus free time between stop and start condition		4.7		1.3		µs
t_{su2}	Setup time, SCL to start condition		4.7		0.6		µs
t_{h2}	Hold time, start condition to SCL		4		0.6		µs
t_{su3}	Setup time, SCL to stop condition		4		0.6		µs

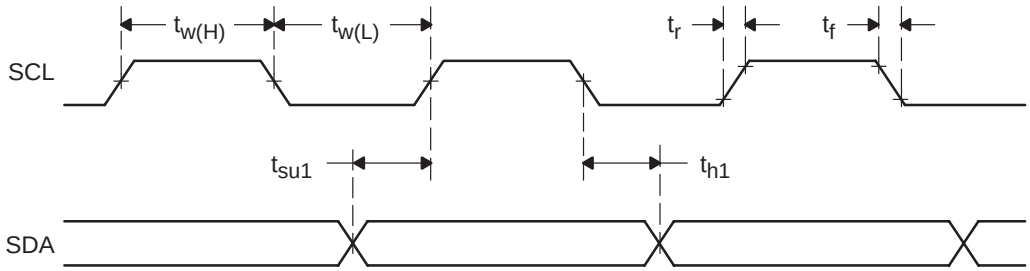


Figure 5–5. SCL and SDA Timing

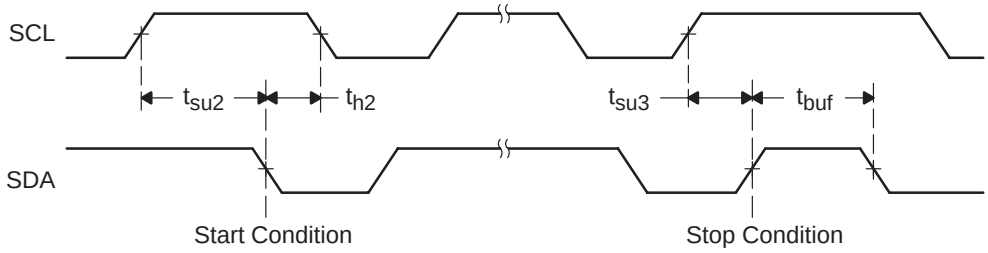


Figure 5–6. Start and Stop Conditions

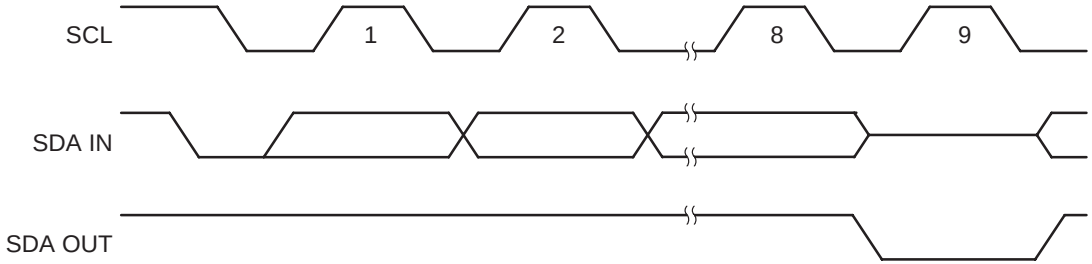


Figure 5–7. Output Acknowledge

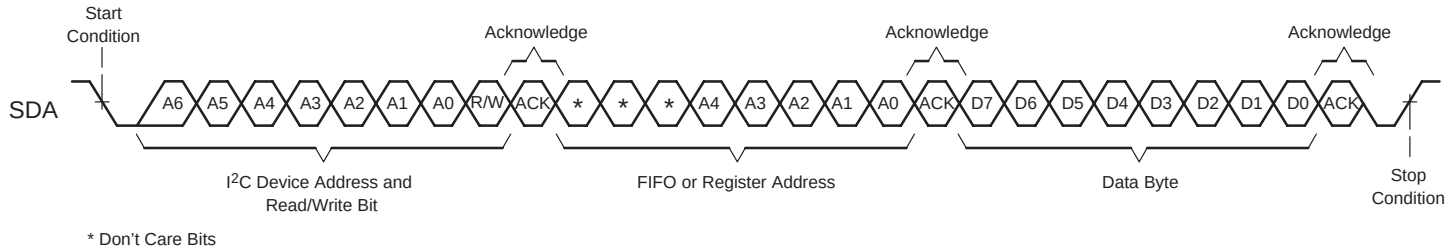


Figure 5–8. Single Byte Write Transfer

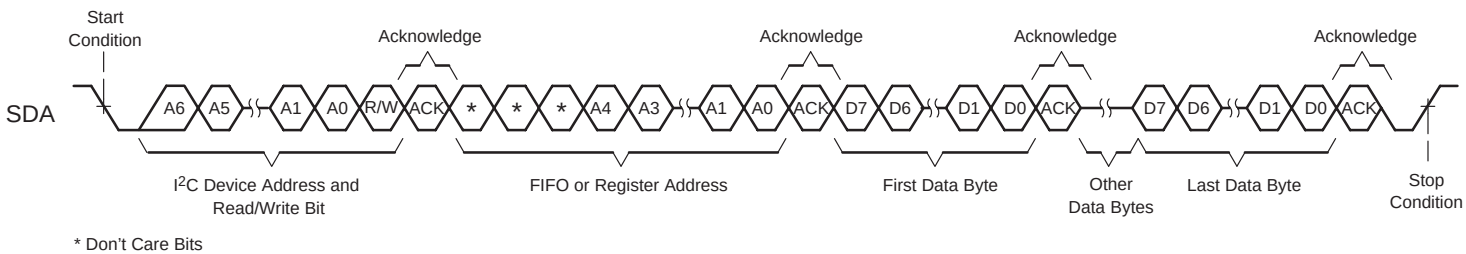


Figure 5–9. Multiple Byte Write Transfer

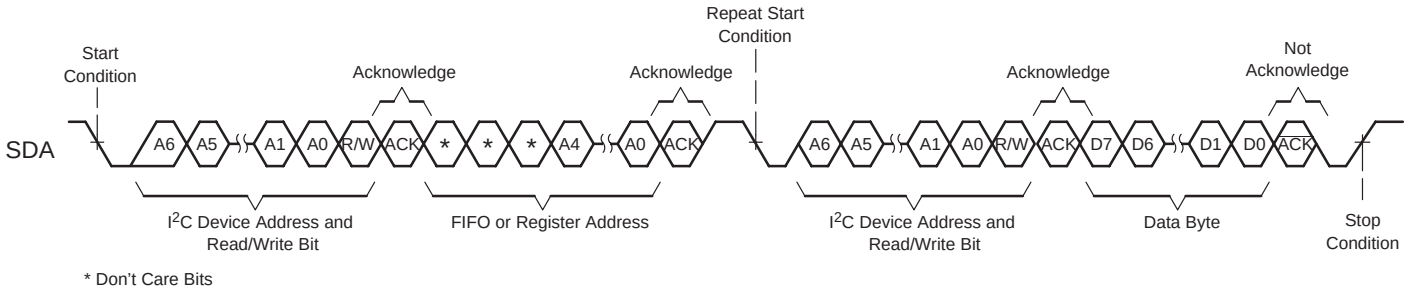


Figure 5–10. Single Byte Read Transfer

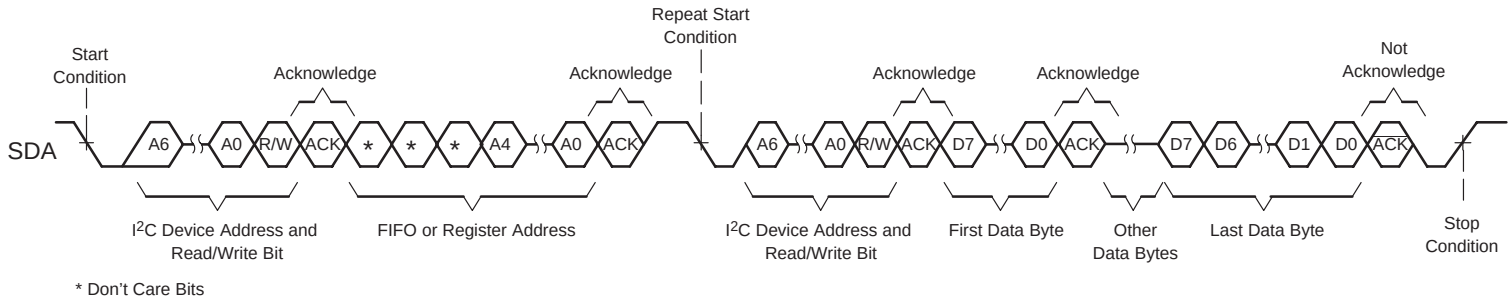


Figure 5–11. Multiple Byte Read Transfer

5.4.3 Timing Characteristics for Remote Wake-up

PARAMETER		TEST CONDITIONS	MIN	MAX	UNITS
$t_{w(H)}$	Pulse duration, WAKEUP high		0.6	10	µs

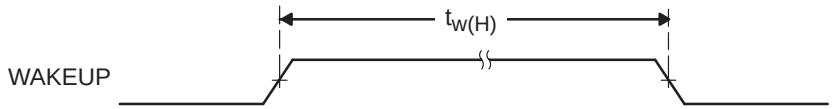


Figure 5–12. Remote Wake-Up

6 USB Overview Description

A major advantage of USB is the ability to connect 127 functions configured in up to 6 logical layers (tiers) to a single personal computer (See Figure 6–1).

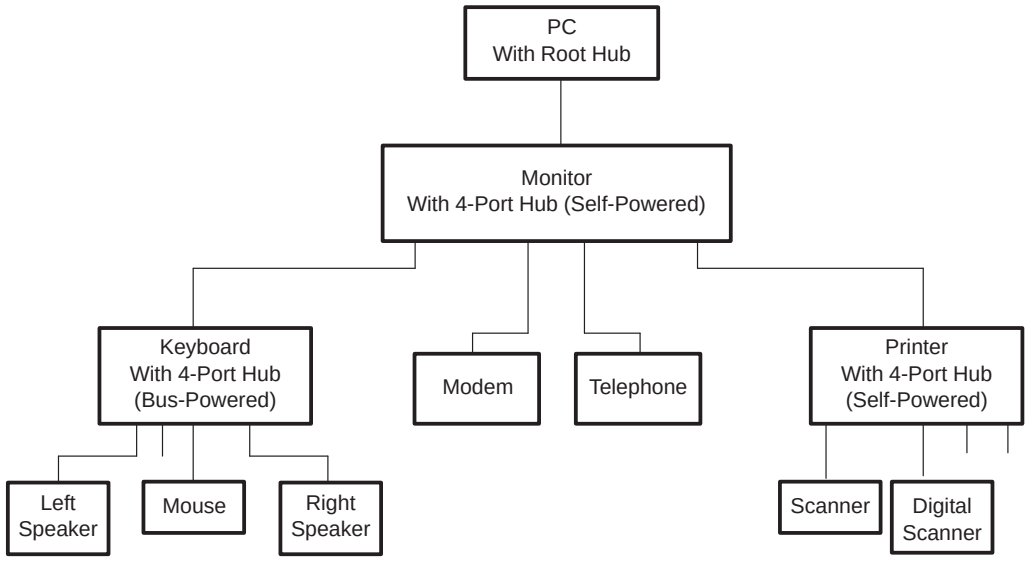


Figure 6–1. USB Tiered Configuration Example

Another advantage of USB is that all peripherals are connected using a standardized 4-wire cable which provides both communication and power distribution. The three power configurations are Bus-Powered, Self-Power and High-Power mode. For all three configurations, 100 mA is the maximum current that may be drawn from the USB 5 V line during power-up. For Bus-Power mode, a hub can draw a maximum of 500 mA from the 5 V line of the USB cable. A Bus-Powered hub must always be connected downstream to a Self-Powered hub unless it is the only hub connected to the PC and there are no High-Powered functions connected downstream. In the Self-Power mode, the hub is connected to its own power supply and can supply up to 500 mA to each downstream port. High-Powered functions may draw a maximum of 500 mA and may only be connected downstream to Self-Powered hubs.

Both Bus-Powered and Self-Powered hubs require over-current protection for all downstream ports. The two types of protection are individual port management (individual port basis) or ganged port management (multiple port basis). Individual port management requires power management devices for each individual downstream port, but adds robustness to your USB system because, in the event of an over-current condition, the USB Host will only power-down the port that has the condition. The ganged configuration uses fewer power management devices and thus has lower system costs, but in the event of an over-current condition on any of the downstream ports, all the ganged ports will be disabled by the USB Host.

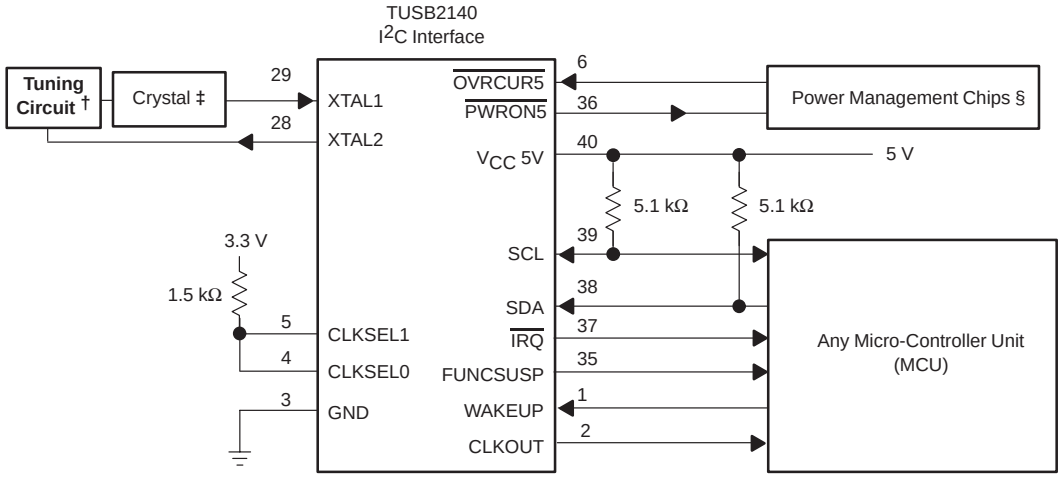
Using a combination of the $\overline{\text{BUSPWR}}$ and GANGED inputs, the TUSB2140 supports four modes of power management: Bus-Powered hub with either individual port power management or ganged port power management and the Self-Powered hub with either individual port power management or ganged port power management. Texas Instruments supplies the complete hub solution because we offer this TUSB2140, the TUSB2040 (4–port) and the TUSB2070 (7-port) hubs along with the power management chips needed to implement a fully USB Specification 1.0 compliant system. See Figure 6–4, 6–5 and 6–6 for example configurations.

6.1 Application Information

The following sections provide examples of how to connect the TUSB2140 chip for different working modes. The terminal number assigned for Figures 6–2, 6–4, 6–5 and 6–6 are for the TUSB2140N DIP package. If the TUSB2140PAG surface mount package is desired, see Section 1.2 for the correct pin-out. Figure 6–2 shows a typical application for the I^2C pin-out portion of the TUSB2140. Depending on the clock rate needed for the MCU, the specific pin configuration for CLKSEL0 and CLKSEL1 is listed on Table 4–2.

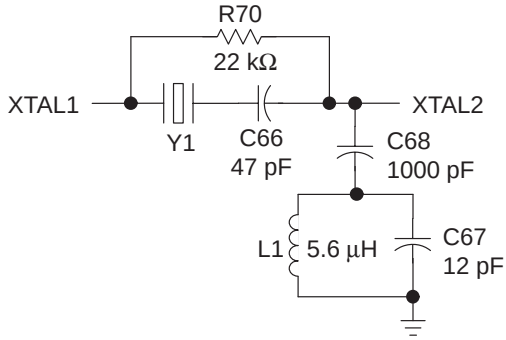
Since the first harmonic of most crystals is not 48-MHz, a tunning circuit such as in Figure 6–3 can be used to tune the crystal to 48-MHz which is required by the TUSB2140.

Figures 6–4, 6–5 and 6–6 show typical applications for the hub pin-out portion of the TUSB2140.



† Values for timing components are subject to change when using different crystals and PCBs·
‡ The crystal in this application is a 48–MHz US Crystal, P/N HC–18/U 48MHZ.
§ Depending on the application, connect as shown in Figures 6–4, 6–5, or 6–6.
NOTE: The CLKSEL1 and CLKSEL0 pins are configured for a 4.0 MHz output at the CLKOUT pin (see Table 4.2)
NOTE: Terminal numbers shown are for the N package

Figure 6–2. Typical I^2C Interface Connection to a Micro-Controller

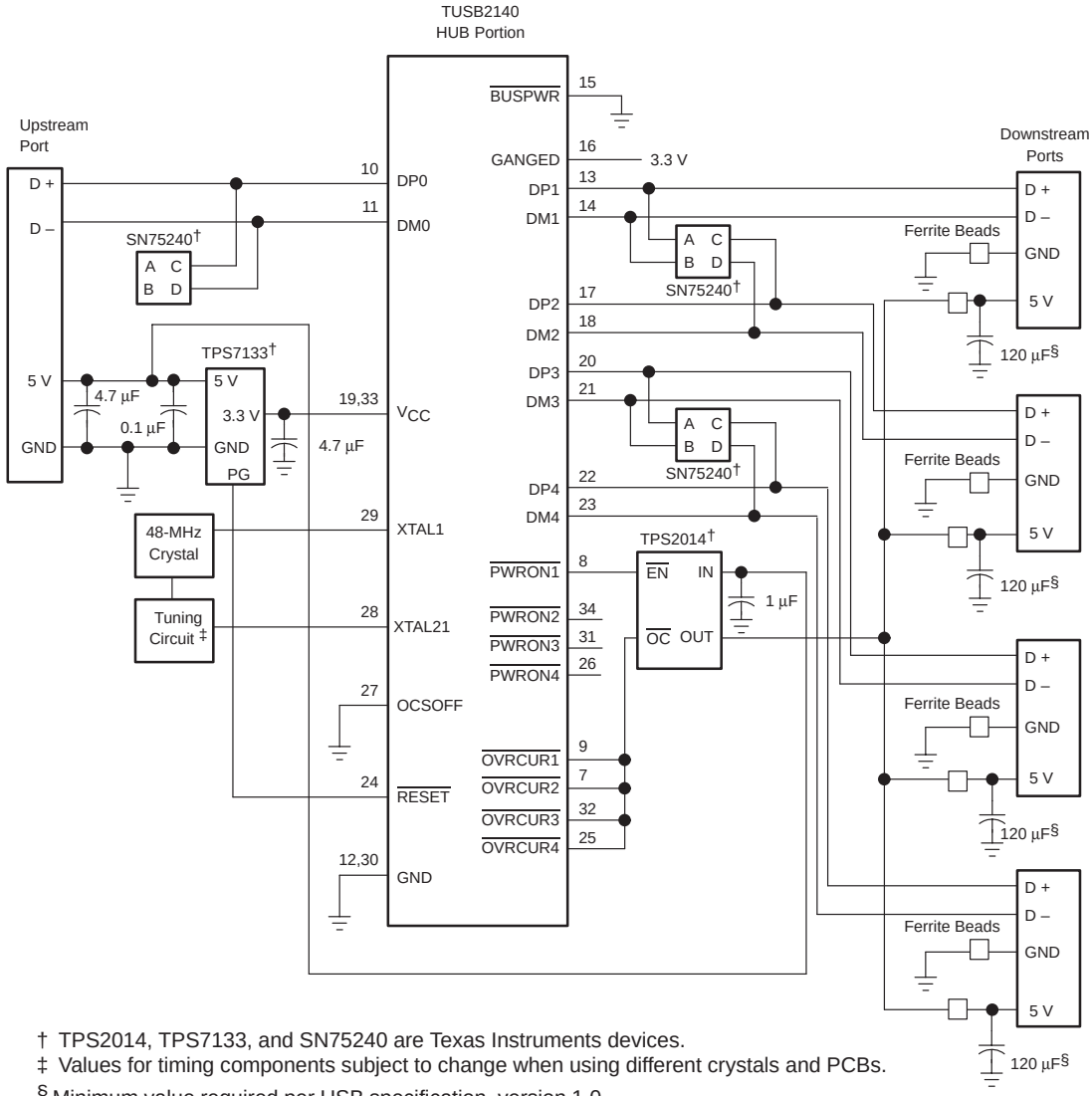


NOTES: A. When tuning the crystal (Y1) for different board implementations, the capacitor (C67) is subject to change. Other components should remain the same.

Figure 6–3. Typical Crystal Tuning Circuit for the TUSB2140 USB Device

6.2 Bus-powered Hub, Ganged Port Power Management

A bus-powered TUSB2140 supports up to four downstream USB ports and is capable of supplying 100 mA of current for devices connected to each downstream port. Bus-powered hubs must implement power switching. Ganged power management utilizes the TPS2014 power switch device and provides overcurrent protection for downstream ports. Individual SN75240 transient suppressors reduce in-rush current and voltage spikes. The TPS7133 low-dropout voltage regulator provides a Power Good (PG) signal for reset at power-up. $\overline{\text{OVRCUR1}}$ – $\overline{\text{OVRCUR5}}$ inputs must be tied together for ganged mode operation.

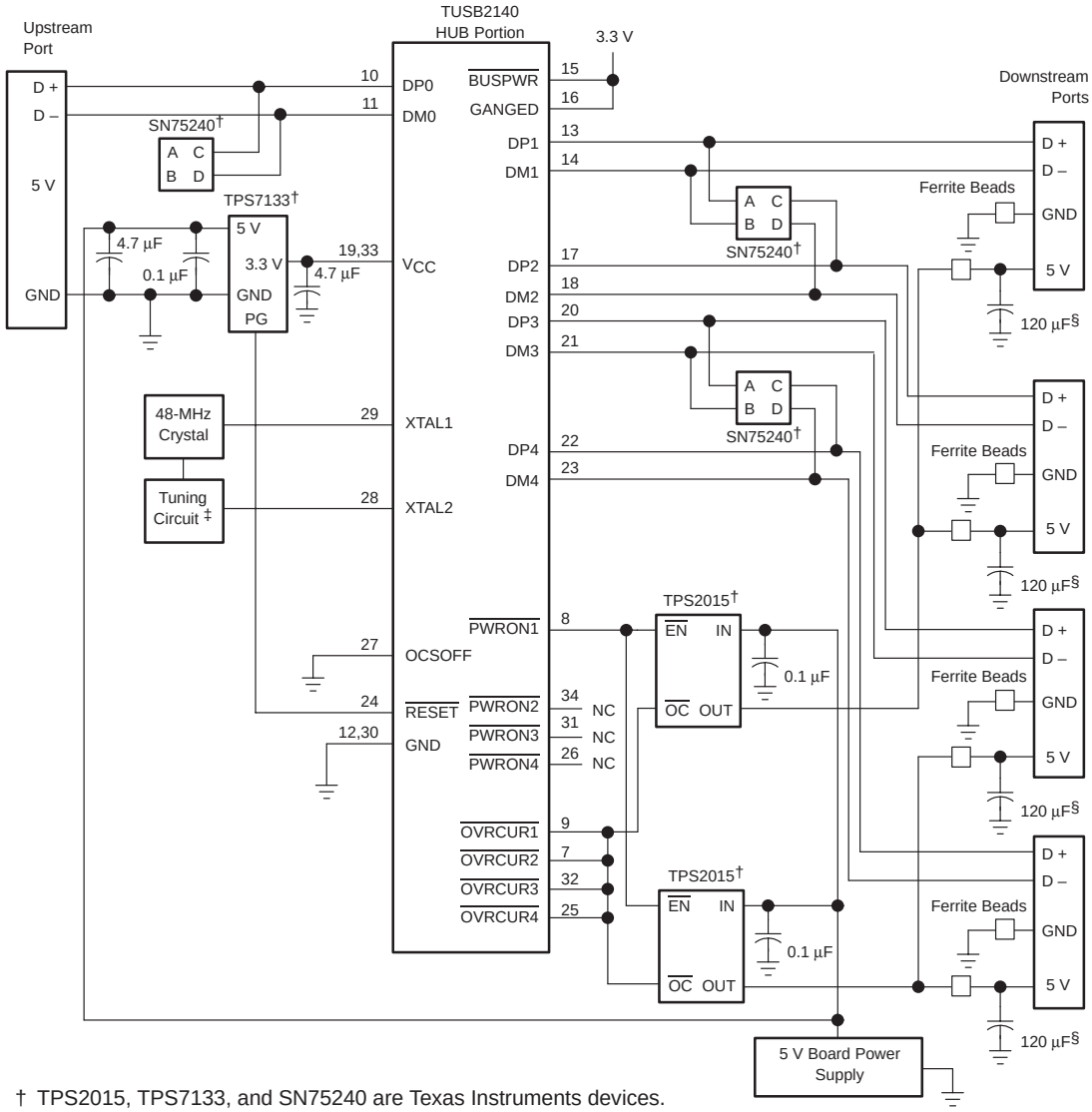


† TPS2014, TPS7133, and SN75240 are Texas Instruments devices.
‡ Values for timing components subject to change when using different crystals and PCBs.
§ Minimum value required per USB specification, version 1.0.
NOTE A: Terminal numbers shown are for the N package

Figure 6–4. TUSB2140 Bus-Powered Hub, Ganged Port Power Management Application

6.3 Self-powered Hub, Ganged Port Power Management

A self-powered TUSB2140 can also be implemented using ganged port power management. This implementation is similar to the individual power management except one TPS2015 provides power switching and overcurrent protection for two ports. Although this is a more economical solution, a fault on one downstream port will cause power to be removed from all downstream ports. The TPS7133 low-dropout voltage regulator provides a Power Good (PG) signal for reset at power-up. $\overline{\text{OVRCUR1}}$ – $\overline{\text{OVRCUR5}}$ inputs must be tied together for ganged mode operation.



† TPS2015, TPS7133, and SN75240 are Texas Instruments devices.
‡ Values for timing components subject to change when using different crystals and PCBs.
§ Minimum value required per USB specification, version 1.0.
NOTE A: Terminal numbers shown are for the N package

Figure 6–5. TUSB2140 Self-Powered Hub, Ganged Port Power Management Application

6.4 Self-powered Hub, Individual Port Power Management

A self-powered TUSB2140 is capable of supplying 500 mA of current for low-power or high-power devices connected to each downstream port. Self-powered hubs are required to implement overcurrent protection. Individual-port power management utilizes the TPS2014 power switching and overcurrent protection for each downstream port. Therefore, providing maximum robustness to the hub system. When the hub detects a downstream port fault, power is removed from the faulty port only, thus allowing other ports to continue normal operation. Individual SN75240 transient suppressors reduce in-rush current and voltage spikes. The TPS7133 low-dropout voltage regulator provides a Power Good (PG) signal for reset at power-up.

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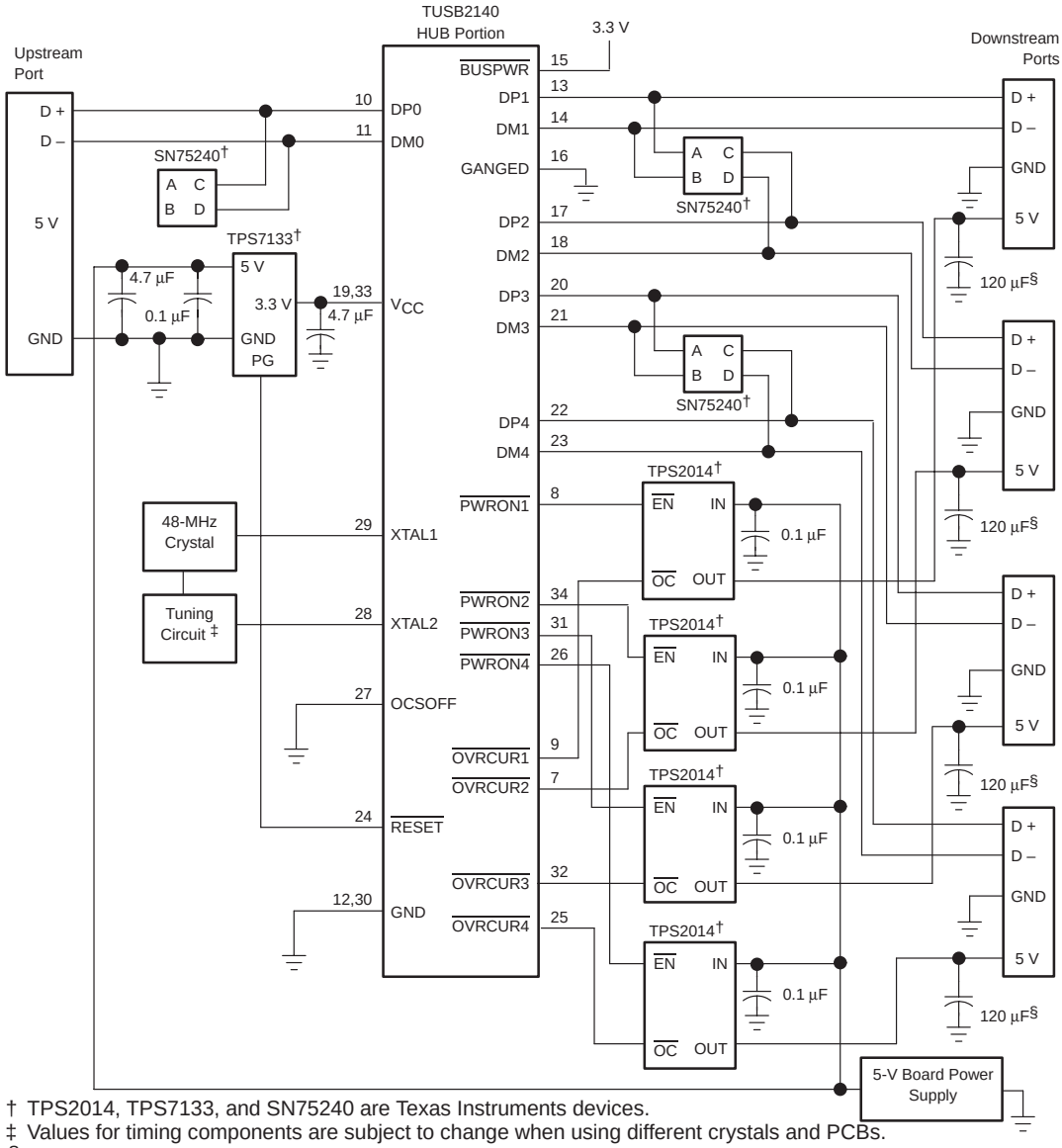


† TPS2014, TPS7133, and SN75240 are Texas Instruments devices.
‡ Values for timing components are subject to change when using different crystals and PCBs.
§ Minimum value required per USB specification, version 1.0.
NOTE A: Terminal numbers shown are for the N package

Figure 6–6. TUSB2140 Self-Powered Hub, Individual-Port Power Management Application

Appendix A
Firmware Development

Overview of Firmware

The flowchart for the main structure of the software program is depicted in Figure A-1. Power up causes all bits in the interrupt register to be set to zeros which then sets the pin $\overline{IRQ}$ = 1 (no interrupt). After power up, the embedded function must then be enabled (connected logically) to the hub. Enabling the embedded function results from enabling endpoint 0. Endpoint 0 is enabled by setting the EP0 TXEN and EP0 RXEN bits to 1. The interrupt mask register bits then need to be set to 1 in order to allow the corresponding bits of the interrupt register to assert the $\overline{IRQ}$ signal. Each bit of the interrupt register corresponds to a different interrupt that could occur. The interrupt routines are EP0 transmit, EP0 receive, EP1 transmit, function reset, and function suspend. If any of the five interrupt routines are not desired, the corresponding bit in the interrupt mask register should remain a 0, thus disabling the interrupt bit from asserting the $\overline{IRQ}$ signal. If the interrupt endpoint (endpoint 1) functionality is desired, the endpoint 1 enable bit (EP1EN) should be set.

Now that the proper bits have been set per the above paragraph, the micro-controller will then be in idle state and ready for an occurrence of an interrupt. Upon an interrupt ($\overline{IRQ}$=0), the MCU will read the value stored in the interrupt register and based on the value, it will execute one of the five interrupt routines. However, the host controller may decide to initiate a reset or another setup transaction before the current interrupt routine has been completed. The reset or setup transaction will cause hardware to write 0 to all the bits in the interrupt register and the $\overline{IRQ}$ bit will be set to 1. Then, the hardware will set a bit in the interrupt register that signals the new interrupt conditions.

If an error occurs, the ACK handshake may become corrupted which will cause the device to hang because the host and function may disagree on whether the transaction was completed successfully. (Please see the “Error Handling on the Last Data Transaction” section of the USB Specification for further explanation of error handling by the USB host.) In order to deal with errors, the software must implement a timeout timer which is used to tell the micro-controller when to check the STSGE bit of the EP0 TX status register. If the timer times out, the micro-controller should set the RXFEN bit to 1 in the EP0 RX control register. This will enable the FIFO to receive the data from the host once again.

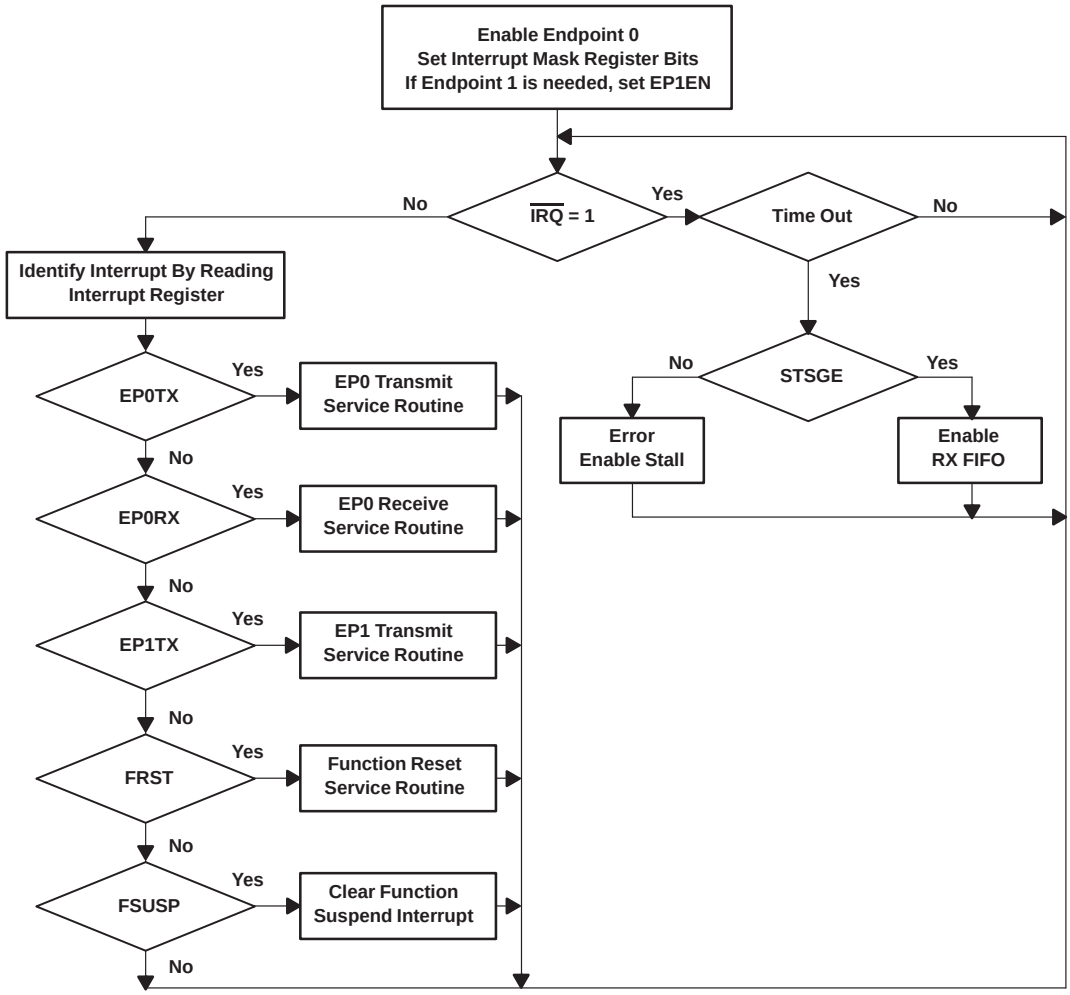


Figure A–1. Flow Chart for TUSB2140 Firmware

Endpoint 0 Transmit Service Routine

The flow diagram for the endpoint 0 transmit service routine is shown in Figure A-2. After detecting the endpoint 0 transmit interrupt bit (EP0TX) has been set, the MCU should branch to the endpoint 0 transmit service routine. First, the endpoint 0 transmit status register should be read to determine the source of the interrupt. If a successful transmit transaction has occurred, the endpoint 0 transmit acknowledge bit (ACK) will be set. The MCU should clear the interrupt condition by clearing the ACK bit. Next, if the next transaction should be an In data stage, the MCU should load the endpoint 0 transmit FIFO with the next data packet, write the new byte count value to the endpoint 0 transmit byte count register, and reset the timeout timer. However, if the next transaction should be an Out status stage, the MCU should set the endpoint 0 receive FIFO enable bit (RXFEN) to allow the status stage to be successfully acknowledged.

If the EP0TX interrupt resulted from an endpoint 0 transmit FIFO under-run or over-run condition, the endpoint 0 transmit FIFO under-run (UNDR) or over-run (OVRR) bit will be set, respectively. The under-run or over-run condition should be cleared by setting the endpoint 0 transmit clear bit (TXCLR).

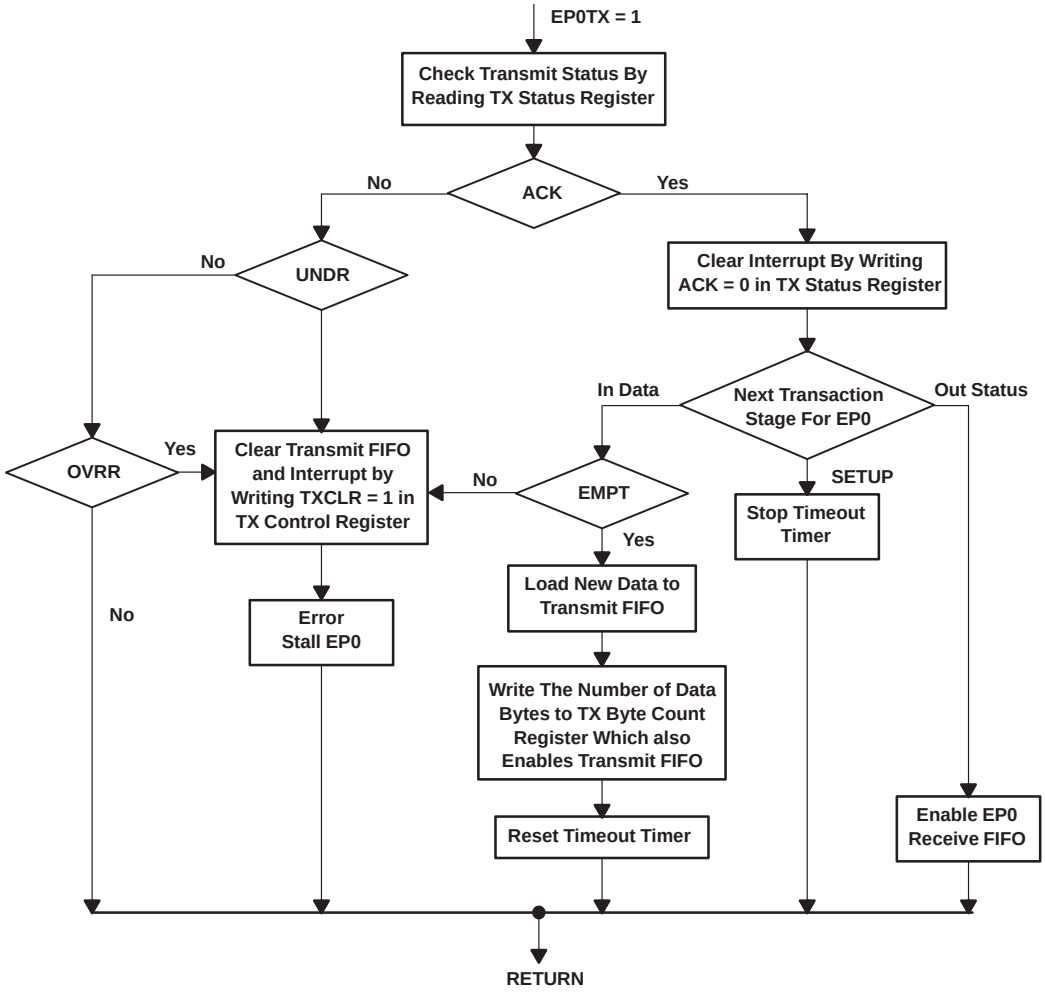


Figure A–2. Endpoint 0 Transmit Interrupt Service Routine

Endpoint 0 Receive Service Routine

The flow diagram for the endpoint 0 receive service routine is shown in Figure A-3. After detecting that the endpoint 0 receive interrupt bit (EP0RX) has been set, the MCU should branch to the endpoint 0 receive service routine. First, the endpoint 0 receive status register should be read to determine the source of the interrupt. If a receive transaction has occurred, the endpoint 0 receive acknowledge bit (ACK) will be set. In addition, if the transaction was a setup stage transaction, the endpoint 0 receive setup stage transaction bit (SETUP) will also be set. The MCU should clear the ACK and SETUP bits to clear the interrupt. Note that the SETUP bit must be cleared to enable reading the endpoint 0 receive FIFO. Next, the endpoint 0 receive byte count should be read to determine the number of bytes in the FIFO. Then the FIFO data should be read based on the byte count value.

If a FIFO under-run occurs while reading the FIFO, the endpoint 0 receive FIFO under-run bit (UNDR) will be set to indicate the condition. To clear an under-run condition, the MCU should set the endpoint 0 receive clear bit (RXCLR). After successfully reading the data packet from the receive FIFO, the MCU should branch to either the Setup Stage, Out Data Stage, or Out Status Stage routine based on the current transaction stage flags.

In the Out Data Stage routine, the MCU should set the endpoint 0 receive FIFO enable bit (RXFEN) to allow the next data stage data packet to be received. However, if the last data stage is detected, then the MCU should write a value of zero to the endpoint 0 transmit byte count register, which will automatically set the endpoint 0 transmit FIFO enable bit (TXFEN). As a result, the TUSB2140 will acknowledge the next In status stage transaction from the host.

In the Setup Stage routine, the MCU should decode the received data to determine the request type. In addition, the data stage length, direction of data transfer, and direction of status stage should be determined. The MCU should take the appropriate action for each control transfer based on this information. A control read for instance, requires the MCU to load data into the endpoint 0 transmit FIFO for each In data stage. The transmit FIFO can hold a maximum of eight bytes per In data stage transaction. Also, the MCU must enable the endpoint 0 receive FIFO to allow the control read Out status stage to be successfully acknowledged.

During endpoint 0 receive operations, a receive FIFO over-run condition could occur, which is indicated by an endpoint 0 receive interrupt being generated and the endpoint 0 receive FIFO over-run bit (OVRR) being set. The over-run condition can be cleared by setting the endpoint 0 receive clear bit (RXCLR) in the control register.

Once in the endpoint 0 service routine, if the MCU determines that neither the ACK bit or OVRR bit has been set, then the MCU should return to the main program. This scenario can occur when a new setup stage transaction is received while the MCU is branching from the main program to the receive service routine. When the new setup stage is received, the ACK bit will automatically be cleared.

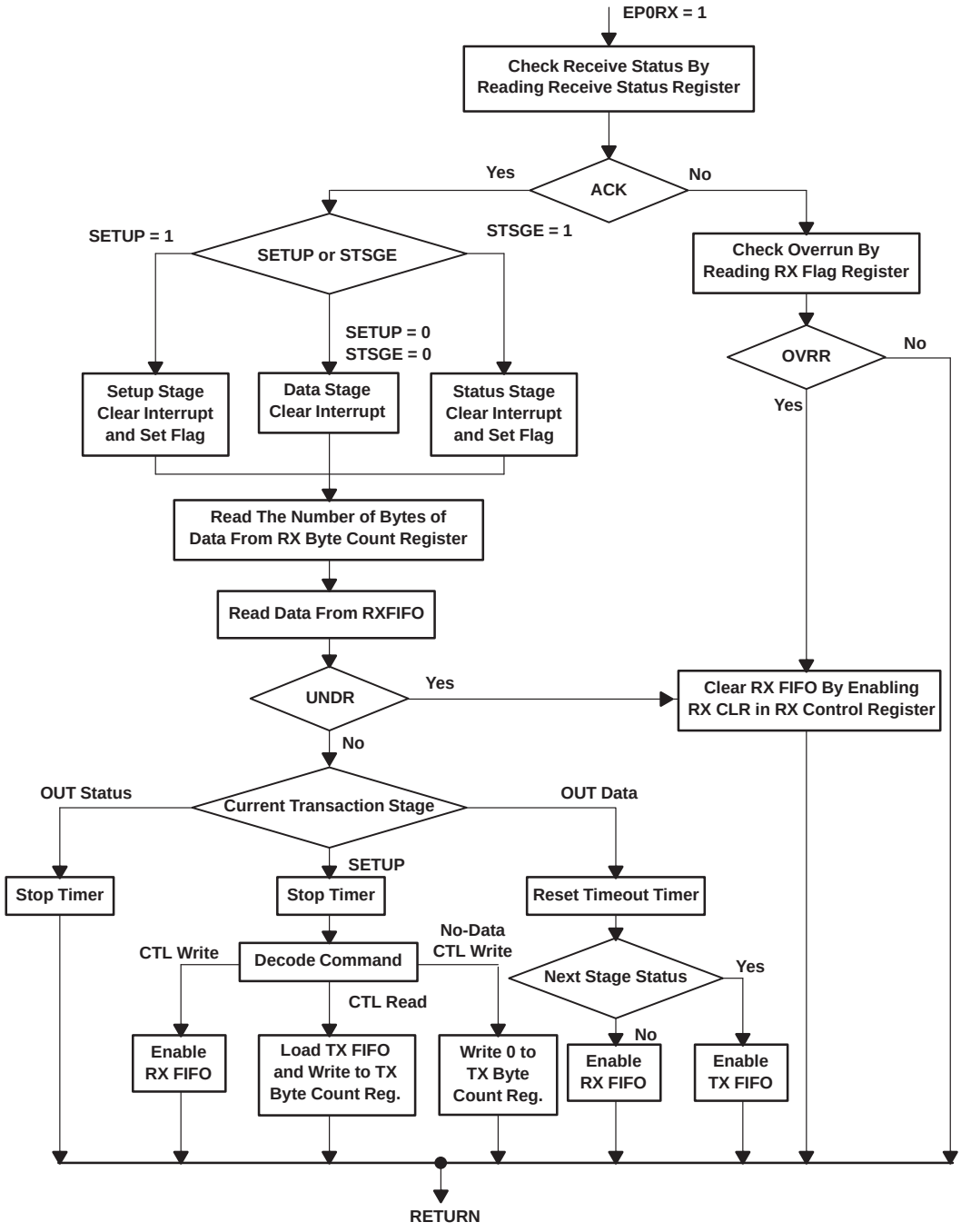


Figure A–3. Endpoint 0 Receive Interrupt Service Routine

Endpoint 1 Transmit Service Routine

The flow diagram for the endpoint 1 transmit service routine is shown in Figure A-4. After detecting the endpoint 1 transmit interrupt bit (EP1TX) has been set, the MCU should branch to the endpoint 1 transmit service routine. First, the endpoint 1 transmit status register should be read to determine the source of the interrupt. If a successful transmit transaction has occurred, the endpoint 1 transmit acknowledge bit (ACK) will be set. The MCU should clear the interrupt condition by clearing the ACK bit. Next, the MCU should load the endpoint 1 transmit FIFO with the next data packet and write the new byte count value to the endpoint 1 transmit byte count register. If the EP1TX interrupt resulted from an endpoint 1 transmit FIFO under-run or over-run condition, the endpoint 1 transmit FIFO under-run (UNDR) or over-run (OVRR) bit will be set, respectively. The under-run or over-run condition should be cleared by setting the endpoint 1 transmit clear bit (TXCLR).

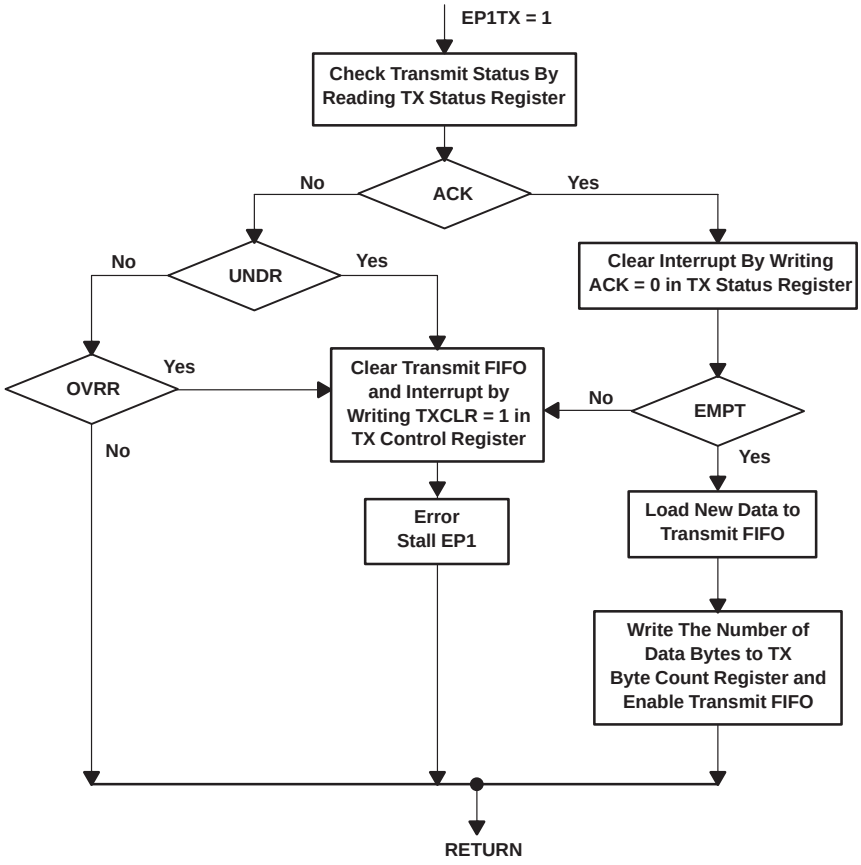


Figure A–4. Endpoint 1 Transmit Interrupt Service Routine

Function Reset Service Routine

After detecting the function reset interrupt bit (FRST) has been set, the MCU should branch to the function reset service routine. As a result of the TUSB2140 device receiving the USB function reset, all control and status registers will be cleared except the interrupt mask register bits, the endpoint 0 receive enable bit (RXEN), the endpoint 0 transmit enable bit (TXEN) and the function reset interrupt bit (FRST). To clear the function reset interrupt, the MCU should write 08h to the interrupt register.

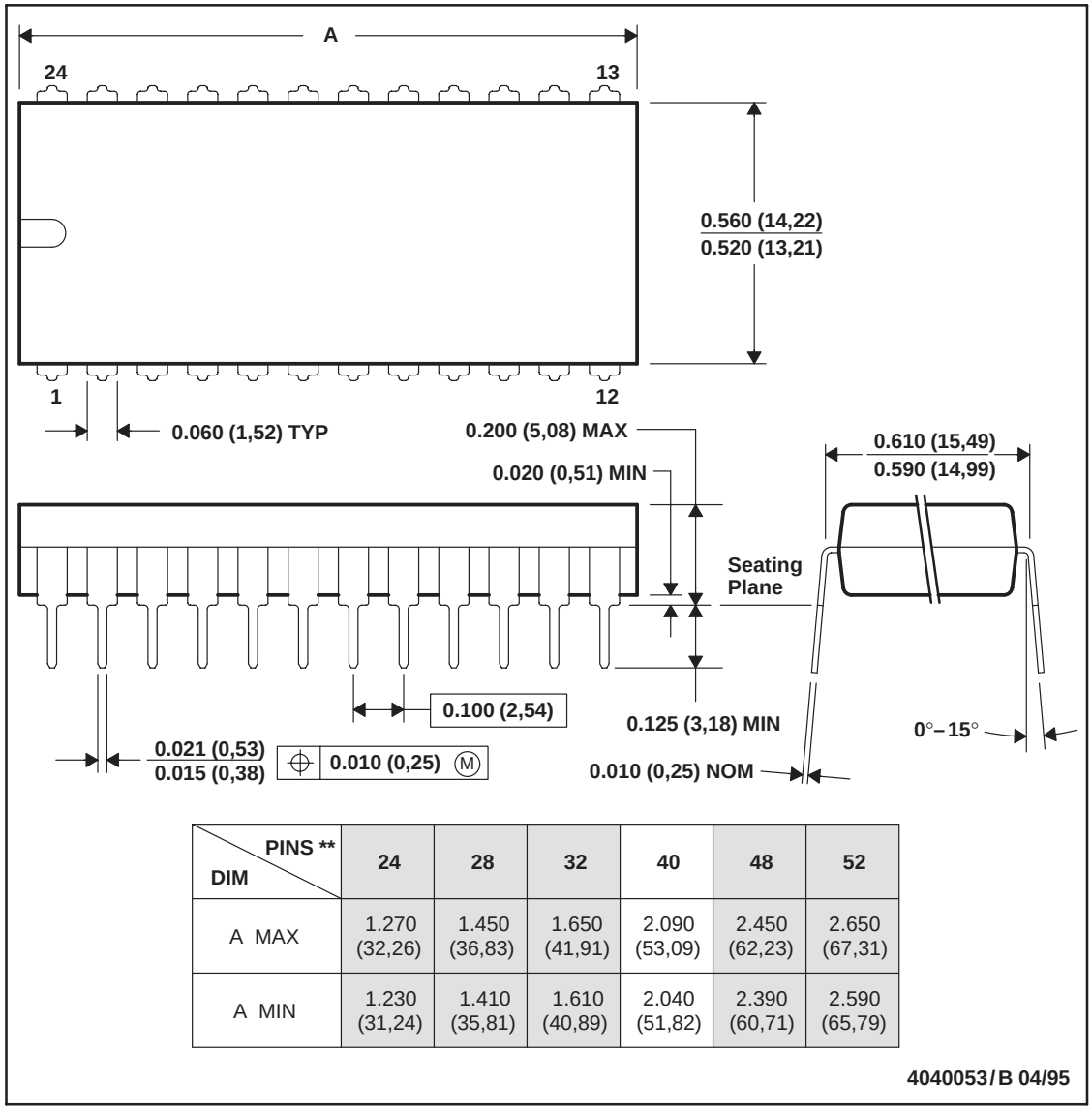
Function Suspend Service Routine

When a global or selective suspend condition is detected by the TUSB2140 device, the function suspend interrupt bit (FSUSP) will be set. After detecting the FSUSP bit has been set, the MCU should complete the current routine being processed then write 10h to the interrupt register in order to clear the function suspend interrupt. As a result of the FSUSP bit being cleared by the MCU, the TUSB2140 device will enter the low-power suspend mode and will disable the device clocks.

Appendix B
Mechanical Data

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN

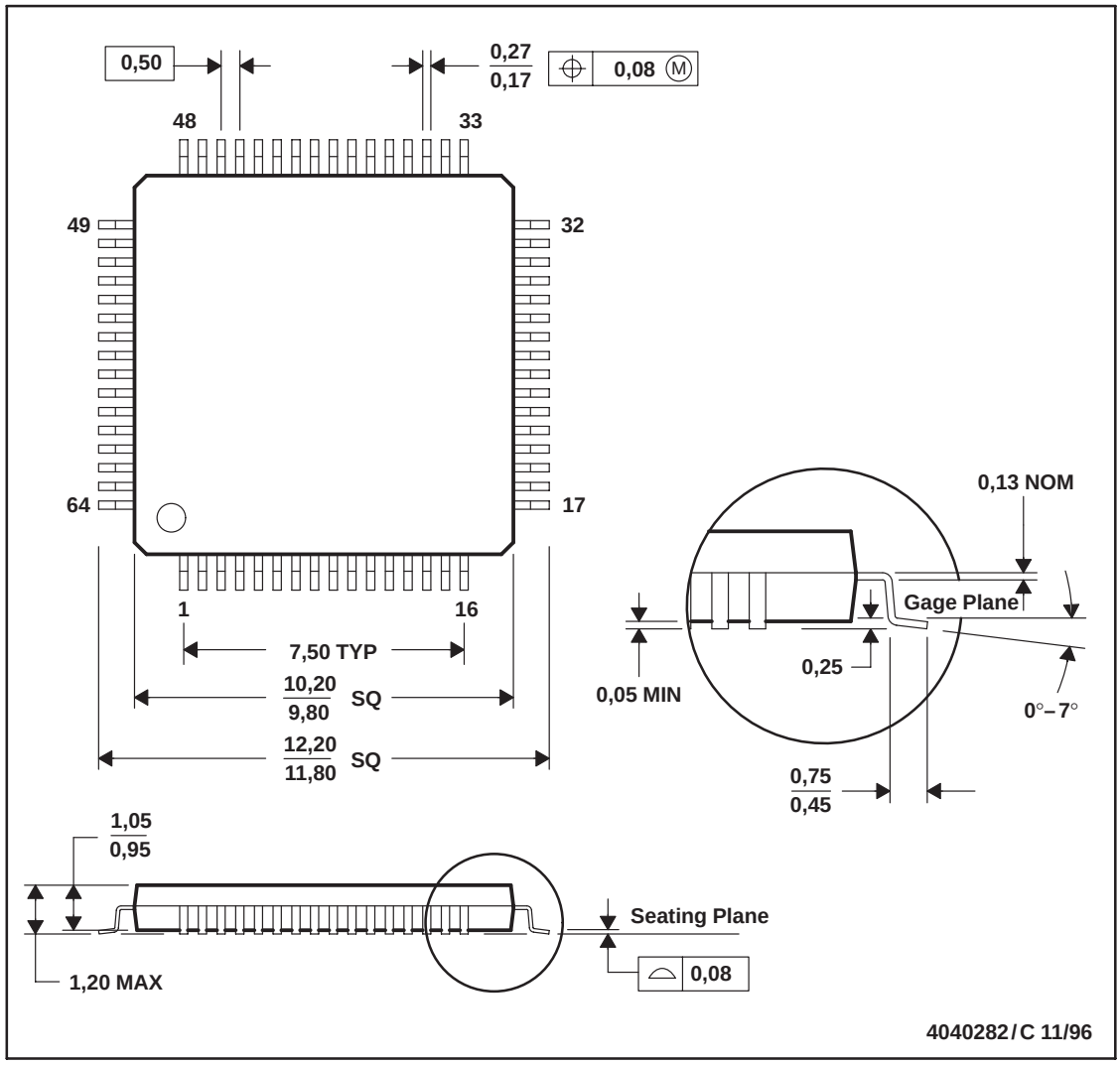


DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026