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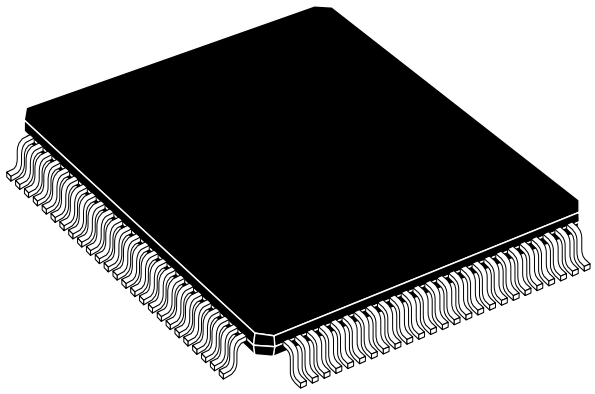
STV7697B

Scan Driver for Plasma Display Panels

Main Features

- **64-output PDP Scan Driver**
- **170V Absolute Maximum Rating**
- **5V Supply for Logic**
- **-200/750 mA Peak Output Current**
- **1 A Source / Sink Output Diode**
- **64-bit Shift Register (8 MHz)**
- **Blank Control**
- **Complementary Output Control**
- **BCD Technology**
- **100 Pin-TQFP Package**



TQFP100 (14 x 14 x 1.4 mm)
(Thin Plastic Quad Flat Pack)

ORDER CODE: STV7697B

Description

The STV7697B is a scan driver for plasma display panels (PDP) implemented in ST's proprietary BCD (Bi-polar CMOS DMOS) technology. Using a 64-bit cascadable 8-MHz shift register, it drives 64 high-current and high-voltage outputs.

By connecting several STV7697B devices in series, any vertical pixel definition can be performed. The STV7697B is supplied with separate 160V power output and 5 V logic supplies. All command inputs are CMOS compatible.

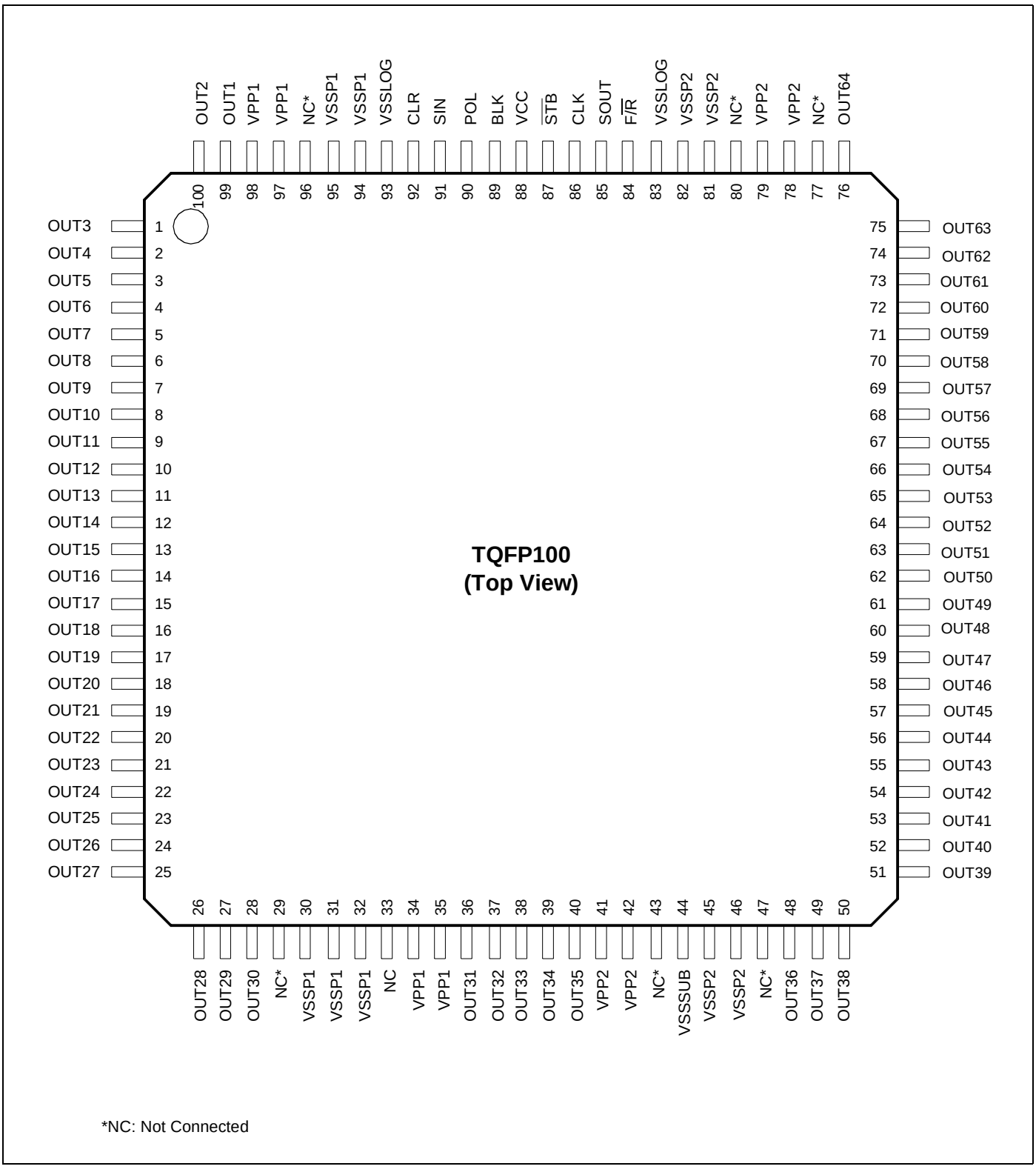
The STV7697B package is a 100-pin TQFP.

Table of Contents

1 Pin Allocation and Descriptions

1.1 Pinout Diagram

Figure 1: STV7697B (TQFP100)



*NC: Not Connected

Table 1: Supply Pins

Pin No.	Pin Name	Pin Description
88	VCC	5V Logic Supply
34	VPP1	High Voltage Supply for Power Outputs
35	VPP1	High Voltage Supply for Power Outputs
41	VPP2	High Voltage Supply for Power Outputs
42	VPP2	High Voltage Supply for Power Outputs
78	VPP2	High Voltage Supply for Power Outputs
79	VPP2	High Voltage Supply for Power Outputs
97	VPP1	High Voltage Supply for Power Outputs
98	VPP1	High Voltage Supply for Power Outputs
83	VSSLOG	Logic Ground
93	VSSLOG	Logic Ground
30	VSSP1	Ground for Power Outputs
31	VSSP1	Ground for Power Outputs
32	VSSP1	Ground for Power Outputs
45	VSSP2	Ground for Power Outputs
46	VSSP2	Ground for Power Outputs
81	VSSP2	Ground for Power Outputs
82	VSSP2	Ground for Power Outputs
94	VSSP1	Ground for Power Outputs
95	VSSP1	Ground for Power Outputs
44	VSSSUB	Substrate Ground

Table 2: Shift Register and Input Pins

Pin No.	Pin Name	Pin Description
85	SOUT	Shift Register Data Output
86	CLK	Clock for Shift Register Data
87	$\overline{STB}$	Latch for Shift Register Data (Strobe Input)
89	BLK	Blanking Control for Power Outputs
90	POL	Polarity Selection
91	SIN	Shift Register Data Input
92	CLR	Clear for Shift Register Data
84	F/$\overline{R}$	Forward/Reserve modes for selecting Shift Register

Table 3: Power Output Pins

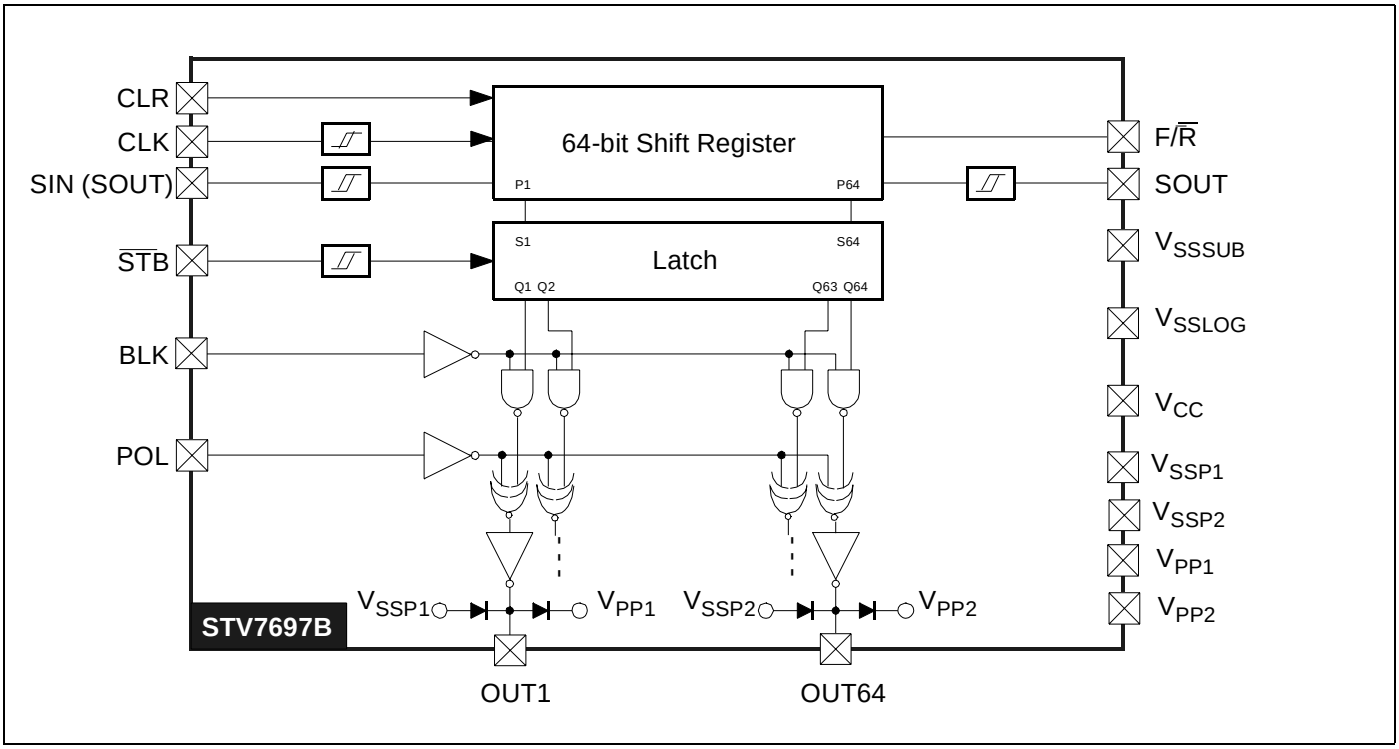
Pin No.	Pin Name	Pin Description	Pin No.	Pin Name	Pin Description
99	OUT1	Power Output 1	38	OUT33	Power Output 33
100	OUT2	Power Output 2	39	OUT34	Power Output 34
1	OUT3	Power Output 3	40	OUT35	Power Output 35
2	OUT4	Power Output 4	48	OUT36	Power Output 36
3	OUT5	Power Output 5	49	OUT37	Power Output 37
4	OUT6	Power Output 6	50	OUT38	Power Output 38
5	OUT7	Power Output 7	51	OUT39	Power Output 39
6	OUT8	Power Output 8	52	OUT40	Power Output 40
7	OUT9	Power Output 9	53	OUT41	Power Output 41
8	OUT10	Power Output 10	54	OUT42	Power Output 42
9	OUT11	Power Output 11	55	OUT43	Power Output 43
10	OUT12	Power Output 12	56	OUT44	Power Output 44
11	OUT13	Power Output 13	57	OUT45	Power Output 45
12	OUT14	Power Output 14	58	OUT46	Power Output 46
13	OUT15	Power Output 15	59	OUT47	Power Output 47
14	OUT16	Power Output 16	60	OUT48	Power Output 48
15	OUT17	Power Output 17	61	OUT49	Power Output 49
16	OUT18	Power Output 18	62	OUT50	Power Output 50
17	OUT19	Power Output 19	63	OUT51	Power Output 51
18	OUT20	Power Output 20	64	OUT52	Power Output 52
19	OUT21	Power Output 21	65	OUT53	Power Output 53
20	OUT22	Power Output 22	66	OUT54	Power Output 54
21	OUT23	Power Output 23	67	OUT55	Power Output 55
22	OUT24	Power Output 24	68	OUT56	Power Output 56
23	OUT25	Power Output 25	69	OUT57	Power Output 57
24	OUT26	Power Output 26	70	OUT58	Power Output 58
25	OUT27	Power Output 27	71	OUT59	Power Output 59
26	OUT28	Power Output 28	72	OUT60	Power Output 60
27	OUT29	Power Output 29	73	OUT61	Power Output 61
28	OUT30	Power Output 30	74	OUT62	Power Output 62
36	OUT31	Power Output 31	75	OUT63	Power Output 63
37	OUT32	Power Output 32	76	OUT64	Power Output 64

Table 4: Miscellaneous Pins

Pin No.	Pin Name	Pin Description
29	NC	Not connected
33	NC	Not connected
43	NC	Not connected
47	NC	Not connected
77	NC	Not connected
80	NC	Not connected
96	NC	Not connected

2 Circuit Description

Figure 2: STV7697B Block Diagram



The STV7697B includes all the necessary logic and power circuits to drive the rows of electrodes of a plasma display panel (PDP). The state of the displayed line is loaded into the shift register. Data is shifted at each low to high transition of the (CLK) shift clock. After 64 shifts, the first bit presented at the serial input (SIN) is available at the serial output (SOUT). This output is used to cascade several drivers to perform any vertical resolution (Table 5). Inputs CLK, STB, SIN and SOUT are Schmitt trigger inputs.

Table 5: Shift Register Truth Table

F/$\overline{R}$	CLK	SIN	SOUT	Comments
H	Rise	In	Out	Forward Shift
H	L or H	In	Out	Steady
L	Rise	Out	In	Reverse Shift
L	L or H	Out	In	Steady

The forward / $\overline{\text{reverse}}$ (F/$\overline{R}$) input is used to select the direction of the shift register where data input/ output status is set according to the selected direction. In Reverse mode (F/$\overline{R}$ = low), data is input on the SOUT pin and output on the SIN pin.

The maximum frequency of the shift clock is 8 MHz.

The clear signal (CLR) resets the shift register data to 0 when it is pulled to a high level.

Shift register outputs (P1, ... P64) are transferred from the shift register to the latch stage when the latch input (STB) is at low level.

All the data are kept memorized in the latch stage when the strobe input (STB) is pulled high.

The Blanking input (BLK) forces the power outputs to high level when pulled high with polarity input (POL) at high level and forced to low level with POL at low level. The level of the power output is inverted when the polarity command (POL) is pulled high.

Driver outputs can be simultaneously polarized at high or low level depending on the biasing of the POL input signal (Table 6).

Sustain current must not be sunk in the power output to V_{PP} when the power supply is applied.

V_{SSLOG} and V_{SSSUB} must be connected as close as possible to the logical reference ground of the application.

Table 6: Power Output Truth Table

P_n*	CLR	$\overline{STB}$	BLK	POL	Driver Output	Comments
X	X	X	H	H	All H	Forced to High
X	X	X	H	L	All L	Forced to Low
H	L	L	L	L	H	Copy Data
L	L	L	L	L	L	Copy Data
H	L	L	L	H	L	Copy Inverted Data
L	L	L	L	H	H	Copy Inverted Data
X	X	H	L	L	Qn	Data Latched
X	X	H	L	H	Qn	Inverted Data Latched
X	H	L	L	L	L	All Low
X	H	L	L	H	H	All High

*P_n is the parallel output of the shift register (n = 1 to 64). P_n takes the value of serial input (SIN) after “n” shift clock periods.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Logic Supply	–0.3, +7	V
V_{PP}	Driver Supply	–0.3, +170	V
V_{IN}	Logic Input Voltage	–0.3, V_{CC} +0.3	V
V_{OUT}	Logic Output Voltage	–0.3, V_{CC} + 0.3	V
V_{POUT}	Driver Output Voltage (Scanning mode)	–0.3, V_{PP}	V
I_{POUT}	Driver Output Current (See Note 1 and Note 3)	–250, +800	mA
I_{DOUT}	Diode Output Current (See Note 2 and Note 3)	±1.2	A
I_L	Latch-up Susceptibility	±200	mA
T_{JMAX}	Junction Temperature	+125	°C
T_{OPER}	Operating Temperature	–20, +85	°C
T_{STG}	Storage Temperature	–50, +150	°C

Note:1. Through one power output.

2. Through one power output with $V_{PP} = V_{SSP}$ (See Figure 4*.)*

3. These parameters are measured during ST's internal qualification which includes temperature characterization on standard batches and on corners batches of the process. These parameters are not tested on the parts.

3.2 Thermal Data

Symbol	Parameter	Value	Units
T_{JOPER}	Maximum Operating Junction	125	°C
R_{thJA}	Junction-ambient Thermal Resistance (See Note 1)	40	°C/W
P_{OPER}	Operating Power Dissipation (T_{OPER} = 25° C)	2	W

Note:1. TQFP soldered on 4-layer printed circuit board.

3.3 Supply Characteristics

(V_{CC} = 5 V, V_{PP} = 160 V, V_{SSP} = 0 V, V_{SSLOG} = V_{SSSUB} = 0 V, T_{AMB} = 25°C and f_{CLK} = 8 MHz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{CC}	Logic Supply Voltage		4.5	5	5.5	V
I_{CCH}	Logic Supply Current (all inputs high)				100	µA
I_{CCL}	Logic Supply Current	f_{CLK} = 8 MHz, SIN =1010		5.8		mA
V_{PP}	Power Output Supply Voltage		15		160	V
I_{PPH}	Power Output Supply Current (steady outputs)				100	µA

3.4 Power Output Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{POUTH}	Power Output High Level (voltage drop versus V_{PP}, V_{PP}=90V)	I_{POUTH} = - 10 mA I_{POUTH} = - 40 mA	5 10	3 5		V
$I_{POUTH-peak}$	Power Output Peak Current (See Note 1)	V_{PP} =130V		-200		mA
V_{POUTL}	Power Output Low Level	I_{POUTL} = 200 mA		2.6	5	V
$I_{POUTL-peak}$	Power Output Peak Current (See Note 2)	V_{POUTL} = 30V V_{CC} = 5V		650		mA
V_{DOUTH1}	Output Diode High Level (See Note 3 and Note 4)	I_{DOUTH} = +400 mA		2	3	V
V_{DOUTL1}	Output Diode Low Level (See Note 3 and Note 4)	I_{DOUTL} = - 400 mA	-2.5	-1.3		V
V_{DOUTH2}	Output Diode High Level (See Note 3)	I_{DOUTH} = +1000 mA		3.5	5	V
V_{DOUTL2}	Output Diode Low Level (See Note 3)	I_{DOUTL} = - 1000 mA	-3.5	-2		V

Note:1. These parameters are measured during ST's internal qualification which includes temperature characterization on standard batches and on corners batches of the process. These parameters are not tested on the parts.

2. Peak current: pulse mode 720 Hz, 200ns pulse width, V_{CC}=5 V.

3. Compatible with power dissipation (see Figure 4: Test Configuration*).*

4. The typical value increases when more than one output is activated.

3.5 SIN and SOUT Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{OH}	Logic Output High Level	I_{OH} = -1 mA	4.4	4.7	4.8	V
V_{OL}	Logic Output Low Level	I_{OL} = 1 mA	0.05	0.1	0.25	V

3.6 Input (CLR, CLK, $\overline{STB}$, BLK, POL, SIN/SOUT, and F/$\overline{R}$) Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Level		0.8 V_{CC}			V
V_{IL}	Input Low Level				0.2V_{CC}	V
I_{IH}	High Level Input Current	$V_{IH} = V_{CC}$	-10		10	µA
I_{IL}	Low Level Input Current Pins CLR, CLK, SIN/SOUT, $\overline{STB}$, F/$\overline{R}$, BLK and POL	V_{IL} = 0 V	-10		10	µA

3.7 AC Timing Requirements

V_{CC} = 4.5 V to 5.5 V, T_{AMB} = -20 to +85°C, max. leading/trailing edge for input signals (t_r, t_f) = 10 ns

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CLK}	Data Clock Period	125			ns
t_{WHCLK}	Duration of clock (CLK) pulse at high level	30			ns
t_{WLCLK}	Duration of clock (CLK) pulse at low level	30			ns
t_{SDAT}	Set-up Time of data input before clock (low to high) transition	10			ns
t_{HDAT}	Hold Time of data input after clock (low to high) transition	10			ns
t_{SFR}	F/$\overline{R}$ Set-up time before low to high transition	100			ns
t_{DSTB}	Minimum Delay to latch $\overline{STB}$ after clock (low to high) transition	10			ns
t_{SSTB}	Set-up Time $\overline{STB}$ before clock (low to high) transition	10			ns
t_{STB}	Strobe $\overline{STB}$ Pulse Duration	30			ns
t_{BLK}	Blanking (BLK) Pulse Duration	100			ns
t_{POL}	Polarity (POL) Pulse Duration	100			ns

3.8 AC Timing Characteristics

(V_{CC} = 5V, V_{PP} = 90V, V_{SSP} = 0V, V_{SSLOG} = 0V, V_{SSSUB} = 0V, T_{amb} = 25°C, $V_{ILMax.}$ = 0.2V_{CC}, $V_{IHMin.}$ = 0.8V_{CC}, V_{OH} = 4.0V, V_{OL} = 0.4V and C_L = 10pF, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CLK}	Data Clock Period	125			ns
t_{RDAT}	Logical Data Output Rise Time		20	40	ns
t_{FDAT}	Logical Data Output Fall Time		15	30	ns
t_{PHL1}	Delay of logic data output (high to low transition) after clock (CLK) transition		45	70	ns
t_{PLH1}	Delay of logic data output (low to high transition) after clock (CLK) transition		50	75	ns
t_{PHL2}	Delay of power output change (high to low transition) after clock (CLK) transition		135	200	ns
t_{PLH2}	Delay of power output change (low to high transition) after clock (CLK) transition		100	170	ns
t_{PHL3}	Delay of power output change (high to low transition) after Latch (STB) transition		120	190	ns
t_{PLH3}	Delay of power output change (low to high transition) after Latch (STB) transition		90	160	ns
t_{PHL4}	Delay of power output change (high to low transition) to Blank ($\overline{BLK}$) or Polarity ($\overline{POL}$) transition		110	180	ns
t_{PLH4}	Delay of power output change (low to high transition) to Blank ($\overline{BLK}$) or Polarity ($\overline{POL}$) transition		80	150	ns
t_{ROUT}	Power Output Rise Time (See Note 2)		40	80	ns
t_{FOUT}	Power Output Fall Time (See Note 2)		130	200	ns

Note:1. See Figure 4: Test Configuration.

2. One output among 64, loading capacitor C_{OUT} = 200 pF, other outputs at low level.

Figure 3: AC Characteristics Waveform

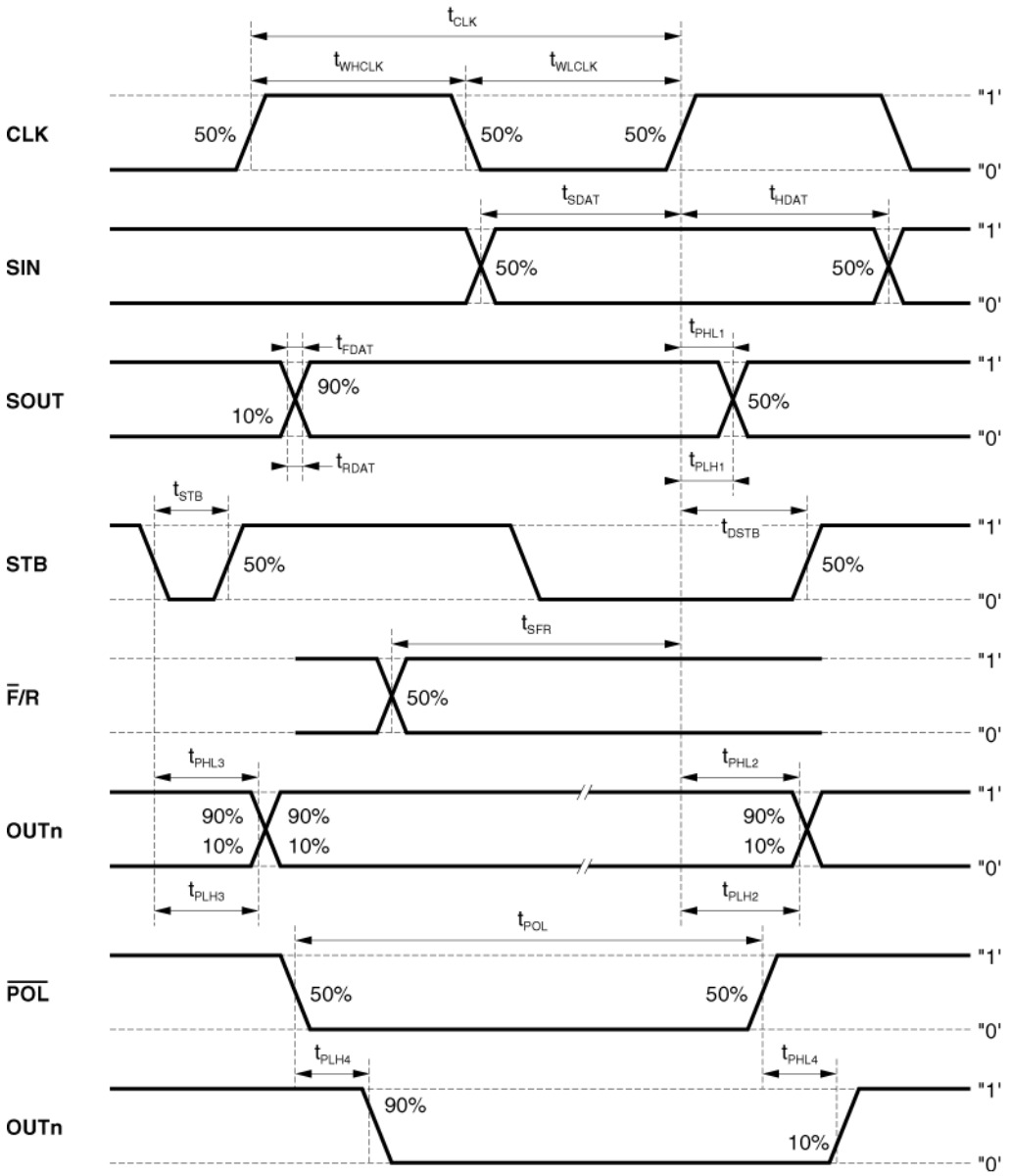
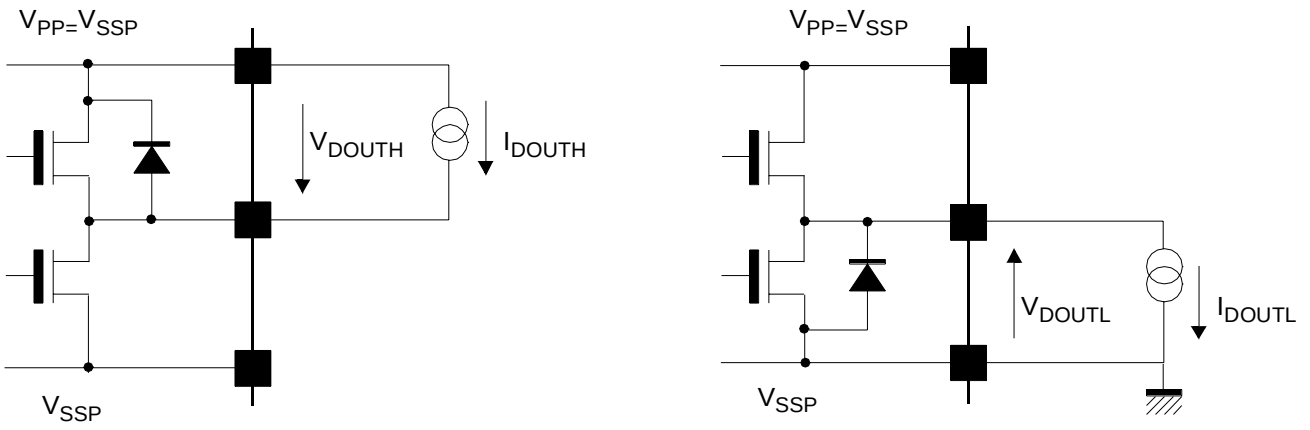


Figure 4: Test Configuration



Output sinking current as positive value, sourcing current as negative value.

4 Input/Output Schematic Diagrams

Figure 5: F/$\overline{R}$, BLK, CLR and POL Inputs

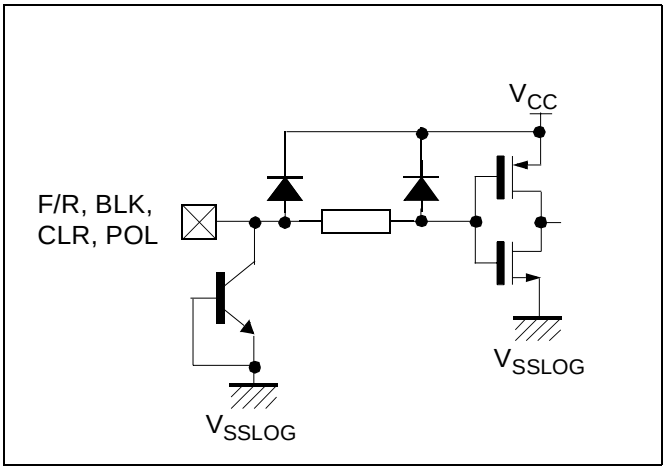


Figure 6: CLK and $\overline{STB}$ Inputs

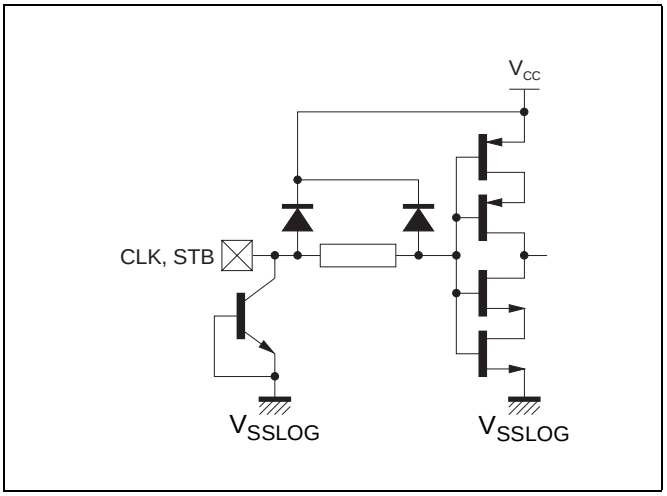


Figure 7: SIN and SOUT Inputs

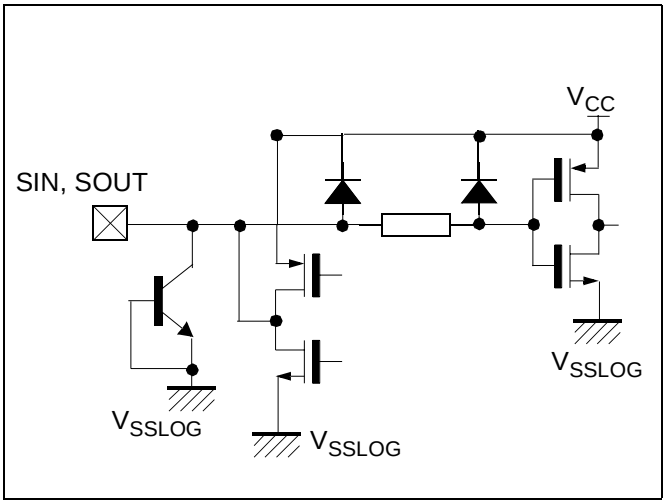
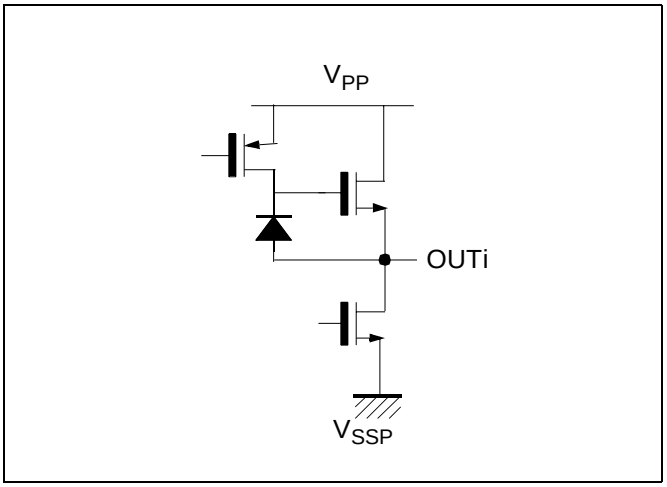


Figure 8: Power Outputs



5 Package Mechanical Data

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.00			0.472	
e		0.50			0.20	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.00			0.472	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0° (Min.), 7° (Max.)					

6 Revision History

Table 7: Summary of Modifications

Version	Date	Description
0.1	2 August 2002	First issue.
0.2	23 Sept. 2002	Modification of Pinout description.
0.3	20 March 2003	Modification of Pinouts. Update of Figure 2: STV7697B Block Diagram, Figure 3: AC Characteristics Waveform, Figure 5: F/R, BLK, CLR and POL Inputs, Figure 7: SIN and SOUT Inputs and Figure 8: Power Outputs. Update of Electrical Characteristic values.
0.4	18 June 2003	Datasheet status changed to “Preliminary Data”. Removed all references to STV7697BD package.
0.5	05 August 2003	Changed value of I_{DOUT} to 1.2 A. Included values for t_{PHL3}, t_{PLH3}, t_{PHL4} and t_{PLH4}. Updated Figure 7 and Figure 8.
0.6	10 September 2003	Updated parameter values in Power Output Characteristics on page 10 and AC Timing Characteristics on page 12.
0.7	23 September 2003	Updated and corrected data in Section 3.5, Section 3.6, Section 3.7 and Section 3.8.

Notes:

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