TVP3025
Data Manual

Video Interface Palette

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TEXAS INSTRUMENTS

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1 Introduction

The TVP3025 is an advanced video interface palette (VIP) from Texas Instruments implemented in EPIC™ 0.8-micron CMOS process. The TVP3025 is a superset of the 64-bit TVP3020 VIP with the addition of Brooktree BT485 register map emulation and frequency synthesis phase locked loops (PLLs). The BT485 register emulation mode allows the device to be software compatible with many graphics controllers, including the S3 Vision964™ and 86C928 VRAM based graphics accelerators. This new 64-bit device provides an effective migration path from lower performance graphics systems which utilize previous generation 32-bit color palettes.

The TVP3025 is a functional superset of the TVP3020 and features the same 64-bit programmable pixel bus interface. Data can be split into 1, 2, 4, or 8 bit planes for pseudo-color mode or split into 12-, 16- or 24-bit true-color and direct-color modes. For the 24-bit direct color modes, an 8-bit overlay plane is available. The 16-bit direct- and true-color modes can be configured to IBM XGA® (5, 6, 5), TARGA® (5, 5, 5, 1), or (6, 6, 4) as another existing format. An additional 12-bit mode (4, 4, 4, 4) is supported with 4 bits for each color and overlay. All color modes support selection of little or big endian data format for the pixel bus. Additionally, the device is also software compatible with the IMSG176/8 and Bt476/8 color palettes.

Clocking is provided through one of four inputs (2 TTL- and 1 ECL / TTL-compatible) or two crystal oscillator inputs, and is software selectable. The video, shift clock, and reference clock outputs provide a software-selected divide ratio of the chosen clock input. Two fully programmable PLLs for pixel clock and memory clock functions are provided, as well as a simple frequency doubler for dramatic improvements in graphics system cost and integration. A third loop clock PLL is incorporated making pixel data latch timing much simpler than with other existing color palettes.

Like the TVP3020, the TVP3025 also integrates a complete, IBM XGA-compatible hardware cursor on chip, making significant graphics performance enhancements possible. Additionally, auxiliary windowing, port-select and color-keyed switching functions are provided, giving the user several efficient means of producing graphical overlays on direct-color backgrounds.

The TVP3025 has three 256-by-8 color lookup tables with triple 8-bit video digital-to-analog converters (DACs) capable of directly driving a doubly terminated 75-Ω line. The lookup tables are designed with a dual-ported RAM architecture that enables ultra-high speed operation. Sync generation is incorporated on the green output channel. Horizontal sync and vertical sync are fed through the device and optionally inverted to indicate screen resolution to the monitor. A palette-page register is available to provide the additional bits of palette address when 1, 2, or 4 bit planes are used. This allows the screen colors to be changed with only one microprocessor interface unit (MPU) write cycle.

The device features a separate VGA bus that allows data from the feature connector of most VGA-supported personal computers to be fed directly into the palette without the need for external data multiplexing. The separate bus also is useful in graphics accelerator applications, allowing effecient VGA and text mode support.

The TVP3025 is highly system integrated. It can be connected to the serial port of VRAM devices without external buffer logic and connected to many graphics engines directly. It also supports the split shift-register transfer function, which is common to many industry standard VRAM devices.

The system-integration concept is carried to manufacturing test and field diagnosis. To support these, several highly integrated test functions have been designed to enable simplified testing of the palette and the entire graphics system.

1.1 Features

- 64-Bit-Wide Multiplexing Pixel Bus
- Compatible with the S3 Vision964 and 86C928
- Brooktree BT485 Register Map Emulation
- Supports System Resolutions of:
  - $1600 \times 1280 \times 1$, 2, 4, 8, 16, 24 Bits/Pixel @ 60-Hz, 72, and 76-Hz Refresh Rate
  - $1536 \times 1152 \times 1$, 2, 4, 8, 16, 24 Bits/Pixel @ 60-Hz, and 72-Hz and Higher Refresh Rates
  - $1280 \times 1024 \times 1$, 2, 4, 8, 16, 24 Bits/Pixel @ 60-Hz and 72-Hz and Higher Refresh Rates
  - $1024 \times 768 \times 1$, 2, 4, 8, 16, 24 Bits/Pixel @ 60-Hz and 72-Hz and Higher Refresh Rates
  - And Lower Resolutions
- Direct-Color Modes:
  - 24-Bit/Pixel with 8-Bit Overlay
  - 16-Bit/Pixel (5, 6, 5) XGA Configuration
  - 16-Bit/Pixel (6, 6, 4) Configuration
  - 15-Bit/Pixel With 1 Bit Overlay (5, 5, 5, 1) TARGA Configuration
  - 12-Bit/Pixel With 4 Bit Overlay (4, 4, 4, 4)
- True-Color Modes:
  - 24-Bit/Pixel With Gamma Correction
  - 16-Bit/Pixel (5, 6, 5) XGA Configuration With Gamma Correction
  - 16-Bit/Pixel (6, 6, 4) Configuration with Gamma Correction
  - 15-Bit/Pixel (5, 5, 5) TARGA Configuration With Gamma Correction
  - 12-Bit/Pixel (4, 4, 4) With Gamma Correction
- RCLK/SCLK/LCLK Data Latching Mechanism Allows Flexible Control of VRAM Timing
- Direct Interfacing to Video RAM
- Support for Split Shift Register Transfers
- 135-, 175-, and 220-MHz Versions
- Integrated Pixel Clock and Memory Clock PLLs
- On-Chip Hardware Cursor:
  - $64 \times 64 \times 2$ Cursor (XGA Functionally Compatible)
  - Full-Window Crosshair
  - Dual-Cursor Mode
- On-Chip Clock Selection
- Supports Overscan for Creation of Custom Screen Borders
- Versatile Pixel Bus Interface Supports Little- and Big-Endian Data Formats
- Windowed Overlay and VGA Capability
- Color-Keyed Switching of Direct Color and Overlay
- Horizontal Zooming Capability
- Triple 8-Bit D/A Converters
- Analog Output Comparators
- Triple 256×8 Color Palette RAMs
- RS-343A Compatible Outputs
- Direct VGA Pass-Through Capability
- Palette Page Register
- Software Downward Compatible With IMSG176/8 and Bt476/8
- EPIC 0.8-µm CMOS Process

1.2 Functional Block Diagram

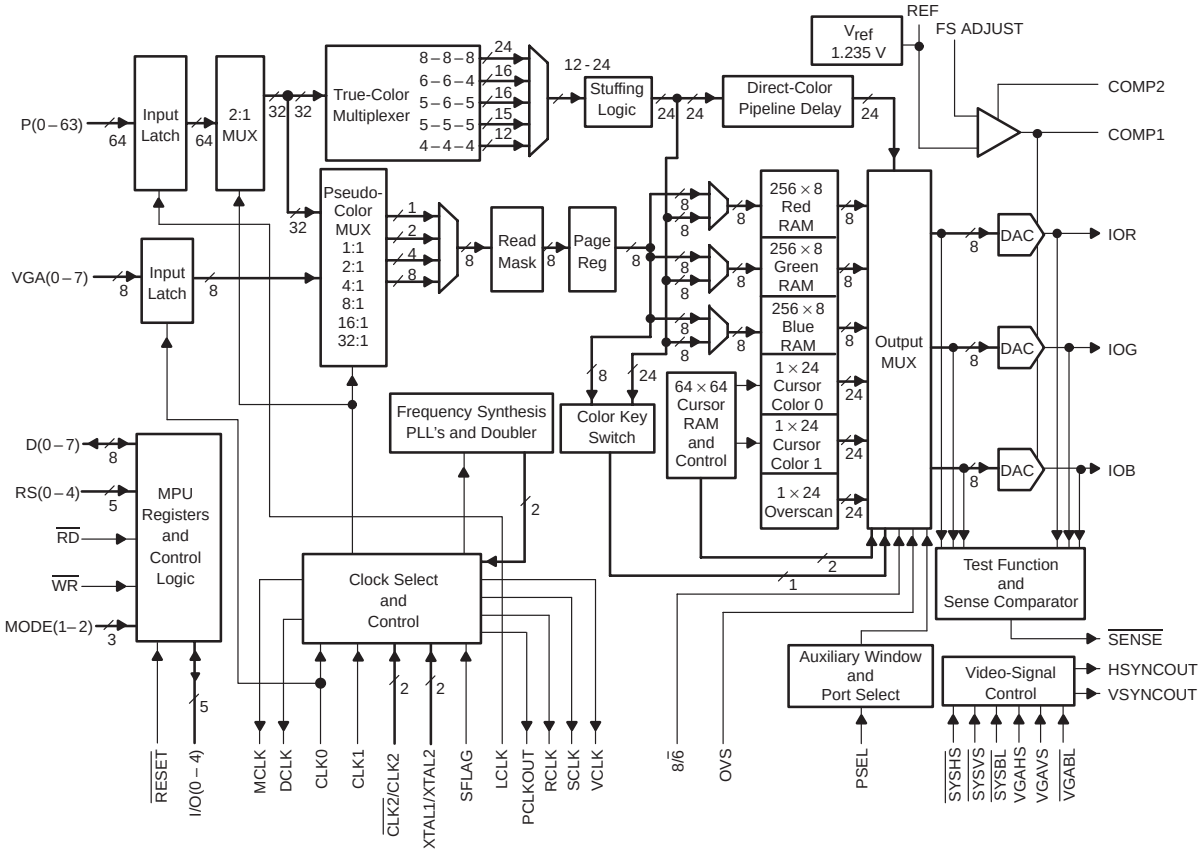
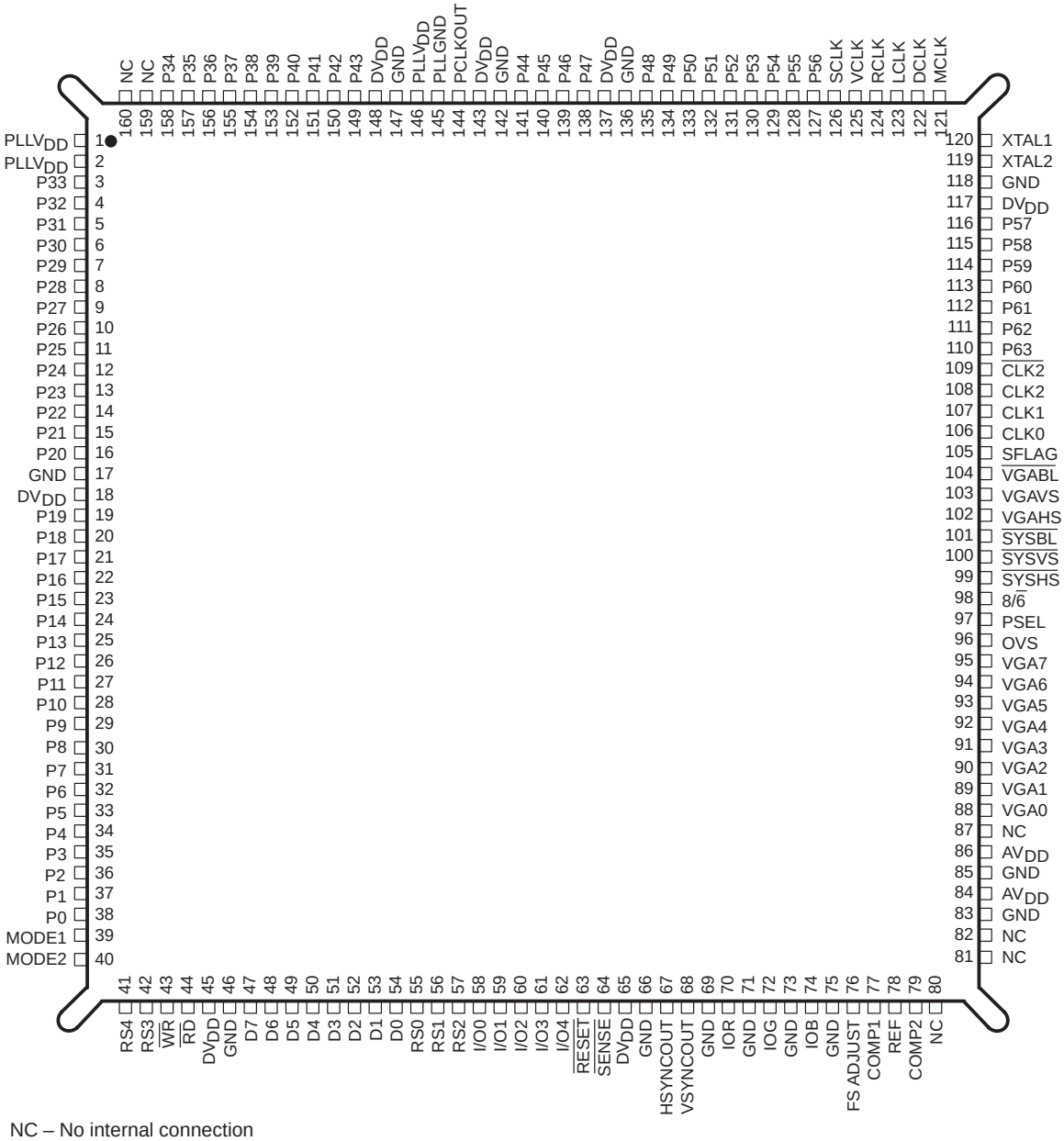


Figure 1–1. Functional Block Diagram

1.3 Terminal Assignments



NC – No internal connection

Figure 1–2. Terminal Assignments

1.4 Ordering Information

TVP3025 – XXX XXX

Pixel Clock Frequency Indicator

MUST CONTAIN THREE CHARACTERS:

- –135: 135-MHz pixel clock
- –175: 175-MHz pixel clock
- –220: 220-MHz pixel clock

Package

MUST CONTAIN THREE LETTERS:

- MDN: Metal, Quad Flat Pack
- PCE: Plastic, Quad Flat Pack (mechanical data unavailable at time of print)

1.5 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AV_{DD}	84, 86		Analog power. All AV_{DD} terminals must be connected.
CLK0	106	I (TTL compatible)	Dot clock 0 input. CLK0 can be selected to drive the dot clock at frequencies up to 140 MHz. When VGA mode is active, the selected clock source is CLK0. The maximum frequency in VGA mode is 85 MHz. The maximum frequency for direct color/VGA switching in self-clocked mode is 50MHz. This clock source is also selected at reset.
CLK1	107	I (TTL compatible)	Dot clock 1 input. CLK1 can be selected to drive the dot clock at frequencies up to 140 MHz.
$\overline{CLK2}$, CLK2	108, 109	I (TTL/ECL compatible)	Dual-mode dot clock input. These inputs are essentially $\overline{ECL}$-compatible inputs, but two TTL clocks may be used on CLK2 and $\overline{CLK2}$ if so selected in the input-clock-selection register. These inputs may be selected as the dot clock up to the device limit while in the ECL mode or up to 140 MHz in the TTL mode.
COMP1, COMP2	77, 79		Compensation. COMP1 and COMP2 provide compensation for the internal reference amplifier. A 0.1-µF ceramic capacitor is required between COMP1 and COMP2. This capacitor must be as close to the device as possible for proper decoupling and to avoid noise pick up.
DCLK	122	O	Dot clock. Divided memory clock output. A frequency divided version of the MCLK output.
DV_{DD}	18, 45, 65, 117, 137, 143, 148		Digital power. All DV_{DD} terminals must be connected.
D0–D7	47–54	I/O (TTL compatible)	MPU interface data bus. These terminals are used to transfer data in and out of the register map and palette/overlay RAM.
FS ADJUST	76	I	Full-scale adjustment. A resistor connected between this terminal and ground controls the full-scale range of the DACs.
GND	17, 46, 66, 69, 71, 73, 75, 83, 85, 118, 136, 142, 147		Ground. All GND terminals must be connected. The GNDs are connected internally.

NOTE: All unused inputs should be tied to a logic level and not be allowed to float.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
HSYNCOUT	67	O (TTL compatible)	Horizontal sync output after pipeline delay. For system mode the output polarity can be programmed using the general-control register, but for the VGA mode the output carries the same polarity as the input.
IOR, IOG, IOB	70, 72, 74	O	Analog current outputs. These outputs can drive a 37.5-Ω load directly (doubly terminated 75-Ω line), thus eliminating the requirement for any external buffering.
I/O0–I/O4	58–62	I/O (TTL compatible)	Software programmable I/O terminals that can be used to control external devices.
LCLK	123	I (TTL compatible)	Pixel-port-latch clock input. LCLK is used to latch pixel-bus-input data. It can also be used to latch the blank and sync inputs if selected by the miscellaneous-control register bit 6.
MCLK	121	O (TTL compatible)	Memory clock output. User programmable frequency synthesis PLL output.
MODE1	39	I (TTL compatible)	Register map select at reset. If this terminal is a logic high around the positive edge of $\overline{\text{RESET}}$, the device assumes the BT485 register emulation map reset default states. It also initiates decoding into the TVP3025 control registers and the BT485 register access monitoring. If the terminal is a logic low at reset, TVP3025 register map reset defaults are assumed. This mode reset function also works with the built in software reset function. This terminal is internally pulled down so that TVP3025 register default settings result if the terminal is not connected.
MODE2	40	I (TTL compatible)	Register select 4 inversion control. If this terminal is held low, the RS4 input is inverted. This causes the BT485 register map to use addresses 0–F instead of 10–1F and the TVP3025 register map to use addresses 10–17 instead of 0–7. This terminal is internally pulled up so no inversion results if the terminal is not connected.
PCLKOUT	144	O (TTL compatible)	Pixel clock PLL output. To enable pixel clock PLL output on the PCLKOUT terminal, the pixel clock P value register bit 3 must be set to logic 1. This output is independent of the dot clock selected in the input-clock-selection register.
PLLGND	145	I (TTL compatible)	PLL ground. PLLGND should be provided from the GND plane through a ferrite bead and decoupled to the $PLLV_{DD}$ supply.
$PLLV_{DD}$	1, 2, 146	I (TTL compatible)	PLL supply. One external voltage regulator is recommended to supply power to the three integrated PLLs. The $PLLV_{DD}$ supply should be decoupled to PLLGND.
OVS	96	I (TTL compatible)	Overscan input. OVS is used to create custom screen borders.
PSEL	97	I (TTL compatible)	Port select. PSEL provides the capability of VGA or overlay windows in a direct color background on a pixel-by-pixel basis. This function is not supported for BT485 mode operation.

NOTE: All unused inputs should be tied to a logic level and not be allowed to float.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
P0–P63	3–16, 19–38, 110–116, 127–135, 138–141, 149–158	I (TTL compatible)	Pixel input port. The port can be used in various modes as shown in Table 2–8 (TVP3020 mode) or Table 2–15 (BT485 mode). All the unused terminals need to be tied to GND.
RCLK	124	O (TTL compatible)	Reference clock output. RCLK is essentially the same as the SCLK output but not gated off during blank. It can be used for pixel-port timing reference or other system synchronization and is programmed through the output-clock-selection register in TVP3020 mode. In BT485 mode RCLK is similar to the BT485 SCLK, with the divide ratio (and hence the multiplex ratio) being automatically set when command register 1 is programmed for the desired operating mode.
REF	78		Voltage reference for DACs. An internal voltage reference of nominally 1.235 V is provided, which requires an external 0.1-µF ceramic capacitor between REF and analog GND. However, the internal reference voltage can be overdriven by an externally supplied reference voltage. Typical connection is shown in Appendix A.
$\overline{\text{RESET}}$	63	I	Chip reset. All the registers default to the VGA mode after reset.
$\overline{\text{RD}}$	44	I (TTL compatible)	Read strobe input. A logic 0 on this terminal initiates a read from the register map. Reads are performed asynchronously and are initiated on the low-going edge of $\overline{\text{RD}}$ (see Figure 3–1).
RS0–RS4	41, 42, 55–57	I (TTL compatible)	Register select inputs. These terminals specify the location in the register map that is to be accessed (see Table 2–1 and 2–2). RS4 may be inverted internally using the MODE2 input. RS3 has an internal pull down resistor so these terminals may be left unconnected if only RS0–2 are used for the TVP3020-only operation.
SCLK	126	O (TTL compatible)	Shift clock output. SCLK is selected as a division of the dot clock input. The output signals are gated off during blank, although SCLK is still used internally to synchronize with the activation of $\overline{\text{BLANK}}$.
$\overline{\text{SENSE}}$	64	O (TTL compatible)	Test mode DAC comparator output signal. This terminal is low if one or more of the DAC output analog levels is above the internal comparator reference of 350 mV ±50 mV.
SFLAG	105	I (TTL compatible)	Split shift register transfer flag. The TVP3025 detects a low-to-high transition on this terminal during a blank sequence and immediately generates an SCLK pulse. This early SCLK pulse replaces the first SCLK pulse in the normal sequence.
$\overline{\text{SYSBL}}$	101	I (TTL compatible)	System blank input. $\overline{\text{SYSBL}}$ is active (low).
$\overline{\text{SYSHS}}$, $\overline{\text{SYSVS}}$	99, 100	I (TTL compatible)	System horizontal and vertical sync inputs. These signals are used to generate the sync level on the green current output. They are active (low) inputs, but the HSYNCOUT and VSYNCOUT output polarities can be programmed through the general-control register.
VCLK	125	O (TTL compatible)	Video clock output. VCLK is the user-programmable output for synchronization to a graphics processor. It can be used to latch $\overline{\text{SYSBL}}$, $\overline{\text{SYSHS}}$, $\overline{\text{SYSVS}}$ inputs (depending on miscellaneous-control register bit 6).

NOTE: All unused inputs should be tied to a logic level and not be allowed to float.

1.5 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{VGABL}}$	104	I (TTL capability)	VGA blank input. $\overline{\text{VGABL}}$ is active (low).
VGAHS, VGAVS	102, 103	I (TTL capability)	VGA horizontal and vertical sync inputs. These signals are used to generate the sync level on the green current output. They can be either polarity, and the TVP3025 passes the polarities to HSYNCOUT and VSYNCOUT without change.
VGA0–VGA7	88–95	I (TTL capability)	VGA pass-through bus. This bus can be selected as the pixel bus for VGA mode, but it does not allow for any multiplexing.
VSYNCOUT	68	O (TTL capability)	Vertical sync output after pipeline delay. For system mode, the output polarity can be programmed but for VGA mode, the output carries the same polarity as the input.
$\overline{\text{WR}}$	43	I (TTL capability)	Write strobe input. A logic 0 on this terminal initiates a write to the register map. As with $\overline{\text{RD}}$, write transfers are asynchronous and initiated on the low-going edge of $\overline{\text{WR}}$ (see Figure 3–1).
XTAL1, XTAL2	119, 120	I (TTL capability)	Series resonant crystal oscillator. This may be used as the reference for the on-chip frequency synthesis PLLs and can be selected through the input-clock-selection register.
8/$\overline{6}$	98	I (TTL capability)	DAC resolution selection. This terminal is used to select the data bus width (8 or 6 bits) for the DAC when in the TVP3020 mode and is essentially provided in order to maintain compatibility with the IMSG176. When this terminal is a logical 1 and the 8/$\overline{6}$ terminal is enabled (miscellaneous-control register bit 2 is logic 0), 8-bit bus transfers are used with D7 the MSB and D0 the LSB. For 6-bit bus operation (8/$\overline{6}$ terminal is a logical 0), while the color palette still has the 8-bit information D5 shifts to the bit 7 position with D0 shifted to the bit 2 position and the two LSBs are filled with zeros at the output multiplexer to the DAC. The palette holding register zeroes the two MSBs when it is read in the 6-bit mode. If miscellaneous-control register bit 2 is logic 1, then the 8/$\overline{6}$ terminal is disabled and 8/$\overline{6}$ operation is specified by bit 3 of the miscellaneous-control register.

NOTE: All unused inputs should be tied to a logic level and not be allowed to float.

2 Detailed Description

2.1 MPU Interface

The standard microprocessor interface is supported, giving the MPU direct access to the color palette RAM. The processor interface is controlled via read and write strobes ($\overline{RD}$, $\overline{WR}$), five register select terminals (RS0–RS4), the D0–D7 data terminals, and the 8/$\overline{6}$-select terminal. The 8/$\overline{6}$ terminal is used to select between an 8- or 6-bit-wide data path to the color palette RAM and is provided in order to maintain compatibility with the IMSG176. The 8/$\overline{6}$ control is dependent on the mode of operation of the device (TVP3025 or BT485 register emulation) and is discussed in more detail in Sections 2.3.1 and 2.4.4.

The TVP3025 provides two methods of register access through the MPU interface to program the hardware features of the device: the TVP3025 direct register map (see Table 2–1) and the BT485 emulation register map (see Table 2–2).

The TVP3025 direct register map is similar to the register map of the TVP3020. The index register and the data register provide access to the TVP3025 indirect register map (see Table 2–3) which allows programming of the device features. In general, the index register must first be loaded with the target address value. Successive reads or writes from and to the data register then access the target location.

2.1.1 BT485 Register Emulation

The BT485 emulation register map provides access to many of the same device features through a BT485 compatible direct access map. This mode is provided to allow previously developed software drivers written for the BT485 device to be used without modification when upgrading the TVP3025. The most popular features of the BT485 are supported by the TVP3025. Section 2.4.17 gives details on TVP3025 compatibility with the BT485 and functions not supported. When accessing the BT485 emulation registers, only features which are supported by the BT485 and have a counterpart on the TVP3025 can be utilized. If additional TVP3025 features are to be used, they must be accessed through the TVP3025 register map.

The BT485 register emulation function uses a set of internal registers to store the information programmed through the BT485 emulation register map. Each register has a flag that indicates when it has been written to, and a state machine monitors all the flags. When a flag has been set, the state machine performs the required sequence of operations to properly update the TVP3025 indirect registers. This internal translation is performed using a succession of byte-writes and bit read-modify-writes as required. During the translation, the TVP3025 indirect register map can not be accessed. The BT485 emulation status register bit 6 indicates when the internal translation is in progress.

Table 2–1. TVP3025 Direct Register Map

RS4	RS3	RS2	RS1	RS0	REGISTER ADDRESSED BY MPU	R/W	DEFAULT (HEX)
0	0	0	0	0	Palette Address – Write Mode	R/W	XX
0	0	0	0	1	Palette Data	R/W	XX
0	0	0	1	0	Pixel Read-Mask	R/W	FF
0	0	0	1	1	Palette Address – Read Mode	R/W	XX
0	0	1	0	0	Reserved		XX
0	0	1	0	1	Reserved		XX
0	0	1	1	0	Index	R/W	XX
0	0	1	1	1	Data	R/W	XX
0	1	0	0	0	Reserved		XX
0	1	0	0	1	Reserved		XX
0	1	0	1	0	Reserved		XX
0	1	0	1	1	Reserved		XX
0	1	1	0	0	Reserved		XX
0	1	1	0	1	Reserved		XX
0	1	1	1	0	Reserved		XX
0	1	1	1	1	Reserved		XX

Table 2–2. BT485 Emulation Register Map

RS4	RS3	RS2	RS1	RS0	REGISTER ADDRESSED BY MPU	R/W	DEFAULT (HEX)
1	0	0	0	0	Palette/Cursor Address – Write Mode	R/W	XX
1	0	0	0	1	Palette RAM Data	R/W	XX
1	0	0	1	0	Pixel Read-Mask	R/W	FF
1	0	0	1	1	Palette/Cursor Address – Read Mode	R/W	XX
1	0	1	0	0	Cursor/Overscan Color Address – Write Mode	R/W	XX
1	0	1	0	1	Cursor/Overscan Color Data	R/W	XX
1	0	1	1	0	Command Register 0	R/W	00
1	0	1	1	1	Cursor/Overscan Color Address – Read Mode	R/W	XX
1	1	0	0	0	Command 1	R/W	00
1	1	0	0	1	Command 2	R/W	00
1	1	0	1	0	Status	R	XX
1	1	0	1	1	Cursor RAM Data	R/W	XX
1	1	1	0	0	Cursor-Position X Low	R/W	XX
1	1	1	0	1	Cursor-Position X High	R/W	XX
1	1	1	1	0	Cursor-Position Y Low	R/W	XX
1	1	1	1	1	Cursor-Position Y High	R/W	XX

2.1.2 TVP3025/BT485 Register Initialization

The MODE1 input determines how the TVP3025 initializes at reset (using the $\overline{\text{RESET}}$ terminal). Upon device reset, if MODE1 is logic 1, the TVP3025 initializes using the BT485 emulation register map (see Table 2–2) and assumes BT485 compatible functionality. All internal BT485 type command registers and data registers are reset to 00 (hex). On the rising edge of the $\overline{\text{RESET}}$ signal, the BT485 emulator translates all of the BT485 internal registers into the TVP3025 indirect registers. It also causes the internal emulator state machine to begin monitoring BT485 register accesses and the cursor RAM interface is set to the planar access mode (TVP3025 cursor control register bit 7 = 1). The translated TVP3025 indirect register map reset defaults for the BT485 mode are shown in Table 2–3.

Additionally, the MCLK and pixel clock PLLs are enabled and set to approximately 45 MHz and 25 MHz, respectively (with an external 14.318 MHz crystal). Also, all command registers are reset to zeroes and blank/sync are configured to be latched on the rising edge of LCLK.

If MODE1 is logic 0 when the TVP3025 is reset, the device initializes the TVP3025 register maps as specified in Table 2–1 and Table 2–3 and translation of the BT485 emulation registers does not take place. Also, the cursor RAM interface is set to the nonplanar access mode (TVP3025 cursor control register bit 7 = 0) with the same operation as the TVP3020. The internal BT485 registers can subsequently be programmed via the RS4 or the MODE2 terminals.

The MODE2 terminal optionally inverts the RS4 register select signal internal to the device. This allows the TVP3025 to be used with graphics controllers that support either four or five register selects. For designs using only four register selects (RS0–RS3), RS4 should be connected to DV_{DD} or GND and the MODE2 terminal can be used to select between the TVP3025 register map and the BT485 emulation register map (see Tables 2–1 and 2–2). When the MODE2 input terminal is logic 0, the RS4 signal is internally inverted. If MODE2 is logic 1, no inversion takes place. MODE2 is internally pulled up so that no inversion occurs if the terminal is not connected. For designs using all five register selects (RS0–RS4), both of the register maps are available with RS4 performing the switching.

Note that general I/O terminal I/O4 is provided through the BT485 command register 4 and can be used to externally connect to RS4.

Table 2–3. TVP3025 Indirect Register Map (Extended Registers)

INDEX REGISTER (HEX)	R/W	DEFAULT TVP3025	DEFAULT BT485	REGISTER ADDRESSED BY INDEX REGISTER
0000	R/W	00	00	Cursor-Position X LSB
0001	R/W	00	00	Cursor-Position X MSB
0002	R/W	00	00	Cursor-Position Y LSB
0003	R/W	00	00	Cursor-Position Y MSB
0004	R/W	1F	3F	Sprite-Origin X
0005	R/W	1F	3F	Sprite-Origin Y
0006	R/W	00	80	Cursor-Control
0007				Reserved
0008	W	XX	XX	Cursor-RAM Address LSB
0009	W	XX	XX	Cursor-RAM Address MSB
000A	R/W	XX	XX	Cursor-RAM Data
000B				Reserved
000C–000D				Reserved-Undefined

NOTE: Reserved registers should be avoided; otherwise, circuit behavior could deviate from that specified. Reserved-undefined registers are nonexistent locations on the register map.

Table 2–3. TVP3025 Indirect Register Map (Extended Registers) (Continued)

INDEX REGISTER (HEX)	R/W	DEFAULT TVP3025	DEFAULT BT485	REGISTER ADDRESSED BY INDEX REGISTER
000E	R/W	00	04	True Color Control
000F	R/W	00	00	VGA Switch Control
0010	R/W	XX	XX	Window-Start X LSB
0011	R/W	XX	XX	Window-Start X MSB
0012	R/W	XX	XX	Window-Stop X LSB
0013	R/W	XX	XX	Window-Stop X MSB
0014	R/W	XX	XX	Window-Start Y LSB
0015	R/W	XX	XX	Window-Start Y MSB
0016	R/W	XX	XX	Window-Stop Y LSB
0017	R/W	XX	XX	Window-Stop Y MSB
0018	R/W	80	47	Multiplexer Control 1
0019	R/W	98	99	Multiplexer Control 2
001A	R/W	00	00	Input-Clock Selection
001B	R/W	3E	00	Output-Clock Selection
001C	R/W	00	00	Palette Page
001D	R/W	20	00	General Control
001E	R/W	00	54	Miscellaneous Control
001F	R/W	XX	XX	Reserved, Undefined
0020	R/W	XX	00	Overscan Color Red
0021	R/W	XX	00	Overscan Color Green
0022	R/W	XX	00	Overscan Color Blue
0023	R/W	XX	00	Cursor Color 0, Red
0024	R/W	XX	00	Cursor Color 0, Green
0025	R/W	XX	00	Cursor Color 0, Blue
0026	R/W	XX	00	Cursor Color 1, Red
0027	R/W	XX	00	Cursor Color 1, Green
0028	R/W	XX	00	Cursor Color 1, Blue
0029	R/W	09	09	Auxiliary Control
002A	R/W	00	00	General-Purpose I/O Control
002B	R/W	XX	XX	General-Purpose I/O Data
002C	R/W	XX	XX	PLL Control
002D	R/W	XX	XX	Pixel Clock PLL Data
002E	R/W	XX	XX	MCLK PLL Data
002F	R/W	XX	XX	Loop Clock PLL Data
0030	R/W	00	XX	Color-Key OL/VGA Low
0031	R/W	FF	XX	Color-Key OL/VGA High

NOTE: Reserved registers should be avoided; otherwise, circuit behavior could deviate from that specified. Reserved-undefined registers are nonexistent locations on the register map.

Table 2–3. TVP3025 Indirect Register Map (Extended Registers) (Continued)

INDEX REGISTER (HEX)	R/W	DEFAULT TVP3025	DEFAULT BT485	REGISTER ADDRESSED BY INDEX REGISTER
0032	R/W	00	XX	Color-Key Red Low
0033	R/W	FF	XX	Color-Key Red High
0034	R/W	00	XX	Color-Key Green Low
0035	R/W	FF	XX	Color-Key Green High
0036	R/W	00	XX	Color-Key Blue Low
0037	R/W	FF	XX	Color-Key Blue High
0038	R/W	10	XX	Color-Key Control
0039	R/W	08	08	MCLK/DCLK Control
003A	R/W	00	00	Sense Test
003B	R	XX	XX	Test Data
003C	R	XX	XX	CRC LSB
003D	R	XX	XX	CRC MSB
003E	W	XX	XX	CRC Control
003F	R	25	XX	ID
00D5	R/W	00	00	Mode85 Control
00FF	W	XX	XX	Reset

NOTE: Reserved registers should be avoided; otherwise, circuit behavior could deviate from that specified. Reserved-undefined registers are nonexistent locations on the register map.

2.2 Color Palette

Operation of a color palette access is essentially identical for both the TVP3020 and BT485 modes. The color palette is addressed by an internal 8-bit address register for reading/writing data from/to the RAM. This register is automatically incremented following a RAM transfer, allowing the entire palette to be read/written with only one access of the address register. When the address register increments beyond the last location in RAM, it is reset to the first location (address 0). All read and write accesses to the RAM are asynchronous to SCLK, VCLK, and dot clock but performed within one dot clock. Therefore, they do not cause any noticeable disturbance on the display.

The color RAM is 24 bits wide for each location and 8 bits wide for each color. Since a MPU access is eight bits wide, the color data stored in the palette is eight bits even when the six-bit mode is chosen ($8/\overline{6} = 0$). If the six-bit mode is chosen, the two MSBs of color data in the palette have the values previously written. However, if they are read back in the six-bit mode, the two MSBs are 0s to be compatible with IMSG176 and Bt476. The output multiplexer shifts the six LSB bits to the six MSB positions and fills the two LSBs with 0s after the color palette. The multiplexer then feeds the data to the DAC. The test register and the CRC calculation both take data after the output multiplexer, enabling total system verification (TVP3020 modes only). The color palette access is described in the following two sections, and it is fully compatible with IMSG176/8 and Bt476/8.

2.2.1 Writing to Color-Palette RAM

To load the color palette, the MPU must first write to the address register (write mode) with the address where the modification is to start. This is then followed by three successive writes to the palette holding register with 8 bits of red, green, and blue data. After the blue write cycle, the three bytes of color data are concatenated into a 24-bit word that is then written to the RAM location specified by the address register. The address register then increments to the next location, which the MPU can modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations can be written to by writing the start address and performing continuous red, green, and blue write cycles until the entire block has been written.

2.2.2 Reading From Color-Palette RAM

Reading from the palette is performed by writing to the address register (read mode) with the location to be read. This then initiates a transfer from the palette RAM into the holding register, followed by an increment of the address register. Three successive MPU reads from the holding register produce red, green, and blue color data (6 or 8 bits depending on the $8/\overline{6}$ mode) for the specified location. Following the blue read cycle, the contents of the color-palette RAM at the address specified by the address register are copied into the holding register and the address register is again incremented. As with writing to the palette, a block of color values in consecutive locations may be read by writing the start address and performing continuous red, green, and blue read cycles until the entire block has been read. Since the color-palette RAM is dual ported, the RAM may be read during active display without disturbing the video.

2.2.3 Read Masking

The pixel read-mask register is an 8-bit register used to enable or disable a bit plane from addressing the color-palette RAM in the pseudo-color modes. Each palette address bit is logically ANDed with the corresponding bit from the pixel read-mask register before going to the palette-page register (TVP3020 mode only) and addressing the palette RAM.

2.3 Circuit Description Using TVP3025 Register Map

In general, the TVP3025 is a superset of the TVP3020, with several advanced features. These features and other differences are discussed in the appropriate description sections and highlighted in Section 2.3.17.

2.3.1 MPU Interface-8/$\overline{6}$ Operation

The 8/$\overline{6}$ terminal is used to select between an 8- or 6-bit wide data path to the color palette RAM and is provided in order to maintain compatibility with the IMSG176. If miscellaneous-control register bit 2 is set to logic 1, then the 8/$\overline{6}$ terminal is disabled and 8/$\overline{6}$ operation is specified by bit 3 of the miscellaneous-control register. The TVP3020 mode reset default is for the 8/$\overline{6}$ terminal to be enabled (miscellaneous-control register bit 2 = logic 0).

2.3.2 Color Palette – Palette-Page Register

The TVP3020 mode of the device defines a palette-page register as an 8-bit register on the indexed register map. When using 1, 2, or 4 bit planes in the pseudo color modes, the additional planes are provided from the page register before the data addresses the color palette. This is illustrated in Table 2–4.

NOTE:

The additional bits from the page register are inserted after the read mask.

The palette-page register specifies the additional bit planes for the overlay field in direct-color modes with less than 8 bits per pixel overlay.

This register should be set to 00 (hex) before reentering the BT485 mode if it has been modified.

Table 2–4. Allocation of Palette-Page Register Bits

NUMBER OF BIT PLANES	MSB	PALETTE ADDRESS BITS						LSB
8	M	M	M	M	M	M	M	M
4	P7	P6	P5	P4	M	M	M	M
2	P7	P6	P5	P4	P3	P2	M	M
1	P7	P6	P5	P4	P3	P2	P1	M

Pn = n bit from page register
M = bit from pixel port

2.3.3 Input Clock Selection

The TVP3025 VIP provides a maximum of four clock inputs. Two are dedicated as TTL inputs; the other two can be selected as either one differential ECL input or two extra TTL inputs. The TTL inputs can be used for video rates up to 140 MHz. The dual-mode clock input (ECL/TTL) is primarily an ECL input but can be used as TTL-compatible inputs if the input-clock-selection register is so programmed. The clock source used at power up is CLK0; an alternative source can be selected by software during normal operation. This chosen clock input can be used unmodified as the dot clock (representing pixel rate to the monitor). Alternatively, if the input-clock-selection register is programmed to use the internal frequency doubler, the chosen clock source is used as a reference for multiplication.

The input-clock-selection register is used to select the desired input clock source. Table 2–5 details how to program the various options.

Table 2–5. Input-Clock-Selection Register (Index 001A)

INPUT-CLOCK-SELECTION REGISTER (HEX) (see Note 1)	FUNCTION (see Note 2)
00	Select CLK0 as clock source†
01	Select CLK1 as clock source
02	Select CLK2 as TTL clock source
03	Select $\overline{\text{CLK2}}$ as TTL clock source
04	Select CLK2 and $\overline{\text{CLK2}}$ as ECL clock source
05	Select pixel clock PLL as clock source
10	Select CLK0 as doubled clock source
11	Select CLK1 as doubled clock source
12	Select CLK2 as TTL doubled clock source
13	Select $\overline{\text{CLK2}}$ as TTL doubled clock source
14	Select CLK2/$\overline{\text{CLK2}}$ as ECL doubled clock source

† CLK0 is chosen at RESET as required for VGA pass-through.

NOTES: 1. Register bits 3 through 7 are reserved.
2. When the clocks are selected from one input clock source to another, a minimum of 30 ns is needed before the new clocks are stabilized and running.

2.3.4 PLL Clock Generators

In addition to externally supplied clock sources, the TVP3025 has three on chip, fully programmable, frequency synthesis phase-locked loops (PLLs). The first (pixel clock) PLL is intended for pixel clock generation for frequencies up to the device limit. The second (MCLK) PLL is provided for general system clocking such as memory clock, and the third PLL (called the loop clock PLL) is useful for synchronizing pixel data and latch timing by minimizing loop delay. The loop clock PLL is discussed in detail in Section 2.3.7.4.

The clock generators use a modified M over (N x 2^P) scheme to enable a wide range of precise frequencies. The advanced PLLs utilize an internal loop filter to provide maximum noise immunity and reduce jitter. Except for the reference crystal or oscillator, no external components or adjustments are necessary. Each PLL can be independently enabled or disabled for maximum system flexibility. Additionally, a separate MCLK/DCLK control register (index 0039) is provided to allow further frequency division and indepedent control of the MCLK and DCLK outputs. Figure 2–1 illustrates the TVP3025 PLL clocking tree for the pixel clock and MCLK generators.

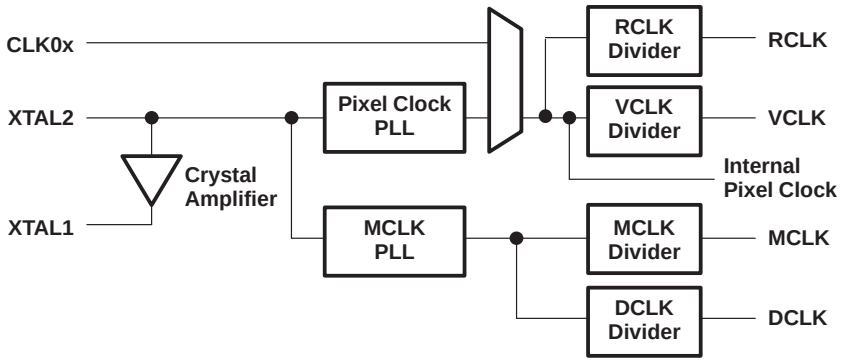


Figure 2–1. Pixel Clock PLL and MCLK PLL Clocking Tree

The PLLs are programmed through a group of four registers on the TVP3025 indirect register map. The registers are listed in the following table.

INDEX	REGISTER
002C	PLL control register
002D	Pixel clock PLL data register
002E	MCLK PLL data register
002F	Loop clock PLL data register

Programming of the M, N, and P value registers is accomplished by writing the appropriate values to bits 0 and 1 of the PLL control register (002C) according to the following table.

BIT 1	BIT 0	REGISTER
0	0	N value register (7-bit)
0	1	M value register(7-bit)
1	0	P value register(post scalar, 2-bit)
1	1	Status register(read-only)

The PLL control register pointer bits above (one set for each PLL data register) are independently auto-incremented following a write cycle to the corresponding PLL data register. Whenever bits 1 and 0 are both written with zeros, all three sets of pointer bits are reset to zero. The current status of each pointer can be identified by reading the PLL control register (002C) according to the following table.

PLL CONTROL REGISTER BITS	POINTER
1:0	Pixel clock PLL data register pointer
3:2	MCLK PLL data register pointer
5:4	Loop clock PLL data register pointer

Since the pointers are auto-incremented, the most efficient way to program the pixel clock PLL is to first write zeros to bits 1 and 0 of the PLL control register, followed by three consecutive writes to the pixel clock PLL data register to program the N, M, and P values. Following the third write, the pixel clock PLL pointer points to the read-only status register, while the MCLK and loop clock PLL pointers point to the corresponding 7-bit N value registers. Two more sets of three consecutive writes to the MCLK and loop clock PLL data registers can be performed, or writes to the PLL registers can be discontinued. Note that these operations do not have to start with the pixel clock PLL data register. The pixel clock PLL can be output on the PCLKOUT terminal by programming the pixel clock PLL P value register bit 3 to a logic 1.

The frequency of the voltage controlled oscillator (VCO) is given by:

$$F_{VCO} = F_{REF} \times ((M + 2) \times 8) / (N + 2)$$

Provided:

$F_{REF} / (N + 2) > 0.5$ MHz and
$110 \text{ MHz} \leq (F_{VCO}) \leq 220$ MHz and
$N, M \geq 1$

Then the PLL output frequency is :

$$F_{PLL} = F_{VCO} / 2^{P}$$

The MCLK and DCLK outputs are further divided and controlled by the MCLK/DCLK control register as detailed in Table 2–6.

Table 2–6. MCLK/DCLK Control Register (Index 0039 hex)

BIT NAME	VALUES	DESCRIPTION
MDCR7	0: Disable (default) 1: Enable	DCLK output enable bit.
MDCR6, MDCR5, MDCR4	000: Divide by 2 (default) 001: Divide by 4 010: Divide by 6 011: Divide by 8 100: Divide by 10 101: Divide by 12 110: Divide by 14 111: Divide by 16	DCLK divide ratio. These bits specify the factor by which the MCLK PLL is divided by before being output on the DCLK output terminal.
MDCR3	0: Disable 1: Enable (default)	MCLK output enable bit.
MDCR2, MDCR1, MDCR0	000: Divide by 2 (default) 001: Divide by 4 010: Divide by 6 011: Divide by 8 100: Divide by 10 101: Divide by 12 110: Divide by 14 111: Divide by 16	MCLK divide ratio. These bits specify the factor by which the MCLK PLL is divided by before being output on the MCLK output terminal. Divide ratios are identical to those specified by bits MDCR6 – MDCR4 for the DCLK divider.

If P value register bit 7 is set to logic 0, then the PLL is disabled upon writing to the corresponding N value register, and the PLL is enabled upon writing to the corresponding P value register. If the P value register bit 7 is set to logic 1, then the PLL is always enabled. If the pixel clock PLL is to be used for pixel clock generation after it has been programmed, the input clock selection register must be set to 05 (hex).

At device reset, the loop clock PLL is disabled and reset, while the MCLK PLL and pixel clock PLL are programmed to give approximately 45 MHz and 25 MHz outputs, respectively with a standard 14.318 MHz crystal reference. For MCLK M = 9, N = 5, P = 1, MCLK/DCLK control = 08 (hex). For pixel clock M = 5, N = 6, P=2.

All PLLs should be programmed such that $F_{REF}/(N + 2) > 1$ MHz and 110 MHz $\leq (F_{VCO}) \leq 220$ MHz for proper operation. Also, N and M should be minimized, but ≥ 1.

For pixel clock PLL output on the PCLKOUT terminal, the pixel clock P value register bit 3 must be set to logic 1.

For the pixel clock PLL to be used as the pixel clock source, it must be selected in the input clock selection register (see Section 2.3.3).

If the MCLK PLL is used to clock the graphics controller, in general, the P value register bit 7 should be set to logic 1 the first time the PLL is written so that the PLL always remains enabled. Otherwise, system lock-up could occur.

2.3.5 Output Clock Selection: RCLK, SCLK, VCLK

The TVP3025 provides user-programmable reference clock (RCLK), shift clock (SCLK), and video clock (VCLK) outputs that can be set as divisions of the dot clock. RCLK is a continuously running reference clock that can be selected as divisions of 1, 2, 4, 8, 16, 32, or 64 of the dot clock (see Table 2–7). It is provided as a clock reference and is typically connected back to the LCLK input to latch pixel-port data or to the graphics controller to provide pixel data and latch timing. Since pixel-port data is latched on the rising edge of LCLK, the RCLK frequency must be set as a function of the desired multiplexing ratio (that depends on the pixel bus width and number of bit planes). See Section 2.3.8 and Table 2–8.

SCLK is the same as RCLK but disabled during the blank active period. SCLK is designed to be used as the shift clock to interface directly with the VRAM. If SCLK is not used, the output can be switched off and held low to protect against VRAM lockup due to invalid SCLK frequencies. The detailed SCLK control timing is discussed in Section 2.3.7.1 and illustrated in Figures 2–3 through 2–5.

VCLK is a general purpose clock that can be selected as divisions of 1, 2, 4, 8, 16, 32, or 64 of the dot clock and can also be held at logic 1 (see Table 2–7). In some systems it can used to generate graphics system control signals ($\overline{\text{SYSBL}}$, $\overline{\text{SYSHS}}$, and $\overline{\text{SYSVS}}$). In this case, it can also be used internally to latch the video control signals into the TVP3025. The default setup is VCLK held at logic 1 since it is not used in VGA pass-through mode.

Internally, RCLK, SCLK, and VCLK are generated from a common clock counter that is counted at the rising edge of the pixel clock as shown in Figure 2–2. VCLK can be programmed to the opposite phase by setting miscellaneous-control register bit 5 to logic 1. The internal clock counter is initialized any time the output-clock-selection register is written with 3F (hex). This provides a simple mechanism to provide a known phase relationship for the various system clocks. Therefore, when VCLK is enabled, it is naturally in phase with RCLK and SCLK as shown in Figure 2–2.

The TVP3020 mode reset default divide ratio for RCLK is 64:1 with SCLK held at logic 0 and VCLK held at logic 1.

When VCLK is used to latch sync and blank, some precautions must be observed when choosing certain video timing parameters if the selected RCLK frequency is less than the selected VCLK frequency. Refer to Appendix B for a more detailed discussion.

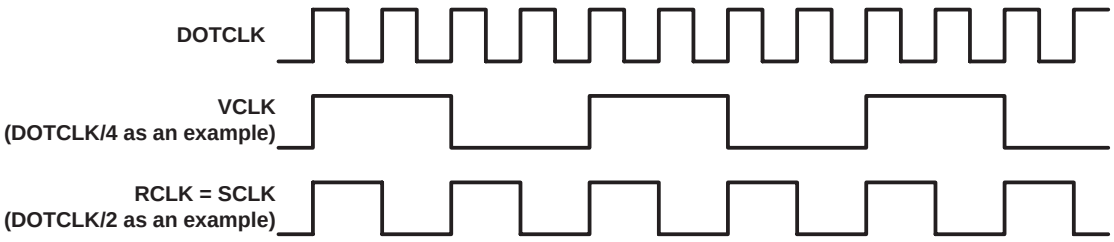


Figure 2–2. DOTCLK / VCLK / RCLK / SCLK Relationship

Table 2–7. Output-Clock-Selection Register Format

OUTPUT-CLOCK-SELECTION-REGISTER BITS (see Note 3)							FUNCTION (see Notes 3, 4, 5, 6, and 7)
6	5	4	3	2	1	0	
x	0	0	0	x	x	x	VCLK/1 output ratio
x	0	0	1	x	x	x	VCLK/2 output ratio
x	0	1	0	x	x	x	VCLK/4 output ration
x	0	1	1	x	x	x	VCLK/8 output ratio
x	1	0	0	x	x	x	VCLK/16 output ratio
x	1	0	1	x	x	x	VCLK/32 output ratio
x	1	1	0	x	x	x	VCLK/64 output ratio
x	1	1	1	x	x	x	VCLK output held at logic 1‡
1	x	x	x	0	0	0	RCLK/1 output ratio
1	x	x	x	0	0	1	RCLK/2 output ratio
1	x	x	x	0	1	0	RCLK/4 output ratio
1	x	x	x	0	1	1	RCLK/8 output ratio
1	x	x	x	1	0	0	RCLK/16 output ratio
1	x	x	x	1	0	1	RCLK/32 output ratio
1	x	x	x	1	1	0	RCLK/64 output ratio
0	x	x	x	1	1	0	RCLK/64, SCLK output held at logic 0‡
x	x	x	x	1	1	1	RCLK, SCLK outputs held at logic 0
x	1	1	1	1	1	1	Clock counter reset

‡ These lines indicate the RESET conditions as required for VGA pass-through mode.

NOTES: 3. Register bit 6 enables (logic 1) and disables (default – logic 0) the SCLK output buffer.
4. Register bit 7 is used for 64-bit BT485 emulation. It is equivalent to BT485 mode command register CR40 (see Section 2.4.15.5). When CR40 is set to logic 1, register bit 7 is set to logic 1, further dividing the RCLK and SCLK by 2. In TVP3025 mode, it should be set to logic 0.
5. When the clocks are selected from one mode to the other, a minimum of 30 ns is needed before the new clocks are stabilized and running.
6. When the output-clock-selection register is written with 3F (hex), the clock counter is reset, RCLK = SCLK = logic 0, and VCLK = logic 1.
7. SCLK is the same as RCLK except that it is disabled during blank. When the RCLK divide ratio is chosen, this sets the SCLK ratio as well.

2.3.6 Frame-Buffer Interface

The TVP3025 provides three output clock signals and one input clock signal for controlling the frame-buffer interface: SCLK, RCLK, LCLK, and VCLK. Clocking of the frame buffer interface is discussed in Section 2.3.7. The 64-terminal interface allows many operational display modes as defined in Section 2.3.8 and Table 2–8. The pixel latching sequence is initiated by a rising edge on LCLK. For those multiplexed modes in which multiple pixels are latched on one LCLK rising edge, the pixel clock shifts the pixels out starting with the pixels that reside on the low numbered pixel port terminals. For example, in an 8-bit-per-pixel pseudo-color mode with an 8:1 multiplex ratio, the pixel display sequence is P(0–7), P(8–15), P(16–23), P(24–31), P(32–39), P(40–47), P(48–55), and P(56–63).

The TVP3025 frame-buffer interface also supports little- and big-endian data formats on the pixel bus. This can be controlled by general-control register bit 3. See Sections 2.3.8.1 and 2.16.1, and Appendix C for details of operation.

2.3.7 Frame-Buffer Clocking

The TVP3025 provides SCLK and RCLK, allowing for flexibility in the frame buffer interface timing. For the pixel port (P0–P63), data is always latched on the rising edge of LCLK. If auxiliary control register bit 3 is

set to logic 1 (default), use of SCLK is assumed and internal pipeline delay is added to sync and blank to account for the delay in the generation of SCLK. If auxiliary control register 3 is set to logic 0, then this pipeline delay is not added, and SCLK should not be used.

2.3.7.1 Frame Buffer Timing Using SCLK

The SCLK signal which is generated in the TVP3025 is intended to be directly connected to VRAM, providing the shift clock to clock data from VRAM onto the TVP3025 pixel input port. The RCLK signal must be used as the timing reference to clock pixel data into this port. Therefore, RCLK is typically directly tied back to LCLK, or LCLK can be a delayed version of RCLK within the timing requirements of the TVP3025. The SCLK timing mode of frame buffer latching is similar to the operation of the TLC3407x VIPs and the same as the TVP3020 VIP device.

The internal TVP3025 blank signal is generated from either $\overline{\text{VGABL}}$ or $\overline{\text{SYSBL}}$, depending on whether the VGA port is enabled (multiplex-control register 2 (MCR2) bit 7 = logic 1) or disabled (MCR2 bit 7 = logic 0). The rising edge of CLK0 is used to latch $\overline{\text{VGABL}}$ when the VGA port is enabled. Unlike the TVP3020, $\overline{\text{SYSBL}}$ can be sampled by either LCLK or VCLK when the VGA port is disabled. The reset default in the TVP3020 mode is for $\overline{\text{SYSBL}}$ to be sampled on the falling edge of VCLK (miscellaneous-control register bit 6 = logic 0). If miscellaneous-control register (index 001E) bit 5 is set to logic 1, then the VCLK polarity is inverted, and $\overline{\text{SYSBL}}$ is sampled on the rising edge of VCLK. To latch $\overline{\text{SYSBL}}$ on the rising edge of LCLK (same timing as the pixel port data on P0–P63), miscellaneous-control register bit 6 should be set to a logic 1.

When the internal blank signal becomes active, SCLK is disabled as soon as possible. For example, if SCLK is high when the sampled $\overline{\text{SYSBL}}$ goes low, SCLK is allowed to complete the clock cycle and return to the low state. SCLK is then held low until the sampled $\overline{\text{SYSBL}}$ signal goes back high. At this time, SCLK is enabled to clock the first pixel data valid from VRAM. The TVP3025 video blanking circuitry is designed with sufficient pipeline delay to allow the internal sampled $\overline{\text{SYSBL}}$ and $\overline{\text{VGABL}}$ signals to align with the pipelined RGB data to the video DACs.

The SCLK control timing is designed to interface directly with the external VRAM. The shift register in the system VRAM is supposed to be updated during the blank active period. When the $\overline{\text{SYSBL}}$ input is sampled system, the VRAM shift clock (SCLK) is restarted to clock the VRAM and enable the first group of pixel data to appear on the pixel bus, as well as at the TVP3025 pixel input port. The second SCLK causes the VRAM shift register to shift out the second group of data. At the same time, LCLK latches the first group of pixel data into the TVP3025 (refer to Figures 2–3 and 2–4 for detailed timing diagrams).

The RCLK/SCLK phase relationship is designed such that timing specifications are satisfied for the case where SCLK is driving a typical 2-MB VRAM load and RCLK is connected to LCLK. If an external buffer is required on SCLK so that it can drive a larger load, a similar buffer can be placed on RCLK to match the signal delay before connecting to LCLK. However, the delay from LCLK to RCLK cannot exceed one RCLK period (7 ns). Refer to the timing parameter specifications for more details.

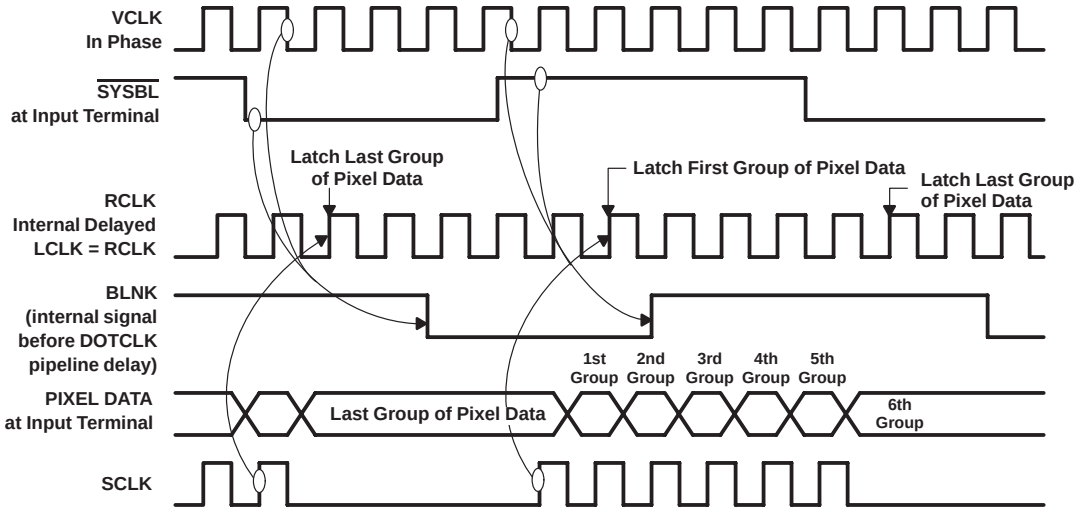


**Figure 2–3. Frame Buffer Timing Using SCLK (VCLK Latched Blank)
(SSRT Disabled, RCLK/SCLK Frequency = VCLK Frequency)**

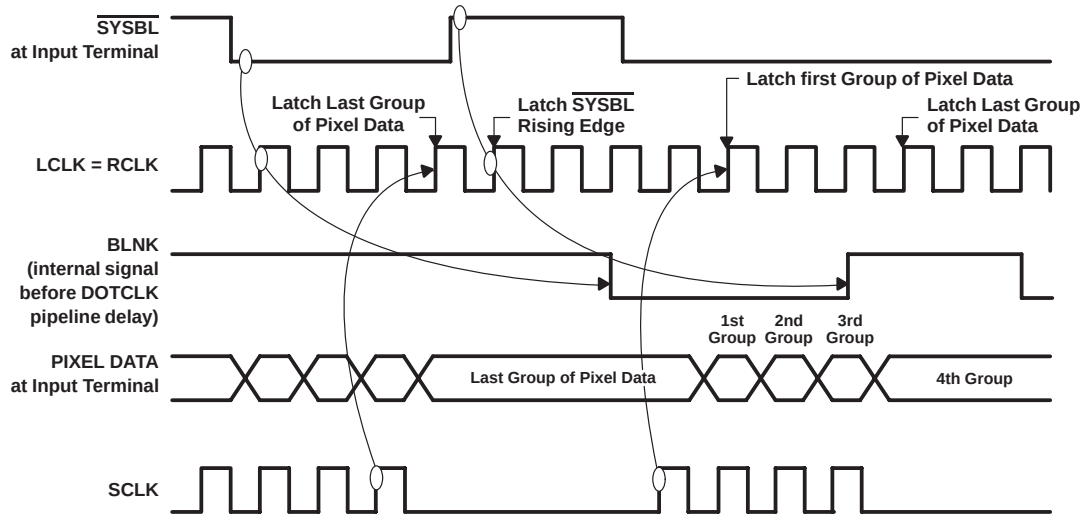


**Figure 2–4. Frame Buffer Timing Using SCLK (LCLK Latched Blank)
(SSRT Disabled, RCLK Connected to LCLK)**

2.3.7.2 Split Shift-Register-Transfer Support

When SCLK is used, the TVP3025 has direct support for split shift-register-transfer (SSRT) VRAMs. In order to allow the VRAMs to perform a split shift-register transfer, an SCLK pulse must be inserted during the blank sequence. This causes the first group of pixel data to appear at the pixel port during blank and allows the first group of data to be displayed as soon as the TVP3025 comes out of blank. When the VRAM split shift-register operation is performed, the SCLK timing is adjusted to work with the SFLAG input. Figure 2–5 shows timing using the SSRT function. When a rising edge occurs on the SFLAG input, one SCLK with a minimum of 15 ns pulse width is generated within the specified delay. The SSRT generated SCLK replaces the first SCLK in the regular shift register transfer case as shown in Figures 2–3 and 2–4.

Note that the SSRT enable bit (bit 2) in the general-control register must be set to a logic 1. The SFLAG minimum duration and other timing requirements and specifications are given in Sections 3.5 and 3.6.

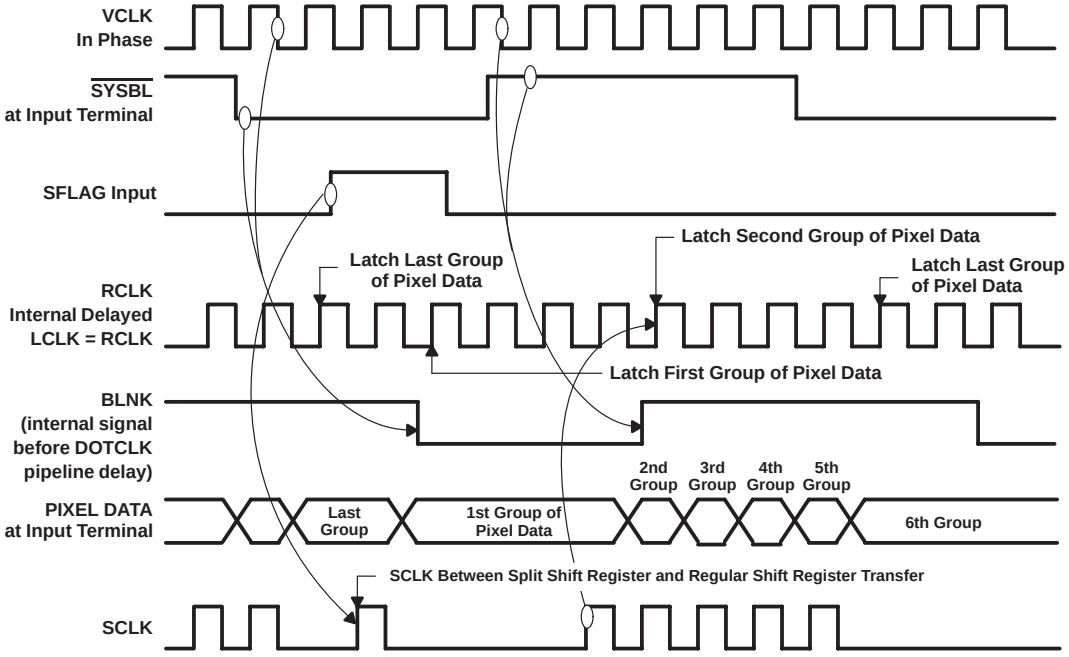


Figure 2–5. Frame Buffer Timing With SSRT (VCLK Latched Blank)
(SSRT Enabled, RCLK/SCLK Frequency = VCLK Frequency)

2.3.7.3 Frame Buffer Timing Without Using SCLK

For those systems where the color palette data latch clock (LCLK) and VRAM shift clock are generated by the graphics controller, the TVP3025 SCLK output cannot be utilized. In these systems, RCLK should be connected to the graphics controller to provide the timing reference for clock generation. Additionally, auxiliary control register bit 3 should be set to a logic 0 so that the video control signals $\overline{\text{SYSBL}}$, $\overline{\text{SYSHS}}$, and $\overline{\text{SYSVS}}$ are aligned with pixel data. These video control signals should be latched on LCLK like the pixel data, so miscellaneous-control register bit 6 should be set to logic 1. Figure 2–6 shows typical frame buffer timing for this case.

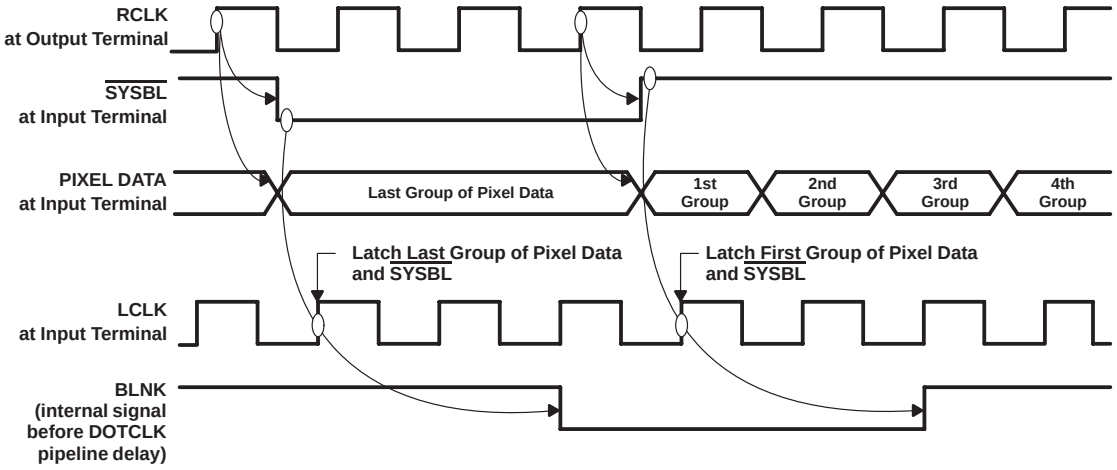


Figure 2–6. Frame Buffer Timing Without Using SCLK

2.3.7.4 Using the Loop Clock PLL to Generate RCLK

Many of the current high performance graphics accelerators with built in VGA support prefer to generate their own VRAM shift clock and pixel data latching clock (LCLK) as discussed in Section 2.3.7.3. As stated before, the TVP3025 provides an RCLK timing reference output to be used by the graphics controller to generate these signals. A common industry problem exists, however in that the delay through the loop (i.e., from RCLK through the controller to produce LCLK and pixel data) may be greater than the RCLK cycle time minus setup time. It then becomes very difficult to resynchronize the rising edges of the LCLK signal to the reference clock (RCLK) within the specified timing requirements. The TVP3025 has incorporated a unique loop clock PLL circuit to maintain a valid LCLK/RCLK phase relationship and ensure that proper LCLK and pixel data setup timing is met, regardless of the amount of system loop delay.

Figure 2–7 illustrates the pixel data latching structure and the operation of the loop clock PLL. RCLK is the internal reference clock signal which is programmed through the output-clock-selection register to be a division of the dot clock. RCLK is very close in phase with the dot clock so that data latched on LCLK can be synchronized to the dot clock within the device. By using the loop clock PLL to phase lock the inverted LCLK input with the TVP3025 generated RCLK signal, an RCLK reference signal is produced that accounts for any delay in the system.

To use the loop clock PLL to generate the RCLK signal, the RCLK divide ratio should first be programmed in the output-clock-selection register to the appropriate divide ratio needed for the pixel data multiplexing mode selected (see Table 2–8). Note that the divide ratio is automatically selected when the multiplex mode is chosen in the BT485 mode of operation. Then the loop clock PLL should be programmed following the procedure in Section 2.3.4. In general, the M and N values should be set to 1. The P value should then be chosen such that, for the expected RCLK frequency, 110 MHz $\leq F_{VCO} \leq$ 220 MHz. Finally the loop clock PLL should be enabled for output on RCLK by setting miscellaneous-control register bit 7 to a logic 1.

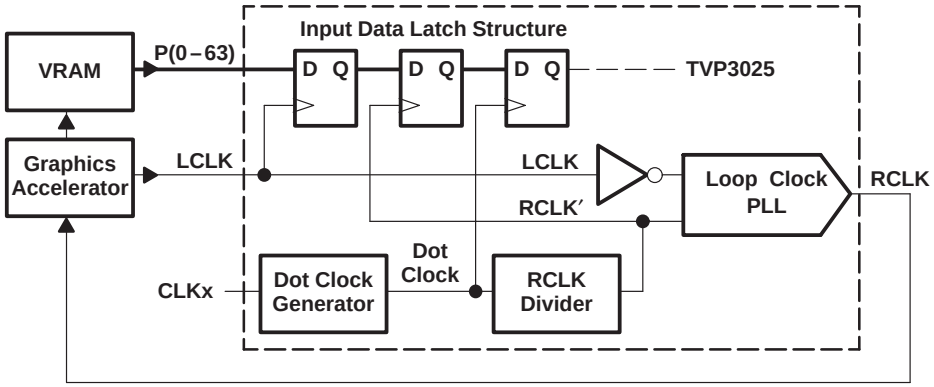


Figure 2–7. Loop Clock PLL Operation

As an example of using the loop clock PLL, consider the case where the pixel clock is running at 128 MHz, and the device is configured for a 64-bit pixel bus, 8-bits/pixel, and 8:1 multiplexing. First the output-clock-selection register should be programmed to 03 (hex) to divide the internal RCLK (see Figure 2–8) by eight. No programming of the output-clock-selection register is needed in the BT485 mode of operation. Then the loop clock PLL N and M value registers should be set to 1. Closed loop PLL dynamics will tend to force the LCLK frequency (derived from the generated RCLK) to equal the RCLK frequency. The P value is chosen such that, for $F_{LCLK} = F_{RCLK}$, the VCO will run in the 110 – 220 MHz range. For this example, the RCLK frequency is simply 128 MHz/8 = 16 MHz. For $F_{LCLK} = F_{RCLK}$, the loop clock PLL needs to generate a signal equal in frequency to RCLK = 16 MHz. Therefore, in order to keep the VCO in the 110–220 MHz range, the P value must be set to 3. Since $F_{PLL} = F_{VCO} / 2^P$ ($F_{VCO} = F_{PLL} \times 2^P$), the VCO frequency will be 128 MHz.

Some graphics controllers internally divide down the RCLK frequency to produce the LCLK. This affects the P value that must be chosen for the loop clock PLL. It does not affect the RCLK divide ratio chosen in the output-clock-selection register, so this should not be changed. For example consider the case above, but with the graphics controller further dividing the generated RCLK reference by eight to produce the LCLK signal. The output-clock-selection register is still programmed to divide by eight, and the M and N PLL values are still set to 1. Again, loop dynamics tend to force $F_{LCLK} = F_{RCLK}$ = 16 MHz. For F_{LCLK} = 16 MHz, the generated RCLK frequency must be eight times this due to the divide by eight in the graphics controller. Therefore, in order to keep the VCO in the 110–220 MHz range, the P value must be set to 0.

Since the maximum P value is 3 (giving $2^P = 8$) and the minimum VCO frequency is 110 MHz, the minimum RCLK frequency that can be generated using the loop clock PLL is 13.75 MHz. For those modes where a lower RCLK frequency is needed, the loop clock PLL is not used, and RCLK is determined from the output-clock-selection register (or multiplexing mode selected in the BT485 mode). Loop delay is not a problem in these cases, since the LCLK signal is at such a low frequency.

Many very efficient graphics system typologies are possible using the loop clock PLL to synchronize the system timing. Implementations are shown in Figures 2–8 and 2–9. Figure 2–8 shows the typical device connection, with PCLKOUT supplying the pixel clock source. If the loop clock PLL is enabled, VGA frequencies over 100 MHz can be achieved. If the loop clock PLL is not enabled, VGA is limited to approximately 25 MHz due to the loop delay in the system. For the highest frequency VGA support, the topology depicted in Figure 2–9 can be utilized, but this requires the use of an external multiplexer.

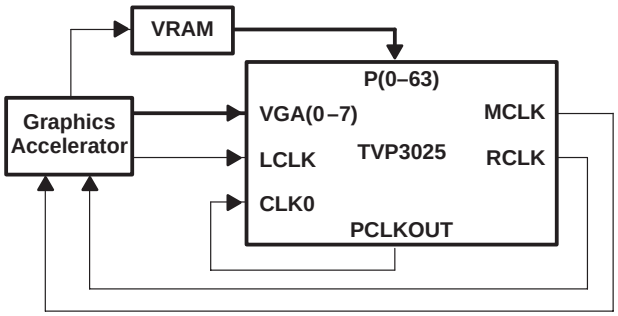


Figure 2–8. Frame Buffer Interface Typical Configuration

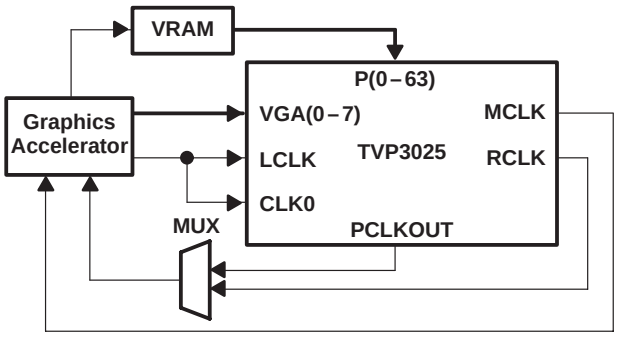


Figure 2–9. Frame Buffer Interface Alternate Configuration

To summarize, the following calculations can be used to select the loop clock PLL P value:

1. F(RCLK′) = F(pixel clock)/multiplex ratio. This is the internal multiplexer clock rate.
2. $110\ \text{MHz}/F(\text{RCLK}')/K \leq 2^P \leq 220\ \text{MHz}/F(\text{RCLK}')/K$
   where:
   P = 0, 1, 2 or 3
   K = any external divide factor
   = 1, 2, 4, ... for /1, /2, /4, ... respectively
3. For reference: $F(\text{RCLK}) = K \times F(\text{RCLK}')$

2.3.8 Multiplexing Modes of Operation

The TVP3025 palette offers a highly versatile multiplexing scheme as illustrated in Table 2–8. The multiplexing modes allow the pixel bus (P0–63) to be programmed to 1, 2, 4, 8, 12, 16, 24, or 32 bits/pixel with pixel bus widths ranging from 1 bit to 64 bits. The use of on-chip multiplexing allows graphics systems to be designed that can support multiple pixel depths and resolutions with no hardware modification. The TVP3025 can also be configured for direct-color or true-color operation.

Multiplexing of the pixel bus is controlled by and programmed through multiplex-control registers 1 and 2. Table 2–8 through 2–11 detail the multiplex-control register settings for each mode of operation.

2.3.8.1 Little-Endian and Big-Endian Data Format

The TVP3025 pixel bus supports both little- and big-endian data formats for all pseudo-color, direct-color, and true-color modes of operation. The data-format select is controlled by general-control register bit 3 (see Section 2.3.18.1). When general-control register (GCR) bit 3 is set to 0 (default), then the format is set to little endian. When GCR bit 3 is set to 1, then the format is set to big endian.

In a big-endian design, the external VRAM data bus bits must be connected in reverse order to the TVP3025 pixel bus; i.e., D63 connected to P0, D0 connected to P63, etc. This ensures that the least significant channel always provides the first pixel to be displayed in the pseudo-color or true-color multiplexing modes. The difference between little- and big-endian data formats and how they affect the pixel bus operation is discussed in detail in Appendix C.

2.3.8.2 VGA Mode

The VGA pass-through mode is used to emulate the VGA modes of most personal computers. The advantage of this mode is that it can take data presented on the feature connector of most VGA-compatible PC systems into the device on a separate bus, thus requiring no external multiplexing. It is also useful for standard VGA and text modes in most graphics applications. VGA is the default mode at reset. If VGA mode is desired at power up, an external resistor, capacitor, and diode network should be connected to the $\overline{\text{RESET}}$ terminal (see Figure A–1).

Since this mode is designed with the feature connector philosophy, all data latching and control timing is referenced to CLK0. When the VGA port is enabled multiplex-control register 2 bit 7 (MCR2 bit 7 = 1), CLK0 is selected as the input clock source independent of the input-clock-selection register. The VGA data latch is always clocked by CLK0. External signals on LCLK have no effect on the VGA port, since LCLK only latches data on the pixel port (P0–P63). CLK0 also latches the $\overline{\text{VGABL}}$, VGAHS, VGAVS video control signals when in the VGA mode.

2.3.8.3 Pseudo-Color Mode

In pseudo-color mode (sometimes called color indexing), the pixel-bus inputs are used to address the palette-RAM color look up table (CLUT). The data in each RAM location is comprised of 24 bits (8 bits for each of the red, green, and blue color DACs). The pseudo-color mode is further grouped into 4 submodes, depending on the data bits per pixel. In each submode, a pixel bus width of 4, 8, 16, 32 or 64 bits may be used. Data should always be presented on the least significant bits of the pixel bus; i.e., when 16 bits are used, the pixel data must be presented on P15–P0, 8 bits on P7–P0, and 4 bits on P3–P0. See Tables 2–8 and 2–9 for more details.

Submode 1 uses a single bit plane to address the color palette. The pixel port bit is fed into bit 0 of the palette address, with the 7 high-order address bits defined by the palette-page register (see Section 2.3.2). This mode allows the maximum amount of multiplexing with a 64:1 ratio.

Submode 2 uses two bit planes to address the color palette. The two bits are fed into the low-order address bits of the palette with the six high-order address bits being defined by the palette-page register. This mode allows a maximum multiplex ratio of 32:1 on the pixel bus and is essentially a four-color alternative to submode 1.

Submode 3 uses four bit planes to address the color palette. The four bits are fed into the low-order address bits of the palette with the four high-order address bits being defined by the palette-page register. This mode provides 16 pages of 16 colors and can be used at multiplex ratios of /1 to /16.

Submode 4 uses eight bit planes to address the color palette. Since all eight bits of palette address are specified from the pixel port, the palette-page register is not used. This mode allows dot clock-to-LCLK ratios of 1:1 (8-bit bus), 2:1 (16-bit bus), 4:1 (32-bit bus) or 8:1 (64-bit bus).

NOTE:

The auxiliary window, port select, and color-key switching functions must be disabled and set for palette graphics when in the pseudo-color mode. This is the default condition at reset. See Section 2.3.10.

2.3.8.4 Direct-Color Mode

In direct-color mode, 24, 16, 15, or 12 bits of data can be transferred directly to the RGB DACs but with the same amount of pipeline delay as the overlay data and the control signals (blank and SYNCs). Depending on which direct-color mode is selected, overlay is provided by utilizing the remaining bits of the pixel bus to address the palette RAM. This results in a 24-bit RAM output that is then used as overlay information to the DACs. The overlay capability is designed to work with the auxiliary window, port select, and color-key switching functions to provide overlay in specific windows or on a pixel-by-pixel basis on the direct-color display as discussed in Section 2.3.10. See Tables 2–8, 2–10, and 2–11 for more details on selecting the direct-color modes.

Submode 1 is the 24-bit direct-color mode that uses eight bits to represent each color and eight bits for overlay. The 64-bit-wide pixel bus of the TVP3025 allows multiplex ratios of 1:1 or 2:1. In this mode, there are basically two different configurations: either the 32-bit data is grouped as overlay, red, green, blue, or blue, green, red, overlay.

Submode 2 is the XGA-compatible (5–6–5) 16-bit-color mode supporting five bits of red, six bits of green, and five bits of blue data. The TVP3025 supports multiplex ratios for this mode of 1:1, 2:1, and 4:1. Overlay is not available in this mode.

Submode 3 is the TARGA-compatible (5–5–5–1) mode that uses 15 bits for color and 1 bit for overlay. It allows 5 bits for each of red, green, and blue data. The TVP3025 supports 1:1, 2:1, and 4:1 multiplexing ratios in this mode.

Submode 4 is the (6–6–4) configuration. It provides six bits of red, six bits of green, and four bits of blue. The TVP3025 also supports 1:1, 2:1, and 4:1 multiplexing in this mode. Overlay is not available in this mode.

Submode 5 is the (4–4–4–4) configuration. It provides 12 bits of direct color and 4 bits of overlay. It allows four bits for each of red, green, and blue data. The TVP3025 supports 1:1, 2:1, and 4:1 multiplexing ratios in this mode.

See NOTES in the following section.

2.3.8.5 True-Color Mode

In true-color mode, the palette RAM is partitioned into three independent 256-word × 8-bit memory blocks that can be individually addressed by each color field of the true-color data. The independent memory blocks provide data for a single DAC output. With this architecture, gamma correction for each color is possible. Since the palette is used in true-color mode, there is no memory space to be used for the overlay function. All of the true-color submodes are the same as direct color except that overlay is not available. See Tables 2–8 through 2–11 for more details on mode selection. See NOTES below.

NOTES:

Since less than 8 bits are defined for each color in the various 12- or 16-bit direct- or true-color modes, the data bits for the individual colors are internally shifted to the MSB locations and the remaining LSB locations for each color are set to logic 0 before 8-bit data is sent to the DACs.

Since the overlay information goes through the pseudo-color data path, it is subject to read masking and the palette-page register. This is especially important for those direct-color modes that have less than eight bits of overlay information. The overlay information in these modes justifies to the LSB positions, and the remaining MSB positions are filled with the corresponding palette-page data before addressing the palette RAM.

In order to display true color (gamma corrected through the palette), either the auxiliary windowing or the color-key switching function must be set for palette graphics. For direct color, both functions must be set for direct color.

In order to use the overlay capability of the direct-color modes, the color-key switching or port-select function must be configured and enabled. Overlay port data in a window is also available by enabling the auxiliary window function. If either the auxiliary windowing or the color-key switching functions point to palette graphics, palette graphics are always displayed (not direct color).

When in the 24-bit direct-color or true-color modes, the data input works only in the 8-bit mode. In other words, if only six bits are used, the two LSB inputs for each color need to be tied to GND. However, the palette, which is used by the overlay input, is still governed by the $8/\overline{6}$ function, and the output multiplexer selects 8 bits or 6 bits of data accordingly. The $8/\overline{6}$ function is also valid in the other 16-bit modes.

The default condition after reset is for the auxiliary window and port select functions to be disabled (ACR1 = ACR2 = logic 0), and the color key comparisons to be disabled (CKC0 = CKC1 = CKC2 = CKC3 = logic 0). Also since multiplex-control register 2 bit 7 = logic 1 and ACR0 = CKC4 = logic 1 at reset, the default is for VGA mode. This is because multiplex-control register 2 bit 7 enables the VGA port, and the switching functions (SWITCH = COLOR-KEY = 1, see Section 2.3.10) are disabled and set for palette graphics (as opposed to direct-color-palette bypass).

Multiplex-control register 1 bit 3 must be set to logic 1 for direct or true color mode operation. This bit setting is different than the TVP3020 VIP.

If the device is reset to the BT485 mode, to program the multiplexer for the TVP3020 true-color modes, true-color control register bit 2 must be set to a logic 0. This is automatically the case if the device is reset into the TVP3020 mode.

The definitions of direct color (palette bypass) and true color are consistent with the IBM XGA terminology.

2.3.8.6 Multiplex-Control Registers

The pixel port multiplexer is controlled by two 8-bit registers in the indirect register map (see Table 2–3). The various multiplexing modes can be selected according to the following table.

Table 2–8. Multiplex Mode and Bus-Width Selection

MODE	SUB-MODE	MULTIPLEX-CONTROL REGISTER 1 (HEX)	MULTIPLEX-CONTROL REGISTER 2 (HEX)	DATA BITS PER PIXEL (see Note 8)	PIXEL BUS WIDTH	MULTI-PLEX RATIO (see Note 9)	OVERLAY BITS PER PIXEL	TABLE REFERENCE (see Note 10)
VGA		80	98	8	8	1	NA	v1
Pseudo-Color	1	80	00	1	4	4	NA	s1
		80	01	1	8	8	NA	s2
		80	02	1	16	16	NA	s3
		80	03	1	32	32	NA	s4
		80	04	1	64	64	NA	s5
	2	80	08	2	4	2	NA	s6
		80	09	2	8	4	NA	s7
		80	0A	2	16	8	NA	s8
		80	0B	2	32	16	NA	s9
		80	0C	2	64	32	NA	s10
	3	80	10	4	4	1	NA	s11
		80	11	4	8	2	NA	s12
		80	12	4	16	4	NA	s13
		80	13	4	32	8	NA	s14
		80	14	4	64	16	NA	s15
	4	80	19	8	8	1	NA	s16
		80	1A	8	16	2	NA	s17
		80	1B	8	32	4	NA	s18
		80	1C	8	64	8	NA	s19

NOTES: 8. Data bits per pixel is the number of bits of pixel port information used as color data for each displayed pixel, often referred to as the number of bit planes.

9. Multiplex ratio indicates the number of pixels per bus load or the number of pixels associated with each LCLK (load clock) pulse. For example, with a 32-bit pixel bus width and 8 bit planes, each bus load consists of four pixels. In a typical implementation, the LCLK signal is either connected to or derived from RCLK. Therefore, the RCLK divide ratio must be chosen as a function of the multiplex mode selected. The RCLK divide ratio is not automatically set by mode selection but must be programmed in the output-clock-selection register by the user.

10. This column is a reference to Tables 2–9 through 2–11, where the actual manipulation of pixel information and pixel latching sequences are illustrated for each of the multiplexing modes.

11. It is recommended that all unused input terminals be connected to ground to conserve power.

12. Auxiliary control register bit 0 and color-key-control register bit 4 default to palette graphics at reset. If direct color operation is desired, then these bits must be set to logic 0.

13. Multiplex-control register 1 bit 3 must be set to logic 1 for direct or true-color mode operation. This bit setting is different than the TVP3020 VIP.

14. If the device is reset to the BT485 mode, to program the multiplexer for the TVP3020 true-color modes, true-color control register bit 2 must be set to a logic 0. This is automatically the case if the device is reset into the TVP3020 mode.

Table 2–8. Multiplex Mode and Bus-Width Selection (Continued)

MODE	SUB-MODE	MULTI-PLEX-CONTROL REGISTER 1 (HEX)	MULTI-PLEX-CONTROL REGISTER 2 (HEX)	DATA BITS PER PIXEL (see Note 8)	PIXEL BUS WIDTH	MULTI-PLEX RATIO (see Note 9)	OVERLAY BITS PER PIXEL	TABLE REFERENCE (see Note 10)
Direct-Color	1 24-bit	0E	1B	24	32	1	8	d1
		0E	1C	24	64	2	8	d2
		0F	1B	24	32	1	8	d3
		0F	1C	24	64	2	8	d4
	2 (5–6–5) XGA	0D	02	16	16	1	NA	d5
		0D	03	16	32	2	NA	d6
		0D	04	16	64	4	NA	d7
	3 (5–5–5–1) TARGA	0C	02	15	16	1	1	d8
		0C	03	15	32	2	1	d9
		0C	04	15	64	4	1	d10
	4 16-bit (6–6–4)	0B	02	16	16	1	NA	d11
		0B	03	16	32	2	NA	d12
		0B	04	16	64	4	NA	d13
	5 12-bit (4–4–4–4)	09	12	12	16	1	4	d14
		09	13	12	32	2	4	d15
		09	14	12	64	4	4	d16

NOTES:
8. Data bits per pixel is the number of bits of pixel port information used as color data for each displayed pixel, often referred to as the number of bit planes.
9. Multiplex ratio indicates the number of pixels per bus load or the number of pixels associated with each LCLK (load clock) pulse. For example, with a 32-bit pixel bus width and 8 bit planes, each bus load consists of four pixels. In a typical implementation, the LCLK signal is either connected to or derived from RCLK. Therefore, the RCLK divide ratio must be chosen as a function of the multiplex mode selected. The RCLK divide ratio is not automatically set by mode selection but must be programmed in the output-clock-selection register by the user.
10. This column is a reference to Tables 2–9 through 2–11, where the actual manipulation of pixel information and pixel latching sequences are illustrated for each of the multiplexing modes.
11. It is recommended that all unused input terminals be connected to ground to conserve power.
12. Auxiliary control register bit 0 and color-key-control register bit 4 default to palette graphics at reset. If direct color operation is desired, then these bits must be set to logic 0.
13. Multiplex-control register 1 bit 3 must be set to logic 1 for direct or true-color mode operation. This bit setting is different than the TVP3020 VIP.
14. If the device is reset to the BT485 mode, to program the multiplexer for the TVP3020 true-color modes, true-color control register bit 2 must be set to a logic 0. This is automatically the case if the device is reset into the TVP3020 mode.

Table 2–8. Multiplex Mode and Bus-Width Selection (Continued)

MODE	SUB-MODE	MULTIPLEX-CONTROL REGISTER 1 (HEX)	MULTIPLEX-CONTROL REGISTER 2 (HEX)	DATA BITS PER PIXEL (see Note 8)	PIXEL BUS WIDTH	MULTI-PLEX RATIO (see Note 9)	OVERLAY BITS PER PIXEL	TABLE REFERENCE (see Note 10)
True-Color	1 24-bit	4E	03	24	32	1	NA	d1
		4E	04	24	64	2	NA	d2
		4F	03	24	32	1	NA	d3
		4F	04	24	64	2	NA	d4
	2 (5–6–5) XGA	4D	02	16	16	1	NA	d5
		4D	03	16	32	2	NA	d6
		4D	04	16	64	4	NA	d7
	3 (5–5–5) TARGA	4C	02	15	16	1	NA	d8
		4C	03	15	32	2	NA	d9
		4C	04	15	64	4	NA	d10
	4 16-bit (6–6–4)	4B	02	16	16	1	NA	d11
		4B	03	16	32	2	NA	d12
		4B	04	16	64	4	NA	d13
	5 12-bit (4–4–4)	49	02	12	16	1	NA	d14
		49	03	12	32	2	NA	d15
		49	04	12	64	4	NA	d16

NOTES:
8. Data bits per pixel is the number of bits of pixel port information used as color data for each displayed pixel, often referred to as the number of bit planes.
9. Multiplex ratio indicates the number of pixels per bus load or the number of pixels associated with each LCLK (load clock) pulse. For example, with a 32-bit pixel bus width and 8 bit planes, each bus load consists of four pixels. In a typical implementation, the LCLK signal is either connected to or derived from RCLK. Therefore, the RCLK divide ratio must be chosen as a function of the multiplex mode selected. The RCLK divide ratio is not automatically set by mode selection but must be programmed in the output-clock-selection register by the user.
10. This column is a reference to Tables 2–9 through 2–11, where the actual manipulation of pixel information and pixel latching sequences are illustrated for each of the multiplexing modes.
11. It is recommended that all unused input terminals be connected to ground to conserve power.
12. Auxiliary control register bit 0 and color-key-control register bit 4 default to palette graphics at reset. If direct color operation is desired, then these bits must be set to logic 0.
13. Multiplex-control register 1 bit 3 must be set to logic 1 for direct or true-color mode operation. This bit setting is different than the TVP3020 VIP.
14. If the device is reset to the BT485 mode, to program the multiplexer for the TVP3020 true-color modes, true-color control register bit 2 must be set to a logic 0. This is automatically the case if the device is reset into the TVP3020 mode.

Table 2–9. Pseudo-Color Mode Pixel-Latching Sequence (see Note 15)

v1	s1	s2	s3	s4	s5	s6	s7
VGA7–VGA0	P0	P0	P0	P0	P0	P1, P0	P1–P0
	P1	P1	P1	P1	P1	P3, P2	P3–P2
	P2	P2	P2	P2	P2		P5–P4
	P3	•	•	•	•		P7–P6
		•	•	•	•		
		P7	P15	P31	P63		

s8	s9	s10	s11	s12	s13	s14	s15
P1–P0	P1–P0	P1–P0	P3–P0	P3–P0	P3–P0	P3–P0	P3–P0
P3–P2	P3–P2	P3–P2		P7–P4	P7–P4	P7–P4	P7–P4
P5–P4	P5–P4	P5–P4			P11–P8	P11–P8	P11–P8
•	•	•			P15–P12	•	•
•	•	•				•	•
P15–P14	P31–P30	P63–P62				P31–P28	P63–P60

s16	s17	s18	s19
P7–P0	P7–P0	P7–P0	P7–P0
	P15–P8	P15–P8	P15–P8
		P23–P16	P23–P16
		P31–P24	•
			•
			P63–P56

NOTE 15: The latching sequence is initiated by a rising edge on LCLK. For modes in which multiple groups of data are latched, the LCLK rising edge latches all the groups and the pixel clock shifts them out starting with the low-numbered group. For example, in pseudo-color submode 3 with a 16-bit pixel bus width, the rising edge of LCLK latches all the data groups shown above (s13) and the pixel clock shifts them out in the order P(3–0), P(7–4), P(11–8), and P(15–12). Note that each line in each subtable above represents one pixel.

Table 2–10. Direct-Color Mode Pixel-Latching Sequence (Little-Endian) (see Note 16)

d1	d2
P31–P24(O), P23–P16(R), P15–P8(G), P7–P0(B) MSB LSB	P31–P24(O), P23–P16(R), P15–P8(G), P7–P0(B) P63–P56(O), P55–P48(R), P47–P40(G), P39–P32(B) MSB LSB
d3	**d4**
P31–P24(B), P23–P16(G), P15–P8(R), P7–P0(O) MSB LSB	P31–P24(B), P23–P16(G), P15–P8(R), P7–P0(O) P63–P56(B), P55–P48(G), P47–P40(R), P39–P32(O) MSB LSB
d5	**d6**
P15–P11(R), P10–P5(G), P4–P0(B) MSB LSB	P15–P11(R), P10–P5(G), P4–P0(B) P31–P27(R), P26–P21(G), P20–P16(B) MSB LSB
d7	**d8**
P15–P11(R), P10–P5(G), P4–P0(B) P31–P27(R), P26–P21(G), P20–P16(B) P47–P43(R), P42–P37(G), P36–P32(B) P63–P59(R), P58–P53(G), P52–P48(B) MSB LSB	P15(O), P14–P10(R), P9–P5(G), P4–P0(B) MSB LSB
d9	**d10**
P15(O), P14–P10(R), P9–P5(G), P4–P0(B) P31(O), P30–P26(R), P25–P21(G), P20–P16(B) MSB LSB	P15(O), P14–P10(R), P9–P5(G), P4–P0(B) P31(O), P30–P26(R), P25–P21(G), P20–P16(B) P47(O), P46–P42(R), P41–P37(G), P36–P32(B) P63(O), P62–P58(R), P57–P53(G), P52–P48(B) MSB LSB
d11	**d12**
P15–P10(R), P9–P4(G), P3–P0(B) MSB LSB	P15–P10(R), P9–P4(G), P3–P0(B) P31–P26(R), P25–P20(G), P19–P16(B) MSB LSB
d13	**d14**
P15–P10(R), P9–P4(G), P3–P0(B) P31–P26(R), P25–P20(G), P19–P16(B) P47–P42(R), P41–P36(G), P35–P32(B) P63–P58(R), P57–P52(G), P12–P48(B) MSB LSB	P15–P12(R), P11–P8(G), P7–P4(B), P3–P0(O) MSB LSB
d15	**d16**
P15–P12(R), P11–P8(G), P7–P4(B), P3–P0(O) P31–P28(R), P27–P24(G), P23–P20(B), P19–P16(O) MSB LSB	P15–P12(R), P11–P8(G), P7–P4(B), P3–P0(O) P31–P28(R), P27–P24(G), P23–P20(B), P19–P16(O) P47–P44(R), P43–P40(G), P39–P36(B), P35–P32(O) P63–P60(R), P59–P56(G), P55–P52(B), P51–P48(O) MSB LSB

NOTE 16: The latching sequence is initiated by a rising edge on LCLK. For modes in which multiple pixel data groups are latched on one LCLK rising edge, the pixel clock shifts them out starting with the low-numbered pixel data group. Note that each line of each subtable above represents one pixel. True-color modes are similar, but the overlay fields are not supported.

Table 2–11. Direct-Color Mode Pixel-Latching Sequence (Big-Endian) (see Note 17)

d1	d2
P31–P24(B), P23–P16(G), P15–P8(R), P7–P0(O) LSB MSB	P31–P24(B), P23–P16(G), P15–P8(R), P7–P0(O) P63–P56(B), P55–P48(G), P47–P40(R), P39–P32(O) LSB MSB
d3	**d4**
P31–P24(O), P23–P16(R), P15–P8(G), P7–P0(B) LSB MSB	P31–P24(O), P23–P16(R), P15–P8(G), P7–P0(B) P63–P56(O), P55–P48(R), P47–P40(G), P39–P32(B) LSB MSB
d5	**d6**
P15–P11(B), P10–P5(G), P4–P0(R) LSB MSB	P15 – P11(B), P10 – P5(G), P4 – P0(R) P31 – P27(B), P26 – P21(G), P20 – P16(R) LSB MSB
d7	**d8**
P15 – P11(B), P10 – P5(G), P4 – P0(R) P31 – P27(B), P26 – P21(G), P20 – P16(R) P47 – P43(B), P42 – P37(G), P36 – P32(R) P63 – P59(B), P58 – P53(G), P52 – P48(R) LSB MSB	P15 – P11(B),P10 – P6(G),P5 – P1(R),P0(O) LSB MSB
d9	**d10**
P15 – P11(B), P10 – P6(G), P5 – P1(R), P0(O) P31 – P27(B), P26 – P22(G), P21 – P17(R), P16(O) LSB MSB	P15 – 11(B), P10 – P6(G), P5 – P1(R), P0(O) P31 – P27(B), P26 – P22(G), P21 – P17(R), P16(O) P47 – P43(B), P42 – P38(G), P37 – P33(R), P32(O) P63 – P59(B), P58 – P54(G), P53 – P49(R), P48(O) LSB MSB
d11	**d12**
P15 – P12(B), P11 – P6(G), P5 – P0(R) LSB MSB	P15 – P12(B), P11 – P6(G), P5 – P0(R) P31 – P28(B), P27 – P22(G), P21 – P16(R) LSB MSB
d13	**d14**
P15 – P12(B), P11 – P6(G), P5 – P0(R) P31 – P28(B), P27 – P22(G), P21 – P16(R) P47 – P44(B), P43 – P38(G), P37 – P32(R) P63 – P60(B), P59 – P54(G), P53 – P48(R) LSB MSB	P15 – P12(O), P11 – P8(B), P7 – P4(G), P3 – P0(R) LSB MSB
d15	**d16**
P15 – P12(O), P11 – P8(B), P7 – P4(G), P3 – P0(R) P31–P28(O), P27– P24(B), P23 – P20(G), P19 – P16(R) LSB MSB	P15 – P12(O), P11 – P8(B), P7 – P4(G), P3 – P0(R) P31–P28(O), P27–P24(B), P23–P20(G), P19–P16(R) P47–P44(O), P43–P40(B), P39–P36(G), P35–P32(R) P63–P60(O), P59–P56(B), P55–P52(G), P51–P48(R) LSB MSB

NOTE 17: The latching sequence is the same as little-endian. Each line represents one pixel. These subtables assume that the pixel bus is externally reverse-wired as shown in Appendix C. True-color modes are similar, but overlay fields are not supported.

2.3.9 On-Chip Cursor

The TVP3025 has an on-chip two-color 64 x 64 pixel user-definable cursor. The cursor operation defaults to the XGA standard, but X-windows compatibility is also available (see Section 2.3.9.2). In addition to the 64 × 64 sprite cursor, the device also supports a two-color crosshair cursor. The cursors only operate in noninterlaced applications.

The pattern for the 64 × 64 cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. Cursor positioning is performed via the cursor-position (x,y) registers and the sprite-origin (x,y) registers (see register bit definitions in Sections 2.3.18.4 and 2.3.18.5). Positions x and y are defined in the TVP3025 increasing from left to right and from top to bottom, respectively, as seen on the display screen. The cursor position (x,y) is relative to the first pixel displayed. In other words, the very first pixel displayed is located at position (0,0), and the last pixel displayed for a 1024 × 768 system is located at position (1023, 767).

On-chip cursor control is performed by the cursor-control register in the indirect register map (06 hex). Bits 0 and 1 control the width of the crosshair (1, 3, 5, or 7 pixels). Bit 2 enables/disables the crosshair cursor, and bit 3 controls the crosshair-cursor color. Bit 4 specifies either XGA or X-window mode for the sprite cursor. Bit 5 controls the color at the intersection of the sprite and crosshair cursors, and bit 6 enables/disables the sprite cursor. See the cursor-control register bit definitions in Section 2.3.18.3 for more details.

2.3.9.1 Cursor RAM

The 64 × 64 × 2 cursor RAM is used to define the pixel pattern within the 64 × 64 pixel cursor window. It is not initialized and may be written to or read by the MPU at any time. The cursor-RAM address zero is at the top left corner of the RAM as shown in Figure 2–10.

The cursor RAM is written to by loading a number into the cursor RAM MS address and cursor RAM LS address. Address registers 09 and 08 (hex) of the index register indicate the location of the first group of four cursor pixels to be updated (two bits per pixel implies four pixels per byte). Then the first four pixels are written to the cursor-RAM data register [0A (hex) of the index register]. This stores the cursor pixel data in the cursor RAM and automatically increments the cursor-RAM address register. A second write to the cursor-RAM data register then loads the next four cursor pixels, and so on. See the register bit definitions in Sections 2.3.18.9 and 2.3.18.10.

To read from the cursor RAM, the address of the first cursor-RAM location to be read is loaded into the cursor-RAM address registers. Then a read is performed on the cursor-RAM data register [0A (hex) of the index register]. Similar to the cursor-RAM write operation, when the read is completed the cursor-RAM address register is automatically incremented and further reads read successive cursor RAM locations.

The cursor RAM is written and read using the same hardware registers, so any task updating either of these on an interrupt thread must save and restore the cursor-RAM LS address [index 08 (hex)] and cursor-RAM MS address [index 09 (hex)] registers.

NOTES:

When the cursor-RAM address is to be written, always write both the cursor-RAM LS and MS address registers with the cursor-RAM LS address register first.

The cursor-generation logic requires the use of active low sync inputs. Vertical retrace is determined by detecting multiple syncs in blank.

The video front-porch time must be at least one RCLK period. The video back-porch time must be at least 80 pixel clock periods.

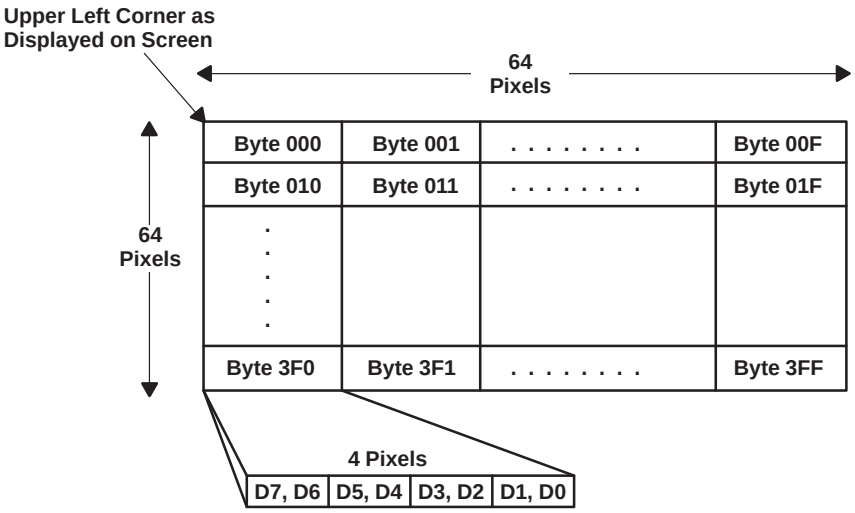


Figure 2–10. Cursor-RAM Organization

2.3.9.2 Two-Color 64 × 64 Cursor

The 64 × 64 × 2 cursor RAM provides two bits of cursor information on every pixel clock (DOTCLK) cycle during the 64 × 64 cursor window. Cursor-control register bit 4 specifies whether the XGA mode (default = logic 0) or X-window mode (logic 1) standard is used to interpret the cursor information. The two bits of cursor pixel data determine the cursor appearance as shown in the table below:

RAM		COLOR SELECTION	
PLANE 1	PLANE 2	XGA MODE	X-WINDOW MODE
0	0	Cursor color 0	Transparent
0	1	Cursor color 1	Transparent
1	0	Transparent	Cursor color 0
1	1	Complement	Cursor color 1

Cursor color 0 and 1: These colors are set by writing to the cursor-color 0 and cursor-color 1 registers [index 23–28 (hex)].

Transparent: The underlying pixel color is displayed.

Complement: The ones complement of the underlying pixel color is displayed.

2.3.9.3 64 × 64 Cursor Positioning

The cursor-position (x,y) registers are used in conjunction with the sprite-origin (x,y) registers to position the 64 × 64 cursor on the display screen. The cursor-position (x,y) registers specify the location of the cursor on the display screen relative to the first displayed pixel out of blank. The sprite-origin (x,y) register specifies where to origin the 64 × 64 cursor array relative to the cursor position (x,y). Upon reset, the sprite-origin (x,y) register automatically defaults to (31, 31). Therefore, the cursor-position (x,y) registers specify the location on the active display screen of the 31st column and 31st row (counting from top left) of the 64 × 64 cursor array. The crosshair cursor intersects at the center of the sprite cursor area.

The sprite-origin (x,y) registers can be programmed from (0,0) to (63,63). For example, if the sprite-origin (x,y) registers are programmed to (0,0), the 64 × 64 cursor array is located in the lower right quadrant with respect to the cursor position (x,y). Figure 2–11 illustrates this more clearly by showing the 64 × 64 cursor array location relative to the cursor position (x) for different sprite-origin values.

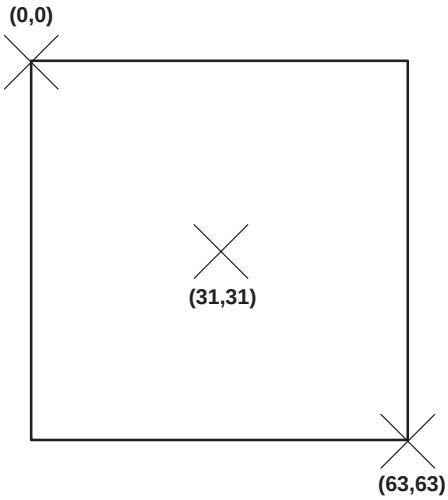


Figure 2–11. Common Sprite-Origin Settings

NOTE:

The programmable sprite-origin feature can be especially useful in creating crosshair cursors and pointers. See Section 2.3.9.5 and Figures 2–11 and 2–12 for more details.

2.3.9.4 Crosshair Cursor

Cursor positioning for the crosshair cursor is also done through the cursor-position (x,y) registers. The intersection of the crosshair cursor is specified by the cursor-position (x,y) registers. If the thickness of the crosshair cursor is greater than one pixel, the center of the intersection is the reference position. The thickness of the crosshair cursor is specified by cursor-control register bits 0 and 1 (see Section 2.3.18.3). The sprite-origin (x,y) registers have no effect on the crosshair cursor location.

In order to display the crosshair cursor, cursor-control register bit 2 needs to be enabled while CCR bit 3 is used to set the desired color as shown in the following table:

CCR2	CCR3	CROSSHAIR COLOR
0	0	Crosshair not displayed
0	1	Crosshair not displayed
1	0	Cursor color 0
1	1	Cursor color 1

The crosshair cursor is limited to being displayed within a window, which is specified by the window-start (x,y) and window-stop (x, y) registers. Since the cursor-position (x,y) registers must specify a point within the window boundaries, it is the responsibility of the user software to ensure that the cursor-position (x,y) registers do not specify a point outside the defined window. Refer to Figure 2–12, which shows the relationship between the different window and cursor register specifying regions.

If a full-screen crosshair cursor is desired, the window-start (x,y) registers should contain 0000 (hex) and the window-stop (x,y) registers should be set to the last pixel location on the active screen. For the crosshair cursor to be displayed, the window-start and window-stop registers must contain locations on the active screen. To temporarily remove the crosshair cursor from the screen without disabling the function, the window-start registers can be programmed with a location off the active screen.

The crosshair cursor and the auxiliary window function utilize the same set of window registers. Therefore, care must be taken if the crosshair cursor is to be displayed when the auxiliary window function is enabled (ACR0 = 1). See Section 2.3.18.11.

2.3.9.5 Dual-Cursor Positioning

Both the user-definable 64 × 64 cursor and the crosshair cursor can be enabled for display simultaneously, allowing the generation of custom crosshair cursors. As previously mentioned, the sprite-origin (x,y) registers specify the 64 × 64 cursor pattern location relative to the cursor position and crosshair cursor.

Figure 2–12 illustrates displaying the dual cursors, showing the relationship between the auxiliary window, the crosshair cursor, and the 64 × 64 cursor for the case where the sprite-origin (x,y) registers are set to (31, 31).

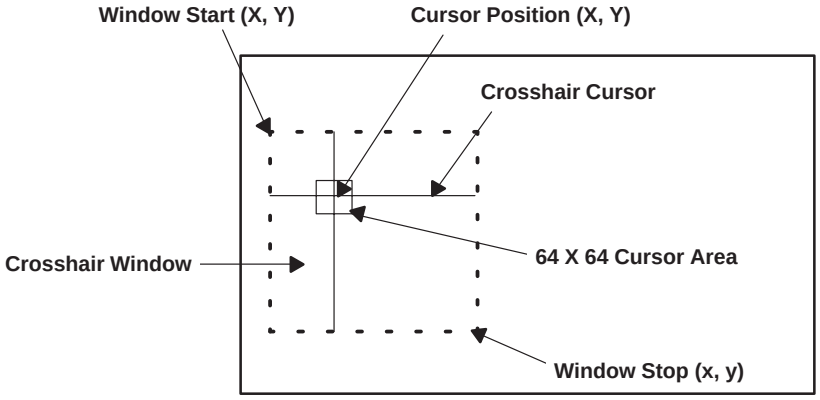


Figure 2–12. Dual-Cursor Positioning

Figure 2–13 shows one possible custom cursor that could be created by setting the sprite-origin registers to (0,0) and drawing an arrow in 64 × 64 cursor RAM. The cursor window has been set to full screen by setting the window-start (x,y) registers to 0000 (hex) and the window-stop registers to the last active pixel location. The 64 × 64 cursor area could be located in different locations about the cursor position by programming the sprite-origin (x,y) registers to different values as described earlier (see Section 2.3.9.3).

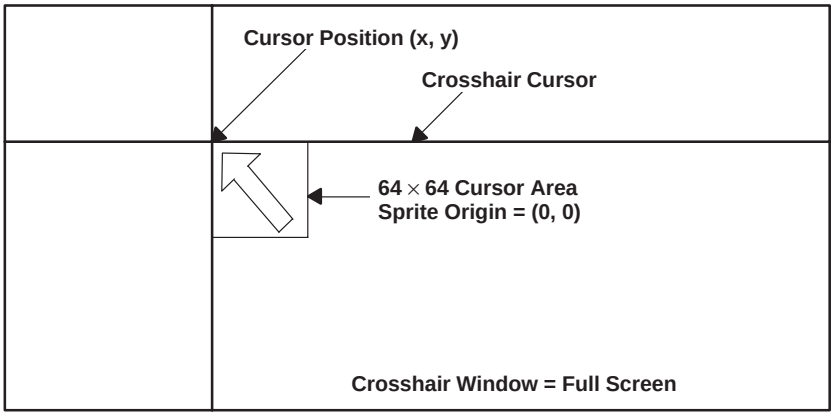


Figure 2–13. One Possible Custom Cursor Creation

When both the 64 x 64 user-definable cursor and the crosshair cursor are enabled, cursor-control register bit 5 specifies the display at the intersection of the crosshair cursor and the 64 × 64 user-definable cursor. The following cursor intersection truth table details the results of all cursor color combinations; see Section 2.3.18.3 for specific cursor-control register bit definitions.

CROSSHAIR	64 x 64 CURSOR	CCR5 = 0	CCR5 = 1
Color 0	Transparent	Color 0	Color 0
Color 1	Transparent	Color 1	Color 1
Color 0	Complement	Color 0	Color 0
Color 1	Complement	Color 1	Color 1
Color 0	Color 0	Color 0	Transparent
Color 1	Color 0	Color 1	Transparent
Color 0	Color 1	Color 0	Complement
Color 1	Color 1	Color 1	Complement

2.3.10 Auxiliary Window, Port Select, and Color-Key Switching

The TVP3025 provides three integrated mechanisms for switching between VGA or overlay images and direct-color images midscreen. The auxiliary window function supports the display of overlay or VGA graphics into a specified window on the screen when in a direct-color mode. The same window registers used to define the crosshair cursor window are used to define the auxiliary window start and window stop (see Sections 2.3.18.6 and 2.3.18.7). One application of this function is to fit a VGA picture in the middle of a direct-color display. The port-select function utilizes an external terminal (PSEL) to switch between VGA or overlay and direct-color on a pixel-by-pixel basis, enabling the generation of multiple VGA or overlay windows on a direct-color screen.

The auxiliary-window and port-select functions are integrated so that they can be enabled simultaneously or separately. They are only operable when in one of the direct-color modes, since both VGA and overlay utilize the palette RAM. Overlay windowing is not supported for those direct-color modes that do not have overlay capability. If VGA windowing is to be performed, multiplex-control register 2 needs to have bit 7 set to a logic 1 (activating the VGA port) and the appropriate direct-color mode must be chosen with the remaining multiplex-control register bits. When the VGA port is activated (MCR2 bit 7 = 1), the overlay is disabled.

The auxiliary-window and port-select functions are controlled by the auxiliary-control register, which is programmed through the indirect register map (29 hex, see Section 2.3.18.11 for register bit definitions).

Like the crosshair cursor window, for auxiliary graphics to be displayed, both the window-start and window-stop registers must contain locations on the active screen. If full-screen auxiliary graphics is desired, the window-start (x,y) registers should contain 0000 (hex) and the window-stop (x,y) registers should be set to the last active pixel location. The window-start registers can be programmed with a location off the active screen to temporarily remove the auxiliary window without disabling the function entirely.

The color-key switching function allows switching between VGA or overlay and direct-color on a pixel-by-pixel basis by comparing the incoming VGA/overlay and direct-color data with user-programmable color-key ranges. The color-key ranges are set by writing to the eight 8-bit color-key range registers: color-key red (low, high), color-key green (low, high), color-key blue (low, high), and color-key OL/VGA (low, high). The color-key switching function is controlled by the color-key-control register (see Section 2.3.9.2) All of the registers can be programmed through the indirect register map. When the VGA port is activated (MCR2 bit 7 = 1), the color-key OL/VGA register (low, high) color comparison is performed on VGA data and the VGA port is color-key switched instead of overlay.

The windowing and color-key switching functions are integrated much like a logical OR function. If either of the functions switches to palette graphics (VGA or overlay through the palette RAM), palette graphics are

displayed instead of direct color. Therefore, when programming the device for any direct-color mode, both the color-key-control and auxiliary-window registers must be set such that direct-color graphics is displayed. For true color (gamma corrected through the palette), one of the functions must be set to palette graphics. If VGA switching is performed, it is recommended that the VGA blank and sync signals also be utilized.

2.3.10.1 VGA Switch Control Register

The VGA switch control register provides synchronization functions needed to allow VGA switching with multiplexed pixel modes. Resynchronization of the internal clock counters to the VGA blank or sync control signals is provided so that the first VGA pixel coming out of blank always aligns with the first pixel in a group of data latched on LCLK. Also, the register allows adjustment of the VGA pipeline delay to account for the differences associated with multiplexed pixel port modes. This register is detailed below.

BIT NAME	VALUES	DESCRIPTION
VSCR4	1: Enable	Divider synchronization enable. If this bit is set to logic 1, resynchronization of the clock counters is enabled.
	0: Disable (default)	
VSCR3	1: Rising edge	Divider reset control edge. Determines which edge of the signal set by VSCR2 is used.
	0: Falling edge	
VSCR2	1: VGAHS	Divider reset control input. This bit determines whether VGA sync or blank resynchronizes the clock counters.
	0: $\overline{\text{VGABL}}$	
VSCR1, 0	11: +6, for 4:1 multiplexing	VGA pipeline delay control. Allows adjustment of the VGA pipeline delay for different pixel port multiplexing modes.
	10: +2, for 2:1 multiplexing	
	00: +0, for 1:1 multiplexing	

2.3.10.2 Windowing Control

The TVP3025 supports several windowing formats. These are specified by the auxiliary-control register bits 0–2 and PSEL as shown below.

Window context switching is determined by the following equation:

$$SWITCH = [(PSEL \times ACR2) + (WINDOW \times ACR1)] \oplus ACR0$$

where:

WINDOW = 1 inside the auxiliary window.
ACR*n* is the nth bit of the auxiliary-control register.

The following table then applies:

MULTIPLEX MODE SELECTED	DISPLAY RESULT	
	SWITCH = 0	SWITCH = 1
Direct-color with VGA	Direct-color	VGA
Direct-color	Direct-color	Overlay

NOTES: 18. The multiplex mode is set by multiplex-control registers 1 and 2. If VGA switching is desired, multiplex-control register 2 bit 7 needs to be set to a logic 1 to enable the VGA port and the desired direct-color mode must be chosen with the remaining MCR bits. For example, if direct-color mode 1 is chosen and multiplex-control register 2 is normally set to 1B (hex), it would instead be set to 9B (hex) for VGA switching.

19. The DAC output is undefined if SWITCH = 1 when doing overlay switching in a direct-color mode that does not have overlay capability.

20. Auxiliary-control register bits ACR2 and ACR1 can be used to independently enable or disable the port-select and windowing functions as shown in the equation above. If both switching functions are disabled, ACR0 is used to default the display to either direct color or palette graphics. Palette graphics are either VGA or overlay if in a direct-color mode or pseudo-color when in the pseudo-color mode. The reset default is for palette graphics to be displayed–as needed for the VGA pass-through mode.

21. The device supports switching when using multiplexing modes. However, caution must be observed when using the port select function with the multiplexing modes other than 1:1, since the PSEL signal is latched on LCLK (same as the pixel port).

2.3.10.3 Color-Key-Switching Control

The TVP3025 supports color-key-switching modes in which color data from the direct-color and overlay or VGA ports is compared to a set of user-definable color-key registers. Based on the outcome of the comparison, either direct color, overlay, or VGA are displayed (see Note 22). High and low color-key registers are provided for each color and overlay/VGA so that ranges of colors can be compared as opposed to a single color value. The register bit definitions for the color-key OL/VGA (low, high), color-key red (low, high), color-key green (low, high), and color-key blue (low, high) range registers are shown in Section 2.3.18. The color-key function is controlled by the color-key-control register bits 0–4. This register definition is shown in Section 2.3.18.12.

Color-key switching is performed according to the following equation:

$$\text{COLOR–KEY} = [(\text{OL} + \overline{\text{CKC0}}) \times (\text{R} + \overline{\text{CKC1}}) \times (\text{G} + \overline{\text{CKC2}}) \times (\text{B} + \overline{\text{CKC3}})] \oplus \overline{\text{CKC4}}$$

where:	OL = 1	if	color-key OL/VGA low	≤ overlay or VGA (Note 22)	≤ color-key OL/VGA high
	R = 1	if	color-key red low	≤ direct color (RED)	≤ color-key red high
	G = 1	if	color-key green low	≤ direct color (GREEN)	≤ color-key green high
	B = 1	if	color-key blue low	≤ direct color (BLUE)	≤ color-key blue high

then if COLOR–KEY = 1, overlay or VGA is displayed.
if COLOR–KEY = 0, direct-color is displayed.

NOTES: 22. When the VGA port is activated (MCR2 bit 7 = 1), the color-key OL/VGA register (low,high) color comparison is performed on VGA data and the VGA port is color-key switched. If the VGA port is not activated (MCR2 bit 7 = 0) the comparison is performed on overlay data and overlay is color-key switched.

23. CKC0–CKC3 can be used to individually enable or disable certain colors in the comparison for maximum flexibility. If color-key switching is not desired, CKC0–CKC3 should be set to logic 0. CKC4 is then used to set the default for either direct color or palette graphics. The default condition at reset is CKC0 = CKC1 = CKC2 = CKC3 = logic 0 and CKC4 = logic 1. This causes the function to default to palette graphics as required for VGA pass-through mode.

24. The color-key comparison for the overlay and VGA data is performed after the read mask and palette page registers so that an 8-bit comparison can be performed. This also gives the maximum flexibility to the user in performing the color comparisons. If the overlay defined for a given mode is less than 8 bits per pixel, the data is shifted to the LSB locations and the palette-page register fills the remaining MSB positions.

25. For those direct-color modes that have less than 8 bits per pixel of red, green, and blue direct-color data, the data is internally shifted to the MSB positions for each color and the remaining LSB bits are filled with logic 0s before the 8-bit comparisons are performed.

26. The windowing and color-key functions are integrated such that if either SWITCH = 1 (windowing case, see Section 2.3.10) or color key = 1, palette graphics are displayed (overlay or VGA depending on multiplex-control register 2 bit 7) instead of direct-color data. Both functions must be correctly set for proper operation.

2.3.11 Overscan

The TVP3025 provides the capability to produce a custom screen border using the overscan function. The overscan function is enabled by general-control register (GCR) bit 6. The overscan color is user-programmable by writing to the overscan color red, green, and blue registers in the indirect register map.

If the overscan function is enabled (GCR6 = logic 1), then overscan color is displayed any time that OVS is high and blank is low (active). Note that blank is the internal blank signal and can either be generated from VGABL or SYSBL depending on the mode selected.

If overscan is enabled, then the blanking pedestal is imposed on the analog outputs when both OVS and blank are low. If overscan is disabled, then the blanking pedestal occurs when blank is low. Blank can be either SYSBL or VGABL depending on the state of multiplex-control register 2 bit 7.

If VGA is disabled, OVS is sampled the same as the SYSBL signal (either on VCLK or LCLK depending on miscellaneous-control register bit 6). If VGA is enabled, then OVS is sampled on the rising edge of CLK0.

In this way, the video timing relationship is maintained since the same method and pipeline delay are applied to the SYSBL and VGABL signals.

Figure 2–14 demonstrates the use of OVS to produce a custom overscan screen border.

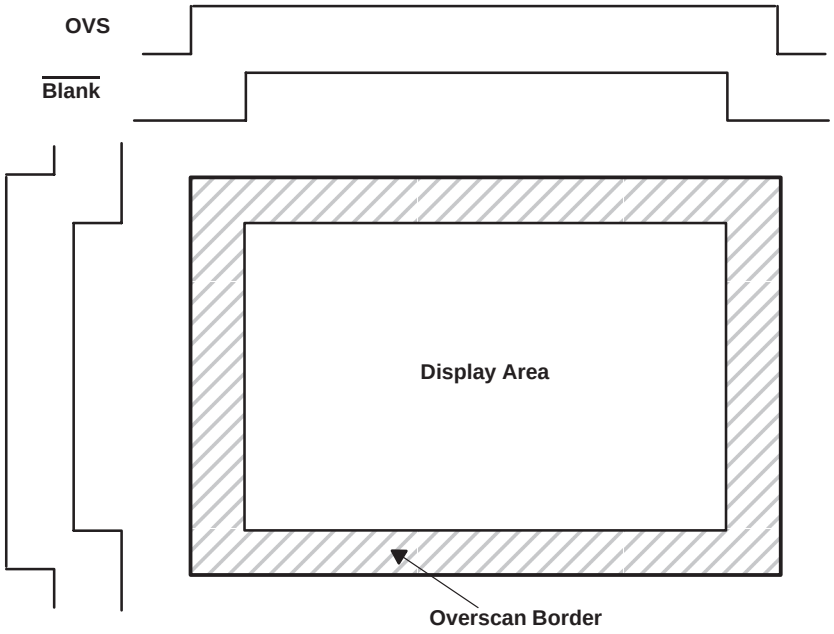


Figure 2–14. Overscan

2.3.12 Horizontal Zooming

The TVP3025 supports a user-programmable horizontal zooming function of 2, 4, 8, 16, or 32x. Zooming can be controlled through the auxiliary control register on the indirect register map as shown by the following table. The RCLK divide ratio also has to be modified in the output-clock-selection register.

ACR7	ACR6	ACR5	HORIZONTAL ZOOM
0	0	0	1x (default)
0	0	1	2x
0	1	0	4x
0	1	1	8x
1	0	0	16x
1	0	1	32x

When one of the horizontal zooms (besides 1x) is chosen, the internal pixel multiplexer is configured such that it replicates the pixel data on successive dot clocks by the number of times specified by ACR(5–7). Also the RCLK divide ratio must be modified in the output-clock-selection register to facilitate the pixel replication. The new RCLK divide ratio should be chosen as the old RCLK divide ratio multiplied by the zoom factor. It is recommended that the zoom only be changed during vertical retrace.

The horizontal zoom function applies only to the pixel port (P0–63) data. VGA data is not zoomed.

2.3.13 Test Functions

The TVP3025 provides several functions that enable system testing and verification. These are detailed in Sections 2.3.13.1 through 2.3.13.3.

2.3.13.1 16-Bit CRC

A 16-bit cyclic redundancy check (CRC) is provided so that video data integrity can be verified at the input to the DACs. The CRC is updated on the second horizontal sync (either SYSHS or VGAHS) rising edge during vertical retrace and is only calculated on the active screen area; i.e., active blank stops the calculation. The CRC can be performed on any of the 24 data lines that enter the DACs and is controlled by the CRC-control register (CRCC bits 0–4). Values from 0 to 23 may be written to this register to select between the 24 different DAC data inputs. Value 0 corresponds to DAC data red 0 (LSB), value 7 to red 7 (MSB), value 8 to green 0 (LSB), value 15 to green 7 (MSB), value 16 to blue 0 (LSB), and value 23 to blue 7 (MSB). The 16-bit remainder that is calculated on the individual DAC data line can be read from the CRC LSB and CRC MSB registers. See Table 2–3 for the indirect register map address. See Sections 2.3.18.15 and 2.3.18.16 for the CRC register bit definitions.

As long as the display pattern for each screen remains fixed, the CRC result should remain constant. If the CRC result changes, an error condition should be assumed. Since the CRC is calculated using the common CRC–16 polynomial ($X^{16} + X^{15} + X^2 + 1$), the user can calculate and store the CRC remainder for a test screen in software and compare this to the TVP3025-calculated CRC remainder to verify data integrity.

2.3.13.2 Sense Comparator Output and Test Register

The TVP3025 provides a $\overline{\text{SENSE}}$ output to support system diagnostics. $\overline{\text{SENSE}}$ can be used to determine the presence of the CRT monitor or verify that the RGB termination is correct. $\overline{\text{SENSE}}$ is a logic 0 if one or more of the DAC outputs exceeds the internal comparator voltage of 350 mV. The internal 350-mV reference has a tolerance of ±50 mV when using an external 1.235-V reference. If the internal voltage reference is used, the tolerance is higher.

The sense comparators are also integrated with the sense test register [index 3A (hex)] so that the comparison results for the red, green, and blue comparators can be read independently through the 8-bit microinterface. When the sense test register (STR) is read, the results are indicated in the bit positions as shown below.

STR BITS	D7	D6	D5	D4	D3	D2	D1	D0
Data	0	0	0	0	0	R	G	B

where: R = logic 1 if IOR > 350 mV
G = logic 1 if IOG > 350 mV
B = logic 1 if IOB > 350 mV
D6 – D3 are reserved
D7 is disable (logic 1) bit

NOTES: A. D7 can be set to a logic 1 to disable the sense comparison function. At reset, the sense comparison is enabled (D7 = logic 0). D6–D3 are reserved. If the sense test register is written to disable the sense comparator function, bits D6–D0 need to be set to a logic 0.

B. Both the $\overline{\text{SENSE}}$ output and the sense test register are latched by the falling edge of the internally sampled blank signal ($\overline{\text{SYSBL}}$ or $\overline{\text{VGABL}}$ depending on the mode). In order to have stable voltage inputs to the comparators, the frame-buffer inputs should be set such that data entering the DACs remains unchanged for a sufficient period of time prior to and after the blank-signal falling edge.

2.3.13.3 Identification Code

An ID register with a hardwired code is provided that can be used as a software verification for different versions of the system design. The ID code in the TVP3025 is static and may be read without consideration to the dot clock or video signals. The ID register is read through the indirect register map [see Table 2–3, index (3F hex)].

The value defined for the TVP3025 is 25 (hex).

2.3.14 General-Purpose I/O Registers and Terminals

The general-purpose (GP) I/O registers and output terminals provide a means of controlling external functions such as external phase-locked loops (PLLs) through the TVP3025 microinterface. The 8-bit general-purpose I/O data register [index 2B (hex)] has five of its bit locations (D0–D4) tied to external I/O terminals (I/O0–I/O4). The other three bits (D5–D7) can be used for general data storage and do not affect any other circuitry. The general-purpose I/O data register is controlled by the general-purpose I/O control register [index 2A (hex)]. GP I/O control register bits IOC0–IOC4 control whether the corresponding general-purpose I/O terminals are configured as inputs or outputs. The reset default condition is for GP I/O control register bits IOC0–IOC4 = logic 0, which configures terminals I/O0–I/O4 as inputs. If any of the GP I/O control register bits are set to a logic 1, the corresponding I/O terminals are configured as outputs.

The general-purpose I/O control register, data register, and terminal relationships are shown in the following table.

	DATA BIT							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
General-Purpose I/O Control Register	X	X	X	IOC4	IOC3	IOC2	IOC1	IOC0
General-Purpose I/O Data Register	X	X	X	D4	D3	D2	D1	D0
General-Purpose I/O Terminal				I/O4	I/O3	I/O2	I/O1	I/O0

NOTE: In BT485 mode, GP I/O4 and IOC4 are controlled through command register 4. See Section 2.4.15.5.

2.3.15 Reset

There are two ways to reset the TVP3025. The $\overline{\text{RESET}}$ input terminal can be used to perform a hardware reset. Alternatively, the device has an integrated software reset function. The hardware and software reset functions work with the MODE1 input terminal to reset the device to either the BT485 or TVP3025 default modes of operation. For TVP3025 operation, the MODE1 input terminal should be low when the reset occurs. For proper BT485 mode register translation after a reset, the microinterface should not be accessed for 30 μs.

A hardware reset is initiated by pulling the $\overline{\text{RESET}}$ input terminal low. When $\overline{\text{RESET}}$ is pulled low all TVP3025 registers go to default states. This reset is asynchronous, and any glitch on this terminal could change the intended register setup. The default state at reset is VGA mode, and all default register settings are given in Table 2–3. If a reset is desired at power up, an external resistor, capacitor, and diode network can be connected to the $\overline{\text{RESET}}$ terminal (see Figure A–1 for a typical circuit). If TTL logic is employed to provide the signal to the $\overline{\text{RESET}}$ terminal, a pull up resistor should be used to make sure that CMOS levels are achieved.

For a software reset, anytime the reset register (FF (hex) on the indirect register map) is written to, all registers are initialized to TVP3025 default settings. Any data can be written into the reset register to cause this reset to occur.

2.3.16 Analog Output Specifications

The DAC outputs are controlled by three current sources (only two for IOR and IOB) as shown in Figure 2–15. The default condition is to have 0 IRE difference between blank and black levels, which is shown in Figure 2–17. If a 7.5-IRE pedestal is desired, it can be selected by setting bit 4 of the general-control register. This video output is shown in Figure 2–16.

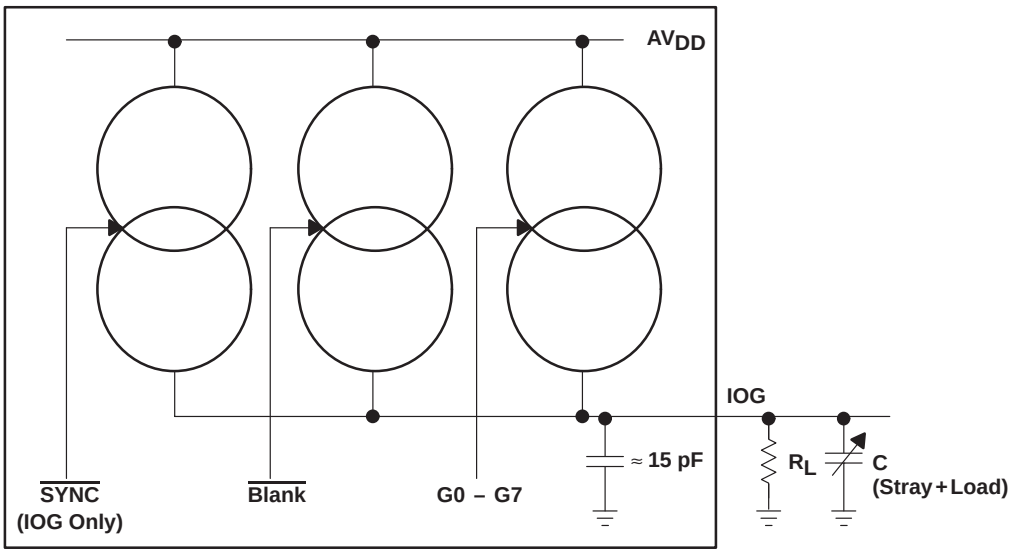


Figure 2–15. Equivalent Circuit of the Current Output (IOG)

A resistor (R_{SET}) is needed between the FS ADJUST terminal and GND to control the magnitude of the full-scale video signal. The IRE relationships in Figures 2–16 and 2–17 are maintained regardless of the full-scale output current.

The relationship between R_{SET} and the full scale output current IOG is:

$$R_{SET}\ (\Omega) = K1 \times V_{ref}\ (V) / IOG\ (mA)$$

The full-scale output current on IOR and IOB for a given R_{SET} is:

$$IOR, IOB\ (mA) = K2 \times V_{ref}\ (V) / R_{SET}\ (\Omega)$$

where K1 and K2 are defined as:

PEDESTAL	IOG		IOR, IOB	
	8-BIT OUTPUT	6-BIT OUTPUT	8-BIT OUTPUT	6-BIT OUTPUT
7.5 IRE	K1 = 11,294	K1 = 11,206	K2 = 8,067	K2 = 7,979
0 IRE	K1 = 10,684	K1 =10,600	K2 = 7,462	K2 = 7,374

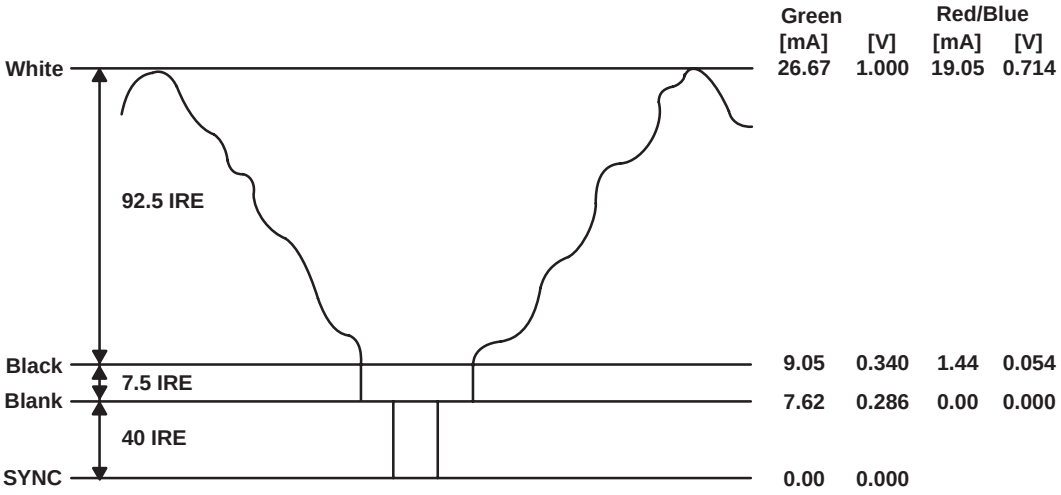


Figure 2–16. Composite Video Output (With 7.5 IRE, 8-Bit Output)

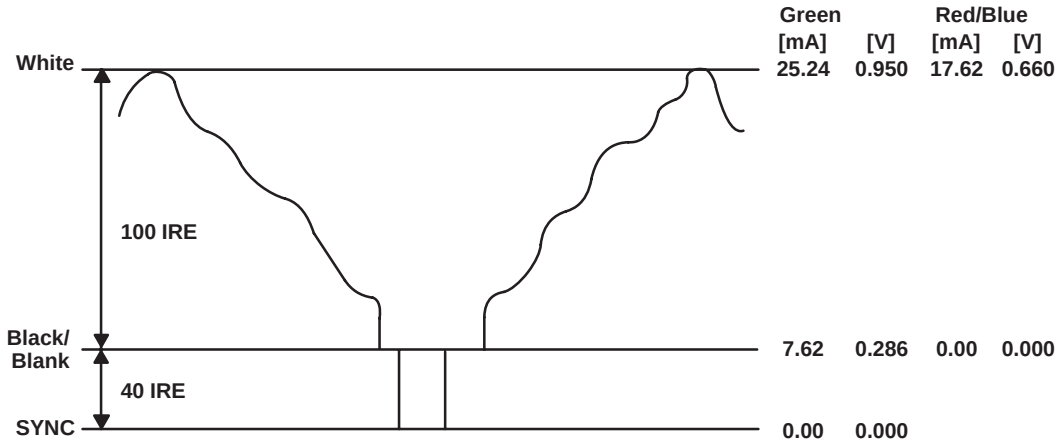


Figure 2–17. Composite Video Output (With 0 IRE, 8-Bit Output)

NOTE: 75-Ω doubly terminated load, V_{ref} = 1.235 V, R_{SET} = 523 Ω. RS343A-levels and tolerances are assumed on all levels.

2.3.17 TVP3025 New Features and Differences from the TVP3020

2.3.17.1 New Features

- PLL clock generators (pixel, memory, divided memory, and loop clock). See Section 2.3.4.
- Crystal oscillator inputs XTL1 and XTL2. See Sections 1.5 and 2.3.3.
- Output clock divider reset control and VGA pipeline adjust for VGA switching. See Section 2.3.10.1.
- Loop clock PLL for generating RCLK. See Section 2.3.7.4 and 2.3.4.
- DAC and dot clock power down modes. See Section 2.3.18.2.
- Video control signal ($\overline{\text{SYSBL}}$, $\overline{\text{SYSHS}}$, $\overline{\text{SYSVS}}$) latching on LCLK. See Section 2.3.7.1.
- Horizontal zooming improved. See Section 2.3.12.

2.3.17.2 Main Differences from the TVP3020

- Horizontal zooming implementation has been changed to a more efficient method. The zooming function must be programmed differently than on the TVP3020. See Section 2.3.12 for details.
- Multiplex-control register 1, bit 3 must now be set to logic 1 for proper true color and direct color operation when in the TVP3025 mode. See Table 2–8 for proper register settings.
- If the device is reset to the BT485 mode, to program the multiplexer for the TVP3020 true-color modes, true-color control register bit 2 must be set to a logic 0. This is automatically the case if the device is reset into the TVP3020 mode.
- Frame buffer interface timing modes are simplified. See Section 2.3.7.

2.3.18 Miscellaneous Control Register Bit Definitions

2.3.18.1 General-Control Register (Index 1D hex)

Table 2–12. General-Control Register

BIT NAME	VALUES	DESCRIPTION
GCR7	0: (default)	Overscan-control signal no longer used. It should be left as logic 0.
	1:	
GCR6	0: Disable (default)	Overscan enable. Specifies whether to enable the user-defined overscan screen borders.
	1: Enable	
GCR5	0: Disable	Sync enable. This bit specifies whether SYNC information is to be output onto IOG.
	1: Enable (default)	
GCR4	0: 0 IRE (default)	Pedestal control. This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs.
	1: 7.5 IRE	
GCR3	0: Little-endian (default)	Little-endian/big-endian select. Selects either little- or big-endian format for the pixel-bus interface.
	1: Big-endian	
GCR2	0: Disable (default)	Split shift-register-transfer enable. See Section 2.3.7.2.
	1: Enable	
GCR1	0: Active (low) (default)	VSYNCOUT output polarity.
	1: Active (high)	
GCR0	0: Disable (default)	HSYNCOUT output polarity.
	1: Enable (high)	

NOTE: BT485 command register bit CR03 is written to GCR5 and CR05 to GCR4 in the BT485 mode of operation.

2.3.18.2 Miscellaneous-Control Register (Index 1E hex)

Table 2–13. Miscellaneous-Control Register

BIT NAME	VALUES	DESCRIPTION
MISC07	0: Disable (default) 1: Enable	Enables loop clock PLL output on RCLK. See Section 2.3.7.4.
MISC06	0: VCLK (default) 1: LCLK	Video control signal latch control. Specifies whether SYSVS, SYSHS, and SYSBL are latched on VLCK or LCLK.
MISC05	0: In phase (default) 1: Opposite phase	VCLK polarity bit. Specifies whether VCLK will be in phase or 180 degrees out of phase with the RCLK signal.
MISC04	0: 0 Disable (default) 1: Enable	RCLK/VCLK divide by one enable . This bit is for BT485 mode only and should not be programmed.
MISC03	0: 6-bit (default) 1: 8-bit	8- or 6-bit operation bit. If bit 2 of this register is set to logic 1, then this bit determines 8- or 6-bit operation.
MISC02	0: Enable (default) 1: Disable	8/$\overline{6}$ terminal disable. If set to logic 1, the 8/$\overline{6}$ terminal is ignored and the 8/$\overline{6}$ function is controlled by bit 3 of this register.
MISC01	0: Enable (default) 1: Disable	Dot clock disable bit. If set to a logic 1, the dot clock is disabled from clocking the internal circuitry to conserve power.
MISC00	0: Disable (default) 1: Enable	DAC power down. If set to logic 1, the DACs power down.

NOTE: If BT485 command register 0 is written (or at reset in the BT485 mode) miscellaneous-control register bit 2 is set to logic 1.
If BT485 command register 4 is written to (or at reset in the BT485 mode) miscellaneous-control register bit 6 is set logic 1.
In the BT485 mode, the following BT485 command register bits are written into the following miscellaneous control register bits: CR00 into MISC00, CR01 into MISC03, CR06 into MISC01, $\overline{CR25}$ into MISC04.

2.3.18.3 Cursor-Control Register (Index 06 hex)

The cursor-control register is used to control various on-chip cursor functions of the palette. It can be accessed by the MPU at any time. Bit 7 of the cursor-control register corresponds to data bus bit 7.

Table 2–14. Cursor-Control Register

BIT NAME	VALUES	DESCRIPTION
CCR7	0: Nonplanar	Cursor format control. Default is nonplanar for TVP3025 mode operation. Planar mode is BT485 like operation.
	1: Planar	
CCR6	0: Disable (default)	Sprite-cursor enable. This bit enables (logic 1) or disables (logic 0) the 64 × 64 sprite cursor.
	1: Enable	
CCR5	0: (default)	Dual-cursor format. This bit specifies the intersection of the crosshair cursor and the 64 x 64 cursor. See Section 2.3.9.5.
	1:	
CCR4	0: XGA (default)	64 × 64 cursor-mode select. This bit specifies whether the XGA or X-windows format is used to interpret the data stored in the 64 × 64 cursor RAM. See Section 2.3.9.2.
	1: X-windows	
CCR3	0: Color 0 (default)	Crosshair color selection. This bit specifies whether the crosshair cursor is to be displayed in color 1 (logic 1) or color 0 (logic 0).
	1: Color 1	
CCR2	0: Disable (default)	Crosshair cursor enable. This bit specifies whether the crosshair cursor is to be displayed (logic 1) or not displayed (logic 0).
	1: Enable	
CCR1, CCR0	00: 1 pixel (default)	Crosshair thickness select. These bits specify the width in pixels of the horizontal and vertical crosshairs when the crosshair cursor is displayed. The segments are centered about the value in the cursor-position (x,y) registers.
	01: 2 pixels	
	10: 3 pixels	
	11: 4 pixels	

NOTE: If BT485 command register 2 is written to (or at reset in the BT485 mode), cursor-control register bits 2 and 5 are set to logic 0.
If BT485 command register 4 is written to (or at reset in the BT485 mode), cursor-control register bit 7 is set to logic 1.
In the BT485 mode, the following BT485 command register bits are written into the following cursor-control register bits: CR20 into CCR4, CR21 into CCR6.

2.3.18.4 Cursor-Position (x, y) Registers (Index 00 – 02 hex)

These registers are used to specify the (x,y) coordinate of the intersection of the crosshair cursor. They are also used in conjunction with the sprite-origin registers to specify the location of the 64 x 64 cursor area (see Section 2.3.9). The cursor position is not updated until the vertical retrace interval after cursor position Y MSB has been written to by the MPU. Bits D4 – D7 of the cursor-position X and Y MSB registers are always logic zero.

	CURSOR-POSITION X MSB								**CURSOR-POSITION X LSB**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Position	0	0	0	0	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	Index = 01 (hex)								Index = 00 (hex)							

	CURSOR-POSITION Y MSB								**CURSOR-POSITION Y LSB**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Position	0	0	0	0	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	Index = 03 (hex)								Index = 02 (hex)							

The cursor-position X and Y values to be written are calculated as follows:

Cx = desired display screen x position

Cy = desired display screen y position

Values from 0000 (hex) to 0fff (hex) can be written into the cursor-position X and Y registers. The values written into the cursor-position X and Y registers should be relative to the first displayed pixel on the screen, i.e., (0,0).

2.3.18.5 Sprite-Origin (x, y) Registers (Index 04 – 05 hex)

These registers are used to specify the (x,y) location of the 64 x 64 sprite with respect to the crosshair location (see Section 2.3.9.3). The sprite-origin X and Y registers can contain values from 0 to 63 decimal. Both registers are initialized to 1F (hex), 31 (decimal), which sets the center of the crosshair at the center of the 64 X 64 sprite. Both registers can be written to or read from by the MPU at any time. The sprite origin is not updated until the vertical retrace interval after sprite-origin X and Y registers have been written by the MPU.

	SPRITE-ORIGIN X							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
X Origin	0	0	X5	X4	X3	X2	X1	X0
	Index = 04 (hex)							

	SPRITE-ORIGIN Y							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Y Origin	0	0	Y5	Y4	Y3	Y2	Y1	Y0
	Index = 05 (hex)							

NOTE: When command register 4 is written in the BT485 mode or when the device is reset in the BT485 mode, 3F (hex) is written to the sprite-origin X and Y registers.

Values from 00 (hex) to 3F (hex) can be written into the sprite-origin X and Y registers. Bits D6 and D7 are always logic 0.

2.3.18.6 Window-Start (x, y) Registers (Index 10, 11, 14, 15 hex)

These registers are used to specify the (x,y) coordinate of the upper-left corner of the crosshair-cursor window or auxiliary window. The window start is not updated until the vertical retrace interval after the Y MSB register has been written to by the MPU. Bits D4–D7 of the window-start X and Y MSB registers are always logic zero.

	WINDOW-START X MSB								WINDOW-START X LSB							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Coordinate	0	0	0	0	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	Index = 11 (hex)								Index = 10 (hex)							

	WINDOW-START Y MSB								WINDOW-START Y LSB							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Coordinate	0	0	0	0	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	Index = 15 (hex)								Index = 14 (hex)							

The window-start X and Y values to be written are calculated as follows:

Wx = desired display screen x position

Wy = desired display screen y position

Values from 0000 (hex) to 0fff (hex) can be written into the window-start X and Y registers. The values written into the window-start X and Y registers should be relative to the first displayed pixel on the screen; i.e., (0,0). The window-start location specified is the first location inside the window. For the crosshair cursor or auxiliary window to be displayed, the window-start registers must specify a point on the active display.

2.3.18.7 Window-Stop (x, y) Registers (Index 12, 13, 16, 17 hex)

These registers are used to specify the (x,y) coordinate of the lower-right corner of the crosshair-cursor or auxiliary window. The window stop is not updated until the vertical retrace interval after the Y MSB register has been written to by the MPU. Bits D4–D7 of the window-stop X and Y registers are always logic zero.

	WINDOW-STOP X MSB								WINDOW-STOP X LSB							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Coordinate	0	0	0	0	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	Index = 13 (hex)								Index = 12 (hex)							

	WINDOW-STOP Y MSB								WINDOW-STOP Y LSB							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Coordinate	0	0	0	0	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	Index = 17 (hex)								Index = 16 (hex)							

The window-stop X and Y values to be written are calculated as follows:

Wx = desired display screen x position

Wy = desired display screen y position

Values from 0000 (hex) to 0fff (hex) can be written into the window-stop X and Y registers. The values written into the window-stop X and Y registers should be relative to the first displayed pixel on the screen; i.e., (0,0). The window-stop location specified is the last location inside the window. For the crosshair-cursor or auxiliary window to be displayed, the window-start registers must specify a point on the active display.

2.3.18.8 Cursor-Color 0, 1 RGB Registers (Index 23 – 28 hex)

These registers are used to specify the two colors for the hardware cursor (see Section 2.3.9). Note that there are six registers total, three for each color. The register formats for both the cursor-color 0 and cursor-color 1 registers are shown below.

	CURSOR-COLOR RED							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Red Value	R7	R6	R5	R4	R3	R2	R1	R0

Index = 23 and 26 (hex)

	CURSOR-COLOR GREEN							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Green Value	G7	G6	G5	G4	G3	G2	G1	G0

Index = 24 and 27 (hex)

	CURSOR-COLOR BLUE							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Blue Value	B7	B6	B5	B4	B3	B2	B1	B0

Index = 25 and 28 (hex)

Values 00 (hex) to FF (hex) can be written into the cursor-color registers at any time.

2.3.18.9 Cursor-RAM Address LSB and MSB Registers (Index 08 – 09 hex)

These registers are used to specify the address of where to write or read sprite cursor data. The nonplanar addressing scheme is depicted in Figure 2–10 of Section 2.3.9.1. The registers are not initialized and can be accessed by the MPU at any time. Bits D2–D7 are always a logic zero.

	CURSOR-RAM ADDRESS MSB								**CURSOR-RAM ADDRESS LSB**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Address	0	0	0	0	0	0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Index = 09 (hex) Index = 08 (hex)

Values from 0000 (hex) to 03FF (hex) can be written into the cursor-RAM address registers.

When the cursor-RAM address is to be written, both registers must be written with the cursor-RAM LSB address written first.

2.3.18.10 Cursor-RAM Data Register (Index 0A hex)

This register is used to read and write the contents of the sprite cursor locations whose address is specified in the cursor-RAM address LSB and MSB registers. The data read from or written to this register contain four pixels of information and two bit planes per cursor pixel (see Figure 2–10 and Section 2.3.9.1). The register is not initialized and can be written to or read from by the MPU at any time. The sprite-cursor data format is shown below.

	CURSOR-RAM DATA							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	$P1_3$	$P0_3$	$P1_2$	$P0_2$	$P1_1$	$P0_1$	$P1_0$	$P0_0$

Index = 0A (hex)

Values from 00 (hex) to FF (hex) can be written into the cursor-RAM data register.

2.3.18.11 Auxiliary Control Register (Index 29 hex)

Table 2–15. Auxiliary-Control Register

BIT NAME	VALUES	DESCRIPTION
ACR7	0: (default)	Horizontal zoom control. See Section 2.3.12.
	1:	
ACR6	0: (default)	Horizontal zoom control. See Section 2.3.12.
	1:	
ACR5	0: (default)	Horizontal zoom control. See Section 2.3.12.
	1:	
ACR4	Reserved	
ACR3	0: SCLK not used	SCLK select. This bit should be set according to whether SCLK is to be used for system timing. See Section 2.3.7.3.
	1: SCLK used (default)	
ACR2	0: PSEL disable (default)	Windowing-function select. This is a port-select enable. See equation in Section 2.3.10.2.
	1: PSEL enable	
ACR1	0: Window disable (default)	Windowing-function select. This is an auxiliary-window enable. See the equation in Section 2.3.10.2.
	1: Window enable	
ACR0	0: True function	Windowing-function select. This is a complementary function bit. See the equation in Section 2.3.10.2.
	1: Complementary (default)	

2.3.18.12 Color-Key Control Register (Index 38 hex)

Table 2–16. Color-Key Control Register

BIT NAME	VALUES	DESCRIPTION
CKC7	Reserved	
CKC6	Reserved	
CKC5	Reserved	
CKC4	0: True function 1: Complementary (default)	Color-key-function select. This is a complementary function bit. See the equation in Section 2.3.10.3.
CKC3	0: Disable compare (default) 1: Enable comparison	Blue-compare enable. This is used to enable or disable the direct-color blue field comparison. See the equation in Section 2.3.10.3.
CKC2	0: Disable compare (default) 1: Enable comparison	Green-compare enable. This is used to enable or disable the direct-color green field comparison. See the equation in Section 2.3.10.3.
CKC1	0: Disable compare (default) 1: Enable comparison	Red-compare enable. This is used to enable or disable the direct-color red field comparison. See the equation in Section 2.3.10.3.
CKC0	0: Disable compare (default) 1: Enable comparison	Overlay/VGA-compare enable. This is used to enable or disable the direct-color overlay/VGA field comparison. See the equation in Section 2.3.10.3.

2.3.18.13 Color-Key (Red, Green, Blue, Overlay/VGA) Low and High Registers (Index 30–37 hex)

These registers are used to specify the color comparison ranges for the four direct-color data fields when performing color-key switching. A low and a high register are provided for each of the four data fields to facilitate the range comparison. See Section 2.3.10 for more details on their usage. All four low registers are initialized with 01 (hex), while all four high registers are initialized with FF (hex). There are eight registers total, two for each color. The register formats for both low and high registers are shown below.

	COLOR-KEY LOW							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Low Value	L7	L6	L5	L4	L3	L2	L1	L0

Index = 30, 32, 34, and 36 (hex)

	COLOR-KEY HIGH							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
High Value	H7	H6	H5	H4	H3	H2	H1	H0

Index = 31, 33, 35, and 37 (hex)

Values 00 (hex) to FF (hex) can be written into the four color-key-low and four color-key-high registers.

2.3.18.14 Overscan Color RGB Registers (Index 20 – 22 hex)

These registers are used to specify the color for the overscan function. This function can be used to create custom screen borders (see Section 2.3.11). They are not initialized and can be written to or read from by the MPU at any time. The register formats for the overscan-color registers are shown below.

	OVERSCAN COLOR RED							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Red Value	R7	R6	R5	R4	R3	R2	R1	R0

Index = 20 (hex)

	OVERSCAN COLOR GREEN							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Green Value	G7	G6	G5	G4	G3	G2	G1	G0

Index = 21 (hex)

	OVERSCAN COLOR BLUE							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Blue Value	B7	B6	B5	B4	B3	B2	B1	B0

Index = 22 (hex)

Values 00 (hex) to FF (hex) can be written into the overscan color registers.

2.3.18.15 CRC LSB and MSB Registers (Index 3C – 3D hex)

These registers are used to read the result of the 16-bit CRC calculation (see Section 2.3.13). They are not initialized and can be read by the MPU at any time. Note, however, that they are only updated on the rising edge of the second horizontal sync during vertical retrace.

CRC LSB and CRC MSB are cascaded to form a 16-bit CRC calculation remainder.

	CRC MSB								**CRC LSB**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
CRC Remainder	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
	Index = 3D (hex)								Index = 3C (hex)							

2.3.18.16 CRC Control Register (Index 3E hex)

This write-only register is used to specify which of the 24 DAC data lines the 16-bit CRC should be calculated on (see Section 2.3.13). The register is not initialized and can be written to by the MPU at any time. The CRC control register format is shown below.

	CRC CONTROL							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Select Data	0	0	0	S4	S3	S2	S1	S0

Index = 3E (hex)

Values from 00 (decimal) to 23 (decimal) can be written into the CRC control register to select the appropriate data line.

2.3.18.17 True Color Control Register (Index 0E hex)

This register is provided to bridge between the BT485 and TVP3025 true color modes.

Table 2–17. True Color Control Register

BIT NAME	VALUES	DESCRIPTION
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	0: TVP3020 mode (default)	True color mode select. If this bit is set to logic 1, then BT485 type true color is assumed using the function specified in bits 1 and 0 of this register. This bit is the same as CR40 in the BT485 mode.
	1: BT485	
1	0:	This bit is identical to BT485 mode bit CR25 from command register 2. See the BT485 description in Section 2.4.
	1:	
0	0:	This bit is identical to BT485 mode bit CR16 from command register 1. See the BT485 description in Section 2.4.
	1:	

2.4 Circuit Description Using BT485 Register Emulation

As discussed in Sections 2.1.1 and 2.1.2, the TVP3025 can be reset and initialized to a BT485 mode of emulation. Table 2–2 lists the BT485 emulation register map. In general, register translations are transparent to the user. An additional command register four is added to provide access to the enhanced features that the TVP3025 provides beyond the BT485. Because of the use of register emulation, operation of the device appears essentially identical to the BT485.

The MPU interface and reading/writing of the color palette operations are covered in Section 2.2, since operation is the same as in the TVP3020 mode.

2.4.1 Writing Cursor and Overscan Color Data

To write cursor color data, the MPU writes the address register (cursor color write mode) with the address of the cursor color location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0 – RS4 to select the cursor color registers. After the blue write cycle, the 3 bytes of red, green, and blue color information are concatenated into a 24-bit word and written to the cursor color location specified by the address register. The address register then increments to the next location, which the MPU can modify by writing another sequence of red, geen, and blue data. A block of color values in consecutive locations can be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written. The address register (write mode) should be written with xx00 for overscan, xx01 for cursor color 0, and xx10 for cursor color 1.

2.4.2 Reading Cursor Color Data

To read cursor color data, the MPU loads the address register (cursor color read mode) with the address of the cursor color location to be read. The contents of the cursor color register at the specified address are copied into the RGB registers, and the address register is incremented to the next cursor color location. The MPU performs three successive read cycles (8 bits for each color) using RS0 – RS4 to select the cursor color registers. Following the blue read cycle, the contents of the cursor color location at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations can be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

2.4.3 Accessing the Cursor RAM

The 64 x 64 x 2 cursor RAM is accessed in a planar format. The TVP3025 does not support a 32 x 32 cursor. Therefore, bit CR32 in command register 3 is nonfunctional and reading/writing to this bit performs no operation. Bits CR30 and CR31 in command register 3 become the load inputs to the 2 MSBs of a 10-bit address counter, therefore, these bits must be written in command register 3 before the lower 8 bits are written to the address counter through the MPU port. In the planar format, only 9 address bits are used. The tenth bit is to determine which plane (0 or 1) data of the cursor RAM array is accessed. A single address presented to the cursor RAM accesses eight bit locations in plane 0 or 1, depending on the state of address bit 9.

After each access in the planar format, the address increments. The MPU uses a 10-bit address counter to access the cursor array RAM array. Any write to the address counter after cursor auto-incrementing has been initiated resets the cursor auto-incrementing logic until the cursor RAM array has again been accessed. Cursor auto-incrementing will then begin from the address written. A read from the address counter does not reset the cursor auto-incrementing logic. The color palette RAM and cursor RAM share the same external address register, and MPU addressing for this and all other registers is determined by the external RS0–RS4 select terminals (see Table 2–2).

2.4.4 6-Bit/8-Bit Operation

The command bit CR01 is used to specify whether the MPU is reading and writing 8- or 6-bits of color information each cycle. For 8-bit operation, D0 is the LSB and D7 is the MSB of color data. For 6-bit operation, color data is contained on the lower 6 bits of the data bus, with D0 the LSB and D5 the MSB of

color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 are logical zeros. In the 6-bit mode, the TVP3025 full scale output current is about 1.5 percent lower than when in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are logical zeros in the 6-bit mode. Accessing the cursor RAM array does not depend on the resolution of the DACs.

2.4.5 Power Down Mode

The TVP3025 incorporates a power down capability, controlled by command bit CR00. While this command bit is logic 0, the device functions normally. When this command bit is set to logic 1, the DACs are powered down such that they output no current. If CR06 is taken to a logic 1 while CR00 is a logic 1, the internal dot clock is halted. While in this sleep mode, the RAM and all registers still retain their data. Also, the MPU may read or write to the RAM while the dot clock is running. The three command registers can still be written to or read from by the MPU. The DACs require about 1 second to turn off or turn on, depending on the compensation capacitor used.

2.4.6 Frame Buffer Clocking

The video RAM shift clock reference signal (RCLK) is generated by the TVP3025. RCLK is one sixteenth, one eighth, one fourth, or one half the pixel clock rate, depending on whether multiplexing is 16:1, 8:1, 4:1, or 2:1, respectively.

P0 – P63 are the pixel data inputs. They support different bits per pixel and multiplexing ratios as discussed in Section 2.4.10. These pixel inputs are always latched on the rising edge of LCLK. The pixel clock is specified to be either CLK0 or CLK1 by command bit CR24.

2.4.7 Onboard 2x TTL Clock Doubler

The TVP3025 provides an onboard clock doubler for high-speed, low cost operation. The clock doubler can be enabled or disabled by programming bit CR33 in command register 3. At reset, the clock doubler is disabled, but can be subsequently be enbled by programming CR33. Either CLK0 or CLK1 can be doubled internally.

2.4.8 Pixel Read-Mask Register

Pixel data is bit-wise logically ANDed with the contents of the pixel read-mask register during each pixel clock cycle. The result is used to address the color palette RAM. In this way, bits can be enabled and disabled from addressing the palette RAM. Pixel masking is enabled for all modes of operation, except where the true color bypass is selected. The pixel read-mask register is not initialized and should be set to logic 1s for proper operation.

2.4.9 Frame Buffer Pixel Port Interface

The 64-bit pixel port interface allows many operational display modes. For those multiplexed modes in which multiple pixels are latched on one LCLK rising edge, the pixel clock shifts the pixels out starting with the pixels that reside on the low numbered pixel port terminals. For example, in an 8-bit per pixel pseudo-color mode with an 8:1 multiplex ratio, the pixel display sequence would be P(0–7), P(8–15), P(16–23), P(24–31), P(32–39), P(40–47), P(48–55), and P(56–63).

2.4.10 Modes of Operation

In addition to the standard modes provided by the 32-bit pixel port on the BT485, the TVP3025 has an additional command register 4 to give access to its enhanced 64-bit pixel port. In general, for all of the operating modes described in the following sections, if CR40 in command register 4 is set to a logic 1, 64-bit pixel bus operation is assumed and all multiplex ratios are doubled.

2.4.10.1 4-Bits/Pixel Operation (8:1 or 16:1 Mux)

If the pixel port interface is operated as a 32-bit bus, it is multiplexed 8:1 and configured for 4 bits per pixel. Alternatively, if CR40 is set to logic 1, then a 64-bit bus is assumed with multiplexing of 16:1 for 4 bits per pixel. As a result, 8 or 16 independent 4-bit pixels are input to the device and latched on the rising edge of

LCLK. One rising edge of LCLK should occur every eight dot clock cycles for a 32-bit bus (every 16 dot clock cycles for a 64-bit bus). RCLK is automatically set when the multiplex mode is chosen such that its frequency equals the selected dot clock frequency divided by the multiplex ratio (i.e., dot clock/8 or dot clock/16 depending on CR40). The 4 bits from each pixel selects 1 of 16 locations (RAM address 0 – 15) in the palette in the order presented in Table 2–18.

2.4.10.2 8-Bits/Pixel Operation (4:1 or 8:1 Mux)

If a 32-bit wide pixel input port is selected, then the bits are multiplexed 4:1 and are configured for 8 bits per pixel. If 64-bit wide operation is chosen, then the port is multiplexed 8:1 with 8 bits per pixel. One rising edge of LCLK should occur every four dot clocks cycles for 32-bit port selection or every eight dot clocks cycles for 64-bit port selection. RCLK automatically equals the dot clock divided by four or eight when the multiplexing mode is selected. The 8 bits from each pixel selects 1 of 256 locations in the palette as shown in Table 2–18.

2.4.10.3 16-Bits/Pixel Operation (2:1 or 4:1 Mux)

If a 32-bit bus is selected, the pixel inputs are multiplexed 2:1 and configured for 16 bits per pixel. If a 64-bit bus is selected, the pixel inputs are multiplexed 4:1 and configured for 16 bits per pixel. One rising edge of LCLK should occur every two or four dot clock cycles depending on pixel bus width. RCLK automatically equals the dot clock divided by 2 or 4 depending on pixel bus width. Both 5:5:5 and 5:6:5 RGB color formats are supported as shown in Table 2–18. With these modes, the display can contain 32 K or 64 K simultaneous colors. The DACs can be configured for 6 or 8 bits of resolution in this mode.

Bit CR14 is used to enable or disable true color palette bypass. This bit should always be programmed to a logic 1, since the TVP3025 only supports direct color (palette bypass) while in the BT485 mode. If true color (gamma corrected) is desired, then it can be programmed through the TVP3025 indirect register mode. Bit CR22 is used in the BT485 to program sparse or contiguous addressing. The TVP3025 only supports sparse addressing, so this bit is nonfunctional, but can be written to or read from with no effect on circuit operation.

2.4.10.4 24-Bit/Pixel Operation (1:1 or 2:1 Mux)

If 32-bit pixel bus width is chosen, then 24 bits per pixel are latched 1:1 with no multiplexing. If a 64-bit bus is chosen, then the 24 bits per pixel are multiplexed 2:1. One rising edge of LCLK should occur every dot clock cycle for 1:1 multiplexing and every two dot clock cycles for 2:1 multiplexing. The RGB color format in this mode is 8:8:8. Again CR14 needs to be set to a logic 1, since only direct color is supported by the TVP3025 in the BT485 mode. With 24-bit true color, 16.8 million simultaneous colors are possible. The DACs should be configured for 8-bit operation in this mode (CR01 = logic 1).

Table 2–18. Modes of Operation (Pixel Port Configuration)

MODE	CR25	CR40	CR13	CR16	CR15	BITS MUXED	MUX RATE	OPERATING MODE
A	0	x	x	x		VGA (7:0)	1:1	VGA
B	1	0	x	1	1	P[3:0] P[7:4] P[11:8] P[15:12] P[19:16] P[23:20] P[27:24] P[31:28]	8:1	4 Bits/pixel
C	1	1	x	1	1	Mode B+ P[35:32] P[39:36] P[43:40] P[47:44] P[51:48] P[55:52] P[59:56] P[63:60]	16:1	4 Bits/pixel
D	1	0	x	1	0	P[7:0] P[15:8] P[23:16] P[31:24]	4:1	8 Bits/pixel
E	1	1	x	1	0	Mode D+ P[39:32} P[47:40] P[55:48] P[63:56]	8:1	8 Bits/pixel
F	1	0	0	0	1	P[15:0] P[31:16]	2:1	16 Bits/pixel (5:5:5) (see Table 2–19)
G	1	1	0	0	1	P[15:0] P[31:16] P[47:32] P[63:48]	4:1	16 Bits/pixel (5:5:5) (see Table 2–19)
H	1	0	1	0	1	P[15:0] P[31:16]	2:1	16 Bits/pixel (5:6:5) (see Table 2–20)
I	1	1	1	0	1	P[15:0] P[31:16] P[47:32] P[63:48]	4:1	16 Bits/pixel (5:6:5) (see Table 2–20)
J	1	0	x	0	0	P[23:0]	1:1	24 Bits/pixel (see Table 2–21)
K	1	1	x	0	0	P[23:0] P[55:32]	2:1	24 Bits/pixel (see Table 2–21)

Table 2–19. 5:5:5 RGB Color Format for 2:1 and 4:1 Multiplex Modes

PIXEL FORM	MSB															LSB
	X	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
PORT BITS	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
	P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
	P47	P46	P45	P44	P43	P42	P41	P40	P39	P38	P37	P36	P35	P34	P33	P32
	P63	P62	P61	P60	P59	P58	P57	P56	P55	P54	P53	P52	P51	P50	P49	P48

Table 2–20. 5:6:5 RGB Color Format for 2:1 and 4:1 Multiplex Modes

PIXEL FORM	MSB															LSB
	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
PORT BITS	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
	P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
	P47	P46	P45	P44	P43	P42	P41	P40	P39	P38	P37	P36	P35	P34	P33	P32
	P63	P62	P61	P60	P59	P58	P57	P56	P55	P54	P53	P52	P51	P50	P49	P48

Table 2–21. 8:8:8 RGB Color Format for 1:1 and 2:1 Multiplex Modes

PIXEL FORM	MSB																							LSB
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
PORT BITS	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
	P55	P54	P53	P52	P51	P50	P49	P48	P47	P46	P45	P44	P43	P42	P41	P40	P39	P38	P37	P36	P35	P34	P33	P32

2.4.11 VGA Mode and Port

An 8-bit VGA pixel port is provided to support basic VGA modes. It is latched on the rising edge of CLK0. In this mode RCLK equals the dot clock. It is assumed that, in most BT485 designs, the PSEL input is tied high and software is used to switch modes. Therefore, the PSEL input performs no function in the BT485 mode of the TVP3025 and the VGA mode is enabled by setting CR25 in command register 2 to logic 0. For modes other than VGA, CR25 needs to be set to a logic 1.

2.4.12 Cursor Operation

The TVP3025 supports an on chip $64 \times 64 \times 2$ user definable cursor. The TVP3025 does not support the 32×32 cursor mode or cursor color 3. The pattern for the cursor is provided by the cursor RAM, which can be accessed by the MPU at any time. The cursor is positioned through the cursor-position (x, y) registers (see Figure 2–18). Writing (0, 0) to the cursor-position registers places the cursor off the screen. Writing (1, 1) to the cursor-position registers places the lower right pixel of the cursor array on the upper left corner of the screen. Only one cursor pattern per frame is displayed at the location specified, regardless of the number of updates to (x, y). The vertical or horizontal location of the cursor is not affected during any frame display. There are no restrictions on updating (x, y) other than both the cursor-position registers must

be written when the cursor location is updated. Internal x- and y-position registers are loaded after the upper byte of y has been written to ensure one cursor pattern per frame at the correct location. The cursor pattern is displayed at the last cursor location written.

Cursor positioning is relative to blank (either $\overline{\text{VGABL}}$ or $\overline{\text{SYSBL}}$ depending on whether the device is in VGA mode). The cursor position is not dependent on OVS (see Figure 2–18). The reference point of the cursor (row 0, column 0) is in the lower right corner. The cursor x position is relative to the first rising edge of LCLK when $\overline{\text{SYSBL}}$ is sampled high in the nonVGA modes. In the VGA modes, the cursor position x is relative to the first rising edge of CLK0 when $\overline{\text{VGABL}}$ is sampled high. The y position is similarly relative, but only after the vertical blanking interval has been determined. The vertical blanking interval is determined by more than one horizontal sync pulse during blank. When in multiplexed modes other than 1:1, the cursor timing is based on the dot clock and LCLK. Note that the BT485 $\overline{\text{CBLANK}}$ and CDE signals are the same as the TVP3025 OVS and $\overline{\text{SYSBL}}$ input signals, respectively. Interlaced cursor operation is not supported by the TVP3025.

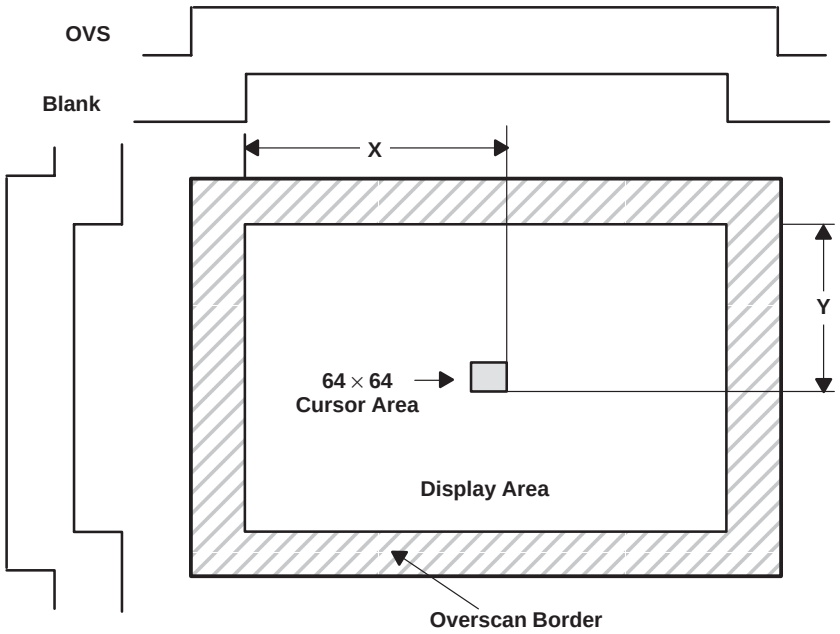


Figure 2–18. Cursor Positioning

The cursor supports two modes of operation as detailed in Table 2-22. Command register bits CR20 and CR21 determine which mode the cursor is supporting. See Section 2.4.15 for command register bit definitions.

Table 2–22. Cursor Color Modes

PLANE 1	PLANE 2	XGA MODE	X-WINDOW MODE
0	0	Cursor color 0	Transparent
0	1	Cursor color 1	Transparent
1	0	Transparent	Cursor color 0
1	1	Complement	Cursor color 1

2.4.13 Video Generation

The video control signals $\overline{\text{SYSBL}}$, $\overline{\text{SYSVS}}$, and $\overline{\text{SYSHS}}$ are latched on the rising edge of LCLK to maintain synchronization with the color data. In the VGA modes, VGAHS, VGAVS, and $\overline{\text{VGABL}}$ are latched on the rising edge of CLK0. These signals add appropriate weighted current sources to the IOG analog output as shown in Figures 2–15, 2–16, 2–17, producing the specific output levels required for video applications. The CR05 command bit is used to specify whether a 0 or 7.5 IRE blanking pedestal is to be used. Command register bit CR03 specifies whether the IOG (green) output channel contains sync information.

2.4.14 $\overline{\text{SENSE}}$ Output

$\overline{\text{SENSE}}$ is a logic 0 if one or more of the IOR, IOG, IOB outputs have exceeded the internal voltage reference level of the $\overline{\text{SENSE}}$ comparator circuit. This output is used to determine the presence of the CRT monitor, and the diagnostic code, the difference between a loaded or an unloaded RGB line can be discerned. The $\overline{\text{SENSE}}$ voltage reference is specified in Section 3.4 under operating characteristics. It is derived from a 1.235-V reference on the REF terminal. If the internal voltage reference is used, then slightly higher tolerances can be assumed. In general, the DAC low voltage should be set to less than 260 mV, and the DAC high voltage to greater than 410 mV.

2.4.15 Control Register Bit Definitions

2.4.15.1 Command Register 0 (RS value = 10110)

Table 2–23. Command Register 0 (RS value = 10110)

BIT NAME	VALUES	DESCRIPTION
CR07	0: Disable (default)	Command register 3 and 4 enable. If this bit is set to logic 1, then command registers 3 and 4 can be accessed indirectly.
	1: Enable	
CR06	0: Normal operation (default)	Clock disable ANDed with CR00. If this bit is set to a logic 1 while CR00 is a logic 1, then the internal dot clock is disabled to conserve system power.
	1: Disable internal dot clock	
CR05	0: 0 IRE (default)	Pedestal control. This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs.
	1: 7.5 IRE	
CR04	0: Disable (default)	Sync on blue – not supported on TVP3025
	1: Enable	
CR03	0: Disable (default)	Sync enable. This bit specifies whether sync information is to be output onto IOG.
	1: Enable	
CR02	0: Disable (default)	Sync on red – not supported on TVP3025
	1: Enable	
CR01	0: 6-bit operation (default)	This bit specifies if the MPU is reading and writing 8 bits (logical 1) or 6 bits (logical 0) of color information
	1: 8-bit operation (high)	
CR00	0: Normal operation (default)	DAC power down bit. If this bit is a logic 1, the DACs are internally powered down for sleep mode operation.
	1: Power down enable	

NOTE: At device reset into BT485 mode or when this register is written in BT485 mode, TVP3025 miscellaneous-control register bit 2 is set to logic 1.
The following command register 0 bits are written into the following TVP3025 indirect register bits: CR00 into miscellaneous-control register bit 0, CR01 into miscellaneous-control register bit 3, CR03 into general-control register bit 5, CR05 into general-control register bit 4, and CR06 into miscellaneous-control register bit 1.
This register is not initialized at power up. All command registers are set to logic 0 when a low signal is asserted at the $\overline{\text{RESET}}$ terminal.

2.4.15.2 Command Register 1 (RS value = 11000)

Writing to command register 1 (or at device reset) sets output-clock-selection register bits 2, 5, and 6 to logic 0.

Table 2–24. Command Register 1 (RS value = 11000)

BIT NAME	VALUES	DESCRIPTION
CR17	Reserved	
CR16, 15	00: 24 bits/pixel	Operation mode selection. See Section 2.4.10 and Tables 2–18 through 2–21.
	01: 16 bits/pixel	
	10: 8 bits/pixel	
	11: 4 bits/pixel	
CR14	0: Nonbypass (default)	This bit must be set to logic 1 for BT485 mode true color operation using the TVP3025.
	1: Palette bypass	
CR13	0: 5:5:5 RGB format (default)	16 bit/pixel data format select. See Section 2.4.10.3 and Tables 2–18 through 2–20.
	1: 5:6:5 RGB format	
CR12	0:	16 bit/pixel multiplex mode select. Not supported on the TVP3025. The default is 2:1, but 4:1 can be selected with CR40.
	1:	
CR11	0:	16 bit real time switch. Not supported on the TVP3025.
	1:	
CR10	0:	16 bit/pixel port switch control. Not supported on the TVP3025.
	1:	

NOTE: The following command register 1 bits are written into the following TVP3025 indirect register bits: CR13 into multiplexer-control register 1 bit 0, $\overline{\text{CR14}}$ into multiplexer-control register 1 bit 6, $\overline{\text{CR15}}$ into multiplexer-control register 2 bit 3, CR15 into output-clock-selection register bits 0 and 3, $\overline{\text{CR15}}$ into multiplexer-control register 1 bit 1, CR15 into multiplexer-control register 1 bit 3, CR16 into multiplexer-control register 1 bit 7, and CR16 into output-clock-selection register bits 1 and 4.
These registers are not initialized at power up. All command registers are set to a logic 0 when a low signal is asserted at the $\overline{\text{RESET}}$ terminal.

2.4.15.3 Command Register 2 (RS value = 11001)

Writing to command register 2 sets input-clock-selection register (see Table 2–5) bits 1 and 2 to logic 0. Also, cursor-control register (see Section 2.3.18.3) bits 2 and 5 are set to logic 0.

Table 2–25. Command Register 2 (RS value = 11001)

BIT NAME	VALUES	DESCRIPTION
CR27	0:	SCLK disable. Not supported in the BT485 mode of the TVP3025.
	1:	
CR26	Reserved (logic 0)	
CR25	0: VGA mode (default)	VGA mode select. Unlike the BT485, this bit solely controls the switching between modes. PSEL is disregarded.
	1: NonVGA mode	
CR24	0: CLK0 selected (default)	Pixel clock input select
	1: CLK1 selected	
CR23	0:	Noninterlaced/interlaced display selection. Interlaced mode is not supported on the TVP3025. This bit is don't care.
	1:	
CR22	0:	Sparse and contiguous indexing select for 16 bpp mode. Not supported on the TVP3025. This bit is don't care.
	1:	
CR21	0: Cursor disable (default)	64 x 64 x 2 cursor enable. A three color cursor is not supported on the TVP3025.
	1: Cursor enable (high)	
CR20	0: XGA cursor (default)	Cursor mode select.
	1: X-windows cursor (high)	

NOTE: The following command register 2 bits are written into the following TVP3025 indirect register bits: CR20 into cursor-control register bit 4, CR21 into cursor-control register bit 6, CR24 into input-clock-selection register bit 0, $\overline{\text{CR25}}$ into multiplexer-control register 2 bit 7, $\overline{\text{CR25}}$ into miscellaneous-control register bit 4, and CR26 into input-clock-selection register bit 3.

2.4.15.4 Command Register 3 (RS value = 11010, when CR07 = logic 1)

Table 2–26. Command Register 3 (RS value = 11010)

BIT NAME	VALUES	DESCRIPTION
CR37	Reserved (logic 0)	
CR36	Reserved (logic 0)	
CR35	Reserved (logic 0)	
CR34	Reserved (logic 0)	
CR33	0: Clock doubler disable (default)	This bit enables or disables the internal 2x clock doubler circuit.
	1: Clock doubler enable	
CR32	0:	Cursor select. Not supported by the TVP3025, since only 64 x 64 cursor is allowed.
	1:	
CR31, 30	CR31 = A9	MSBs for 10-bit address counter for cursor RAM addressing. See Section 2.4.3.
	CR30 = A8	

NOTE: CR33 is written into input-clock-selection register bit 4 in the BT485 mode of operation.
These registers are not initialized at power up. All command registers are set to a logic 0 when a low signal is asserted at the $\overline{\text{RESET}}$ terminal.

2.4.15.5 Command Register 4 (RS value = 11010, when CR07 = logic 1)

Table 2–27. Command Register 4 (RS value = 11010)

BIT NAME	VALUES	DESCRIPTION
CR47	Reserved (logic 0)	
CR46	Reserved (logic 0)	
CR45	Reserved (logic 0)	
CR44	Reserved (logic 0)	
CR43	0: GP I/O4 disabled (default)	This bit enables or disables general-purpose I/O bit GP I/O4 for output. When it is disabled, the terminal is tri-state like the other GP I/O terminals. This can possibly be used to drive RS4 input.
	1: GP I/O4 enabled for output	
CR42	0: GP I/O4 = logic 0 (default)	GP I/O4 input value. When CR43 is set to a logic 1, GP I/O4 is enabled as an output. The logic signal provided by this bit is output on GP I/04.
	1: GP I/O4 = logic 1	
CR41	Reserved (logic 0)	
CR40	0: 32-bit pixel bus	Pixel bus width select. This bit sets the pixel bus width to either 32 bits or 64 bits. See Table 2–18 and Section 2.4.10.
	1: 64-bit pixel bus	

NOTE: The following command register 4 bits are written into the following TVP3025 indirect register bits: CR40 into multiplexer-control register 2 bits $\overline{0}$, $\overline{1}$, and 2; CR40 into output-clock-selection register bit 7, CR40 into true color control register bit 2, CR40 into auxiliary control register bit 3, CR42 into general-purpose I/O data register bit 4, CR43 into general-purpose I/O control register bit 4.
These registers are not initialized at power up. All command registers are set to a logic 0 when a low signal is asserted at the $\overline{\text{RESET}}$ terminal.

When command register 4 is written, 003F (hex) is loaded into the TVP3020 sprite-origin x and y registers (index 04 and 05 hex) and the cursor addressing is set to planar format (cursor-control register bit 7 = logic 1) to provide cursor positioning similar to the BT485. If these indexed registers are subsequently overwritten in the TVP3020 mode and then the device is operated in the BT485 mode, they must be reset to proper BT485 values. This can be accomplished by writing to those registers in the TVP3020 mode, performing a BT485 register initialization by resetting the device with the MODE1 terminal high or by writing to command register 4.

When command register 4 is written, miscellaneous-control register bit 6 is set to logic 1 to enable $\overline{\text{SYSBL}}$, $\overline{\text{SYSHS}}$, and $\overline{\text{SYSVS}}$ latching on LCLK. This also occurs when the device is reset with MODE1 terminal high.

Command register 4 bit CR40 sets the output-clock-selection register bit 7 to logic 1, which further divides the RCLK by 2 because of the higher multiplexing rate used in the 64-bit modes. See Table 2–7 notes.

2.4.16 Internal Registers

2.4.16.1 Pixel Read-Mask Register (RS value =10010)

The 8-bit pixel read-mask register can be written to or read by the MPU at any time and is not initialized at power up. The contents of this register are bit-wise ANDed with the pixel data prior to addressing the color palette RAM. The pixel read-mask register is initialized to logic ones using the $\overline{\text{RESET}}$ terminal.

2.4.16.2 Status Register (RS value = 11010)

The 8-bit status register monitors certain device states and identifies devices. It can be read by the MPU at any time; MPU write cycles are ignored. This register is not reset during power up or at reset.

Table 2–28. Status Register (RS value = 11010)

BIT NAME	VALUES	DESCRIPTION
SR07	Reserved (logic 0)	
SR06	0: Idle	BT485 register translation state machine indicator. If this bit is a logic 1, then the TVP3020 index registers should not be accessed.
	1: Busy	
SR05, SR04	Revision bit values	These two bits are for revision numbers. Initially they contain zeros.
SR03	SENSE bit	SENSE bit. If it is a logic 0, one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference. See Section 2.4.14.
SR02	0: Write cycle	Read/write cycle status. This bit provides read/write status when the register select bits 0, 3, 4, or 7 (hex) have been written.
	1: Read cycle	
SR01, SR00	00: Red color component	These bits reflect the color component address of the next read/write cycle when the palette, cursor color, or overscan registers are accessed.
	01: Green color component	
	10: Blue color component	

2.4.16.3 Accessing Command Registers 3 and 4

A fourth and fifth command register, command register 3 and command register 4 are added to address the extended functions of the TVP3025 and remain backward compatible with the BT485. Since there are only 4 register select lines defined on the BT485 (all 16 combinations are used), command register 3 and command register 4 must be accessed indirectly. Command registers 3 and 4 are accessed with the following sequence of operations:

1. Set RS3 – RS0 to 0110, command register 0.
2. Write a logic 1 to CR07.
3. Set RS3 – RS0 to 0000, address register.
4. Write address register to 0000 0001 (command register 3) or 0000 0010 (command register 4).
5. Set RS3 – RS0 to 1010.
6. Read or write command register 3 or 4.

With this indirect addressing, the status register can be accessed by writing 0000 0000 to the address register, as in step 4 above.

To address the 64 × 64 cursor RAM, CR31 and CR30 must be written to provide the 2 MSBs for the 10-bit address counter. Therefore, to set the counter to access a particular location in the RAM array, these 2 bits must be written to command register 3 before the lower 8 bits are written to the address counter through the MPU port. As the 10-bit address counter auto-increments, the new value of this counter can be read back through CR31 and CR30. The contents of this register are reset with the assertion of the external $\overline{\text{RESET}}$ terminal. See Section 2.4.15.5 and the notes in that section.

2.4.16.4 Cursor-Position (x,y) Registers

These registers are used to specify the (x,y) coordinates of the 64 × 64 × 2 hardware cursor. The cursor registers contain low and high value registers. The last value written by the MPU to these registers is the value returned on a read. These registers can be read/written by the MPU at any time. Bits D4 – D7 of both high registers are ignored.

	CURSOR-POSITION X HIGH								CURSOR-POSITION X LOW							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Position	0	0	0	0	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	RS value = 11101								RS value = 11100							

	CURSOR-POSITION Y HIGH								CURSOR-POSITION Y LOW							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Position	0	0	0	0	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	RS value = 11110								RS value = 11110							

The cursor-position X and Y values to be written are calculated as follows:

X = desired display screen x position + 64 (or 0040 hex)

Y = desired display screen y position + 64 (or 0040 hex)

The x and y reference point (x = 0, y = 0) is the upper left corner of the screen. Values from 0 (0000 hex) to 4095 (0fff hex) can be written into the X and Y registers. If X = 0, the cursor is off the screen. If Y = 0, the cursor is entirely off the screen. See cursor operation in Section 2.4.12.

2.4.17 BT485 Features Not Supported and Differences

- Cursor color 3. See Section 2.4.12
- Interleaved cursor mode
- 32 x 32 cursor
- Cursor highlight logic
- Sync on all three channels red, green, blue. The TVP3025 supports sync on green only.
- Real time switching of 16-bit per pixel data using pixel bit P7D.
- Contiguous addressing for 16-bit pixel data.
- 16-bit per pixel operation with 1:1 multiplexing. Only multiplexing modes of 2:1 or 4:1 are supported for 16-bit per pixel operation.
- Tri-state SCLK
- Test functions
- Port select mask. CR25 is used to switch between VGA and non-VGA.
- Four bit per pixel sequencing is made consistent, i.e., always the low numbered nibble is displayed first.
- Power down mode circuitry slightly different than the BT485.
- Overscan must be enabled in the TVP3025 indirect register general-control register bit 6.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 7 V
Input voltage range, V_I . . . . . −0.5 V to V_{DD} + 0.5 V
Analog output short-circuit duration to any power supply or common . . . . . unlimited
Operating free-air temperature, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Junction temperature . . . . . 175°C
Case temperature for 10 seconds: PCE package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltages, AV_{DD}, DV_{DD}	4.75	5	5.25	V
Reference voltage, V_{ref}	1.15	1.235	1.26	V
High-level input voltage, V_{IH}	2.4		V_{DD}+0.5	V
Low-level input voltage, V_{IL}			0.8	V
Output load resistance, R_L		37.5		Ω
FS ADJUST resistor, R_{SET}		523		Ω
Operating free-air temperature, T_A	0		70	°C

3.3 Electrical Characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = –800 µA	2.4			V
V_{OL}	Low-level output voltage	D<0:7>, I/O 0–4, VCLK, RCLK, SENSE, PCLKOUT, MCLK, DCLK	I_{OL} = 3.2 mA			0.4	V
		HSYNCOUT, VSYNCOUT	I_{OL} = 15 mA			0.4	
		SCLK	I_{OL} = 18 mA			0.4	
I_{IH}	High-level input current	TTL inputs	V_I = 2.4 V			1	µA
		ECL inputs	V_I = 4 V			1	
I_{IL}	Low-level input current	TTL inputs	V_I = 0.8 V			–1	µA
		ECL inputs	V_I = 0.4 V			–1	
I_{DD}	Supply current, pseudo-color mode (see Note 2)	TVP3025-135	V_{DD} = 5		470	550	mA
		TVP3025-175			550	630	
		TVP3025-220			630	720	
	Supply current, true-color mode	TVP3025-135			510	570	
		TVP3025-175			580	650	
		TVP3025-220			670	750	
I_{OZ}	High-impedance-state output current					10	µA
C_i	Input capacitance	TTL inputs	f = 1 MHz, V_I = 2.4 V		4		pF
		ECL inputs	f = 1 MHz, V_I = 4 V		4		
V_{ID}	Differential input voltage	ECL inputs		0.6		6	V
V_{IC}	Common-mode input voltage	ECL inputs		2.85	3.15	V_{DD}–0.5	V

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

NOTE 2: I_{DD} is measured with DOTCLK running at the maximum specified frequency, SCLK frequency = DOTCLK frequency/8, and the palette RAM loaded with repeating full-range toggling patterns (00h/00h/00h/00h/FFh/FFh/FFh/FFh). Pseudo-color mode is also known as color indexing mode.

3.4 Operating Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution (each DAC)	8/$\overline{6}$ high		8		bits
		8/$\overline{6}$ low		6		
E_L	End-point linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
E_D	Differential linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
	Gray scale error				5%	
	Output current (see Note 3)	White level relative to blank	17.69	19.05	20.4	mA
		White level relative to black (7.5 IRE only)	16.74	17.62	18.5	mA
		Black level relative to blank (7.5 IRE only)	0.95	1.44	1.9	mA
		Blank level on IOR, IOB	0	5	50	μA
		Blank level on IOG (with SYNC enabled)	6.29	7.6	8.96	mA
		Sync level on IOG (with SYNC enabled)	0	5	50	μA
		One LSB (8/$\overline{6}$ high)		69.1		μA
		One LSB (8/$\overline{6}$ low)		276.4		μA
	DAC-to-DAC matching			2%	5%	
	DAC-to-DAC crosstalk			–20		dB
	Output compliance		–1		1.2	V
	Voltage reference output voltage		1.15	1.235	1.26	V
	Output impedance			50		kΩ
	Output capacitance	f = 1 MHz, I_{OUT} = 0		13		pF
	Sense voltage reference		300	350	400	mV
	Clock and data feedthrough			–20		dB
	Glitch impulse (see Note 4)			50		pV–s
	Pipeline delay, VGA port	Self clocked timing		18 DOT		periods
		Externally clocked timing		15 DOT		periods
	Pipeline delay, pixel port	Self clocked timing		2 RCLK + 14 DOT		periods
		Externally clocked timing		1 RCLK +14 DOT		periods
	Pixel clock PLL	Lock time		15		ms
		Jitter		±200		ps

NOTES: 3. Test conditions for RS343-A video signals (unless otherwise specified): “Recommended Operating Conditions”, using external voltage reference V_{ref} = 1.235 V, R_{SET} = 523 Ω. When using the internal voltage reference, R_{SET} may need to be adjusted in order to meet these limits.

4. Glitch impulse does not include clock and data feedthrough. The – 3-dB test bandwidth is twice the clock rate.

3.5 Timing Requirements (see Note 5)

			TVP3025 -135		TVP3025 -175		TVP3025 -220		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
	DOTCLK frequency			135		175		220	MHz
	Pixel clock PLL	Internal frequency		135		175		220	MHz
		PCLKOUT frequency		110		110		110	MHz
	CLK0 frequency for VGA pass-through mode (see Note 6)			85		85		85	MHz
t_{cyc}	Clock cycle time	TTL	7.4		7.1		7.1		ns
		ECL	7.4		5.8		4.54		
t_{su1}	Setup time, RS(0 – 3) valid before $\overline{RD}$ or $\overline{WR}\downarrow$		10		10		10		ns
t_{h1}	Hold time, RS(0 – 3) valid after $\overline{RD}$ or $\overline{WR}\downarrow$		10		10		10		ns
t_{su2}	Setup time, D(0 – 7) valid before $\overline{WR}\uparrow$		35		35		35		ns
t_{h2}	Hold time, D(0 – 7) valid after $\overline{WR}\uparrow$		0		0		0		ns
t_{su3}	Setup time, VGA(0 – 7) and VGAHS, VGAVS, and $\overline{VGABL}$ valid before CLK0$\uparrow$ (see Note 7)		2		2		2		ns
t_{h3}	Hold time, VGA(0 – 7) and VGAHS, VGAVS, and $\overline{VGABL}$ valid after CLK0$\uparrow$ (see Note 7)		2		2		2		ns
t_{su4}	Setup time, P(0 – 63) and PSEL valid before LCLK$\uparrow$ (see Note 8) $\overline{SYSHS}$, $\overline{SYSVS}$, $\overline{SYSBL}$		2		2		2		ns
t_{h4}	Hold time, P(0 – 63) and PSEL valid after LCLK$\uparrow$ (see Note 8) $\overline{SYSHS}$, $\overline{SYSVS}$, $\overline{SYSBL}$		1		1		1		ns
t_{su5}	Setup time, $\overline{SYSHS}$, $\overline{SYSVS}$, and $\overline{SYSBL}$ valid before VCLK$\downarrow$ (VCLK lactched)		5		5		5		ns
t_{h5}	Hold time, $\overline{SYSHS}$, $\overline{SYSVS}$, and $\overline{SYSBL}$ valid after VCLK$\downarrow$ (VCLK lactched)		1		1		1		ns
t_{w1}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ low		50		50		50		ns
t_{w2}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ high		30		30		30		ns
t_{w3}	Pulse duration, clock high	TTL	3		3		3		ns
		ECL	3		2.5		2		
t_{w4}	Pulse duration, clock low	TTL	3		3		3		ns
		ECL	3		2.5		2		
t_{w5}	Pulse duration, SFLAG high (see Note 9)		30		30		30		ns
t_{w6}	Pulse duration, SCLK high (see Note 9)		15	55	15	55	15	55	ns

NOTES: 5. TTL input signals are 0 to 3 V with less than 3 ns rise/fall time between the 10% and 90% levels unless otherwise specified. ECL input signals are V_{DD}–1.8 V to V_{DD}–0.8 V with less than 2 ns rise/fall time between the 20% and 80% levels. For input and output signals, timing reference points are at the 10% and 90% signal levels. Analog output loads are less than 10 pF. D<0:7> output loads are less than 50 pF. All other output loads are less than 50 pF unless otherwise specified.

6. In VGA mode, CLK0 minimum pulse duration for clock low should be greater than 4.8 ns. If VGA switching is to be performed using self-clocked timing, the maximum pixel rate cannot exceed 50 MHz.
7. Reference to CLK0 input only.
8. RCLK is delayed from SCLK in such a way that when RCLK is connected to LCLK, the timing is essentially the same as the TLC3407x family of parts.
9. This parameter applies when the split shift-register transfer (SSRT) function is enabled. See Section 2.3.7.2 for details.

3.6 Switching Characteristics

	PARAMETER	TVP3025-135			UNIT
		MIN	TYP	MAX	
	SCLK frequency (C_{LOAD} ≤ 15 pF) (see Note 10)			85	MHz
	SCLK frequency (C_{LOAD} ≤ 60 pF) (see Note 10)			85	MHz
	RCLK/VCLK frequency (see Note 10)			85	MHz
t_{en1}	Enable time, $\overline{RD}$ low to D(0 – 7) valid			40	ns
t_{dis1}	Disable time, $\overline{RD}$ high to D(0 – 7) disabled			17	ns
t_{v1}	Valid time, D(0 – 7) valid after $\overline{RD}$ high	5			ns
t_{PLH1}	Propagation delay, SFLAG↑ to SCLK high (see Note 10 and 11)	0		20	ns
t_{d1}	Delay time, $\overline{RD}$ low to D(0 – 7) starting to turn on	5			ns
t_{d2}	Delay time, selected input clock high/low to DOTCLK (internal signal) high/low		7		ns
t_{d3}	Delay time, SCLK high/low to RCLK high/low (see Note 12)	1	2	5	ns
t_{d4}	Delay time, VCLK high/low to RCLK high/low (see Note 12)	1	3	6	ns
t_{d5}	Delay time, RCLK high/low from DOTCLK high/low (internal signal)		7		ns
t_{d6}	Delay time, LCLK from RCLK			t_{RCLK-7}	ns
t_{d7}	Delay time, DOTCLK high to IOR/IOG/IOB active (analog output delay time) (see Note 13)		4		ns
t_{d8}	Analog output settling time (see Note 14)		6		ns
t_{d9}	Delay time, DOTCLK high to HSYNCOUT and VSYNCOUT valid		9		ns
t_r	Analog output rise time (see Note 15)		2		ns
	Analog output skew	0		2	ns

NOTES: 10. SCLK can drive an output capacitive load up to 60 pF. The worst-case transition time between the 10% and 90% levels is less than 4 ns (typical 3 ns). RCLK and VCLK can drive output capacitive loads up to 15 pF, with worst case transition times between 10% and 90% levels less than 4 ns (typical 3 ns).

11. This parameter applies when the split shift-register transfer (SSRT) function is enabled. See Section 2.3.7.2 for details.
12. The SCLK and VCLK delay time to RCLK depends on the load that the signals drive. This parameter is measured with an RCLK to VCLK ratio of 1:1, and VCLK = RCLK load of 15 pF and SCLK load of 60 pF.
13. Measured from the 90% point of the rising edge of DOTCLK to 50% of the full-scale transition.
14. Measured from the 50% point of the full-scale transition to the point at which the output has settled, within ± 1 LSB (settling time does not include clock and data feedthrough).
15. Measured between 10% and 90% of the full-scale transition.

3.6 Switching Characteristics (Continued)

PARAMETER		TVP3025-175			TVP3025-220			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
	SCLK frequency ($C_{LOAD} \leq 15$ pF) (see Note 10)		87.5			110		MHz
	SCLK frequency ($C_{LOAD} \leq 60$ pF) (see Note 10)			85			85	MHz
	RCLK, VCLK frequency (see Note 10)			87.5			110	MHz
t_{en1}	Enable time, $\overline{RD}$ low to D(0–7) valid			40			40	ns
t_{dis1}	Disable time, $\overline{RD}$ high to D(0–7) disabled			17			17	ns
t_{v1}	Valid time, D(0–7) valid after $\overline{RD}$ high	5			5			ns
t_{PLH1}	Propagation delay, SFLAG↑ to SCLK high (see Note 10 and 11)	0		20	0		20	ns
t_{d1}	Delay time, $\overline{RD}$ low to D(0–7) starting to turn on	5			5			ns
t_{d2}	Delay time, selected input clock high/low to DOTCLK (internal signal) high/low		7			7		ns
t_{d3}	Delay time, SCLK high/low to RCLK high/low (see Note 12)	1	2	5	1	2	5	ns
t_{d4}	Delay time, VCLK high/low to RCLK high/low (see Note 12)	1	3	6	1	3	6	ns
t_{d5}	Delay time, RCLK high/low from DOTCLK high/low (internal signal)		7			7		ns
t_{d6}	Delay time, LCLK from RCLK			t_{RCLK-7}			t_{RCLK-7}	ns
t_{d7}	Delay time, DOTCLK high to IOR/IOG/IOB active (analog output delay time) (see Note 13)		4			4		ns
t_{d8}	Analog output settling time (see Note 14)		5			5		ns
t_{d9}	Delay time, DOTCLK high to HSYNCOUT and VSYNCOUT valid		9			9		ns
t_r	Analog output rise time (see Note 15)		2			2		ns
	Analog output skew	0		2	0		2	ns

NOTES: 10. SCLK can drive an output capacitive load up to 60 pF. The worst-case transition time between the 10% and 90% levels is less than 4 ns (typical 3 ns). RCLK and VCLK can drive output capacitive loads up to 15 pF, with worst case transition times between 10% and 90% levels less than 4 ns (typical 3 ns).

11. This parameter applies when the split shift-register transfer (SSRT) function is enabled. See Section 2.3.7.2 for details.
12. The SCLK and VCLK delay time to RCLK depends on the load that the signals drive. This parameter is measured with an RCLK to VCLK ratio of 1:1, and VCLK = RCLK load of 15 pF and SCLK load of 60 pF.
13. Measured from the 90% point of the rising edge of DOTCLK to 50% of the full-scale transition.
14. Measured from the 50% point of the full-scale transition to the point at which the output has settled, within ± 1 LSB (settling time does not include clock and data feedthrough).
15. Measured between 10% and 90% of the full-scale transition.

3.7 Timing Diagrams

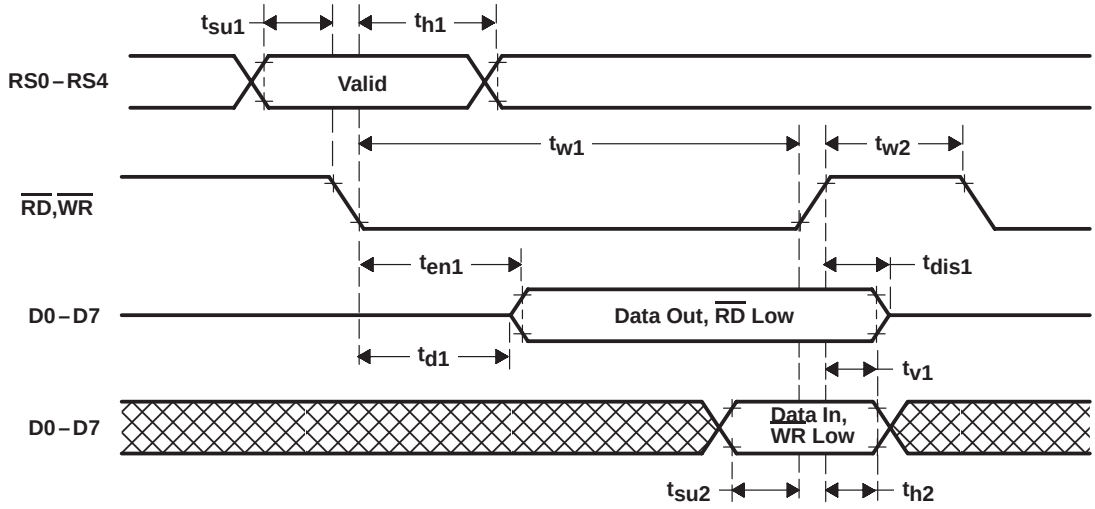


Figure 3–1. MPU Interface Timing

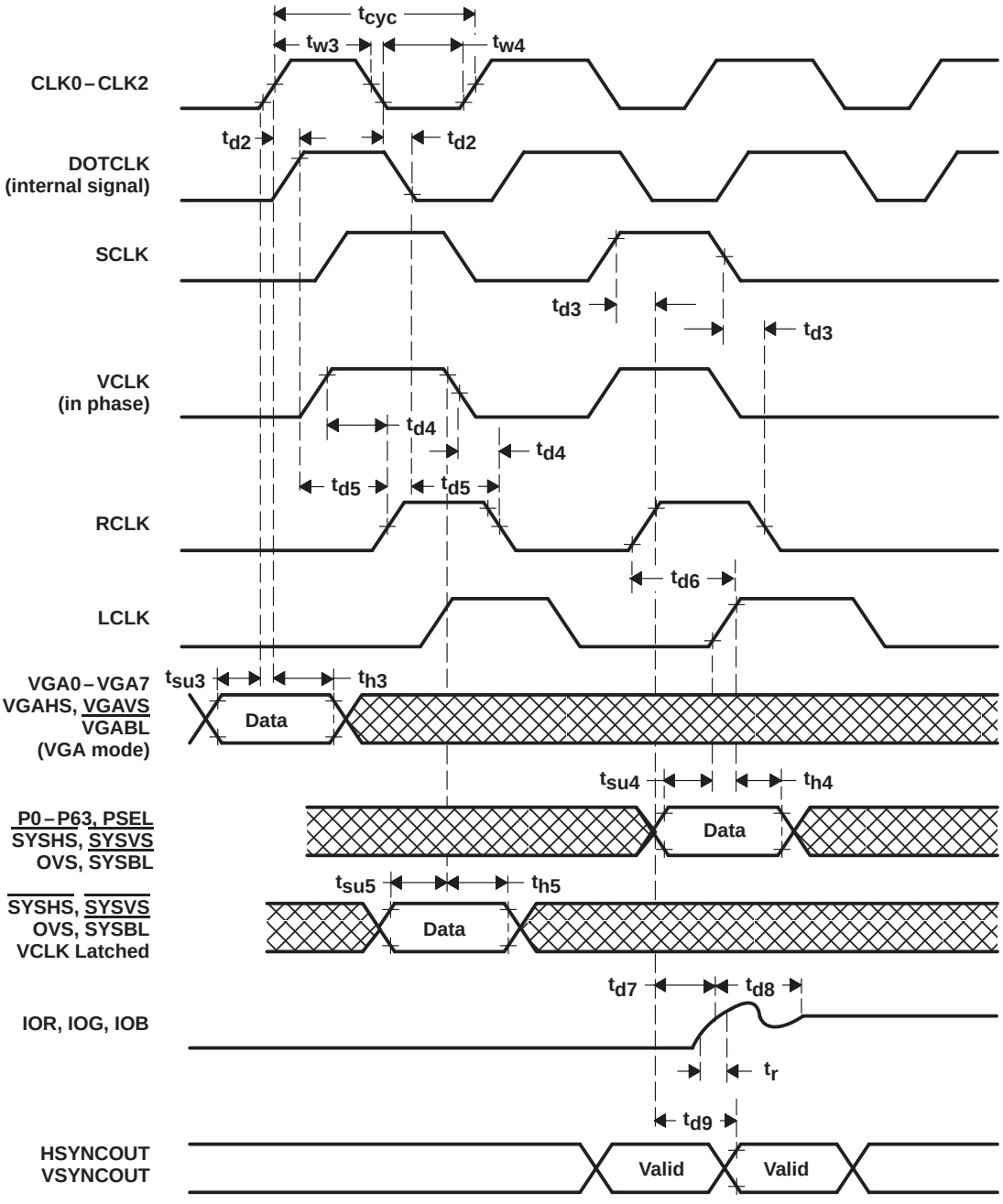


Figure 3–2. Video Input/Output Timing

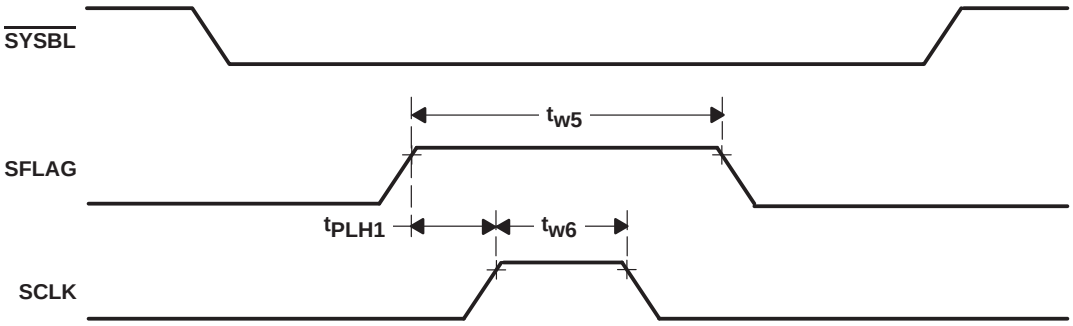


Figure 3–3. SFLAG Timing (When SSRT Function is Enabled)

Appendix A
PC-Board Layout Considerations

PC-Board Considerations

It is recommended that a four-layer PC board be used with the TVP3025 video interface palette: one layer for 5-V power, one for GND, and two for signals. The layout should be optimized for the lowest noise on the TVP3025 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of analog V_{DD} and GND terminals (see Figure A–1) should be minimized so as to minimize inductive ringing. The TVP3025 P0–P63 terminal assignments have been selected for minimum interconnect lengths between these inputs and the standard VRAM pixel data outputs. The TVP3025 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

For maximum performance, the analog-video-output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the TVP3025 to minimize reflections. Unused analog outputs should be connected to GND.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length-dependent ghosts. Simple pulse filters can reduce high-frequency energy, thus reducing EMI and noise. The filter impedance must match the line impedance.

Ground Plane

It is also recommended that only one ground plane be used for both the TVP3025 and the rest of the logic. Separate digital and analog ground planes are not needed and can potentially cause system problems.

Power Plane

Split-power planes for the TVP3025 and the rest of the logic are recommended. The TVP3025 VIP analog circuitry should have its own power plane, referred to as AV_{DD}. These two power planes should be connected at a single point through a ferrite bead, as shown in Figures A–1 and A–2.This bead should be located as near as possible to where the power supply connects to the board. To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible. This reduces the lead inductance and is consistent with reliable operation.

For the best performance, a 0.1-µF ceramic capacitor in parallel with a 0.01-µF chip capacitor should be used to decouple each of the groups of power terminals to GND. These capacitors should be placed as close as possible to the device, as shown in Figure A–2.

If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three-terminal voltage regulator for supplying power to AV_{DD}.

COMP and REF Pins

A 0.1-μF ceramic capacitor should be connected between COMP1 and COMP2 to avoid noise and color-smearing problems. A 0.1-μF ceramic capacitor is also recommended between GND and REF to further stabilize the output image. This 0.1-μF capacitor is needed for either internal or external voltage references. These capacitor values may depend on the board layout; experimentation may be required in order to determine optimum values.

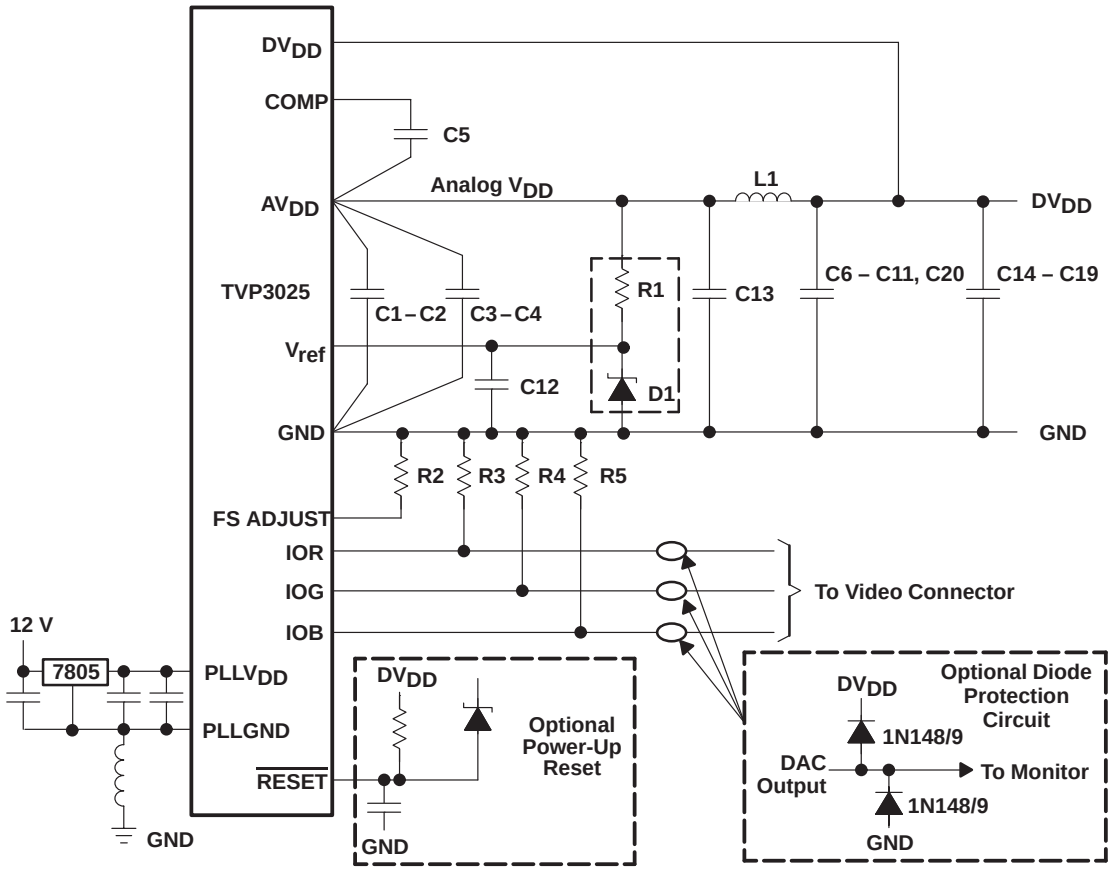
Analog Output Protection

The TVP3025 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching ac-coupled monitors.

The diode protection circuit shown in Figure A–1 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The IN4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PLL Supply

A separate 5V regulator is recommended for the PLL supply. A typical circuit is shown in Figure A–1.



Location	Description	VENDOR PART NUMBER†
C1, C2, C5–C12, C20	0.1-µF ceramic capacitor	Erie RPE110Z5U104M50V
C3, C4, C14–C19	0.01-µF ceramic chip capacitor	AVX 12102T103QA1018
C13	33-µF tantalum capacitor	Mallory CSR13F336KM
L1	Ferrite bead	Fair-Rite 2743001111‡
R1	1000-Ω 1% metal-film resistor	Dale CMF-55C
R2	523-Ω 1% metal-film resistor	Dale CMF-55C
R3, R4, R5	75-Ω 1% metal-film resistor	Dale CMF-55C
D1	1.2-V voltage reference	TI LM385-1.2

† The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the TVP3025.

‡ Or equivalent only.

Figure A–1. Typical Connection Diagram and Parts

NOTE: R1, D1, and reset circuit are optional. In general, each pair of device power and GND pins should be separately decoupled with 0.1-µF and 0.01-µF capacitors.

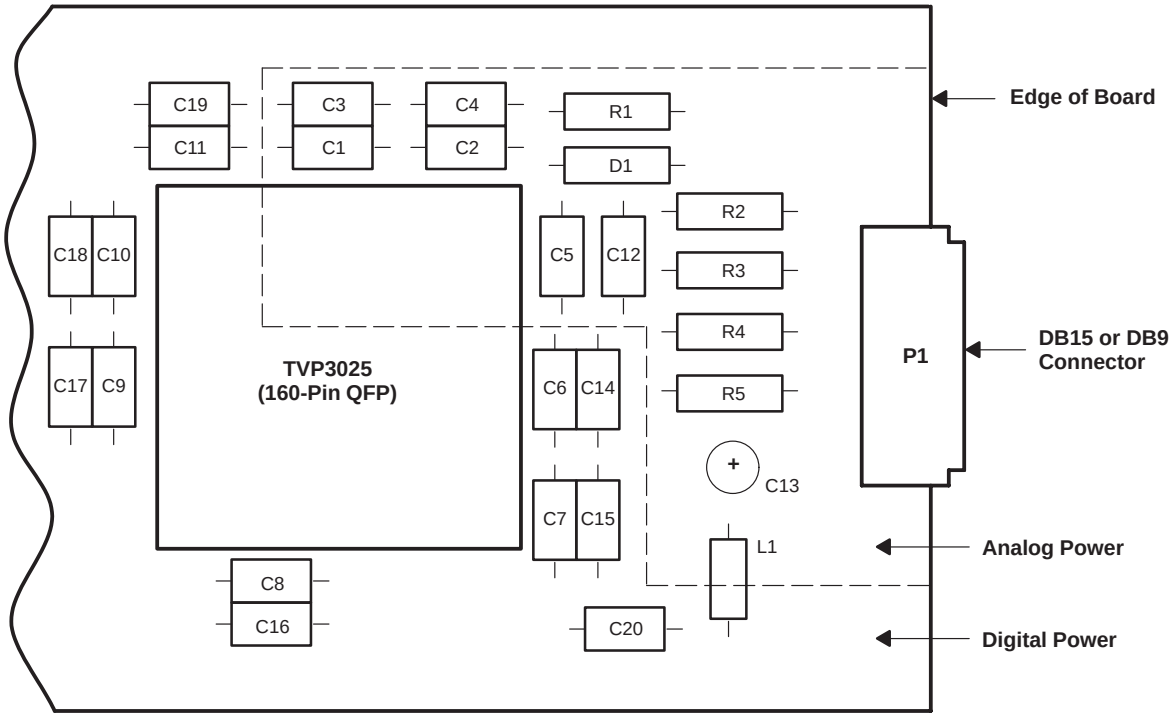


Figure A–2. Typical Component Placement With Split-Power Plane

Appendix B
RCLK Frequency < VCLK Frequency

The VCLK, RCLK, and SCLK outputs generated by the TVP3025 VIP are free-running clocks. The video-control signals (i.e., $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$) are normally generated from VCLK, and a fixed relationship between video-control signals and VCLK can be expected. If the TVP3025 is programmed to sample and latch the $\overline{\text{BLANK}}$ input on the falling edge of VCLK some precautions must be observed. After being sampled, it then looks at the internal RCLK signal to determine when to enable or disable SCLK at the output terminal. The decision is determined when the RCLK frequency is greater than or equal to the VCLK frequency. However, when the RCLK frequency is less than the VCLK frequency, the appearance of the SCLK waveform at the output terminal (when $\overline{\text{BLANK}}$ is sampled low on the falling edge of VCLK) can vary (see Figures B–1 and B–2).

To avoid this variation in the SCLK output waveform, the RCLK and VCLK frequencies should be chosen so that HTOTAL is evenly divisible by the ratio of the VCLK frequency to the RCLK frequency:

remainder of [HTOTAL / (VCLK frequency / RCLK frequency)] = 0

For example, if HTOTAL is even, VCLK frequency = DOTCLK frequency/8 and RCLK frequency = DOTCLK frequency/16. Then the above formula is satisfied. NOTE: When HTOTAL starts at zero, then the formula becomes:

remainder of [(HTOTAL + 1) / (VCLK frequency / SCLK frequency)] = 0.

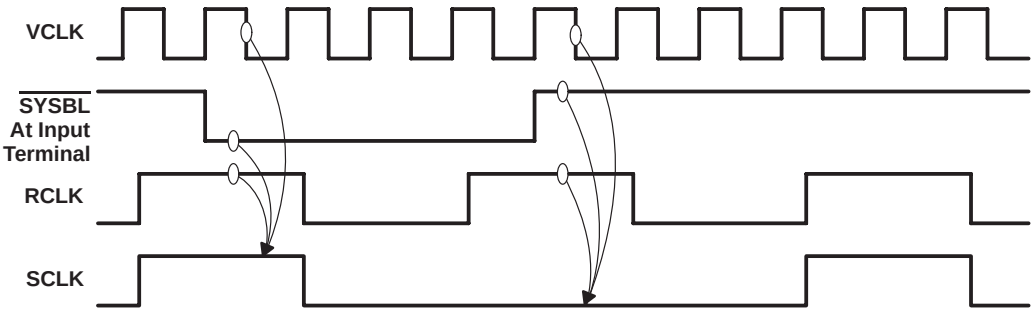


Figure B–1. VCLK and SCLK Phase Relationship (Case 1)

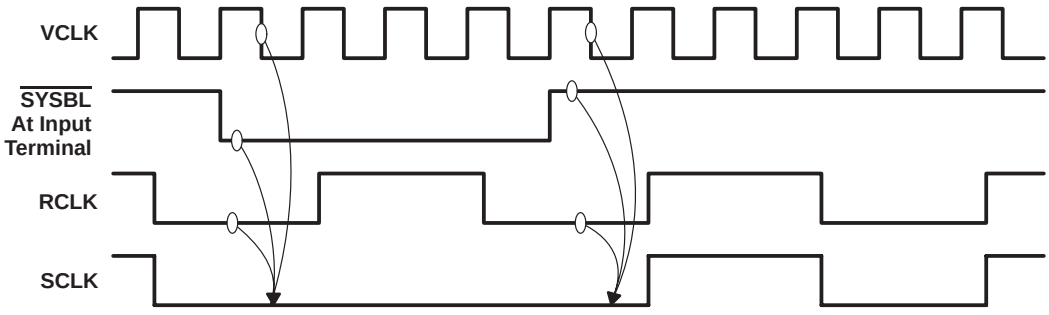


Figure B–2. VCLK and SCLK Phase Relationship (Case 2)

Appendix C
Little-Endian and Big-Endian Data Formats

It is commonly known in the computer industry that there are two different formats for memory configuration: little-endian (Intel microprocessor format) and big-endian (Motorola microprocessor-based format). When the Texas Instruments programmable pixel bus was introduced on the TLC34075 video interface palette, it allowed little-endian-based graphics-board manufacturers to design a single graphics board that could be programmed to support multiple resolutions and pixel depths. The connection of the pixel bus from the video RAM to the palette device was not a problem until big-endian-based customers desired the same capability to program their graphics designs from 1 bit/pixel (bpp), 2 bpp, 4 bpp, 8 bpp, 12 bpp, 16 bpp, 24 bpp, to 32 bpp.

For this reason, the TVP3025 video interface palette supports both little- and big-endian data formats on its pixel-bus/frame-buffer interface. The device defaults to little-endian mode at reset (general-control register bit 3 set to logic 0) to be compatible with most PC-based systems. Big-endian-mode operation can be achieved by configuring the device to the big-endian mode (general-control register bit 3 set to logic 1) and externally reverse wiring the pixel bus from video RAM to TVP3025 on the graphics board.

The differences between the big-endian and little-endian data formats are illustrated in Figure C–1. The figure shows that the data fields representing the individual pixels in the big-endian format are in the reverse order of the little-endian format. Since the TVP3025 VIP always shifts data from low-numbered data fields to high-numbered data fields, external swapping of the pixel bus (i.e., D63 connected to P0, D0 connected to P63) ensures that the pixels are displayed on the monitor in the correct sequence. However, swapping the big-endian pixel bus causes the bits within each data field to be reversed (i.e., MSB to LSB instead of LSB to MSB). When general-control register bit 3 is set to a logic 1, unique circuitry within the TVP3025 corrects the bit sequence in each data field as it is shifted into the part. This correction is bit-plane independent and occurs regardless of whether 8, 4, 2, or 1 bits/pixel are being used.

TVP3025 also supports 12-, 16-, and 24-bit true-/direct-color for both little- and big-endian data formats on the pixel bus. By using the same wiring for big-endian operation as described above, all true-/direct-color modes are made available without hardware modification. Tables 2–8 through 2–11 give the true-/direct-color bit definitions for all modes. For example, when in one of the 16-bit true-color modes (big-endian), the first RGB data word to be displayed is located in bits 48–63 of VRAM. Swapping the external pixel bus when designing the graphics board ensures the correct display sequence by causing the first RGB word to appear at pixel bus inputs P0–P15. However, the bit order within the word is reversed. When general-control register bit 3 is set to a logic 1, the bit sequence is automatically corrected by circuitry within the TVP3025.

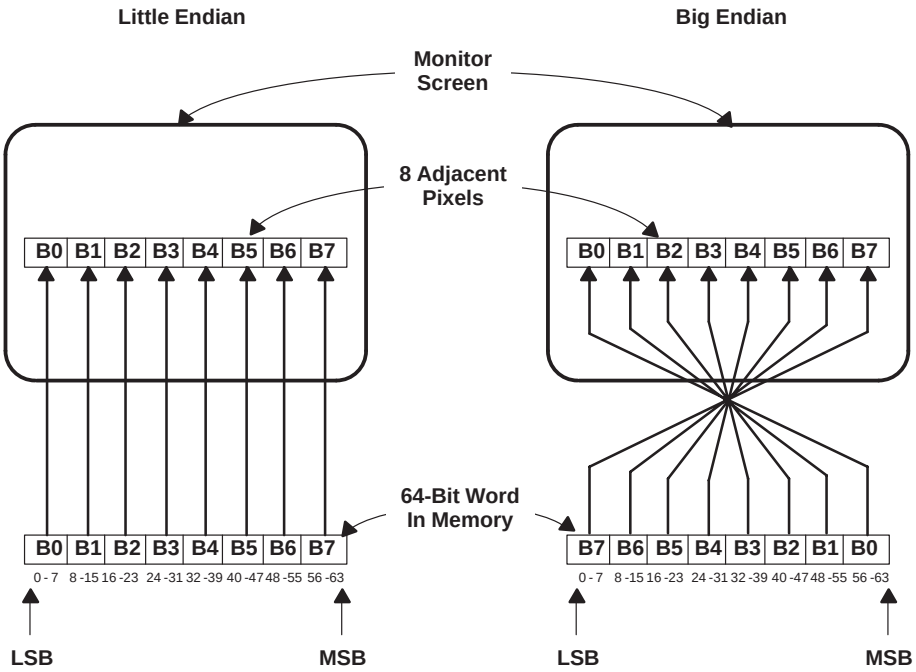
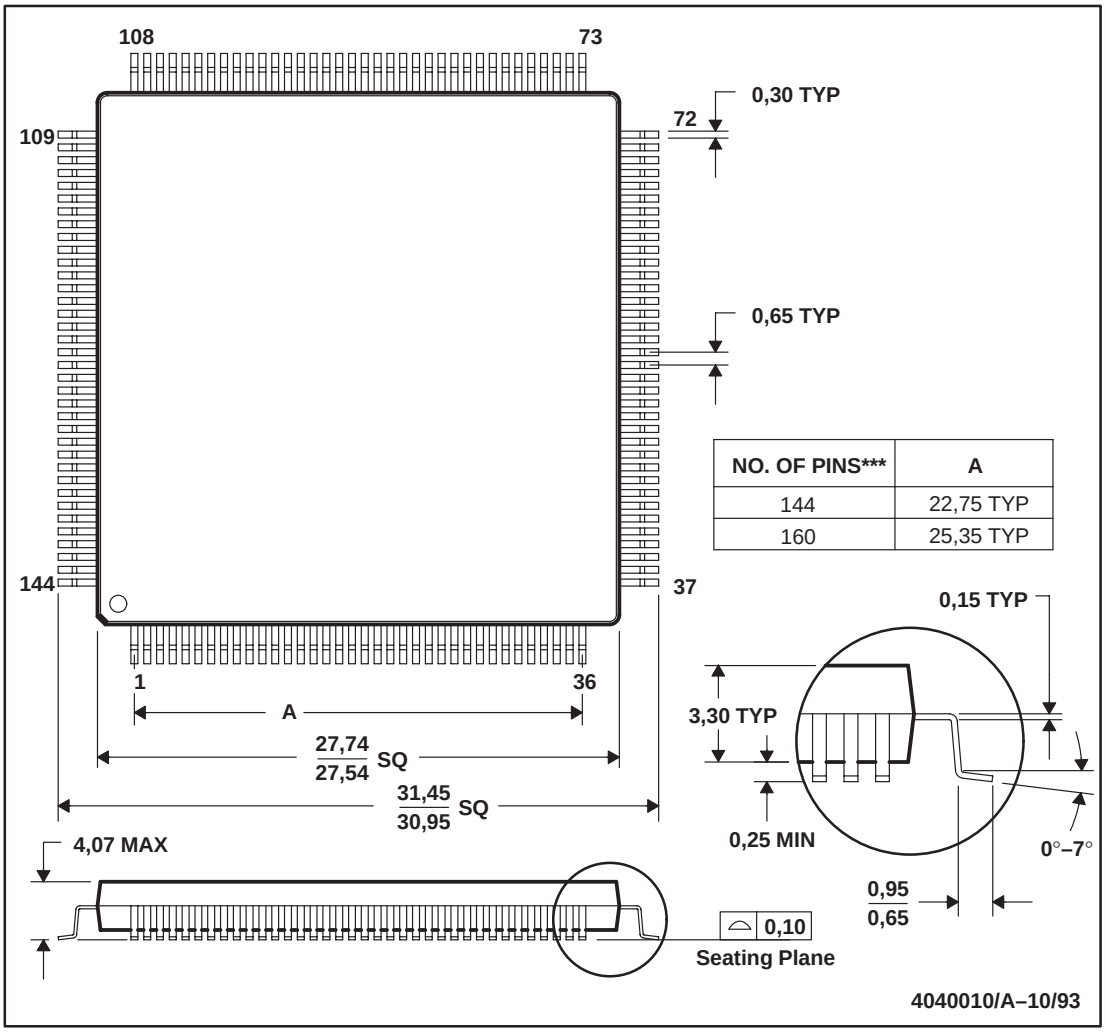


Figure C–1. Little-Endian and Big-Endian Mapping of 8-Bit/Pixel Pseudo-Color Data in Memory to Monitor Screen

Appendix D
Mechanical Data

MDN/S-MQFP-G* METAL QUAD (MQUAD®) CAVITY-UP FLAT PACKAGE**

144-PIN SHOWN

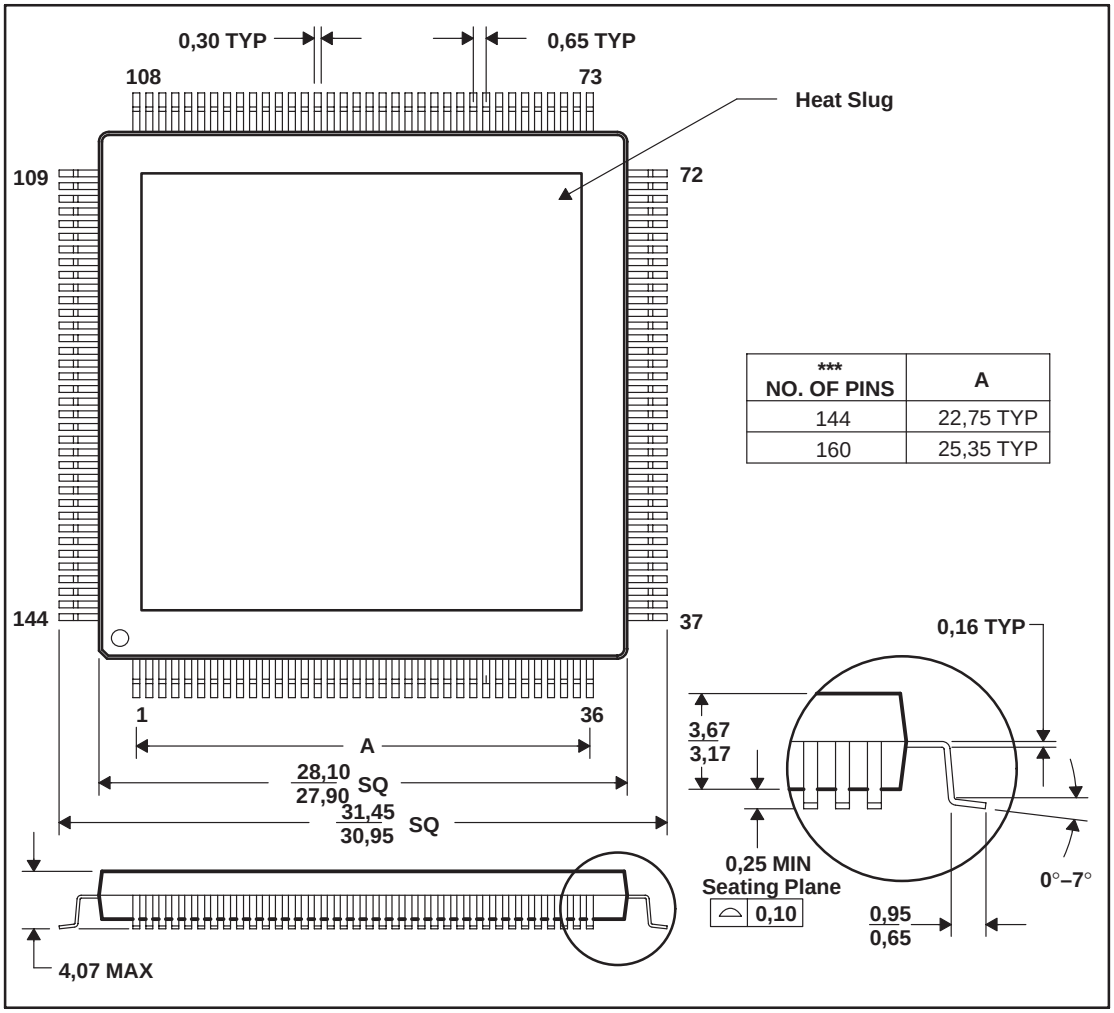


NO. OF PINS***	A
144	22,75 TYP
160	25,35 TYP

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MQUAD is a registered trademark of Olin Corporation.
D. This quad flat package consists of a circuit mounted on a lead frame and encased within an anodized aluminum shell. The package is intended for parts requiring either a lower stress environment or higher thermal dissipation capabilities than can be supplied by plastic. Ultrasonic cleaning of this package or boards with this package is not permissible.
E. The 144 MDN is identical to 160 MDN except 4 leads per corner are removed.

PCE/S-PQFP-G* PLASTIC QUAD FLATPACK**

144-PIN SHOWN

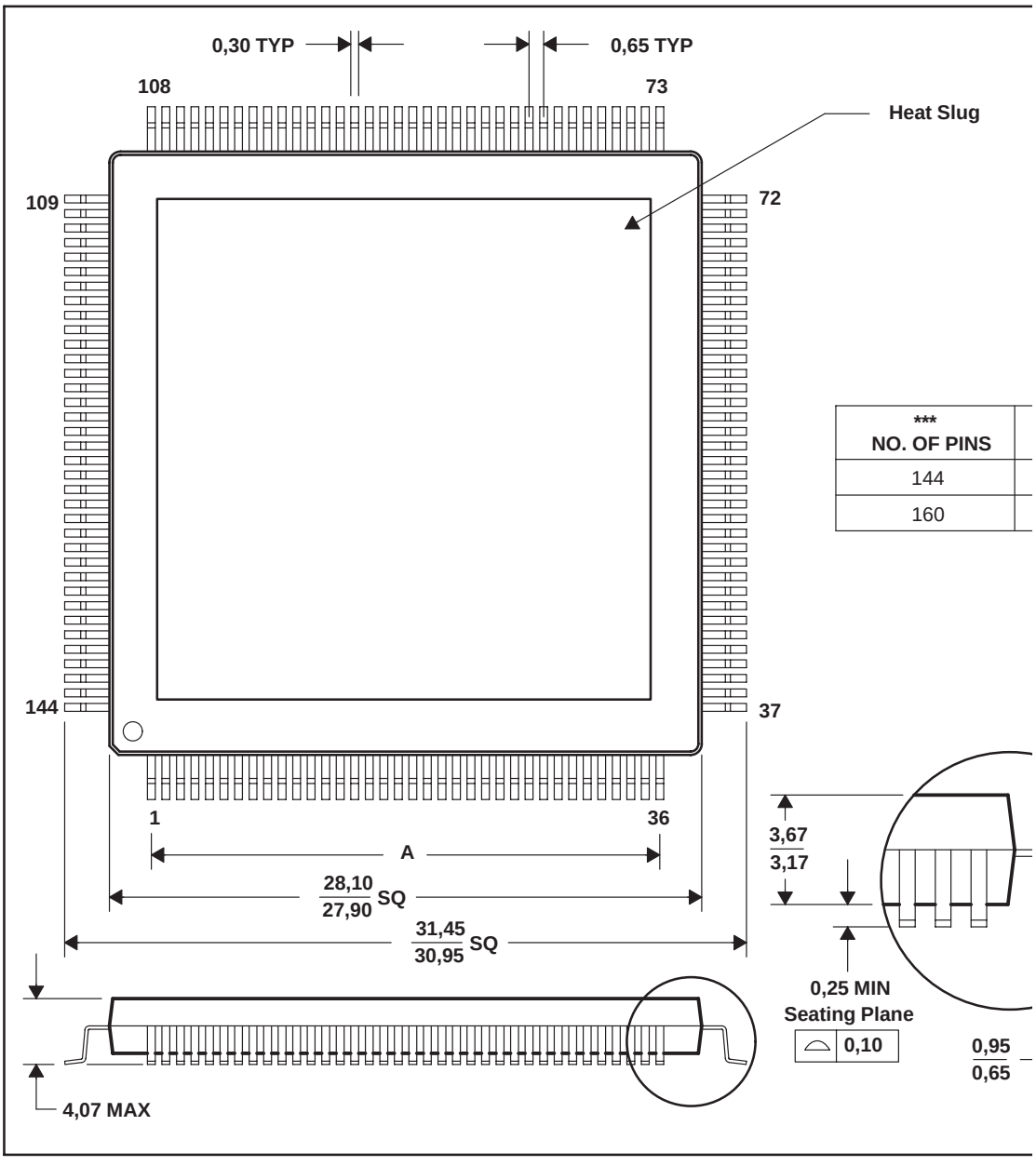


*** NO. OF PINS	A
144	22,75 TYP
160	25,35 TYP

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced molded plastic package (HSL).

PCE/S-PQFP-G* PLASTIC QUAD FLATPACK**

144-PIN SHOWN



*** NO. OF PINS	
144	
160	

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced molded plastic package (HSL).

PACKAGE OPTION ADDENDUM

30-Mar-2005

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TVP3025-135PCE	OBSOLETE	HQFP	PCE	160		TBD	Call TI	Call TI
TVP3025-175PCE	OBSOLETE	HQFP	PCE	160		TBD	Call TI	Call TI
TVP3025-220MDN	OBSOLETE	MQFP	MDN	160		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.