Attansic Technology Corporation

ATXP5

Jumper Free Over Clock Controller

Datasheet

Release Date: Jan. 2005
Revision: 1.0

Revision History

Version	Date	Changes from Last Version
1.0	Jan/19/2005	Add “Ordering Information” about green device description

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1. General Description

ATXP5 is a full feature of over clocking device. It integrates all functions that are possible to be utilized for over-clocking purpose.

2. Features

- Provide Four FID Input (FIDIN0-3) and Eight Output Pins (FIDOCS0-3 & FIDOCPU0-3)
  - FIDCS0-3 Outputs for Chip Set & FIDCPU0-3 Outputs for CPU
- Provide NBPWROK pin
- Provide Five GPIO Pins
- Support Auto-Recover
  - Build-in Watch Dog Timer & Reset Output Signal Pin
- Provide CPU Changing Detect Pin (SLOTOCC#)
- SM Bus Interface
- Package: SSOP 28-Pin

3. Pin Configuration

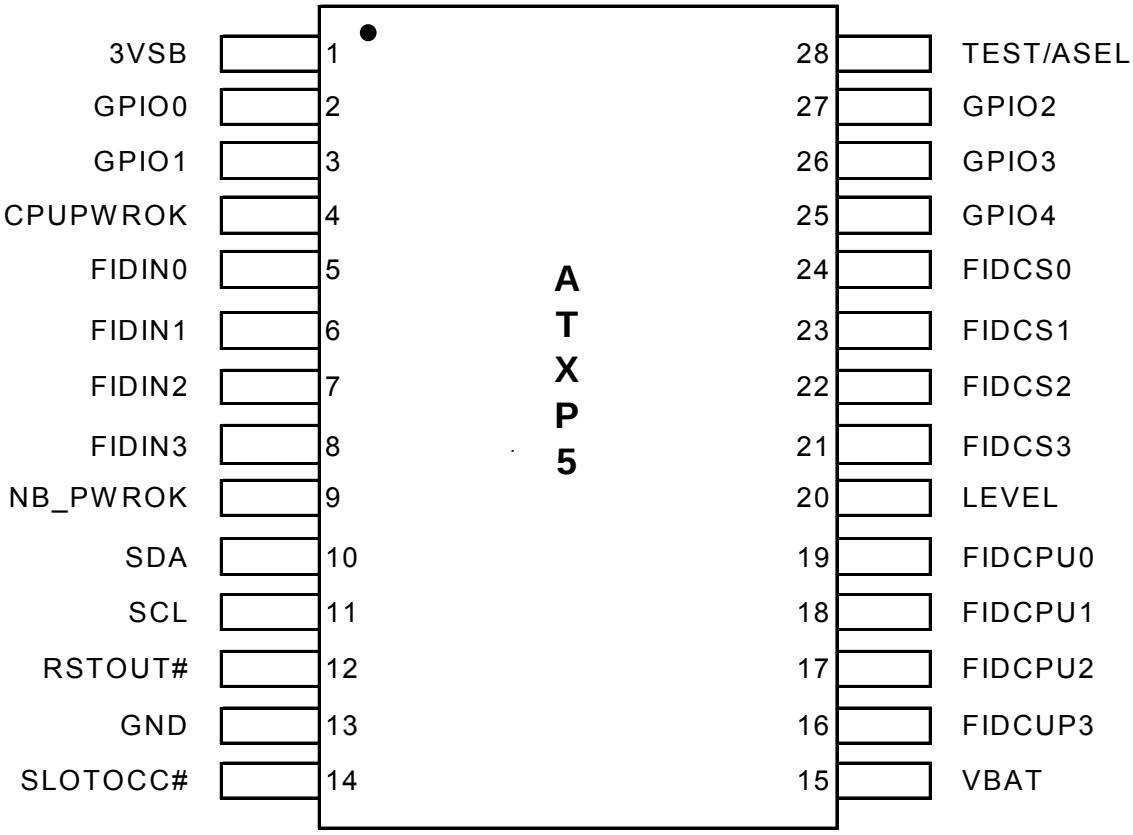

Figure 1. ATXP5 Pin Diagram (Top View)

※ **Ordering Information**

ATXP5- Commercial Standard
ATXP5G- Green Device with Commercial Standard

4. Pin Description

I/O TYPE DESCRIPTION

IN_t ---- TTL level input.
IN_{ts} ---- TTL level input with Schmitt-trigger.
$IN_{t\text{-}10k\text{-}up}$ ---- TTL level input I pin with 12mA drive/sink current and10K ohm pull-up resistor.
$IN_{t\text{-}47k\text{-}up}$ ---- TTL level input I pin with 12mA drive/sink current and47K ohm pull-up resistor.
OD_{12} ---- Open-drain with 12mA sink current.
O_{12} ---- Output buffer with 12mA drive/sink current
I/OD_{12} ---- TTL level bi-directional pin, and open-drain output with 12mA sink current.
I/O_{12} ---- TTL level bi-directional pin, and output with 12mA drive/sink current.

Pin No.	Pin name	I/O Type	Function
1	3VSB	POWER	Power Pin
2	GPIO0	I/O_{12}	General Purpose I/O Pin
3	GPIO1	I/O_{12}	General Purpose I/O Pin
4	CPUPWROK	$IN_{t\text{-}47k\text{-}up}$	Receive CPUPWROK Signal form CPU
5	FIDIN0	IN_{tx}	Receive FID0 Signal form CPU
6	FIDIN1	IN_{tx}	Receive FID1 Signal form CPU
7	FIDIN2	IN_{tx}	Receive FID2 Signal form CPU
8	FIDIN3	IN_{tx}	Receive FID3 Signal form CPU
9	NB_PWROK	OD_{12}	North-Bridge Power-OK.
10	SDA	I/OD_{12}	SMB Data Signal
11	SCL	IN_{ts}	SMB Clock Signal
12	RSTOUT#	OD_{12}	Rest Output Signal
13	GND		GROUND Pin
14	SLOTOCC#	IN_{ts}	Receive SLOTOCC# from CPU
15	VBAT		Power Pin
16	FIDCPU3	O_{12}	FID3 Signal Output Pin to CPU
17	FIDCPU2	O_{12}	FID2 Signal Output Pin to CPU
18	FIDCPU1	O_{12}	FID1 Signal Output Pin to CPU
19	FIDCPU0	O_{12}	FID0 Signal Output Pin to CPU
20	LEVEL		Power Pin
21	FIDCS3	OD_{12}	FID3 Signal Output Pin to Chip Set
22	FIDCS2	OD_{12}	FID2 Signal Output Pin to Chip Set
23	FIDCS1	OD_{12}	FID1 Signal Output Pin to Chip Set

24	FIDCS0	OD12	FID0 Signal Output Pin to Chip Set
25	GPIO4	I/O12	General Purpose I/O Pin
26	GPIO3	I/O12	General Purpose I/O Pin
27	GPIO2	I/O12	General Purpose I/O Pin
28	Test /ASEL	INt-10k-up	Test Pin/Power-Strapping Device Address Select Pin.

Table1. Pin Description Table

5. Configuration Registers

Register	Offset	Power on/Reset Default value	Description
CPU FID Output Control Register	02h	00000000b	<7:5> Reserved. <4> CPU/CS FID Output Enable = 0 FIDIN pins pass to FIDCS and FIDCPU pins. = 1 FIDCS pins are controlled by CR03 bit 3~0(CS FID) and FIDCPU pins are controlled by CR02 bit 3~0(CPU FID). <3:0> CPU FID output value. This register is reset by 3VSB, RSTOUT#, and New CPU events.
Chipset FID Output Data Register	03h	00000000b	<7:4> Reserved. <3:0> CS FID Output Value. This register is reset by VBAT.
NEW CPU Status/Control / GPIO4-0 Input Enable Register	05h	00000000b	<7> New CPU Status <6> Clear New CPU Status. <5:0> Reserved.
Watching-Dog Timer Register	07h	00000000b	Watching-Dog Timer Register <7:0> Read this register means how much time left that Watching-Dog Timer will be time-out. Write this register to set a time into Watching-Dog Timer.
Watching-Dog Timer Status/MISC Control Register	08h	00000000b	<7> Watching-Dog Timer time-out status Register = 0 No Watching-Dog time-out event. = 1 Watching-Dog time-out event exists. Write “0” clear this status <6> Watching-Dog Timer Enable <5:4> Reserved. <3:2> Watching-Dog Timer time-unit select = 00 1 second. = 01 0.1 second. = 10 10 mini-second. = 11 1 mini-second. <1:0> RSTOUT# pulse width select = 00 1 second. = 01 0.1 second. = 10 10 mini-second. = 11 1 mini-second.

GPIO4-0 Input Enable Register	09h	00000000b	<7> Reserved. <6:3> GPIO4~1 input enable= 0 the corresponding GPIO is an output pin = 1 the corresponding GPIO is an input pin. <2:1> Reserved. <0> GPIO0 input enable= 0 the corresponding GPIO0 is an output pin = 1 the corresponding GPIO0 is an input pin.
GPIO4-0 Data Register	0Ah	111111111b	<7> Reserved. <6:3> GPIO4-1 data register If the GPIO pin is set as an input pin, the input value can be obtained by reading this register. If the GPIO pin is set as an output pin, the output value can be controlled by writing this register, and the output value can also be read back. <2:1>Reserved. <0> GPIO0 data register If the GPIO0 pin is set as an input pin, the input value can be obtained by reading this register. If the GPIO0 pin is set as an output pin, the output value can be controlled by writing this register, and the output value can also be read back.
GPIO4-0 Output Type Select Register	0Bh	00000000b	<7> Reserved. <6:3> GPIO4-1 output type = 0 The corresponding GPIO pin is open-drain output pin. = 1 The corresponding GPIO pin is push-pull output pin. <2:1>Reserved. <0> GPIO0 output type = 0 The corresponding GPIO0 pin is open-drain output pin. = 1 The corresponding GPIO0 pin is push-pull output pin.

6. Package Information
SSOP 28 pin Outline Dimension

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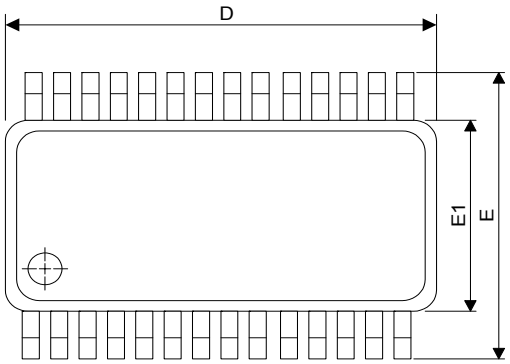

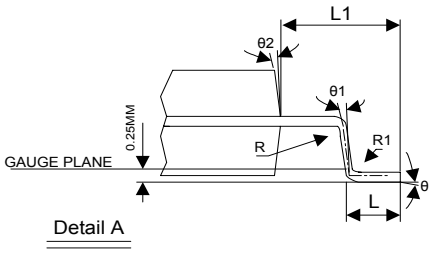

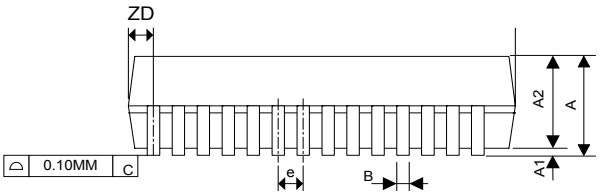

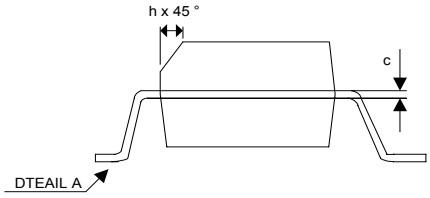

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			0.50			0.059
B	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
E	0.635 BASIC			0.025 BASIC		
D	9.80	9.91	10.01	0.386	0.390	0.394
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
H	0.25		0.50	0.010		0.020
ZD	0.838 REF			0.033 REF		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
θ 1	0°			0°		
θ 2	5°	10°	15°	5°	10°	15°
JEDEC	MO-137 (AF)					

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