DATA SHEET

TZA3004HL
SDH/SONET data and clock recovery unit STM1/4 OC3/12

Objective specification
File under Integrated Circuits, IC19

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Philips Semiconductors

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SDH/SONET data and clock recovery unit STM1/4 OC3/12

TZA3004HL

FEATURES

- Data and clock recovery up to 622 Mbits/s (STM1/OC3 and STM4/OC12)
- Differential data input with 2.5 mV peak-to-peak typical sensitivity
- Differential CML (Current-Mode Logic) data and clock outputs with 50 Ω driving capability
- Adjustable CML output level
- Loop mode for system testing
- BER related LOS detection
- Few external components needed
- LQFP48 plastic package
- Power dissipation typical 370 mW
- Single supply voltage.

DESCRIPTION

The TZA3004HL is a data and clock recovery IC intended for use in SDH (Synchronous Digital Hierarchy) and SONET (Synchronous Optical Network) systems.
The circuit recovers data and extracts the clock signal from an incoming bitstream up to 622 Mbits/s. It can be configured for use in STM1/OC3 and STM4/OC12 systems.

APPLICATIONS

- Data and clock recovery in STM1/OC3 and STM4/OC12 transmission systems (up to 622 Mbits/s).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3004HL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM

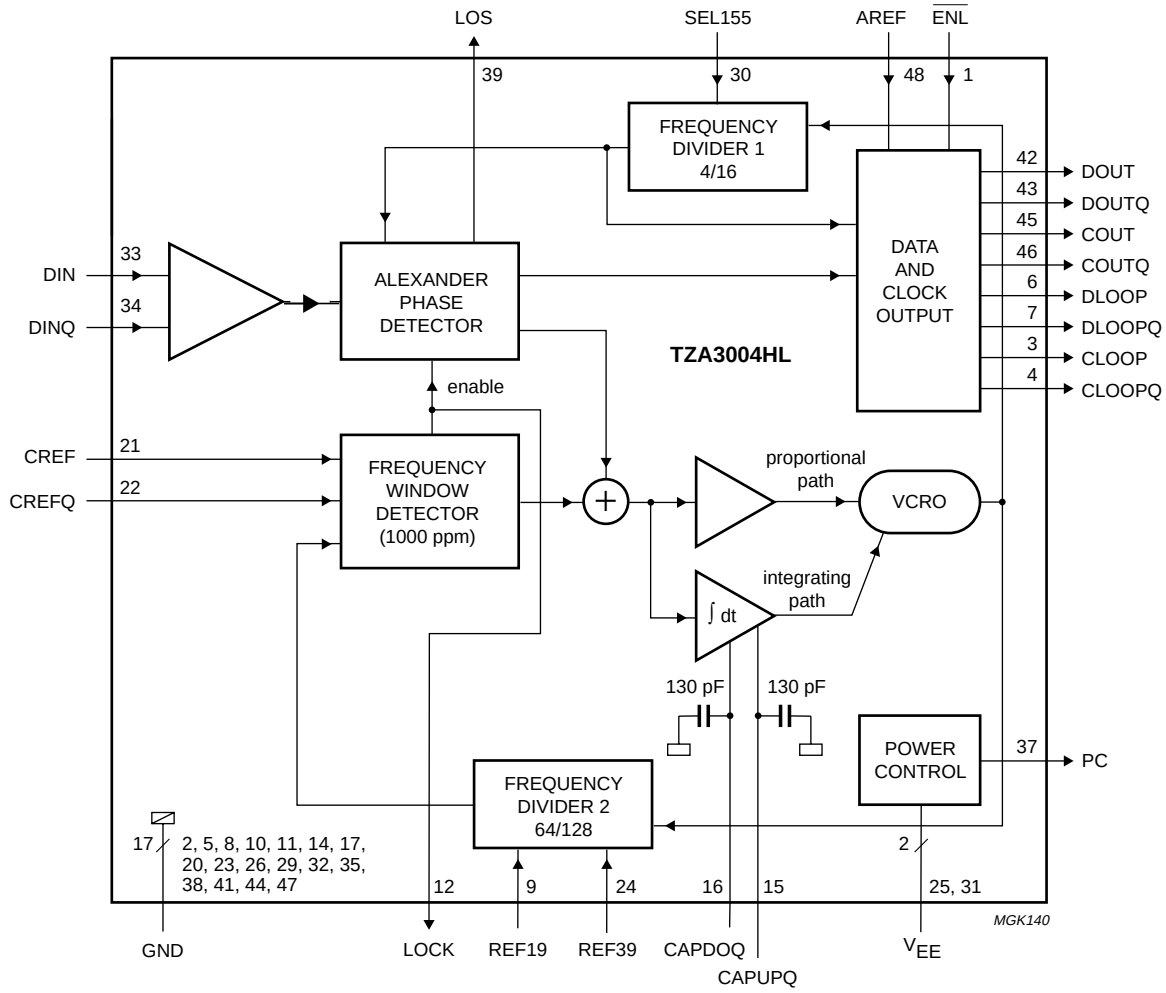


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{ENL}$	1	loop mode enable input (active low)
GND	2	ground
CLOOP	3	clock output in loop mode (differential)
CLOOPQ	4	inverted clock output in loop mode (differential)
GND	5	ground
DLOOP	6	data output in loop mode (differential)
DLOOPQ	7	inverted data output in loop mode (differential)
GND	8	ground
REF19	9	reference frequency select input (see Table 2)
GND	10	ground
GND	11	ground
LOCK	12	phase lock detection output
i.c	13	internally connected (leave open)
GND	14	ground
CAPUPQ	15	external loop filter capacitor
CAPDOQ	16	external loop filter capacitor return
GND	17	ground
i.c.	18	internally connected (leave open)
i.c.	19	internally connected (leave open)
GND	20	ground
CREF	21	reference clock input (differential)
CREFQ	22	inverting reference clock input (differential)
GND	23	ground
REF39	24	reference frequency select input (see Table 2)
V_{EE}	25	negative supply voltage
GND	26	ground
V_{EE}	27	negative supply voltage
V_{EE}	28	negative supply voltage
GND	29	ground
SEL155	30	STM mode select input (see Table 1)
V_{EE}	31	negative supply voltage
GND	32	ground
DIN	33	data input (differential)
DINQ	34	inverting data input (differential)
GND	35	ground
i.c.	36	internally connected (leave open)
PC	37	negative power supply control signal output
GND	38	ground
LOS	39	loss-of-signal detection output
i.c.	40	internally connected (leave open)

SYMBOL	PIN	DESCRIPTION
GND	41	ground
DOUT	42	data output in normal mode (differential)
DOUTQ	43	inverted data output in normal mode (differential)
GND	44	ground
COUT	45	clock output in normal mode (differential)
COUTQ	46	inverted clock output in normal mode (differential)
GND	47	ground
AREF	48	reference voltage input for controlling voltage swing on data and clock outputs

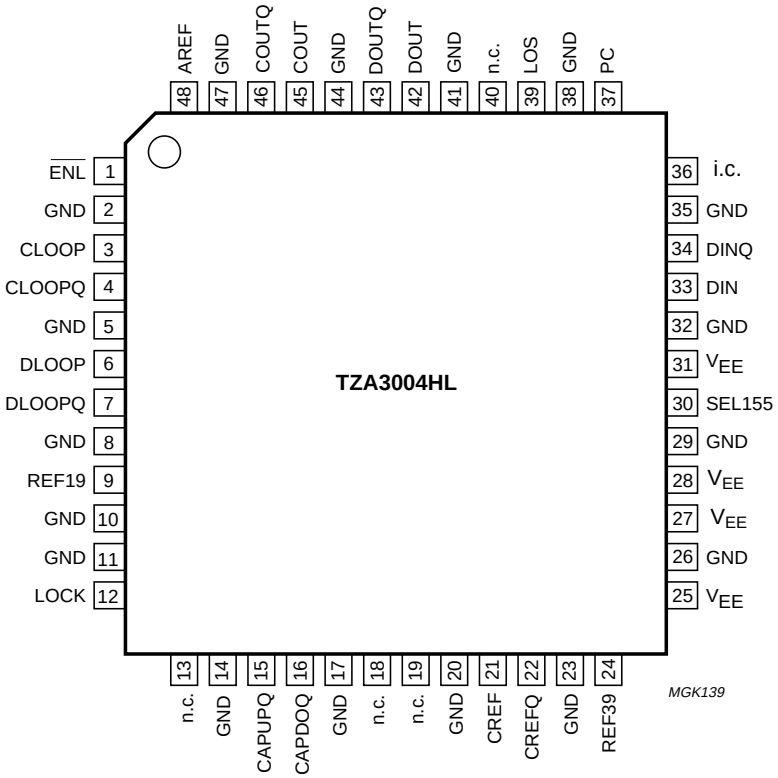


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TZA3004HL recovers data and clock signals from an incoming high speed bitstream. The input signal on DIN, DINQ is buffered and amplified by the input circuitry.

The signal is then fed to the Alexander phase detector where the phase of the incoming data is compared with that of the internal clock. If the signals are out of phase, the phase detector generates (UP or DOWN) correction pulses that shift the phase of the VCRO (Voltage Controlled Ring Oscillator) output in discrete amounts, $\Delta\varphi$, until the clock and data signals are in phase.
The technique used is based on principles first proposed by J.D.H. Alexander, hence the phase detector's name.

The eye pattern of the incoming data is sampled at three instants **A**, **T** and **B** (see Fig.3). When clock and data signals are synchronized (locked), A is in the centre of the data bit, T is in the vicinity of the next transition, and B is in the centre of the bit following the transition. If the same level is recorded at both A and B, a transition has not occurred and no action is taken regardless of the value at T. If A and B are different, however, a transition has occurred and the phase detector uses the value at T to determine whether the clock was too early or too late with respect to the data transition. If A and T are the same, but different from B, the clock was too early and needs to be slowed down a little. The Alexander phase detector then generates a DOWN pulse which stretches a single output pulse from the ring oscillator by approximately 0.25% (or 4 ps in STM4 mode; 4 ps is 0.25% of the 1.608 ns bit period). This forces the VCRO to run at a slightly lower frequency for one bit period. The phase of the clock is thus shifted fractionally with respect to the data.

If, on the other hand, B and T are the same but different from A, the clock was too late and needs to be speeded up for synchronization. The phase detector generates an UP pulse forcing the VCRO to run at a slightly higher frequency (+0.25%) for one bit period. The phase of the clock is shifted with respect to the data (as above, but in the opposite direction). Only the proportional path is active while these phase adjustments are being made. Because the instantaneous frequency of the VCRO can be changed only in one of two discrete steps (±0.25%), this type of loop is also known as a Bang/Bang PLL.

If not only the phase but also the frequency of the VCRO is incorrect, a long train of UP or DOWN pulses will be generated. This pulse train is integrated to generate a control voltage that is used to shift the centre frequency of the VCRO. Once the correct frequency has been established, the phase will need to be adjusted for synchronization. The proportional path adjusts the phase of the clock signal, while the integrating path adjusts the centre frequency.

The frequency window detector checks that the VCRO frequency is within a 1000 ppm (parts per million) window around the required frequency. It compares the output of frequency divider 2 with the reference frequency at CREF, CREFQ (19.44 MHz or 38.88 MHz as available; see Table 2). If the VCRO frequency is found to be outside this window, the frequency window detector disables the Alexander phase detector and forces the VCRO output to a frequency within the window. The phase detector then starts acquiring lock again. Because of the loose coupling (1000 ppm), the reference frequency doesn't need to be highly accurate or stable. Any crystal based oscillator that generates a reasonably accurate frequency (e.g. 100ppm))will do.

Since sampling point A is always in the centre of the eye pattern when the data and clock signals are in phase (locked), the values recorded at this point are taken as the retrieved data. The data and clock signals are available at the CML output buffers, which are capable of driving a 50 Ω load.

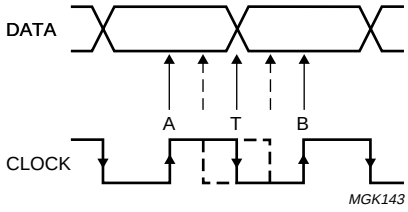


Fig.3 Data sampling.

Power Control (PC)

The TZA3004HL contains an on-board voltage regulator. An external power transistor is needed to deliver supply current, I_{EE}, to this circuit. The required external circuit is straightforward, and can be built using a few components. A suitable circuit is depicted in Fig.4. A different configuration could be used, as long as the power supply rejection ratio is greater than 60 dB for all frequencies. The inductor is a (lossy) 1 μH RF-choke (EMI) with an impedance greater than 50 Ω at frequencies higher than 2 MHz. Any transistor with a $\beta > 100$ and enough current sink capability can be used.

The TZA3004HL can also be used with a -5V or -5.2V supply voltage. The only adaption that has to be made to the Power Control circuit is resistor R of 2Ω. This should be 6.8Ω with a -5V supply and 8.2Ω with a -5.2V supply.

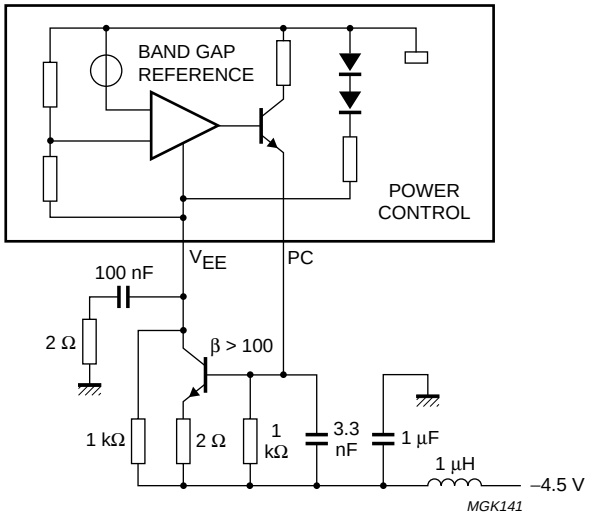


Fig.4 Schematic diagram of TZA3004HL power control loop.

Output amplitude reference (AREF)

The voltage swing at the CML compatible output stages DOUT, DOUTQ; COUT, COUTQ; DLOOP, DLOOPQ and CLOOP, CLOOPQ can be controlled by adjusting the voltage at the AREF pin. An internal voltage divider of 500 Ω and16 kΩ between GND and V_{EE} initially fixes this level.

In most applications the outputs will be DC coupled to a load, which can be as low as 50 Ω (±0.20%). The output level regulation circuit will maintain a 200 mV peak-to-peak single-ended swing across this load. The voltage at AREF is half the single-ended peak-to-peak value of the output signal (or –100 mV in this case). No adjustments are necessary with DC coupling.

If the outputs are AC coupled, however, the voltage at AREF is half the single-ended peak-to-peak value of the output signal multiplied by a factor $\frac{R_L + R_o}{R_L}$

where R_L is the external load and R_o is the output impedance of the TZA3004HL.

To maintain a 200 mV peak-to-peak single-ended swing across a 50 Ω AC coupled load, the voltage at AREF must be $\frac{-100\ \text{mV} \times (50\ \Omega + 100\ \Omega)}{50\ \Omega} = -300\ \text{mV}$.

This can be achieved by connecting a 7.3 kΩ resistor between AREF and V_{EE}.

The formulae for calculating the required voltage at AREF and the external resistance needed between AREF and V_{EE} when the outputs are AC coupled are:

$$V_{AREF} = -\frac{R_L + R_o}{R_L} \times \frac{1}{2} V_{swing} \quad (1)$$

and:

$$R_{AREF} = \frac{R1 \times \left(\frac{V_{EE}}{V_{AREF}} - 1 \right)}{1 - \left(\frac{R1}{R2} \times \left(\frac{V_{EE}}{V_{AREF}} - 1 \right) \right)} \quad (2)$$

where R1 = 500 Ω, R2 = 16 kΩ and V_{EE} = –3.3 V. R_{AREF} is connected between AREF and V_{EE}.

Loop mode enable ($\overline{ENL}$)

Loop mode is provided for system testing. Loop mode is enabled by applying a voltage lower than 0.8 V (TTL LOW) to the $\overline{ENL}$ pin. This selects loop mode outputs DLOOP, DLOOPQ and CLOOP, CLOOPQ. If a voltage greater than 2.0 V (TTL HIGH) is applied to $\overline{ENL}$, then DOUT, DOUTQ and COUT, COUTQ are switched in while DLOOP, DLOOPQ and CLOOP, CLOOPQ are disabled to minimize power consumption. If $\overline{ENL}$ is connected to V_{EE} (–3.3 V), all outputs are enabled.

External capacitor for loop filter (CAPUPQ; CAPDOQ)

The loop filter is an integrator with a built in capacitance of 2×130 pF. An external 200 nF capacitance must be connected between CAPUPQ and CAPDOQ to ensure loop stability while the frequency window detector is active.

Lock detection (LOCK)

The LOCK pin should be interpreted as an indication if the reference clock (CREF) is present and if the acquisition aid (frequency window detector) is working properly. The LOCK pin is an open collector TTL output and should be pulled up with a 10kΩ resistor to the positive supply. If the VCO frequency is within a 1000 ppm window around the desired frequency the LOCK pin will go HIGH. If no reference clock is present, or the VCO is outside the 1000 ppm window, the LOCK pin will be LOW. The logic level of LOCK does not indicate if the PLL is locked onto the incoming data; this is indicated by the LOS signal.

STM mode selection (SEL155)

SEL155 should be connected to V_{EE} for STM1/OC3 (155.52 Mbits/s) operation. For STM4/OC12 (622.08 Mbits/s) systems, SEL155 should be connected to GND. The connections to V_{EE} and GND should have low resistance and inductance. Short PCB tracks are recommended.

Table 1 STM Mode Select

MODE	BIT RATE Mbits/s	DIV #	SEL155
STM1	155.52	16	V_{EE}
STM4	622.08	4	GND

Loss-of-signal detection (LOS)

The Loss of Signal (LOS) function is closely related to the Alexander Phase Detector functionality. Refer to Fig.3 for the meaning of A,B and T in this section.

In the functional description it is described that the phase detector doesn't take any action if the value at sample points A and B is the same, because there hasn't been any transition. However, if the values at A and B are the same, but different from T, this still means there hasn't been any transition, but somehow T got the wrong value. This is probably due to noise or bad signal integrity, which will lead to a Bit Error. Hence the occurrence of this particular situation is an indication for Bit Errors. If too many of these Bit Errors occur per time and the PLL is gradually losing lock, the LOS alarm is asserted. The LOS assert level is around a Bit Error Rate (BER) of $5 \cdot 10^{-2}$ and the de-assert level is around BER of $1 \cdot 10^{-3}$.

The LOS detection is BER related, but neither dependent of datastream content, nor protocol. Therefore, a SDH/SONET datastream is no prerequisite for a proper LOS function. Since the LOS function of the TZA3004HL is derived from digital signals, it is a good supplement to an analog, amplitude based, LOS indication.

The LOS alarm is an open collector TTL compatible output. A pull-up resistor should be connected to a positive supply. LOS will be HIGH (TTL) if the data signal is absent at DIN, DINQ or BER is $> 5 \cdot 10^{-2}$, otherwise it will be LOW (BER $< 1 \cdot 10^{-3}$).

Reference frequency select (REF19, REF39)

A reference clock signal (either 19.44 MHz or 38.88 MHz, whichever is available) must be connected to CREF and CREFQ. Pins REF19 and REF39 are used to select the appropriate output frequency at frequency divider 2. Since the reference clock is only used as acquisition aid for the PLL (Frequency Window Detector), the quality of the reference clock is not important. There is no phase noise specification imposed on the reference clock generator and even frequency stability may be in the order of 100 ppm. In general most inexpensive crystal based oscillators are suitable.

Table 2 Reference Frequency Select

FREQUENCY MHz	DIV #	REF19	REF39
38.88	64	V_{EE}	V_{EE}
19.44	128	GND	V_{EE}

POSITIVE SUPPLY APPLICATION

Due to the versatile design of the TZA3004HL, the device can also operate in a positive supply application, although some pins have a different mode of operation. This section deals with these differences and supports the user with successful application of the TZA3004HL in a +5V environment. A sample application diagram can be found in figure 4. Note that all GND pins are now connected to VCC. All VEE pins are not connected to ground, but to pin 25, the regulated voltage from the power controller.

Loop mode and normal mode output select ($\overline{ENL}$)

In a positive supply application, the default RF output will be the LOOP MODE outputs. Due to the decoding logic at the $\overline{ENL}$ pin, it is only possible to select the pins DLOOP(Q) and CLOOP(Q) as outputs or enable **all** outputs. If $\overline{ENL}$ is connected to VCC (+5V), the LOOP MODE outputs are active. All outputs become active If $\overline{ENL}$ is connected to pin VEE (the voltage on pin 25 is approximately 3.3V below VCC). Beware not to connect $\overline{ENL}$ to ground, this would destroy the IC. In the positive supply application the NORMAL MODE outputs can not be selected anymore.

Loss of signal detect and Lock detect (LOS & LOCK)

In the negative supply application, LOS and LOCK are open collector outputs, that require pull-up resistors to a positive supply. In the positive supply application, the pull-up voltage would be higher then the positive supply and the LOS and LOCK signals would not be TTL compatible. The internal circuit at pins LOS and LOCK can however be used in a current mirror configuration. It requires only an external PNP transistor, BC857 or equivalent, to mirror the current. A 10kΩ pull-down resistor to ground yields a TTL compatible signal again, albeit inverted. The table below shows the meaning of the LOS and LOCK flag, when used according to the application schematic of figure 4.

Table 3 LOS and LOCK indication for positive supply

SIGNAL	DESCRIPTION	LEVEL	TTL
LOS active	Loss-of-signal; BER >5 10^{-2}	0V (ground)	LOW
LOS inactive	No loss-of-signal; BER < 1 10^{-3}	+5V (VCC)	HIGH
LOCK active	Reference clock present and VCO in 1000 ppm window	0V (ground)	LOW
LOCK inactive	No reference clock present or VCO outside 1000 ppm window	+5V (VCC)	HIGH

Divider settings

The reference frequency dividers and the STM mode selectors still operate the same in a positive supply application. The only difference is that pins formerly connected to GND (ground) should now be connected to VCC (+5V), whereas pins connected to VEE still should be connected to pin VEE (pin 25). Connection to ground (0V) will damage the IC.

RF input/outputs

All RF inputs, outputs and internal signals of the TZA3004HL are referenced to the most positive supply, pins GND. In the positive supply application, this means all RF signals are referenced to VCC. Therefore a clean VCC rail is of ultimate importance for proper RF performance. The best performance is obtained when the transmission line reference plane is also decoupled to the VCC. Careful design of VCC and good decoupling schemes should be taken into account. While designing the printed circuit board, bear in mind that the VCC has become what was formerly ground.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{EE}	negative supply voltage	–6	+0.5	V
V_n	DC voltages			
	pins 3, 4, 6, 7, 21, 22, 33, 34, 42, 43, 45, 46	–1	+0.5	V
	pins 1, 12, 39	V_{EE} – 0.5	+5.5	V
	pins 9, 24, 30, 37, 48	V_{EE} – 0.5	+0.5	V
	pins 15, 16	V_{EE} + 0.5	–0.5	V
I_n	input current			
	pin 1	–	1	mA
	pins 21, 22, 33, 34	–20	+10	mA
P_{tot}	total power dissipation	–	700	mW
T_{amb}	ambient temperature	–40	+85	°C
T_j	junction temperature	–40	+110	°C
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-s)}$	thermal resistance from junction to solder point		46	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	67	K/W

Note

1. Thermal resistance from junction to ambient is determined with the IC soldered on a standard single sided 57x57x1.6mm FR4 epoxy PCB with 35µm thick copper traces. The measurements are performed in free air.

CHARACTERISTICS

External supply voltage = –4.5 V; T_{amb} = -40°C to +85°C; Typical values at T_{amb}=25°C; all voltages referenced to GND.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EE}	negative supply voltage	note 1	–3.50	–3.30	–3.10	V
I_{EE}	negative supply current	open outputs	–	112	155	mA
P	power dissipation		–	370	550	mW
Data and Clock inputs: DIN, DINQ and CREF, CREFQ						
$V_{i(p-p)}$	input voltage (peak-to-peak) (2)(3)	50 Ω measurement system	7	200	450	mV
$V_{sens(p-p)}$	input sensitivity (peak-to-peak) (2)(4)		–	2.5	7	mV
VIO	input offset voltage		–3	0	+3	mV
V_I, V_{IQ}	input voltages		–600	–200	+250	mV
Z_i	single ended input impedance(2)		–	50	–	Ω
Data and Clock outputs: DOUT, DOUTQ; DLOOP, DLOOPQ; COUT, COUTQ and CLOOP, CLOOPQ						
$V_{o(p-p)}$	voltage swing (single ended)(6)	50 Ω measurement system	170	200	210	mV
	voltage swing (single ended) (7)		50	–	400	mV
V_O, V_{OQ}	output voltages		–600	–	0	mV
Z_o	single ended output impedance		–	100	–	Ω
t_r, t_f	rise/fall time	differential				
	data outputs		–	116	–	ps
	clock outputs		–	54	–	ps
t_d	data to clock delay	note 8	50	80	110	ps
Output amplitude adjustment: AREF						
V_{AREF}	output amplitude reference voltage	floating pin	–110	–100	–90	mV
Power Control output: PC						
g_m	transconductance		–84	–60	–42	mA/V
I_O	output current		1	–	3.5	mA
Loop mode enable input: $\overline{\text{ENL}}$						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
Phase lock and loss-of-signal indicators: LOCK and LOS						
V_{OL}	HIGH-level output voltage	note 9	–0.6	–	–	V
V_{OH}	LOW-level output voltage	note 9	–	–	3.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_a	LOS assert time	note 10	–	0.1	–	µs
t_d	LOS de-assert time		–	10	–	µs
BER_{LOS}	LOS assert Bit Error Rate		–	$5 \cdot 10^{-2}$	–	BER
	LOS de-assert Bit Error Rate		–	$1 \cdot 10^{-3}$	–	BER
PLL Characteristics						
t_{acq}	acquisition time	CREF = 19.44 MHz	–	50	200	µs
		CREF = 38.88 MHz	–	100	200	µs
$J_{tol(p-p)}$(5)	jitter tolerance (peak-to-peak)	STM1/OC3 mode				
		f = 6.5 kHz	1.5	>5	–	UI
		f = 65 kHz	0.15	1.3	–	UI
		f = 1 MHz	0.15	0.8	–	UI
		STM4/OC12 mode				
		f = 25 kHz	1.5	>5	–	UI
		f = 100 kHz	0.7	3	–	UI
		f = 250 kHz	0.15	1.3	–	UI
		f = 1 MHz	0.15	0.50	–	UI
		f = 5 MHz	0.15	0.35	–	UI
TDR	transitionless data run	note 6	–	2000	–	bits

Notes

1. Typical supply voltage for the voltage regulator is –4.5 V (see Fig.4).
2. It is assumed that both CML inputs carry a complementary signal with the specified peak-to-peak value. (true differential excitation)
3. The specified input voltage range is the guaranteed and tested range for proper operation; BER $<10^{-10}$.
4. An input sensitivity for BER $<10^{-10}$ of 7 mVpp is guaranteed. Typical input sensitivity for BER $<10^{-10}$ is 2.5mVpp.
5. CML inputs are terminated internally using 50 Ω on-chip resistors to ground (GND).
6. Output voltage range with default reference voltage on AREF (floating pin).
7. Output voltage range with adjustment of voltage on AREF (see section “Output amplitude reference (AREF)”).
8. Data to clock delay according to figure 7. Measured with 1010 data pattern, single ended output signals and rising edge of COUT to DOUT or CLOOP to DLOOP. Note that small deviations from specified value are possible if differentially measured.
9. External 10 kΩ pull-up resistor to +3.3 V.
10. LOS assert/de-assert timing and BER level are for indication only. The values are neither production tested nor guaranteed.
11. Measured according ITU specification G.958 on the OM5800 STM4 demoboard.
12. TDR is bitrate independent.

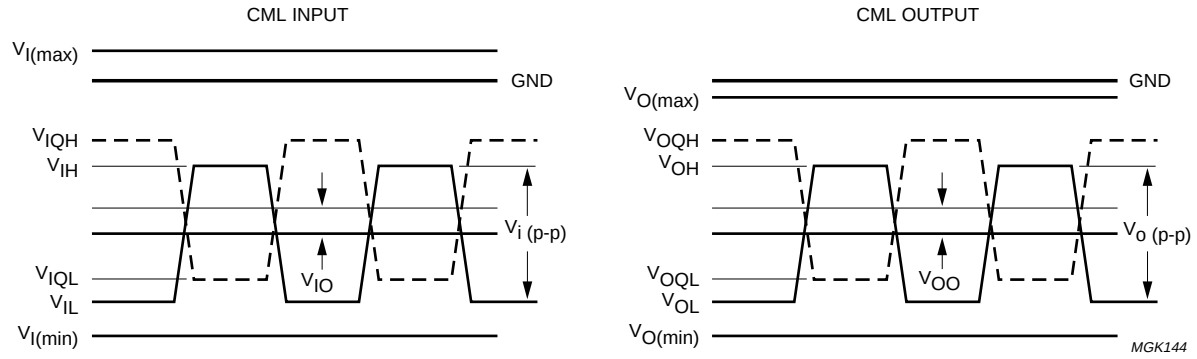


Fig.5 Logic level symbol definitions for CML.

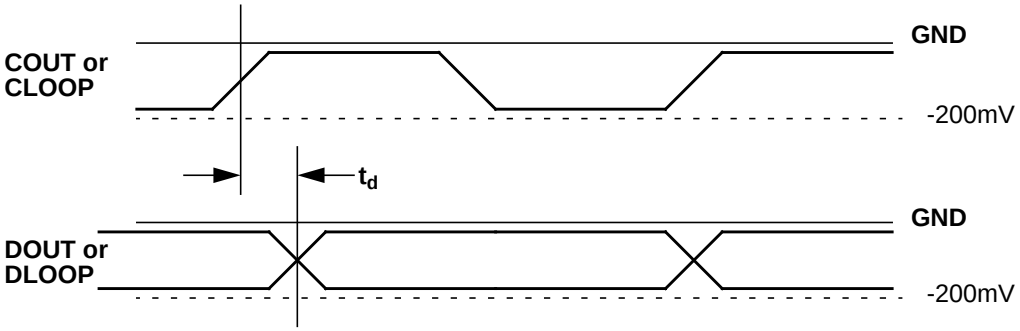


Fig.6 Data to clock delay for CML outputs; COUT to DOUT or CLOOP to DLOOP.

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

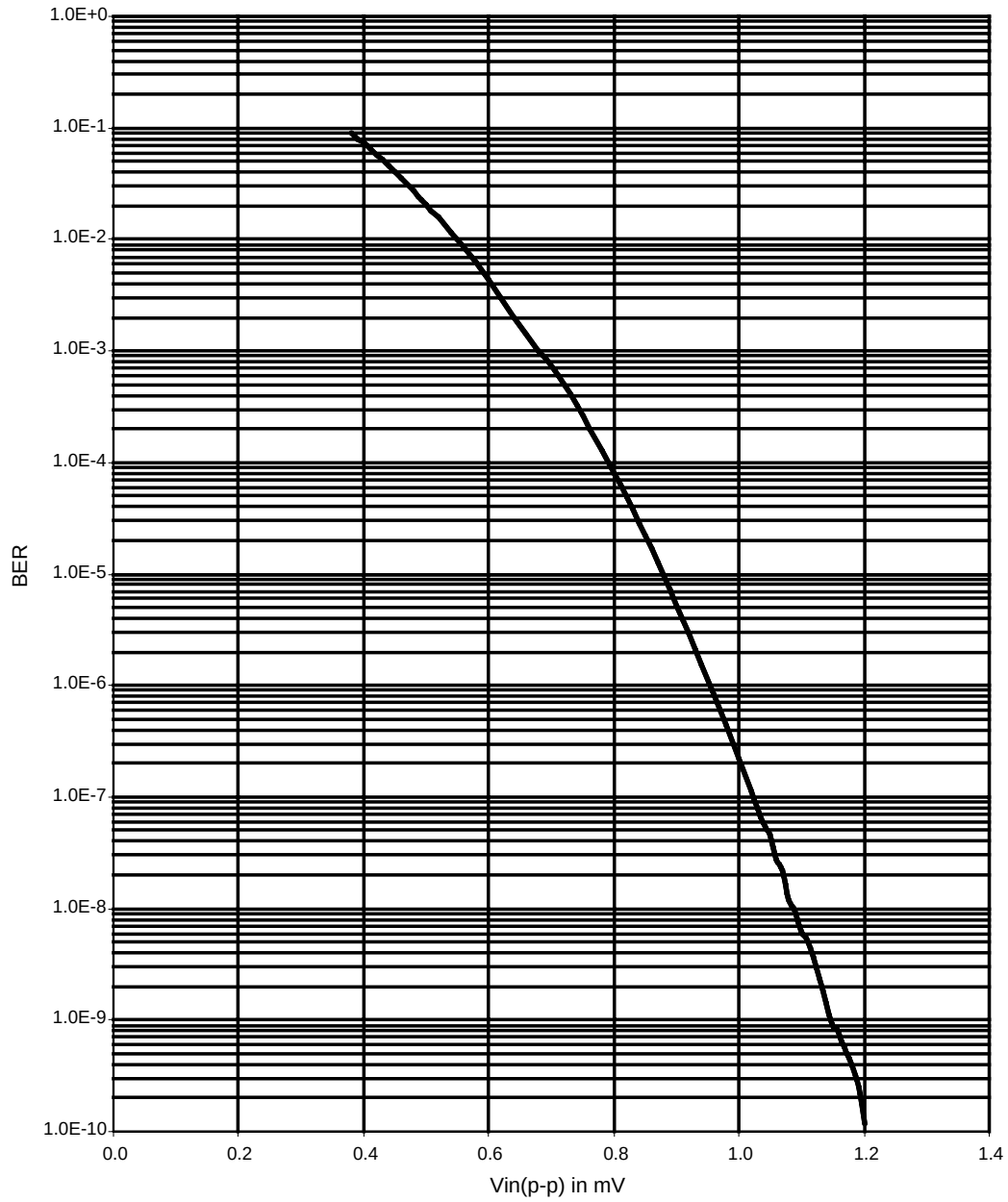


Fig.7 Bit Error Rate versus input signal on DI/DIQ in STM1 mode(155.52 Mbits/s).
(A complementary input signal of the indicated value is applied to DI and DIQ).

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

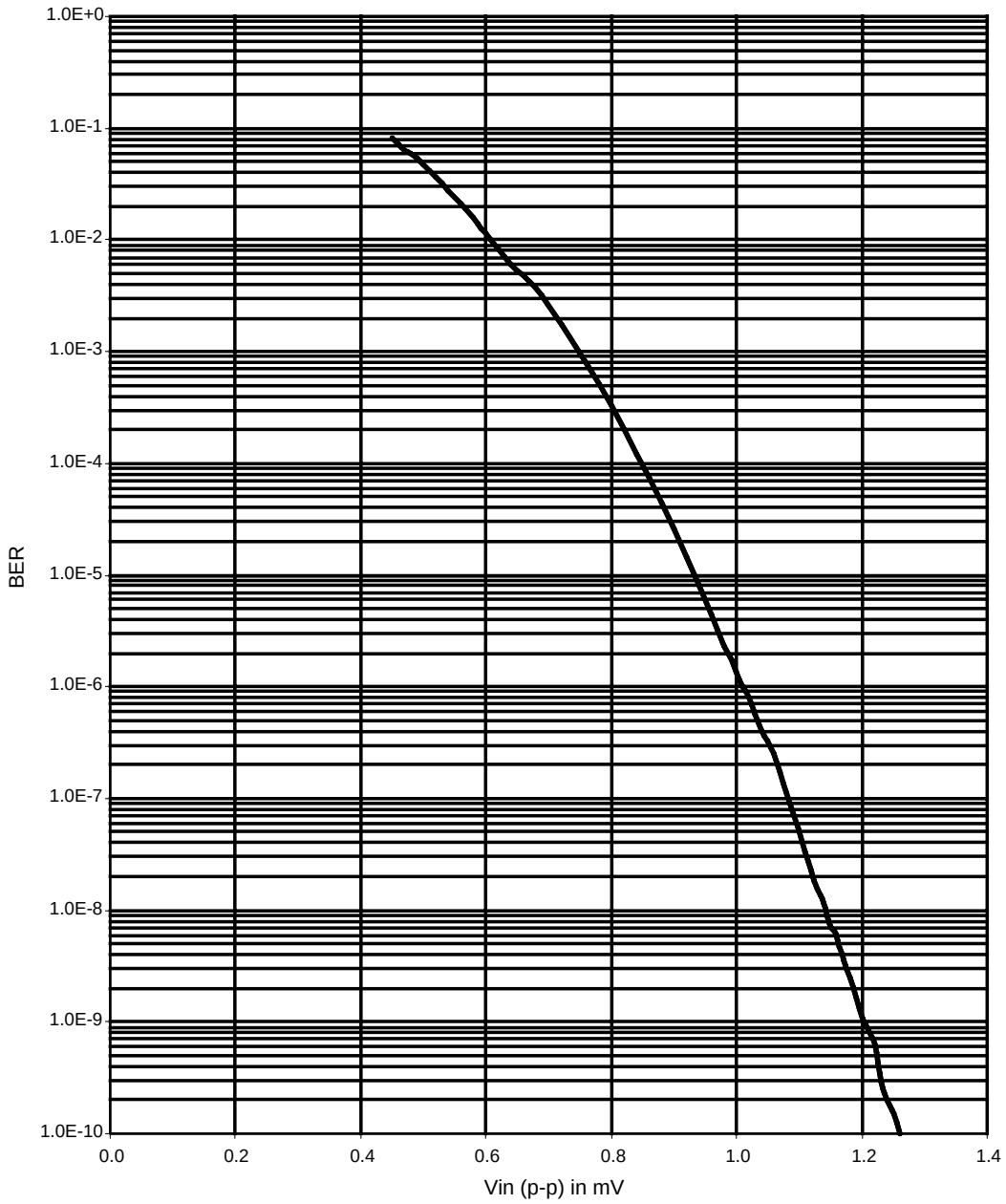


Fig.8 Bit Error Rate versus input signal on DI/DIQ in STM4 mode (622.08 Mbits/s).
(A complementary input signal of the indicated value is applied to DI and DIQ..

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

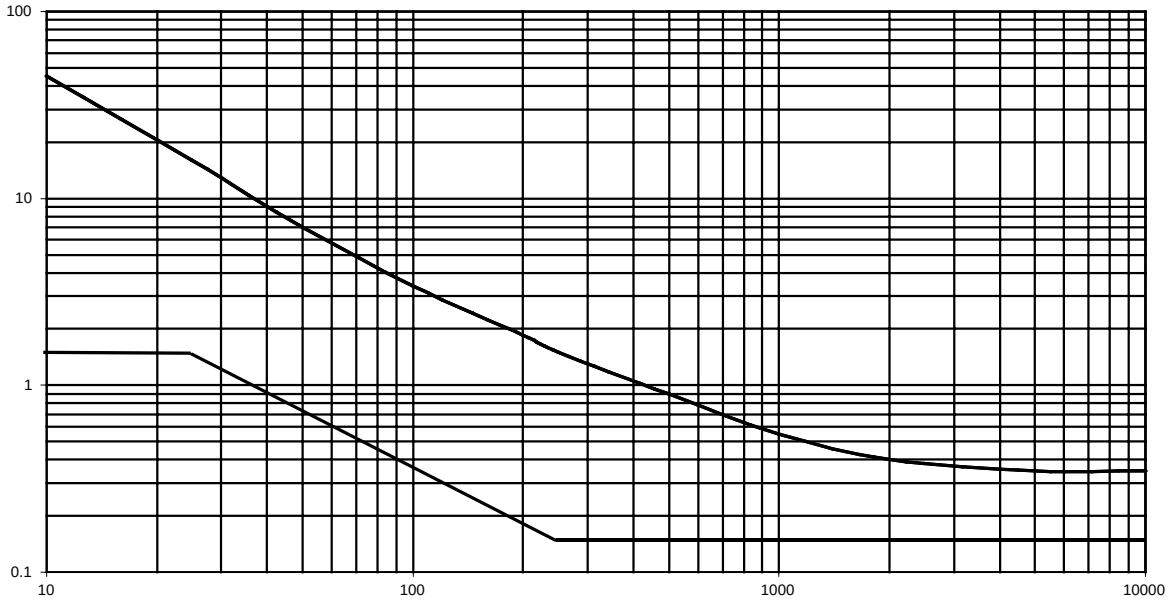


Fig.9 Jitter Tolerance in STM4 mode (622.08 Mbits/s). Measured on OM5800 demoboard

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

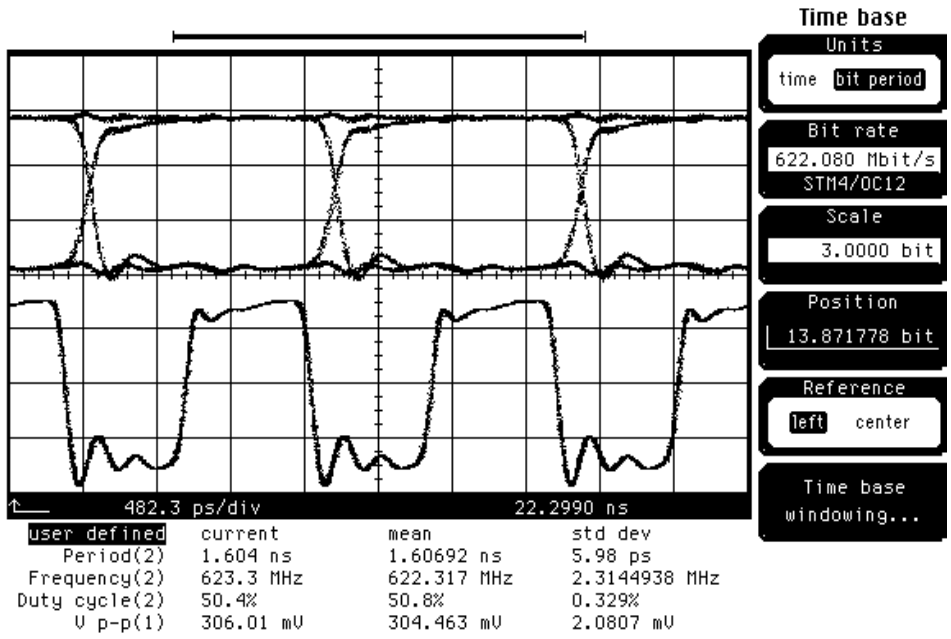
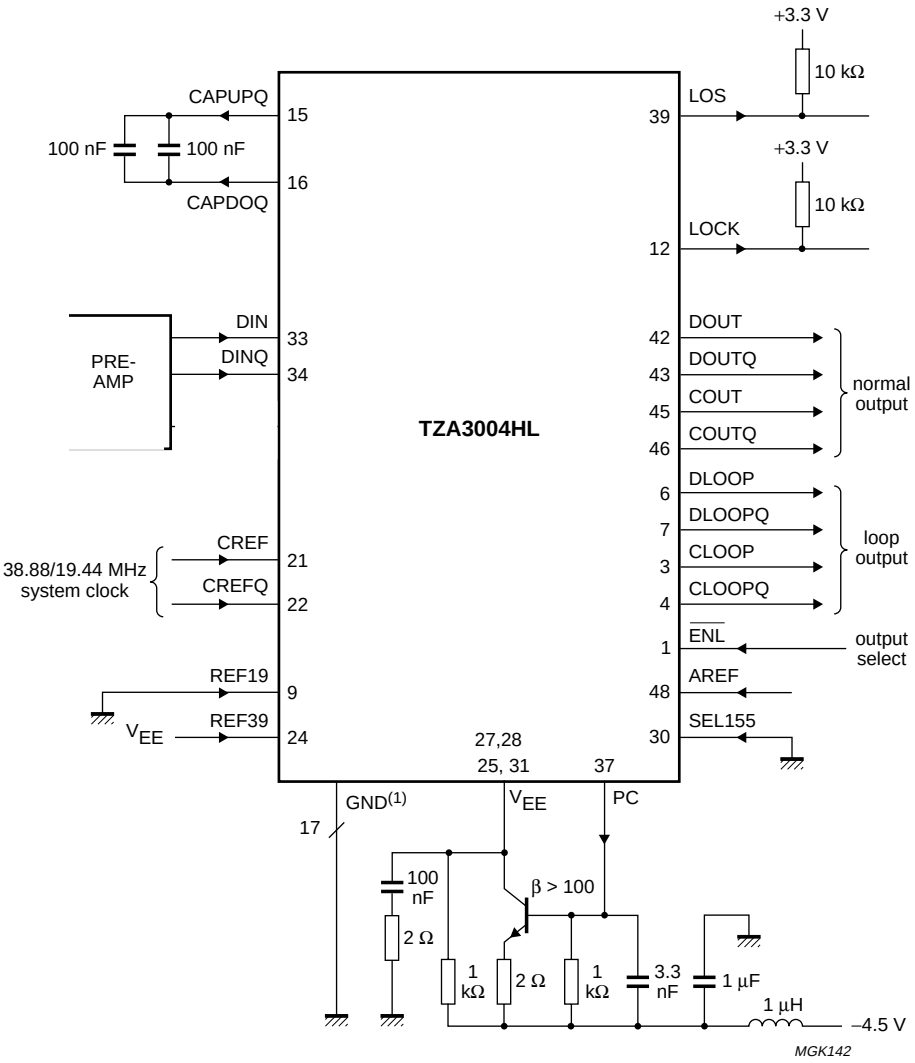


Fig.10 Output waveforms on Data and Clock outputs in STM4 mode (622.08 Mbits/s). (single ended)

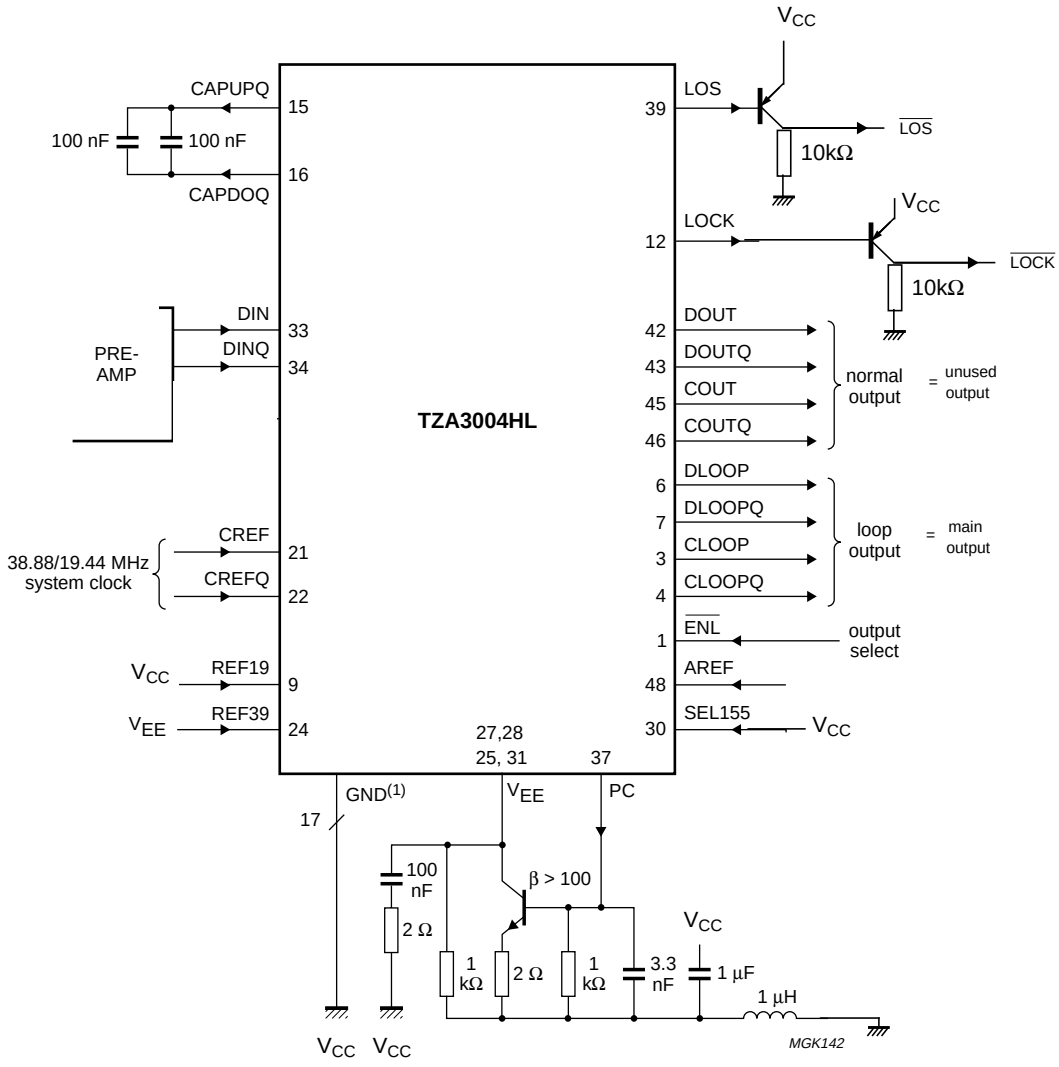
APPLICATION SCHEMATIC



(1) All GND pins must be connected directly to the PCB ground plane (pins 2, 5, 8, 10, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44 and 47).

Fig.11 Application diagram showing the TZA3004HL configured for 622.08 Mbits/s DCR mode (STM4/OC12).

APPLICATION INFORMATION (POSITIVE SUPPLY)

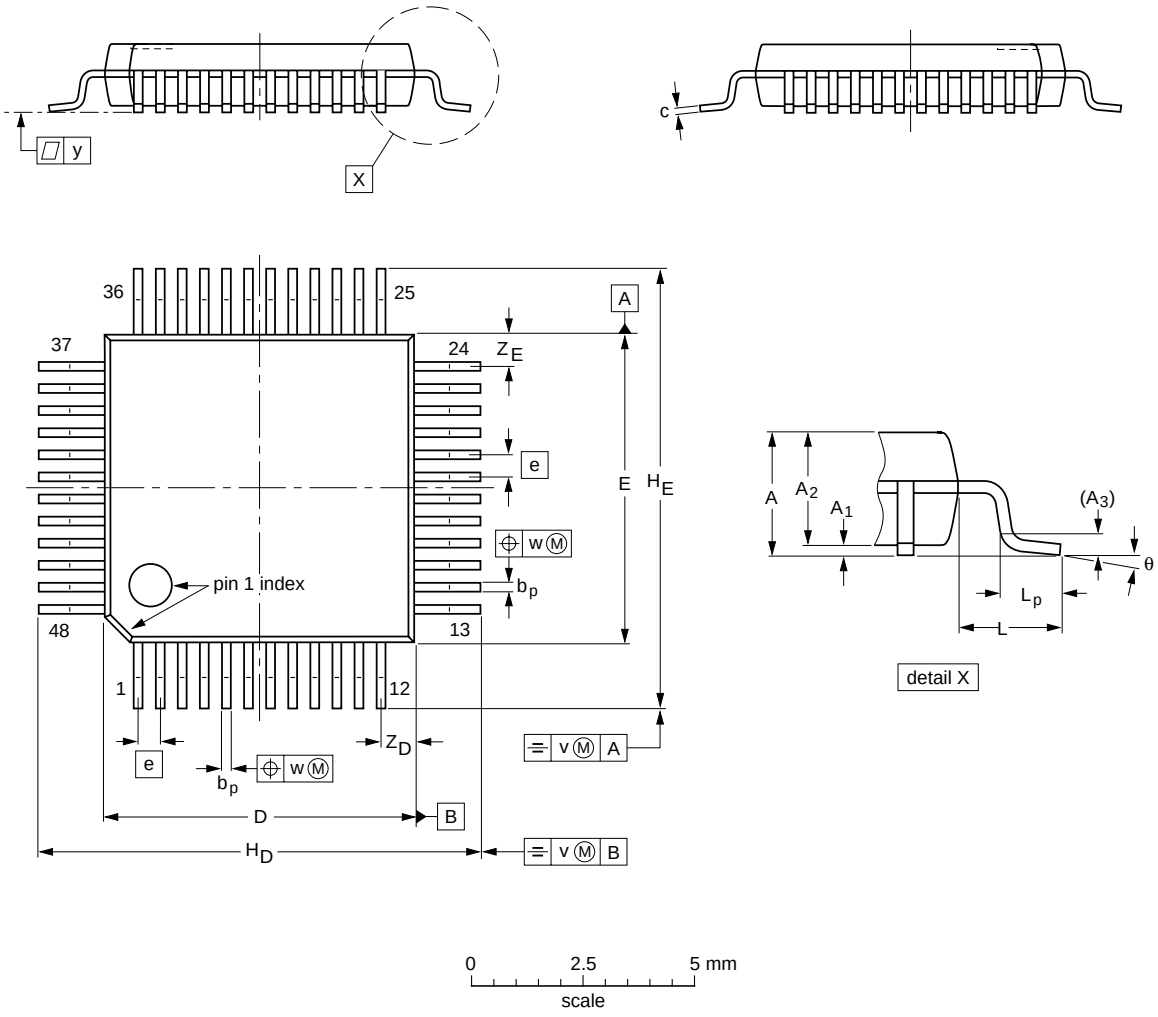


(1) All GND pins must be connected directly to the PCB +5V (VCC) plane (pins 2, 5, 8, 10, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44 and 47).

Fig.12 Application diagram showing the TZA3004HL configured for 622.08 Mbits/s positive supply application. Note that loopmode outputs are used as outputs. $\overline{ENL}$=HIGH selects these outputs. $\overline{ENL}$=LOW selects loopmode and normal mode outputs simultaneously.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~94-12-19~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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