

Structure Silicon Monolithic Integrated Circuit

Product Name 16bit D/A Converter + Audio Path

Type **BU7858KN**

Features stereo 16-bit DAC, internal stereo headphone output function  
Multi Output/Input system, Include multi mixing function

○Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit	Condition
Supply Voltage	VDD	-0.3 to 4.5	V	
Input Voltage	VIN	DVSS-0.3 to DVDD+0.3 AVSS-0.3 to AVDD+0.3	V	
Input Current	IIN	-1 to 1	mA	
Power Dissipation	Pd	580(*1)	mW	
Storage Temperature Range	Tstg	-55 to 125	°C	
Operation Temperature Range	Topr	-20 to 85	°C	

(\*1) To use at a temperature higher than Ta=25 °C, delete 5.8mW/°C  
This value is the package on ROHM standard board.

○Recommended operating conditions (Ta=-20 to 85 °C)

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Supply Voltage	VDD	2.7	3.0	3.3	V	

This product isn't designed to protect itself against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification.  
A customer may use this translation version only for a reference to help reading the formal version.  
If there are any differences in translation version of this document, formal version takes priority.

Application example

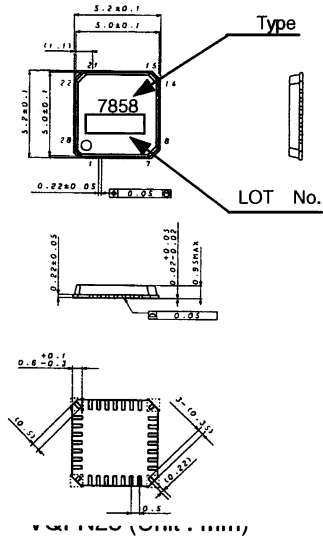
The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).  
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## ○Electrical Characteristics

Unless otherwise specified, Ta=25 °C, AVDD=DVDD=3.0V, f=1kHz, VIN=-10dBV, fs=44.1kHz, BCLK=64fs, BW=10Hz to 20kHz

Parameter	Symbol	Rating			Unit	Conditions
		MIN	TYP	MAX		
<b>Circuit Current</b>						
Stand-by current	Istb	-	-	3	μA	stand-by mode
Operation current 1	Idd1	-	5.85	9.4	mA	DAC part, No signal
<b>16Bit DAC</b>						
S/(N+D)	SN+D	-	85	-	dB	-0.5dB input
D-Range	DR	-	92	-	dB	-60dB input, A-weighted
S/N	SNR	-	92	-	dB	0dB input, A-weighted
<b>ATT1</b>						
Number of volume steps	Stg1	-	2	-	dB	
Muting level	Mut1	-	-95	-80	dB	At mute setting
<b>ATT2</b>						
Number of volume steps	Stg2	-	2	-	dB	
Muting level	Mut2	-	-95	-80	dB	At mute setting
<b>ATT3</b>						
Number of volume steps	Stg3	-	2	-	dB	
Muting level	Mut1	-	-95	-80	dB	At mute setting
<b>ATT4</b>						
Number of volume steps	Stg4	-	2	-	dB	
Muting level	Mut4	-	-95	-80	dB	At mute setting
<b>ATT5</b>						
Number of volume steps	Stg5	-	2	-	dB	
Muting level	Mut5	-	-95	-80	dB	At mute setting
<b>Headphone AMP</b>						
Total Harmonic Distortion	THDhp	-	0.05	0.5	%	VO=-10dBV 20kHz LPF
Output Power	PO	-	10	-	mW	THD=10%, RL=16Ω
Output Noise Voltage	VNO	-	-94	-80	dBV	JIS A weighting
<b>SPO</b>						
Maximum Output Level 1	VOMAX1	2.0	-	-	V <sub>P-P</sub>	1kHz, 10kΩLoad, THD≤1%
<b>EXTO</b>						
Maximum Output Level 2	VOMAX2	2.0	-	-	V <sub>P-P</sub>	1kHz, 600ΩLoad, THD≤1%
<b>Digital Input Operation</b>						
MCLKI Frequency	fMCLK	4.096	-	18.432	MHz	
LRCLK Frequency	fs	16.0	-	48	kHz	
Digital Input Voltage "L"	VIL	-	-	0.2 x DVDD	V	
Digital Input Voltage "H"	VIH	0.8 x DVDD	-	-	V	
Digital Output Voltage "L"	VOL	-	-	0.5	V	Iol=-500μA
Digital Output Voltage "H"	VOH	DVDD -0.5	-	-	V	Ioh=500μA
Input Leak Current 1	IIN1	-	-	±2	μA	0V, 3V Force

External dimensions

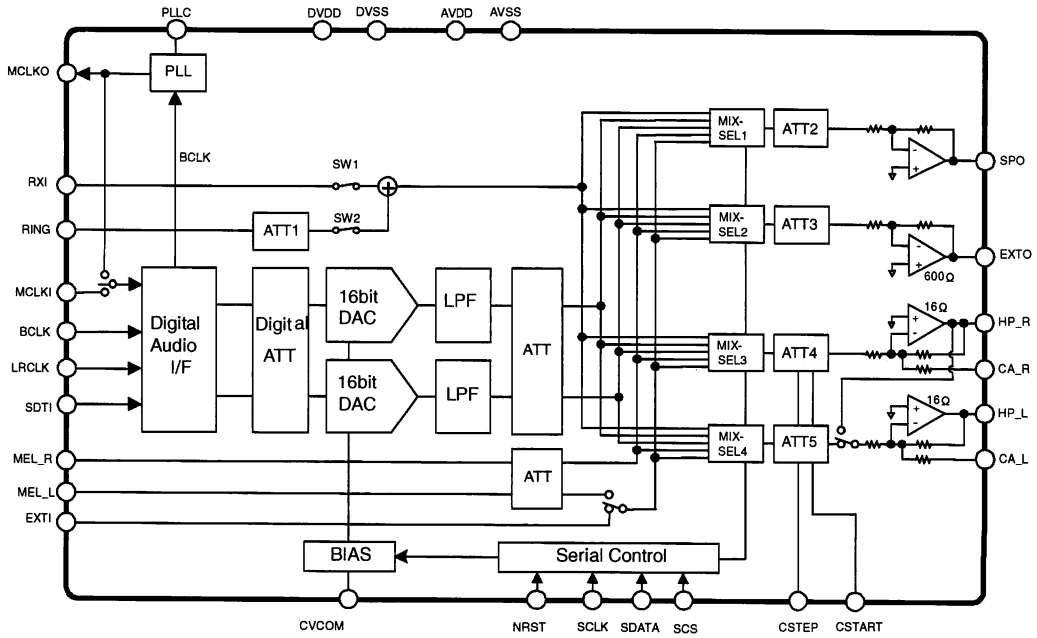


Terminals

PIN	PIN Name	PIN	PIN Name
1	SDTI	15	CA_L
2	LRCLK	16	HP_L
3	BCLK	17	AVSS
4	DVDD	18	AVDD
5	DVSS	19	EXTO
6	SCLK	20	SPO
7	SDATA	21	EXTI
8	NCS	22	MEL_L
9	NRST	23	MEL_R
10	CSTEP	24	RING
11	CSTART	25	RXI
12	CVCOM	26	PLL
13	HP_R	27	MCLKO
14	CA_R	28	MCLKI

Note) Un-recommended installation at oclosed area with a dotted line.

Block diagram



## ○Cautions on use

## (1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

## (2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, please separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

## (3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

## (4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

## (5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

## (6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

## (7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

## (8) Other cautions on use

Please consult supplementary documents such as technical notebook, function manual and application notebook of this LSI.

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