

◆ STRUCTURE Silicon Monolithic Integrated Circuit

◆ PRODUCT DDC2™ DISPLAY ID ROM

◊ PART NUMBER BU9882-W Series

PART NUMBER	PACKAGE
BU9882-W	DIP14
BU9882F-W	SOP14
BU9882FV-W	SSOP14

- ◆ FEATURES
 - For DDC2™
 - 2kbit (128word × 8bit × 2port) EEPROM
 - Single power supply (2.5V~5.5V)
 - 100,000 erase/write cycles endurance

◇ ABSOLUTE MAXIMUM RATING (Ta=25°C)

Parameter	Symbol	Rating		Unit
Supply Voltage	Vcc	-0.3~6.5		V
Power Dissipation	Pd	950	(BU9882-W)	*1
		450	(BU9882F-W)	*2
		350	(BU9882FV-W)	*3
Storage Temperature	Tstg	-65~125		°C
Operating Temperature	Topr	-40~85		°C
Terminal Voltage	—	-0.3~Vcc+1.0	*4	V

* Degradation is done at 9.5mW/°C(*1), 4.5mW/°C(*2), 3.5mW/°C(*3) for operation above 25°C

*4 Max 6.8V

◆ RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	2.5~5.5	V
Input Voltage	VIN	0~Vcc+1.0	V

Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

◇ MEMORY CELL CHARACTERISTICS (Ta=25°C, Vcc=2.5~5.5V)

Parameter	Specification			Unit
	Min.	Typ.	Max.	
Write/Erase Cycle *1	100,000	—	—	Cycle
Data Retention *1	10	—	—	Year

○ Initial Data: Memory array FFh *1 Not 100% TESTED

◇ DC OPERATING CHARACTERISTICS
(Unless otherwise specified Ta=-40~85°C, Vcc=2.5~5.5V)

Parameter	Symbol	Specification			Unit
		Min.	Typ.	Max.	
"H" Input Voltage1	VIH1	2	—	—	V
"L" Input Voltage1	VIL1	—	—	0.8	V $V_{cc} \geq 4.0V$
"L" Input Voltage2	VIL2	—	—	0.2Vcc	V $V_{cc} < 4.0V$
"L" Output Voltage	VOL	—	—	0.4	V SDA,PC0/1, IOL=3.0mA *1
Input Leakage Current1	IL11	-1	—	1	μA SCL,PC0/1, DDCENA, BANKSEL VIN=0V~Vcc+1.0
Input Leakage Current2	IL12	-1	—	50	μA WPB
Output Leakage Current	IL0	-1	—	1	μA SDA,PC0/1,SCL/SDA_MON(DDCENA=GND); VOUT=0V~Vcc+1.0
Operating Current	ICC	—	1.5	3	mA fSCL=400kHz, Vcc=5.5V tWR=10ms
Standby Current	ISB	—	0.1	5	μA SCL/SDA,PC0/1=Vcc SCL/SDA_MON=High-Z DDCENA=WPB=BANKSEL=GND DUALPCB=Vcc

○ This product is not designed for protection against radioactive rays.

*1 IOL at monitor mode (DDCENA=HIGH) is sum of current flowed from Pull up resistor on SDA_MON Side, and Pull up resistance on SDA,PC0/PC1.

◇ BLOCK DIAGRAM

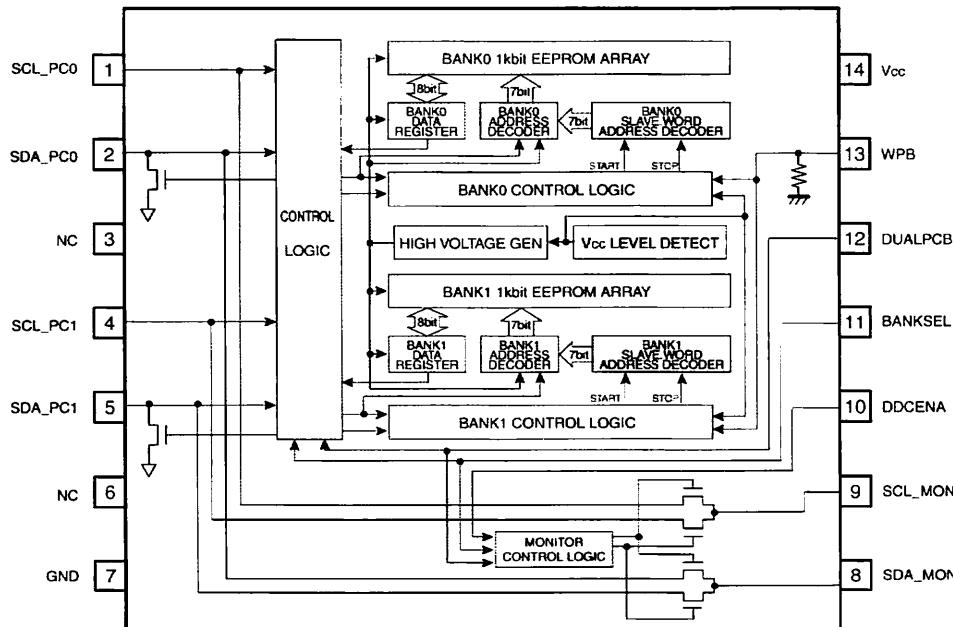


Fig.1 BLOCK DIAGRAM

◇ AC OPERATING CHARACTERISTICS
(Unless otherwise specified Ta=-40~85°C)

Parameter	Symbol	Fast-mode 2.5 ≤ Vcc ≤ 5.5V			Standard-mode 2.5 ≤ Vcc ≤ 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fSCL	—	—	400	—	—	100	kHz
Data Clock High Period	tHIGH	0.6	—	—	4.0	—	—	μs
Data Clock Low Period	tLOW	1.3	—	—	4.7	—	—	μs
SDA and SCL Rise Time	tR	—	—	0.3	—	—	1.0	μs
SDA and SCL Fall Time	tF	—	—	0.3	—	—	0.3	μs
Start Condition Hold Time	tHD STA	0.6	—	—	4.0	—	—	μs
Start Condition Setup Time	tSU:STA	0.6	—	—	4.7	—	—	μs
Input Data Hold Time	tHD:DAT	0	—	—	0	—	—	μs
Input Data Setup Time	tSU:DAT	100	—	—	250	—	—	μs
Output Data Delay Time	tPD	—	—	0.9	—	—	3.5	μs
Stop Condition Setup Time	tSU:STO	0.6	—	—	4.0	—	—	μs
Bus Free Time	tBUF	1.3	—	—	4.7	—	—	μs
Write Cycle Time	tWR	—	—	10	—	—	10	ms
Noise Spike Width (SDA and SCL)	tl	—	—	0.1	—	—	0.1	μs

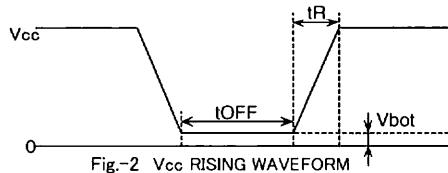
◇ PIN No./PIN NAME

PIN No.	PIN NAME
1	SCL,PC0
2	SDA,PC0
3	NC
4	SCL,PC1
5	SDA,PC1
6	NC
7	GND
8	SDA_MON
9	SCL_MON
10	DDCENA
11	BANKSEL
12	DUALPCB
13	WPB
14	Vcc

◇NOTES FOR POWER SUPPLY

V_{CC} rises through the low voltage region in which internal circuit of IC and the controller are unstable, so that device may not work properly due to an incomplete reset of internal circuit. To prevent this, the device has the feature of P.O.R. and LVCC. In the case of power up, keep the following conditions to ensure functions of P.O.R. and LVCC.

1. It is necessary for SDA_{PC0} and SDA_{PC1} to be "HIGH", for SCL_{PC0} and SCL_{PC1} to be either "HIGH" or "LOW".
2. Follow the recommended conditions of t_R, t_{OFF}, V_{bot} for the function of P.O.R. during power up.



◇Recommended conditions of t_R, t_{OFF}, V_{bot}

t _R	t _{OFF}	V _{bot}
Below 10ms	Above 10ms	Below 0.2V
Below 100ms	Above 10ms	Below 0.1V

3. Prevent SDA_{PC0}, SDA_{PC1}, SCL_{PC0} and SCL_{PC1} from being "High-Z".

In case that condition 1. and/or 2. cannot be met, take following actions.

A) Unable to keep condition 1. (SDA_{PC0} is "LOW" during power up, for example.)

→ Control SDA_{PC0} and SCL_{PC0} to be "HIGH" as figure below.

It applies to SDA_{PC1} and SCL_{PC1} also.

B) Unable to keep condition 2.

→ After power becomes stable,
execute software reset.

C) Unable to keep both conditions 1 and 2.

→ Follow the instruction A first,
then the instruction B.

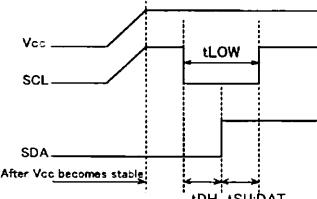


Fig.3-(a) SCL_{PC0}/1='H' and
SDA_{PC0}/1='L'

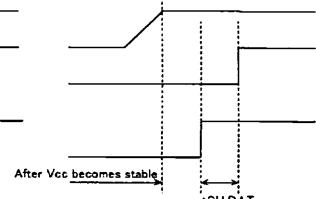


Fig.3-(b) SCL_{PC0}/1='L' and
SDA_{PC0}/1='L'

◇CAUTIONS ON USE

(1) Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and operating temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(2) GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltages is lower than that of GND terminal.

(3) Heat design

In consideration of permissible dissipation in actual use condition, carry out heat design with sufficient margin.

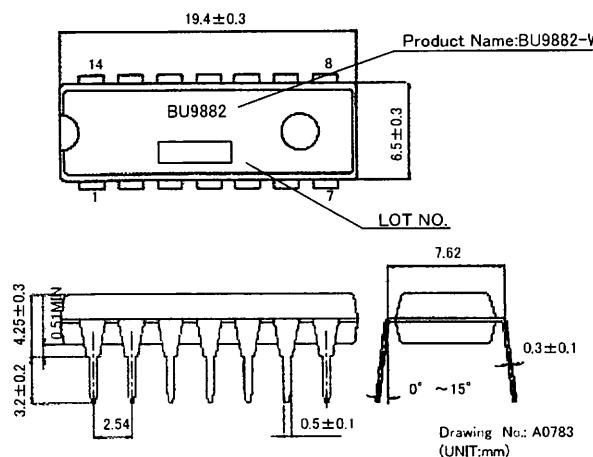
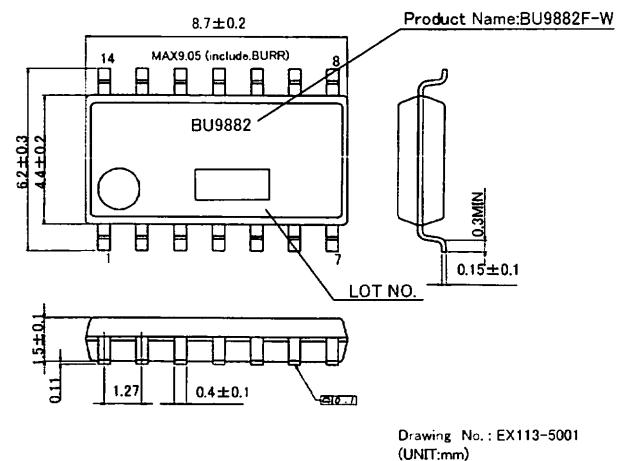
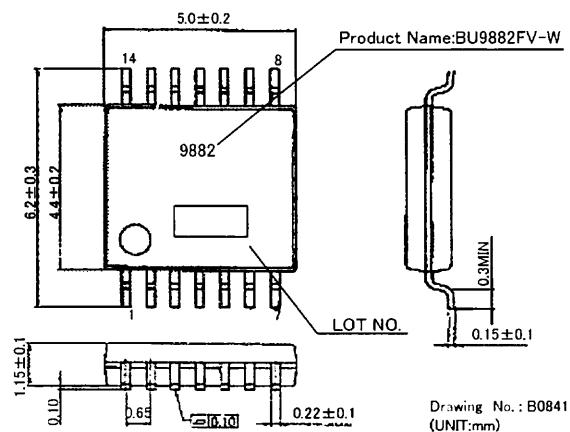
(4) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(5) Strong electromagnetic field

Use in a strong electromagnetic field may cause malfunction, therefore, evaluated design sufficiently.

◇ PHYSICAL DIMENSION

Fig.4-(a) PHYSICAL DIMENSION
DIP14 (BU9882-W)Fig.4-(b) PHYSICAL DIMENSION
SOP14 (BU9882F-W)Fig.4-(c) PHYSICAL DIMENSION
SSOP14 (BU9882FV-W)

Appendix

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