

μ A726 TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μ A726 is a monolithic transistor pair in high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling, and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift DC amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar* process.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range

Military (312 Grade)

Commercial (323 Grade)

Storage Temperature Range

Lead Temperature (Soldering, 60 seconds)

Supply Voltage

Internal Power Dissipation

−55°C to +125°C

0°C to +85°C

−65°C to +150°C

300°C

±18 V

500 mW

MAXIMUM RATINGS FOR EACH TRANSISTOR

Maximum collector-to-substrate voltage

BVC_{BO}

LV_{CEO} (Note 1)

BVE_{BO}

Collector Current

40 V

40 V

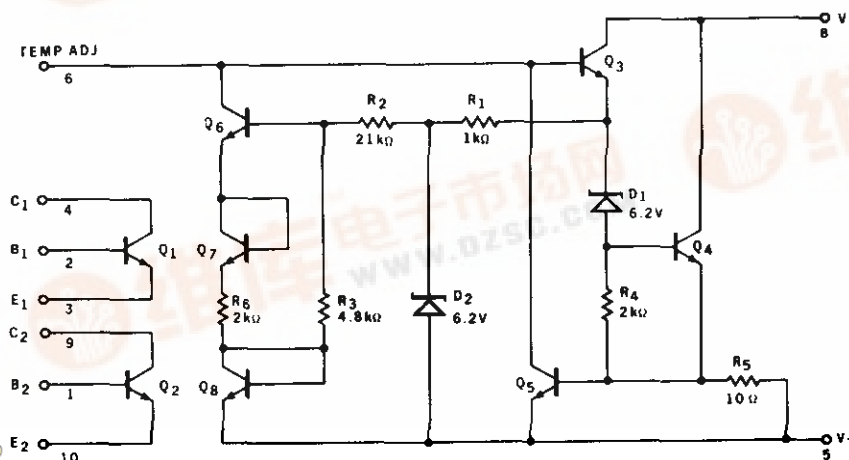
30 V

5 V

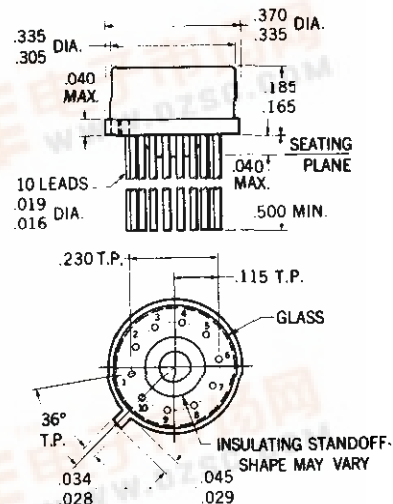
5 mA

Note 1: Measured at 1 mA collector current.

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS



NOTES

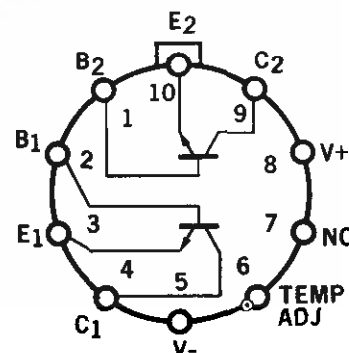
All dimensions in inches

Leads are gold-plated kovar

Package weight is 1.32 grams

ORDER PART NOS. U5U7726312
U5U7726323

CONNECTION DIAGRAM (TOP VIEW)



*Planar is a patented Fairchild process

FAIRCHILD LINEAR INTEGRATED CIRCUITS • $\mu A726$

312 GRADE

ELECTRICAL CHARACTERISTICS ($-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $V_S = \pm 15\text{ V}$, $R_{adj} = 62\text{ k}\Omega$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$10\text{ }\mu\text{A} \leq I_C \leq 100\text{ }\mu\text{A}$ $V_{CE} = 5\text{ V}$, $R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current	$I_C = 10\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$		10	50	nA
Input Offset Current	$I_C = 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$		50	200	nA
Average Input Bias Current	$I_C = 10\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$		50	150	nA
Average Input Bias Current	$I_C = 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$		250	500	nA
Offset Voltage Change	$I_C = 10\text{ }\mu\text{A}$, $5\text{ V} \leq V_{CE} \leq 25\text{ V}$, $R_S \leq 100\text{ k}\Omega$		0.3	6.0	mV
Offset Voltage Change	$I_C = 100\text{ }\mu\text{A}$, $5\text{ V} \leq V_{CE} \leq 25\text{ V}$, $R_S \leq 10\text{ k}\Omega$		0.3	6.0	mV
Input Offset Voltage Drift	$10\text{ }\mu\text{A} \leq I_C \leq 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$, $R_S \leq 50\Omega$, $+25^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		0.2	1.0	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Voltage Drift	$10\text{ }\mu\text{A} \leq I_C \leq 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$, $R_S \leq 50\Omega$, $-55^{\circ}\text{C} \leq T_A \leq +25^{\circ}\text{C}$		0.2	1.0	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Current Drift	$I_C = 10\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$		10		$\text{pA}/^{\circ}\text{C}$
Input Offset Current Drift	$I_C = 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$		30		$\text{pA}/^{\circ}\text{C}$
Supply Voltage Rejection Ratio	$10\text{ }\mu\text{A} \leq I_C \leq 100\text{ }\mu\text{A}$, $R_S \leq 50\Omega$,		25		$\mu\text{V}/\text{V}$
Low-Frequency Noise	$I_C = 10\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$, $R_S \leq 50\Omega$ $\text{BW} = .001\text{ Hz to }0.1\text{ Hz}$		4.0		$\mu\text{V pp}$
Broadband Noise	$I_C = 10\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$, $R_S \leq 50\Omega$ $\text{BW} = 0.1\text{ Hz to }10\text{ kHz}$		10		$\mu\text{V pp}$
Long-term Drift	$10\text{ }\mu\text{A} \leq I_C \leq 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$, $R_S \leq 50\Omega$, $T_A = 25^{\circ}\text{C}$		5.0		$\mu\text{V}/\text{week}$
High Frequency Current Gain	$f = 20\text{ MHz}$, $I_C = 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CE} = 5\text{ V}$		1.0		pF
Emitter Transition Capacitance	$I_E = 100\text{ }\mu\text{A}$		1.0		pF
Collector Saturation Voltage	$I_E = 100\text{ }\mu\text{A}$, $I_C = 1\text{ mA}$		0.5	1.0	V

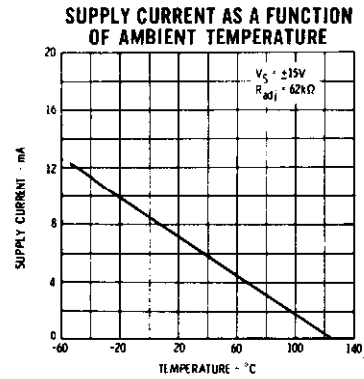
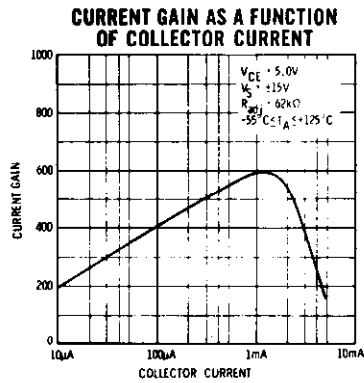
323 GRADE

ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, $V_S = \pm 15\text{ V}$, $R_{adj} = 75\text{ k}\Omega$ unless otherwise specified)

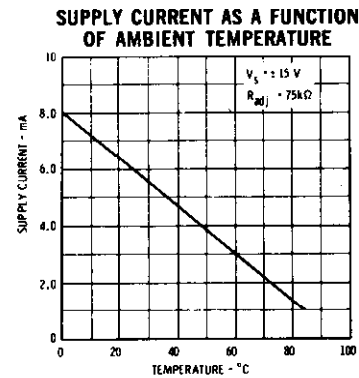
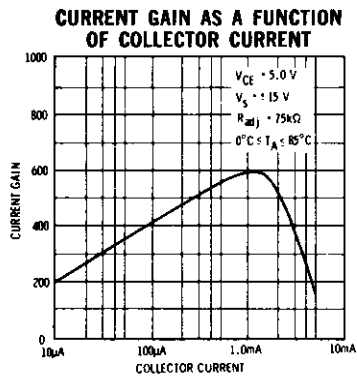
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$10\text{ }\mu\text{A} \leq I_C \leq 100\text{ }\mu\text{A}$ $V_{CE} = 5\text{ V}$, $R_S \leq 50\Omega$		1.0	3.0	mV
Input Offset Current	$I_C = 10\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$		10	100	nA
Input Offset Current	$I_C = 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$		50	400	nA
Average Input Bias Current	$I_C = 10\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$		50	300	nA
Average Input Bias Current	$I_C = 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$		250	1000	nA
Offset Voltage Change	$I_C = 10\text{ }\mu\text{A}$, $5\text{ V} \leq V_{CE} \leq 25\text{ V}$, $R_S \leq 100\text{ k}\Omega$		0.3	6.0	mV
Offset Voltage Change	$I_C = 100\text{ }\mu\text{A}$, $5\text{ V} \leq V_{CE} \leq 25\text{ V}$, $R_S \leq 10\text{ k}\Omega$		0.3	6.0	mV
Input Offset Voltage Drift	$I_C = 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$, $R_S \leq 50\Omega$		0.2	2.0	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Current Drift	$I_C = 10\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$		10		$\text{pA}/^{\circ}\text{C}$
Input Offset Current Drift	$I_C = 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$		30		$\text{pA}/^{\circ}\text{C}$
Supply Voltage Rejection Ratio	$I_C = 100\text{ }\mu\text{A}$, $R_S = 50\Omega$		25		$\mu\text{V}/\text{V}$
Low-Frequency Noise	$I_C = 10\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$, $R_S \leq 50\Omega$, $\text{BW} = 0.001\text{ Hz to }0.1\text{ Hz}$		4.0		$\mu\text{V pp}$
Broadband Noise	$I_C = 10\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$, $R_S \leq 50\Omega$, $\text{BW} = 0.1\text{ Hz to }10\text{ kHz}$		10		$\mu\text{V pp}$
Long-Term Drift	$I_C = 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$, $R_S \leq 50\Omega$, $T_A = 25^{\circ}\text{C}$		5.0		$\mu\text{V}/\text{week}$
High-Frequency Current Gain	$f = 20\text{ MHz}$, $I_C = 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5\text{ V}$		1.0		pF
Emitter Transition Capacitance	$I_E = 100\text{ }\mu\text{A}$		1.0		pF
Collector Saturation Voltage	$I_E = 100\text{ }\mu\text{A}$, $I_C = 1\text{ mA}$		0.5	1.0	V

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TYPICAL PERFORMANCE CURVES 312 GRADE



323 GRADE



TYPICAL X1000 CIRCUIT

