

INTEGRATED CIRCUITS

DATA SHEET

UAA2073M

Image rejecting front-end
for GSM applications

Product specification

1995 Dec 07

Supersedes data of July 1995

File under Integrated Circuits, IC03

Image rejecting front-end for GSM applications

UAA2073M

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for at least 30 dB; on-chip image rejection
- IF I/Q combination network for 50 to 100 MHz
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast **on/off** power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 900 MHz front-end for GSM hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2073M contains both a receiver front-end and a high frequency transmit mixer intended for GSM (Global System for Mobile communications) cellular telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2073M is its ability to provide over 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed and the duplexer design is eased, compared with a conventional front-end design.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows to reject the upper or lower image frequency. Image rejection is at an optimum when the IF is 71 MHz and local oscillator is above the wanted signal.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The all-pass filters outputs are buffered before been fed to the receive mixers.

The transmit section consists of a down-conversion mixer and a transmit IF driver stage. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced to reduce EMC issues.

Fast power-up switching is possible. A synthesizer-on (synthon) mode enables LO buffers independent of the other circuits. When SYNTHON pin is HIGH, all internal buffers on the LO path of the circuit are turned **on**, thus minimizing LO pulling when remainder of receive chain is powered-up.

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|---|----------|
| | NAME | DESCRIPTION | VERSION |
| UAA2073M | SSOP20 | plastic shrink small outline package; 20 leads; body width 4.4 mm | SOT266-1 |

Image rejecting front-end
for GSM applications

UAA2073M

QUICK REFERENCE DATA

Note 1.

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---------------------|---|------|------|------|------|
| V _{CC} | supply voltage | 3.6 | 3.75 | 5.3 | V |
| I _{CC(RX)} | receive supply current | 21 | 26 | 32 | mA |
| I _{CC(TX)} | transmit supply current | 9 | 12 | 15 | mA |
| NF | noise figure on demonstration board (including matching and PCB losses) | – | 3.25 | 4.3 | dB |
| G _{CP} | conversion power gain | 20 | 23 | 26 | dB |
| IR | image frequency rejection | 30 | 37 | – | dB |
| T _{amb} | operating ambient temperature | –30 | +25 | +85 | °C |

Note

1. For conditions see Chapters “DC characteristics” and “AC characteristics”.

BLOCK DIAGRAM

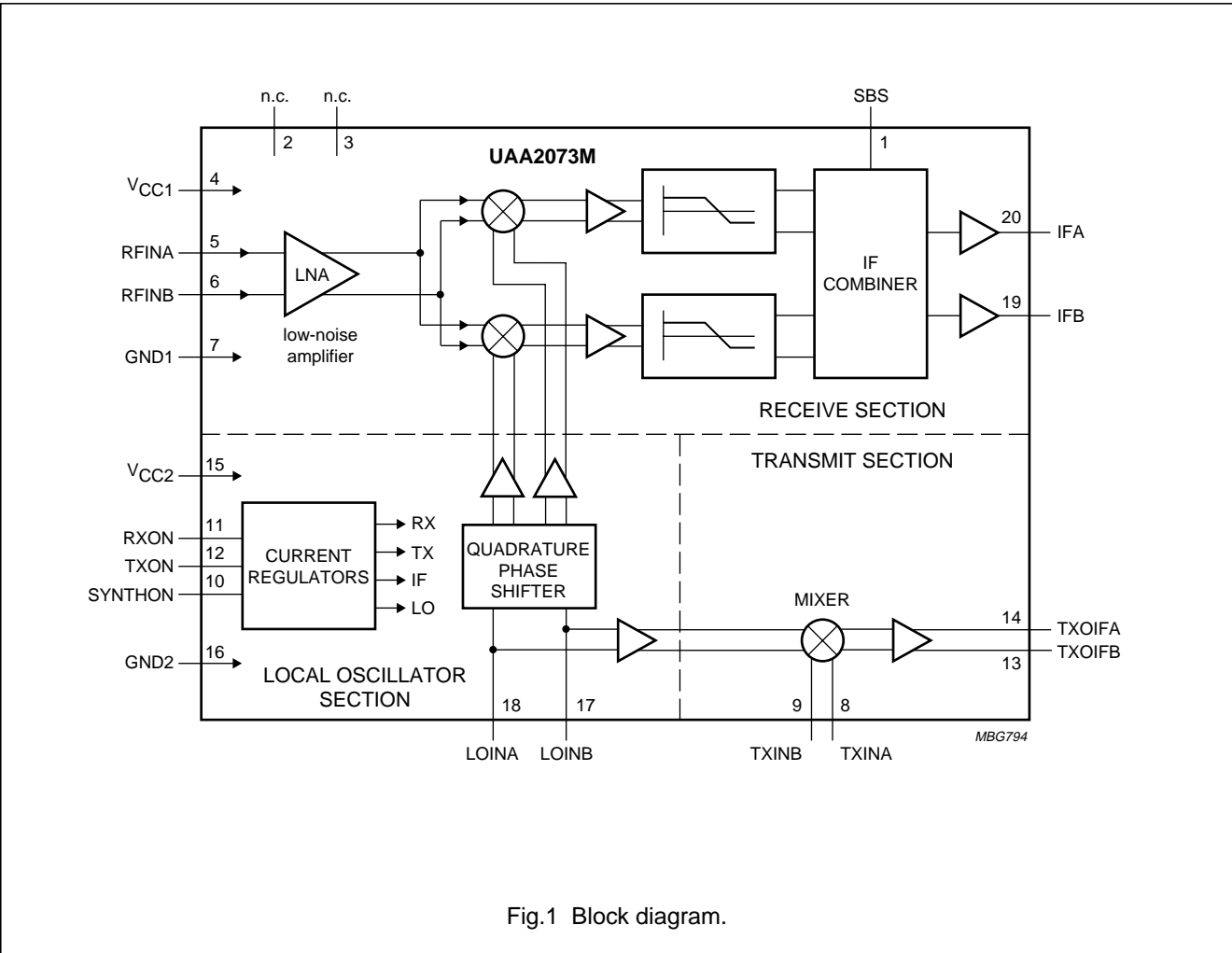


Image rejecting front-end
for GSM applications

UAA2073M

PINNING

| SYMBOL | PIN | DESCRIPTION |
|------------------|-----|--|
| SBS | 1 | sideband selection |
| n.c. | 2 | not connected |
| n.c. | 3 | not connected |
| V _{CC1} | 4 | supply voltage for receive and transmit sections |
| RFINA | 5 | RF input A (balanced) |
| RFINB | 6 | RF input B (balanced) |
| GND1 | 7 | ground 1 for receive and transmit sections |
| TXINA | 8 | transmit mixer input A (balanced) |
| TXINB | 9 | transmit mixer input B (balanced) |
| SYNTHON | 10 | hardware power-on of LO section (including buffers to RX and TX) |
| RXON | 11 | hardware power-on for receive section and LO buffers to RX |
| TXON | 12 | hardware power-on for transmit section and LO buffers to TX |
| TXOIFB | 13 | transmit mixer IF output B (balanced) |
| TXOIFA | 14 | transmit mixer IF output A (balanced) |
| V _{CC2} | 15 | supply voltage for LO section |
| GND2 | 16 | ground 2 for LO section |
| LOINB | 17 | LO input B (balanced) |
| LOINA | 18 | LO input A (balanced) |
| IFB | 19 | IF output B (balanced) |
| IFA | 20 | IF output A (balanced) |

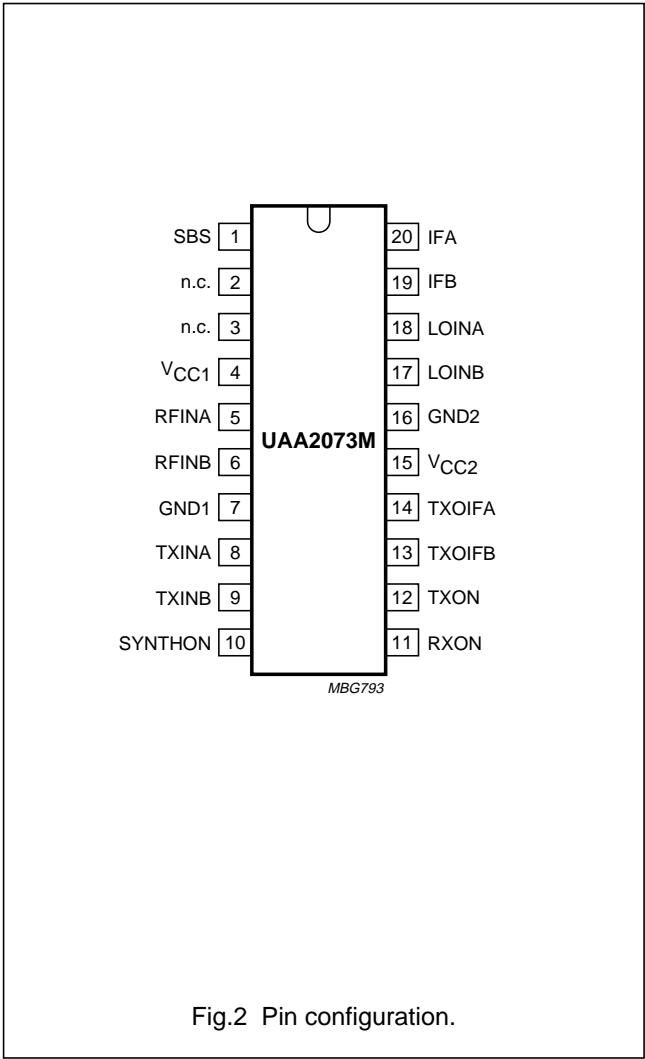


Image rejecting front-end for GSM applications

UAA2073M

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type. The whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135° , mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Pin SBS allows sideband selection:

- $f_{LO} < f_{RF}$ (SBS = 1)
- $f_{LO} > f_{RF}$ (SBS = 0).

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF differential input impedance is $150\ \Omega$ (parallel real part), chosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type, tuned for 71 MHz. Typical application will load the output with a differential $500\ \Omega$ load; i.e. a $500\ \Omega$ resistor load at each IF output, plus a $1\ \text{k}\Omega$ to $x\ \Omega$ narrow band matching network ($x\ \Omega$ being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, **on/off**, of the receive section is controlled by the hardware input RXON.

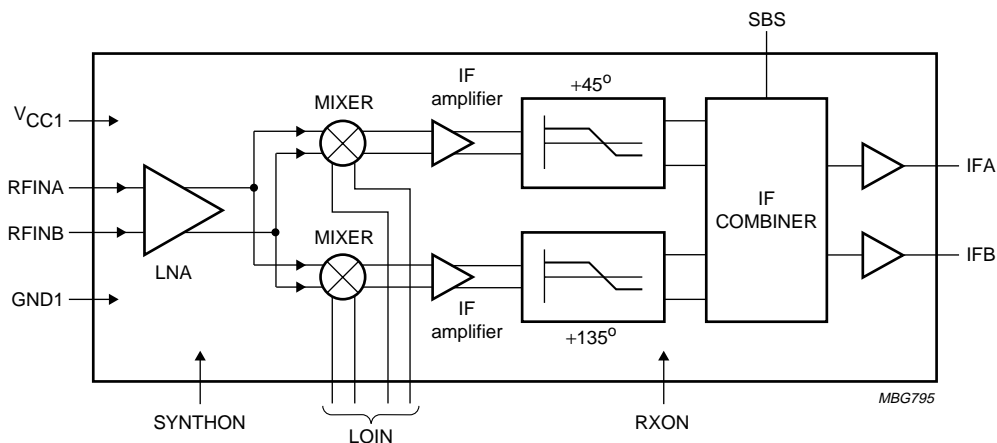


Fig.3 Block diagram, receive section.

Image rejecting front-end
for GSM applications

UAA2073M

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The LO differential input impedance is 50 Ω (parallel real part).

A synthesizer-on (synthon) mode is used to power-up the buffering on the LO inputs, minimizing the pulling effect on the external VCO when entering transmit or receive modes.

This mode is active when the SYNTHON input is HIGH. Table 1 shows status of circuit in accordance with TXON, RXON and SYNTHON inputs.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF and down-convert it to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 200 Ω and a differential output driver buffer for a 1 k Ω load. The IF outputs are low impedance (emitter followers).

Fast switching, **on/off**, of the transmit section is controlled by the hardware input TXON.

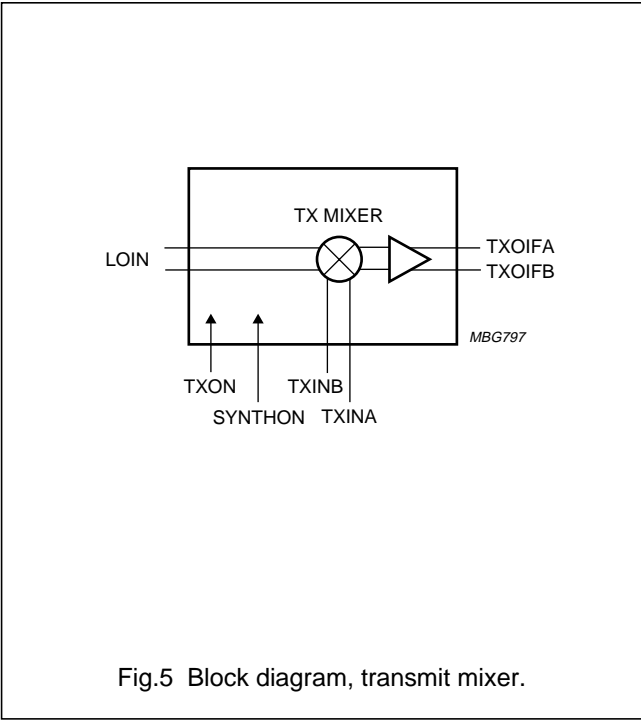
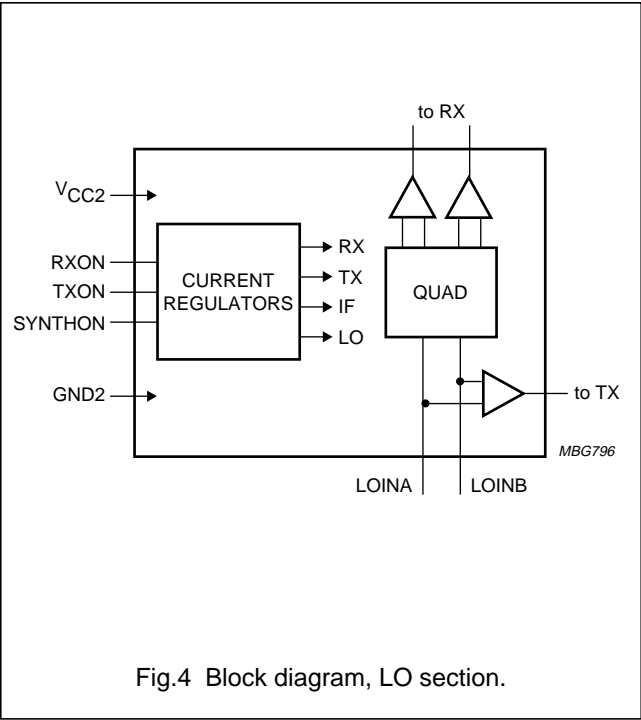


Image rejecting front-end for GSM applications

UAA2073M

Table 1 Control of power status

| EXTERNAL PIN LEVEL | | | CIRCUIT MODE OF OPERATION |
|--------------------|------|---------|--|
| TXON | RXON | SYNTHON | |
| LOW | LOW | LOW | power-down mode |
| LOW | HIGH | LOW | RX mode: receive section and LO buffers to RX on |
| HIGH | LOW | LOW | TX mode: transmit section and LO buffers to TX on |
| LOW | LOW | HIGH | synthon mode: complete LO section on |
| LOW | HIGH | HIGH | SRX mode: receive section on and synthon mode active |
| HIGH | LOW | HIGH | STX mode: transmit section on and synthon mode active |
| HIGH | HIGH | LOW | receive and transmit sections on ; specification not guaranteed |
| HIGH | HIGH | HIGH | receive and transmit sections on ; specification not guaranteed |

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|----------------|---|------|------|------|
| V_{CC} | supply voltage | – | 9 | V |
| ΔGND | difference in ground supply voltage applied between GND1 and GND2 | – | 0.6 | V |
| $P_{I(max)}$ | maximum power input | – | +20 | dBm |
| $P_{dis(max)}$ | maximum power dissipation in quiet air | – | 250 | mW |
| $T_{j(max)}$ | maximum operating junction temperature | – | +150 | °C |
| T_{stg} | storage temperature | –65 | +150 | °C |

THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---------------|---|-------|------|
| $R_{th\ j-a}$ | thermal resistance from junction to ambient in free air | 120 | K/W |

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

Image rejecting front-end for GSM applications

UAA2073M

DC CHARACTERISTICS

$V_{CC} = 3.75\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|-----------------------------------|--------------------------------|-------------|------|----------|---------------|
| Pins V_{CC1} and V_{CC2} | | | | | | |
| V_{CC} | supply voltage | over full temperature range | 3.6 | 3.75 | 5.3 | V |
| $I_{CC(RX)}$ | supply current in RX mode | | 21 | 26 | 32 | mA |
| $I_{CC(TX)}$ | supply current in TX mode | | 9 | 12 | 15 | mA |
| $I_{CC(SX)}$ | supply current in synthon mode | | 4.4 | 5.6 | 6.6 | mA |
| $I_{CC(SRX)}$ | supply current in SRX mode | | 23 | 28 | 34 | mA |
| $I_{CC(STX)}$ | supply current in STX mode | | 12.5 | 15.0 | 19.5 | mA |
| $I_{CC(PD)}$ | supply current in power-down mode | | – | 0.01 | 50 | μA |
| Pins SYNTHON, RXON, TXON and SBS | | | | | | |
| V_{th} | CMOS threshold voltage | note 1 | – | 1.25 | – | V |
| V_{IH} | HIGH level input voltage | | $0.7V_{CC}$ | – | V_{CC} | V |
| V_{IL} | LOW level input voltage | | –0.3 | – | 0.8 | V |
| I_{IH} | HIGH level static input current | pin at $V_{CC} - 0.4\text{ V}$ | –1 | – | +1 | μA |
| I_{IL} | LOW level static input current | pin at 0.4 V | –1 | – | +1 | μA |
| Pins RFINA and RFINB | | | | | | |
| $V_{I(RFIN)}$ | DC input voltage level | receive section on | 2.0 | 2.2 | 2.4 | V |
| Pins IFA and IFB | | | | | | |
| $I_{O(IF)}$ | DC output current | receive section on | 2.3 | 3.0 | 3.8 | mA |
| Pins TXINA and TXINB | | | | | | |
| $V_{I(TXIN)}$ | DC input voltage level | transmit section on | 2.1 | 2.4 | 2.6 | V |
| Pins TXOIFA and TXOIFB | | | | | | |
| $V_{O(TXOIF)}$ | DC output voltage level | transmit section on | 1.8 | 1.9 | 2.1 | V |
| Pins LOINA and LOINB | | | | | | |
| $V_{I(LOIN)}$ | DC input voltage level | receive section on | 2.3 | 2.5 | 2.8 | V |
| | | transmit section on | 2.3 | 2.5 | 2.8 | V |

Note

1. The referenced inputs should be connected to a valid CMOS input level.

Image rejecting front-end for GSM applications

UAA2073M

AC CHARACTERISTICS

 $V_{CC} = 3.75\text{ V}$; $T_{amb} = -30\text{ to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|--|-------|-------|-------|----------|
| Receive section (receive section on) | | | | | | |
| Z_{RF} | RF input impedance (real part) | balanced parallel | – | 150 | – | Ω |
| f_{RF} | RF input frequency | | 925 | – | 960 | MHz |
| RL_{RF} | return loss on matched RF input | note 1 | 15 | 20 | – | dB |
| G_{CP} | conversion power gain | differential RF input to differential IF output matched to 1 k Ω differential | 20 | 23 | 26 | dB |
| G_{rip} | gain ripple as a function of RF frequency | note 2 | – | 0.2 | 0.5 | dB |
| $\Delta G/T$ | gain variation with temperature | note 2 | –20 | –15 | –10 | mdB/K |
| DES1 | 1 dB desensitization input power | interferer frequency offset 3 MHz | – | –30 | – | dBm |
| CP1 _{RX} | 1 dB input compression point | note 1 | –24.5 | –23.0 | – | dBm |
| IP2D _{RX} | 2nd order intercept point referenced to the RF differential input | differential output; note 2 | +30 | +40 | – | dBm |
| IP3 _{RX} | 3rd order intercept point referenced to the RF input | note 2 | –18 | –15 | – | dBm |
| NF _{RX} | overall noise figure | RF input to differential IF output; notes 2 and 3 | – | 3.25 | 4.30 | dB |
| $R_{L(IF)}$ | typical application IF output load resistor | between pin and V_{CC} | – | 500 | – | Ω |
| $C_{L(IF)}$ | IF output load capacitance | unbalanced | – | – | 2 | pF |
| f_{IF} | IF frequency range | $f_{LO} > f_{RF}$ | 50 | 71 | 100 | MHz |
| | | $f_{LO} < f_{RF}$ | 50 | 71 | 100 | MHz |
| IR | image frequency rejection | | 30 | 37 | – | dB |
| Local oscillator section (RXON or TXON or SYNTHON = 1) | | | | | | |
| f_{LO} | LO input frequency | | 850 | – | 1 100 | MHz |
| Z_{LO} | LO input impedance | balanced | – | 50 | – | Ω |
| ΔZ_{LO} | impedance change when switching from synthon mode to SRX or STX mode | mUnits measured on Smith chart; note 1 | – | 20 | – | Ω |
| RL_{LO} | return loss on matched input (including power-down mode) | note 2 | 10 | 15 | – | dB |
| $P_{i(LO)}$ | LO input power level | | –7 | –4 | 0 | dBm |
| RI_{LO} | reverse isolation | LOIN to RFIN at LO frequency; note 2 | 40 | – | – | dB |

Image rejecting front-end for GSM applications

UAA2073M

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---------------------------------|--|------|-------|------|-----------|
| Transmit section (transmit section on) | | | | | | |
| $Z_{O(TX)}$ | TX IF output impedance | | – | – | 200 | Ω |
| $Z_{L(TX)}$ | TX IF load impedance | | – | 1 | – | $k\Omega$ |
| $C_{L(TX)}$ | TX IF load capacitance | | – | – | 2 | pF |
| $Z_{i(TX)}$ | TX RF input impedance | balanced | – | 200 | – | Ω |
| $f_{i(TX)}$ | TX input frequency | | 880 | – | 915 | MHz |
| RL_{TX} | return loss on matched TX input | note 1 | 15 | 20 | – | dB |
| G_{CP} | conversion power gain | from 200 Ω to 1 $k\Omega$ output; note 2 | 5 | 7.4 | 10 | dB |
| $f_{o(TX)}$ | TX output frequency | | 40 | – | 200 | MHz |
| $CP1_{TX}$ | 1 dB input compression point | note 1 | –22 | –17.5 | – | dBm |
| $IP2_{TX}$ | 2nd order intercept point | | – | +20 | – | dBm |
| $IP3_{TX}$ | 3rd order intercept point | | –12 | –9 | – | dBm |
| NF_{TX} | noise figure | double sideband; notes 2 and 3 | – | 9.8 | 12 | dB |
| RI_{TX} | reverse isolation | TXIN to LOIN; note 2 | 40 | – | – | dB |
| I_{TX} | isolation | LOIN to TXIN; note 2 | 40 | – | – | dB |
| Timing | | | | | | |
| t_{start} | start-up time of each block | | 1 | 5 | 20 | μs |

Notes

1. Measured and guaranteed only on Philips UAA2073M demonstration board at $T_{amb} = +25\text{ }^{\circ}\text{C}$.
2. Measured and guaranteed only on Philips UAA2073M demonstration board.
3. This value includes printed-circuit board and balun losses on Philips UAA2073M demonstration board over full temperature range.

Image rejecting front-end
for GSM applications

UAA2073M

APPLICATION INFORMATION

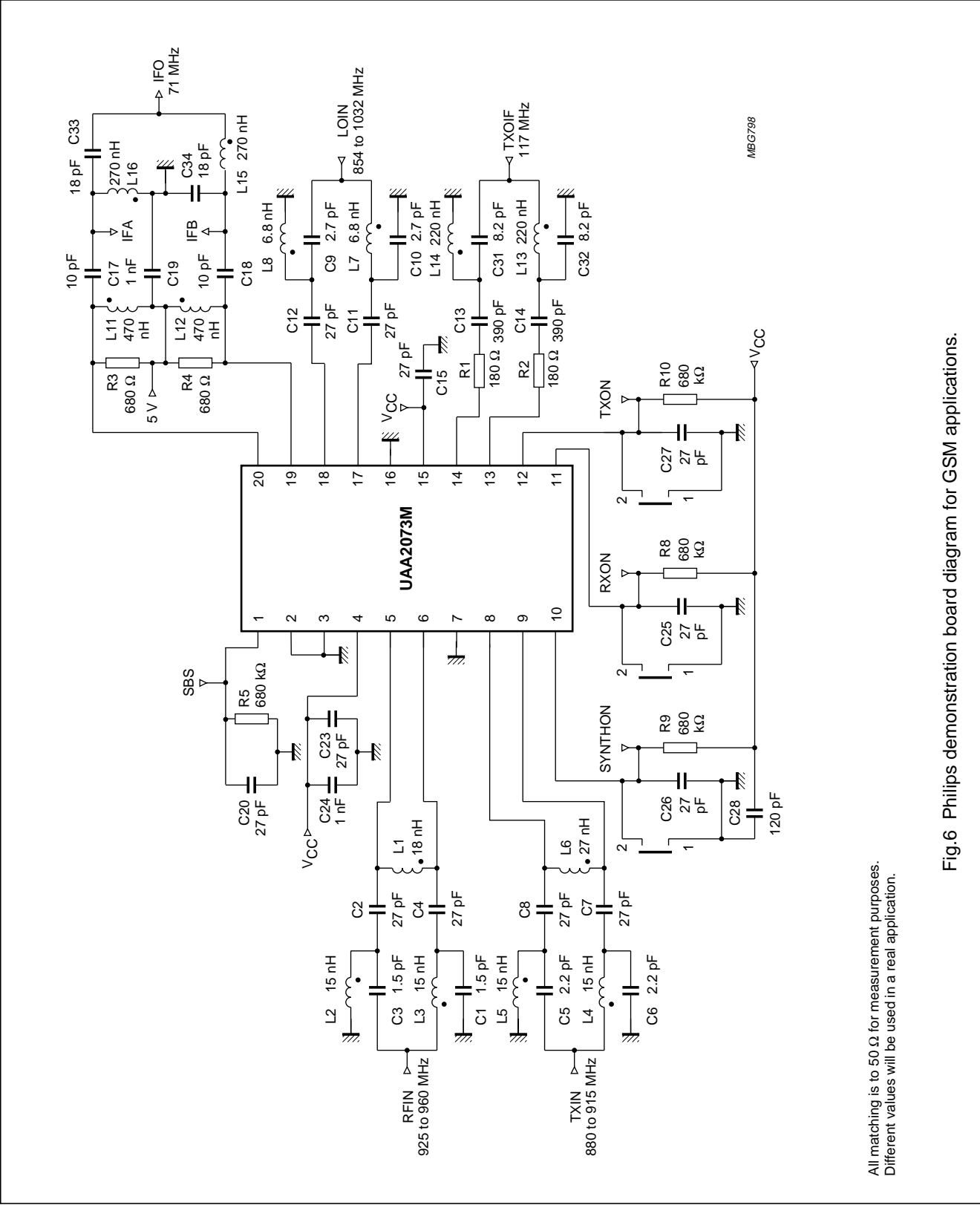


Image rejecting front-end for GSM applications

UAA2073M

Table 2 UAA2073M demonstration board parts list

| PART | VALUE | SIZE | LOCATION |
|-------------------|----------------|------|--------------------|
| Resistors | | | |
| R1 | 180 Ω | 0805 | TXOIF |
| R2 | 180 Ω | 0805 | TXOIF |
| R3 | 680 Ω | 0805 | IFO |
| R4 | 680 Ω | 0805 | IFO |
| R5 | 680 k Ω | 0805 | SBS |
| R8 | 680 k Ω | 0805 | RXON |
| R9 | 680 k Ω | 0805 | SYNTHON |
| R10 | 680 k Ω | 0805 | TXON |
| Capacitors | | | |
| C1 | 1.5 pF | 0805 | RFIN |
| C2 | 27 pF | 0805 | RFIN |
| C3 | 1.5 pF | 0805 | RFIN |
| C4 | 27 pF | 0805 | RFIN |
| C5 | 2.2 pF | 0805 | TXIN |
| C6 | 2.2 pF | 0805 | TXIN |
| C7 | 27 pF | 0805 | TXIN |
| C8 | 27 pF | 0805 | TXIN |
| C9 | 2.7 pF | 0805 | LOIN |
| C10 | 2.7 pF | 0805 | LOIN |
| C11 | 27 pF | 0805 | LOIN |
| C12 | 27 pF | 0805 | LOIN |
| C13 | 390 pF | 0805 | TXOIF |
| C14 | 390 pF | 0805 | TXOIF |
| C15 | 27 pF | 0805 | V _{CCLO} |
| C17 | 10 pF | 0805 | IFO |
| C18 | 10 pF | 0805 | IFO |
| C19 | 1 nF | 0805 | IF/V _{CC} |
| C20 | 27 pF | 0805 | SBS |
| C23 | 27 pF | 0805 | V _{CCLNA} |
| C24 | 1 nF | 0805 | V _{CCLNA} |
| C25 | 27 pF | 0805 | RXON |
| C26 | 27 pF | 0805 | SYNTHON |
| C27 | 27 pF | 0805 | TXON |
| C28 | 120 pF | 0805 | V _{CC} |
| C31 | 8.2 pF | 0805 | TXOIF |
| C32 | 8.2 pF | 0805 | TXOIF |
| C33 | 18 pF | 0805 | IFO |
| C34 | 18 pF | 0805 | IFO |

| PART | VALUE | SIZE | LOCATION |
|------------------|--------|------|----------|
| Inductors | | | |
| L1 | 18 nH | 0805 | RFIN |
| L2 | 15 nH | 0805 | RFIN |
| L3 | 15 nH | 0805 | RFIN |
| L4 | 15 nH | 0805 | TXIN |
| L5 | 15 nH | 0805 | TXIN |
| L6 | 27 nH | 0805 | TXIN |
| L7 | 6.8 nH | 0805 | LOIN |
| L8 | 6.8 nH | 0805 | LOIN |
| L11 | 470 nH | 1008 | IFO |
| L12 | 470 nH | 1008 | IFO |
| L13 | 220 nH | 0805 | TXOIF |
| L14 | 220 nH | 0805 | TXOIF |
| L15 | 270 nH | 1008 | IFO |
| L16 | 270 nH | 1008 | IFO |

Other components

| COMPONENT | DESCRIPTIONS |
|-----------|--------------------------------------|
| IC1 | UAA2073M |
| SMA/RIM | sockets for RF and IF inputs/outputs |
| SMB | V _{CC} socket |

Component manufacturers

All surface mounted resistors and capacitors are from Philips Components. The small value capacitors are multilayer ceramic with NPO dielectric. The inductors are from Coilcraft UK.

Image rejecting front-end
for GSM applications

UAA2073M

PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm

SOT266-1

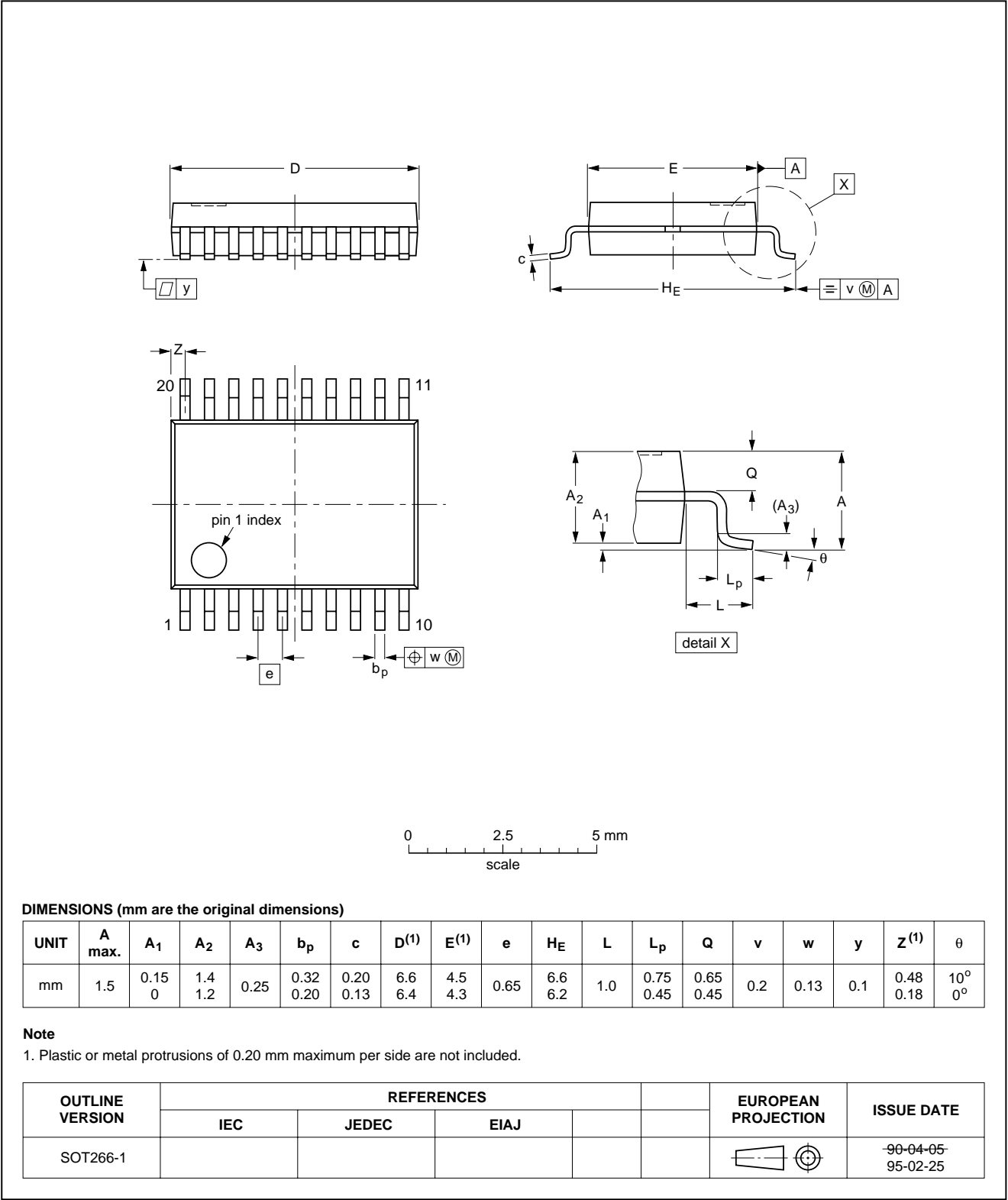


Image rejecting front-end for GSM applications

UAA2073M

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

**Image rejecting front-end
for GSM applications**

UAA2073M

DEFINITIONS

| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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