DATA SHEET

UAA3522HL
Low power dual-band GSM transceiver with an image rejecting front-end

Objective specification
File under Integrated Circuits, IC17

2000 Feb 18

Philips Semiconductors

PHILIPS

Low power dual-band GSM transceiver with an image rejecting front-end

UAA3522HL

FEATURES

- Dual-band application for Global System for Mobile communication (GSM) and Digital Cellular communication Systems (DCS)
- Low noise and wide dynamic range single Intermediate Frequency (IF) transceiver
- More than 30 dB on-chip image rejection in the receiver
- More than 60 dB gain control range
- I/Q demodulator with high performance integrated baseband channel filter
- High precision I/Q modulator
- Transmit modulation loop architecture including offset mixer and phase detector
- Dual Phase-Locked Loop (PLL) with on-chip IF Voltage Controlled Oscillator (VCO)
- Fully differential design minimizing cross-talk and spurii
- 3-wire serial bus interface
- Functional down to 2.7 V and up to 3.3 V
- LQFP48 package.

APPLICATIONS

- GSM 900 MHz hand-held transceiver
- GSM/DCS dual-band solution with the UAA2077CM (down to 3.2 V) or UAA2077TS/D (down to 2.7 V).

GENERAL DESCRIPTION

The UAA3522HL integrates the receiver and most of the transmitter section of a GSM hand-held transceiver. It also integrates the receiver IF and the transmitter section of a DCS transceiver.

The receiver comprises an RF and an IF section. The RF (GSM) front-end amplifies the aerial signal, converts the chosen channel frequency to an IF of 200 MHz, and also provides more than 30 dB of image suppression. Some selectivity is provided at this stage by an off-chip bandpass pre-filter. The IF section further amplifies the chosen channel, maintains the gain at the required level, demodulates the signal into I and Q components, and provides channel selectivity at a baseband stage using a high performance integrated low-pass filter. The IF gain can be varied over a range of more than 60 dB. The offset at the I and Q outputs can be cancelled out by software using the 3-wire serial programming bus.

The input Low Noise Amplifier (LNA) can be switched off via the bus to allow accurate calibration in the offset cancellation mode.

The transmitter comprises a high precision I/Q modulator and modulation loop architecture. The I/Q modulator converts the baseband modulation frequency to the transmit IF. The modulation loop architecture, which includes an on-chip offset mixer and phase detector, controls an external transmit RF VCO which converts the transmit modulated IF signal to RF.

A receive RF VCO provides the Local Oscillator (LO) signal to the image rejection mixers in the RF receiver. An IF VCO provides the LO signal to the I/Q demodulator and I/Q modulator in the receiver and transmitter sections respectively.

The frequencies of the RF VCO and the IF VCO are set by internal PLL circuits, which are programmable via the 3-wire serial bus. The RF and IF PLL comparison frequencies are 200 kHz and 1 MHz respectively, derived from a 13 MHz reference signal which has to be supplied externally. The quadrature RF LO signals required by the image rejection mixers are obtained using on-chip Resistor Capacitor (RC) networks. The quadrature IF LO signals required by the I/Q modulator and I/Q demodulator are obtained by dividing the frequency of the IF VCO signal.

The IC can be powered on in either receiver (RX), transmitter (TX) or synthesizer (SYN) operating mode depending on the logic level at pins RXON, TXON and SYNON, respectively. Alternatively, an operating mode can be selected by software using the 3-wire serial programming bus. In RX or TX mode, only those sections of the IC which are required are switched on.

The GSM or DCS band is selected by the 3-wire serial programming bus. When activating RX mode for DCS applications, the receiver RF section can be disabled by software so that only the receiver IF section is powered-on.

The SYN mode is used to power-on the synthesizer prior to activating the RX or TX mode. In SYN mode, some internal LO buffers are also powered-on to minimize the ‘pulling’ effect of the VCO when either the receiver or the transmitter are switched on.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$f_{i(RF)(RX)}$	GSM band RF input frequency in RX mode	925	–	960	MHz
$f_{o(RF)(TX)(GSM)}$	GSM band RF output frequency in TX mode	880	–	915	MHz
$f_{o(RF)(TX)(DCS)}$	DCS band RF output frequency in TX mode	1710	–	1785	MHz
f_{IF}	IF frequency in all modes	–	200	–	MHz

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA3522HL	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm	SOT313-2

BLOCK DIAGRAM

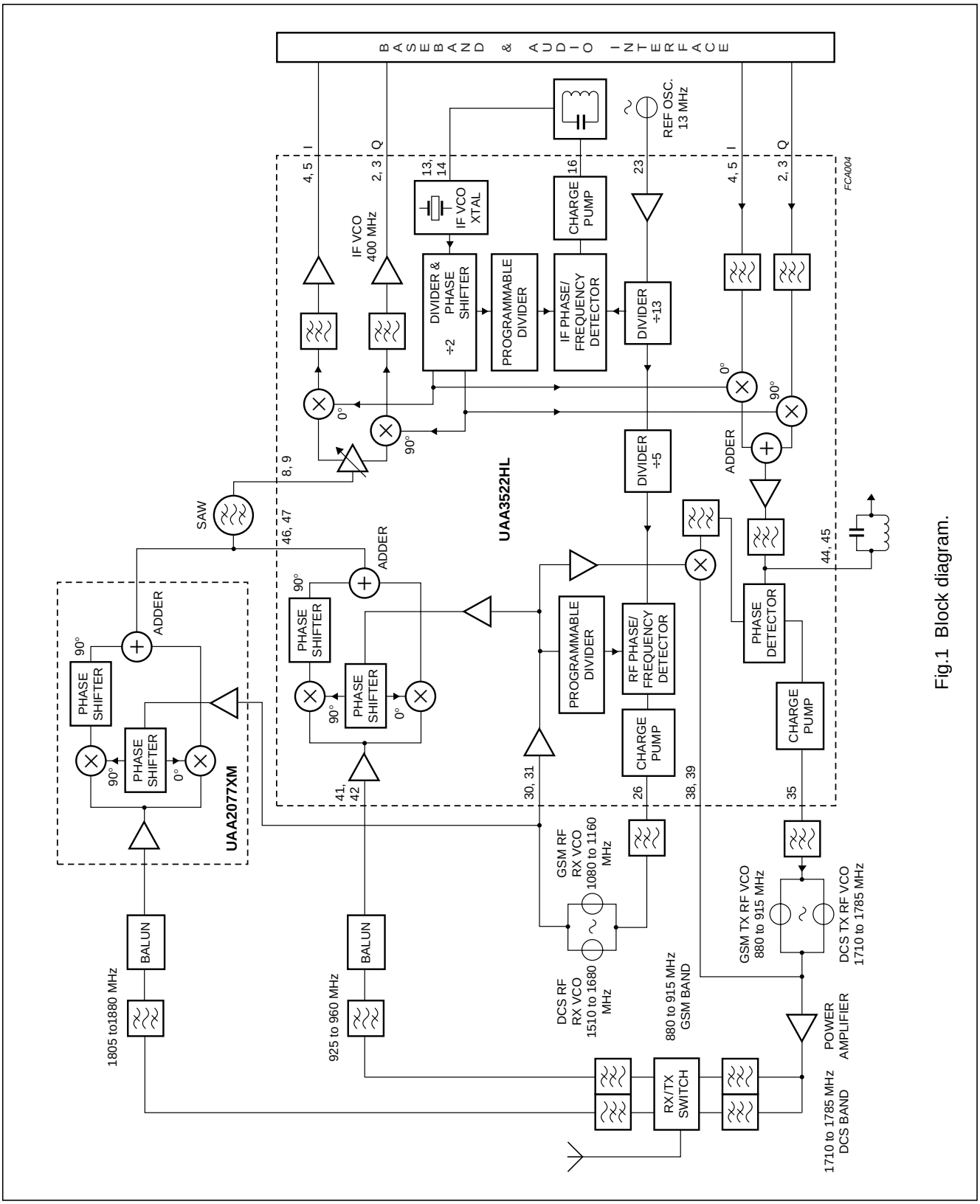


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{CCIF1}	1	IF section of RF receiver supply voltage 1
QA	2	Q path A baseband input/output
QB	3	Q path B baseband input/output
IA	4	I path A baseband input/output
IB	5	I path B baseband input/output
REFAGC	6	AGC reference resistor
GNDIF2	7	I/Q modulator and I/Q demodulator ground 2
RXIIFA	8	RX IF input A to AGC amplifier
RXIIFB	9	RX IF input B to AGC amplifier
V_{CCIF2}	10	I/Q modulator and I/Q demodulator supply voltage 2
TXON	11	TX mode control pin
V_{CCIFLO}	12	IF LO supply voltage
IFLOC	13	IF LO signal input from IF VCO resonator
IFLOE	14	IF LO signal input from IF VCO resonator
GNDIFLO	15	IF LO ground
CPOIF	16	IF charge pump output
GNDCPIF	17	IF charge pump and phase detector ground
V_{CCCPIF}	18	IF charge pump and phase detector supply voltage
EN	19	serial programming bus enable control pin
DATA	20	serial programming bus data input
CLK	21	serial programming bus clock input
GNDSYN	22	synthesizer ground
REFIN	23	13 MHz reference input
V_{CCSYN}	24	synthesizer supply voltage
V_{CCCPRF}	25	RF charge pump and phase detector supply voltage
CPORF	26	RF charge pump output
GNDCP	27	RF charge pump ground
SYNON	28	SYN mode control pin
V_{CCRFLO}	29	RF LO section supply voltage
RFLOC	30	LO signal input from RF VCO
RFLOE	31	LO signal input from RF VCO
GNDRFLO	32	RF LO section ground
RXON	33	RX mode control pin
GNDPHD	34	transmit modulation loop charge pump ground
PHDOUT	35	charge pump output
V_{CCPHD}	36	transmit modulation loop charge pump supply voltage
RESEXT	37	reference resistor for transmit modulation loop
TXIRFA	38	TX RF VCO signal input
TXIRFB	39	TX RF VCO signal input
V_{CCRF}	40	RF receiver and transmit modulation loop supply voltage
RXIRFA	41	RF receiver input A
RXIRFB	42	RF receiver input B
GNDRF	43	RF receiver and transmit modulation loop ground
TXIFA	44	transmit IF external filter A
TXIFB	45	transmit IF external filter B
RXOIFA	46	receiver IF output A
RXOIFB	47	receiver IF output B
GNDIF1	48	IF section of RF receiver ground 1

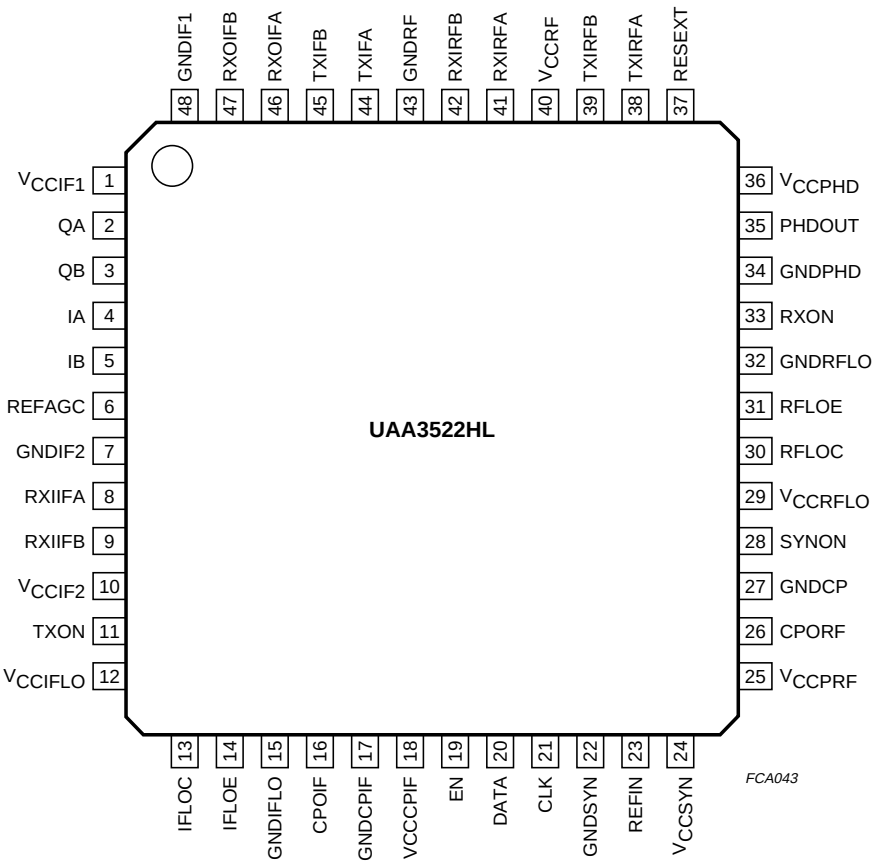


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

RF receiver

The receiver front-end converts the aerial RF signal, in the GSM band (925 to 960 MHz), to an IF signal of approximately 200 MHz. The first stage of the receiver is a symmetrical LNA that is matched to 50 Ω by an external balun. The LNA is followed by an image rejection mixer which suppresses the image by more than 30 dB. It comprises two mixers in parallel driven by 0° and 90° quadrature LO signals respectively. The IF signal from one mixer is shifted by 90° with respect to the IF signal from the other mixer, then both signals are added together to cancel out the image signal. The resultant IF signal is fed to the output via a high output impedance open-collector stage which drives an external Surface Acoustical Wave (SAW) filter which selects the required channel.

I/Q demodulator

The signal from the SAW filter enters the I/Q demodulator section. In addition to I/Q demodulation, this section performs Automatic Gain Control (AGC) over a range of 60 dB to maintain a constant output level irrespective of the antenna input level, and also applies additional channel selectivity at the baseband stage using an integrated high-order low-pass filter.

The AGC amplifier output can be adjusted for a static offset of less than 50 mV. Its design prevents the offset from varying by more than ±5 mV. To allow a more accurate offset calibration, the RF LNA can be switched off to ensure that no IF signal is present at the AGC amplifier input during the offset measurement.

I/Q modulator

Baseband I and Q signals are applied to the I/Q modulator which shifts the modulation spectrum up to the transmit IF. The I/Q modulator is designed for low harmonic distortion, low carrier leakage and high image rejection to keep the phase error as small as possible. Its IF output is loaded by an integrated low-pass filter and by an external LC tuned-circuit to prevent unwanted spurii from entering the phase detector in the transmit modulation loop.

Transmit modulation loop

The analog transmit modulation loop comprises an on-chip offset mixer and simple phase detector in switching mode (triangular transfer function) forming an analog PLL with an off-chip loop filter and transmit RF VCO.

The phase detector output transfers the modulation of the I/Q IF signal to the off-chip transmit RF VCO making the analog PLL act as a tracking filter. A PLL of at least third-order is needed to meet noise requirements at 20 MHz offset from the carrier.

RF and IF LO sections

The active components required for the design of a low noise IF VCO are provided on-chip. Pins IFLOC and IFLOE connect the on-chip IF VCO components to an external resonator and feedback circuit.

A divider and phase shifter divides the frequency of the IF VCO signal by 2 and splits it into two signals having phases of respectively 0° and 90° which are both fed to the I/Q modulator and to the I/Q demodulator. The IF VCO frequency is twice the IF to suppress the effects of self-mixing and parasitic VCO modulation.

Pins TXIRFA and TXIRFAB connect an external receive RF VCO module to the on-chip RF LO section. This section includes a RC phase shifter which splits the RF VCO signal into two signals having phases of respectively 0° and 90° which are both fed to the RX image rejection mixer.

Dual PLL

An on-chip high performance dual PLL synthesizes the frequencies of the receive RF VCO and IF VCO signals. Very low close-in phase noise is achieved which provides a wide PLL bandwidth with a short settling time.

A dual programmable divider chain reduces the frequency of the receive RF and IF LO signals to 200 kHz and 1 MHz respectively. A digital phase/frequency detector compares their phases to a reference signal derived from an external 13 MHz clock signal. Phase error information is fed back to both VCOs via the dual charge pump circuit which adjusts the phase of each VCO signal by either ‘sinking’ current into, or ‘sourcing’ current from, its loop filter capacitor, phase locking both RF and IF loops. The very low leakage current of the dual charge pump circuit ensures that any spurii are negligible.

Operating modes

BASIC OPERATING MODES

The circuit can be powered on in one of four operating modes in which different parts of the device are enabled or disabled. The four operating modes are called Idle, RX, TX and SYN, and are selected by the hardware control voltage level applied to pins RXON, TXON and SYNON.

The synthesizer, receiver and transmitter cannot all be on at the same time. Table 1 shows which parts of the device are enabled (on) or disabled (off) in each mode.

Table 1 Operating modes

MODE	POWER STATUS		
	SYNTHESIZER	RECEIVER	TRANSMITTER
Idle	off	off	off
SYN	on	off	off
RX	on	on	off
TX	on	off	on

The synthesizer includes the oscillators and LO buffers common to the receive and transmit sections. The receiver includes the RF section and the I/Q demodulator. When the receiver is on, the LNA can be switched off to allow DC offset compensation to be performed. The RF section can also be switched off for DCS applications. See Section “Receiver power status control”.

RECEIVER POWER STATUS CONTROL

- DC offset compensation: This feature allows the DC offset of the receiver output to be set accurately. When the receiver is on, the LNA can be switched off to isolate the antenna input from the I/Q demodulator input. The offset at the I and Q outputs can be independently reduced to less than 50 mV by adequately programming two 5-bit data registers, see Table 4 “Register bit allocation”. The LNA is switched on or off by the status of bit LNA (see Table 2).
- Disabling RF section: For DCS applications, the RF section can be disabled in RX mode. The same IF circuits are used for both GSM and DCS applications to avoid duplication. For DCS applications using the UAA2077XM, for example, the RF section of the UAA3522HL does not have to be powered on. The RF section is enabled or disabled by the status of bit RF when the RX mode is activated (see Table 3).

Table 2 Bit LNA status

BIT LNA STATUS	POWER STATUS OF BIT LNA
0	off
1	on

Table 3 Bit RF status

BIT RF STATUS	POWER STATUS OF RECEIVER RF SECTION IN RX MODE
1	on (GSM)
0	off (DCS)

Programming

SERIAL PROGRAMMING BUS

A simple 3-wire unidirectional serial bus is used for programming the IC. The lines are called DATA, CLK and EN (enable). Programming data is sent to the IC in bursts which are separated from each other by EN. Programming clock edges are ignored until EN goes active LOW. The data is loaded into the addressed register when EN returns inactive HIGH, and when the CLK is in either state, without affecting the data in the register. The register only holds the last 18 bits that are serially clocked into the IC.

Additional leading bits are ignored, and no check is made on the number of clock pulses received. The fully static CMOS design uses virtually no current when the bus is inactive. It can always accept new programming data even when both synthesizers are powered-off.

DATA FORMAT

Data is loaded into the register with the most significant bit (MSB) first. The first 14 bits are data, while the last 4 bits are the register address. The address bits are decoded on the rising edge of EN. This internally generates a load pulse to store the data in the addressed register.
To ensure that data loads correctly after the device has powered-up, EN should be held LOW and only taken HIGH after the appropriate register has been loaded.
The EN pulse is inhibited during the period when data is read by the frequency dividers to prevent divider ratio data from being read incorrectly. This state is guaranteed by always allowing for a minimum EN pulse width after data transfer.

Table 4 Register bit allocation

X = don't care; MSB = Most Significant Bit; LSB = Least Significant Bit.

DATA BITS														ADDRESS BITS			
FIRST BIT													**LAST BIT**				
13	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**3**	**2**	**1**	**0**
X	X	X	X	X	X	MSB	IF LO frequency divider ratio						LSB	0	1	1	0
MSB	RF LO frequency divider ratio												LSB	0	1	0	0
X	X	X	X	X	X	LNA(1)	X	MSB	AGC amplifier gain (RX mode) see Table 5				LSB	0	0	1	1
X	X	MSB	Q output offset adjust			LSB	Q sign (2)	MSB	I output offset adjust			LSB	I sign(2)	0	0	1	0
X	X	X	X	X	IF RD (3)	IF VCO (4)	0	0	RF(5)	X	SYN ON	RX ON	TX ON	0	0	0	1
For test purposes only(6)														0	0	0	0

Notes

1. Bit LNA: 1 = LNA ON in RX mode; 0 = LNA OFF in RX mode.
2. Bits Q sign and I sign = polarity of offset at Q/I channel outputs: 0 = negative offset step (output A with respect to output B); 1 = positive offset step (output A with respect to output B).
3. Bit IF RD: 0 = frequency dividers programmed for GSM applications; 1 = frequency dividers programmed for DCS applications.
4. Bit IF VCO: 0 = IF LO buffer ON (external IF LO source connected); 1 = IF VCO ON (external IF LO source not connected).
5. Bit RF: 1 = RF section ON when RX mode is activated; 0 = RF section OFF when RX mode is activated.
6. This address must not be used. Data bits to be defined.

Table 5 AGC amplifier gain register look-up table
All codes not included in the table are forbidden.

BIT 5 (MSB)	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	AGC AMPLIFIER GAIN (dB)(1)
0	0	0	0	1	1	−1
0	0	0	1	0	0	+1
0	0	0	1	0	1	+3
0	0	0	1	1	0	+5
0	0	0	1	1	1	+7
0	0	1	0	0	0	+9
0	0	1	0	0	1	+11
0	0	1	0	1	0	+13
0	0	1	0	1	1	+15
0	0	1	1	0	0	+17
0	0	1	1	0	1	+19
0	1	0	1	1	0	+21
0	1	0	1	1	1	+23
0	1	1	0	0	0	+25
0	1	1	0	0	1	+27
0	1	1	0	1	0	+29
0	1	1	0	1	1	+31
1	0	0	1	1	1	+33
1	0	1	0	0	0	+35
1	0	1	0	0	1	+37
1	0	1	0	1	0	+39
1	0	1	0	1	1	+41
1	1	0	1	0	0	+43
1	1	0	1	0	1	+45
1	1	0	1	1	0	+47
1	1	0	1	1	1	+49
1	1	1	0	0	0	+51
1	1	1	0	0	1	+53
1	1	1	0	1	0	+55
1	1	1	0	1	1	+57
1	1	1	1	0	0	+59
1	1	1	1	0	1	+61

Note

1. Voltage gain is defined as the differential baseband output voltage (either at pins IA/IB or pins QA/QB) divided by the differential input voltage at pins RXIIFA and RXIIFB.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCn}	supply voltage	–0.3	–	+6	V
P_{tot}	total power dissipation	–	–	1	W
T_{stg}	storage temperature	–40	–	+150	°C
T_{amb}	ambient temperature	–30	–	+70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	65	K/W

DC CHARACTERISTICS

All parameters are guaranteed at V_{CC} = 2.8 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply pins V_{CCIF1}, V_{CCIF2}, V_{CCIFLO}, V_{CCRFLO}, V_{CCSYN}, and V_{CCRF}						
V_{CC}	supply voltage	note 1	2.7	–	3.3	V
Supply pins V_{CCCPIF} and V_{CCCPRF}						
V_{CCCPIF}; V_{CCCPRF}	supply voltage	note 1	2.7	–	4	V
Supply pin V_{CCPHD}						
V_{CCPHD}	supply voltage for charge pump of phase detector in transmit modulation loop	note 1	2.7	–	5.5	V
Supply pins V_{CCIF1}, V_{CCIF2}, V_{CCIFLO}, V_{CCRFLO}, V_{CCSYN}, V_{CCCPIF}, V_{CCCPRF}, V_{CCPHD} and V_{CCRF}						
$I_{CC(pd)(tot)}$	total power-down supply current	pins TXON, RXON, SYNON = LOW-level; pins EN, DATA, CLK = HIGH-level; note 2	–	40	100	µA
RF receiver IF section (pins V_{CCIF1}, RXOIFA and RXOIFB)						
$I_{CC(RFIF)(RX)}$	RF receiver and IF section total supply current	RX mode active	–	16.9	21.9	mA
IF section supply (pin V_{CCIF2})						
$I_{CCIF(RX)}$	I/Q demodulator supply current	RX mode active	–	10.1	14.1	mA
$I_{CCIF(TX)}$	I/Q modulator supply current	TX mode active	–	7.4	9.6	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF LO section supply (pin V_{CCIFLO})						
$I_{CCIFLO(SYN)}$	IF LO section supply current	SYN mode active	–	5.5	6.6	mA
IF charge pump supply (pin V_{CCCPIF})						
$I_{CCCPIF(SYN)}$	IF LO charge pump supply current	SYN mode active; phase locked	–	1.2	1.5	mA
Synthesizer supply (pin V_{CCSYN})						
$I_{CCSYN(SYN)}$	synthesizer supply current	SYN mode active	–	5	6.7	mA
RF LO charge pump and phase detector supply (pin V_{CCCPRF})						
$I_{CCCPRF(SYN)}$	RF LO charge pump supply current	SYN mode active; phase locked	–	1.4	1.7	mA
RF LO supply (pin V_{CCRFLO})						
$I_{CCRFLO(RX)}$	RF LO buffer receive section supply current	SYN mode active; RX mode active	–	8.6	10.9	mA
$I_{CCRFLO(TX)}$	RF LO buffer transmit section supply current	TX mode active	–	9.8	12.6	mA
Closed-loop charge pump supply (pin V_{CCPHD})						
$I_{CCPHD(TX)}$	closed-loop charge pump supply current	TX mode active; phase locked	–	5.6	7.5	mA
RF receiver and transmit modulation loop supply (pin V_{CCRF})						
$I_{CCRF(RX)on}$	supply current of RF receiver (receive IF section disconnected) with RX image rejection mixer and LNA ON	RX mode active; LNA ON	–	17.9	23.6	mA
$I_{CCRF(RX)off}$	supply current of RF receiver (receive IF section disconnected) with RX image rejection mixer and LNA OFF	RX mode active; LNA OFF	–	11.2	14.6	mA
$I_{CCRF(TX)}$	supply current of transmit modulation loop (charge pump disconnected)	TX mode active	–	6.1	7.6	mA
Pins V_{CCIF1}, V_{CCIF2}, V_{CCIFLO}, V_{CCCPIF}, V_{CCSYN}, V_{CCCPRF}, V_{CCPHD}, V_{CCRF} and RXOIFA, RXOIFB						
$I_{CC(RX)}$	supply current in RX mode	RX mode active; note 3	–	44.9	59.6	mA
$I_{CC(TX)}$	supply current in TX mode	TX mode active; note 3	–	20.3	26.4	mA
$I_{CC(SYN)}$	supply current in SYN mode	SYN mode active; note 3	–	21.7	27.4	mA
Pins IA IB, QA and QB						
$V_{O(IQ)}$	DC voltage at I/Q baseband outputs	TX mode active	1.125	1.25	1.325	V
$V_{I(IQ)}$	DC voltage at I/Q baseband inputs	RX mode active	1.175	1.25	1.35	V
Logic levels (pins EN, DATA, CLK, TXON, RXON and SYNON)						
V_{IH}	HIGH-level input voltage		1.9	–	–	V
V_{IL}	LOW-level input voltage		–	–	0.7	V

Notes:

1. V_{CCCPRF}, V_{CCCPIF} and V_{CCPHD} must be equal to, or greater than, the other supply voltages. The other supply voltages must be equal.
2. 'HIGH-level' means the control pin voltage must be equal to the supply voltage V_{CC}. 'LOW-level' means the control pin voltage must be equal to the supply ground.
3. $I_{CC(RX)} = I_{CC(RFIF)(RX)} + I_{CCIF(RX)} + I_{CCRF(RX)}$; $I_{CC(TX)} = I_{CCIF(TX)} + [I_{CCRFLO(TX)} - I_{CCRFLO(RX)}] + I_{CCPHD(TX)} + I_{CCRF(TX)}$; $I_{CC(SYN)} = I_{CCIFLO(SYN)} + I_{CCCPIF(SYN)} + I_{CCPLL(SYN)} + I_{CCCPRF(SYN)} + I_{CCRFLO(SYN)}$.

AC CHARACTERISTICS

All parameters are guaranteed at V_{CC} = 2.8 V; T_{amb} = 25 °C; unless specified otherwise.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF receiver section; measured in a 50 Ω impedance system, including external input/output baluns and matching networks to 50 Ω (see Fig.3)						
RF RECEIVER INPUTS (PINS RXIRFA AND RXIRFB)						
$f_{i(RF)(GSM)}$	GSM band RF input frequency		925	–	960	MHz
$R_{i(dif)}$	differential input resistance		–	146	–	Ω
$C_{i(dif)}$	differential input capacitance		–	0.85	–	pF
S_{11}	input power matching	note 1	–	–15	–10	dB
$P_{i(spur)}$	level of spurious input power due to LO leakage		–	–50	–40	dBm
RECEIVER IF OUTPUT (PINS RXOIFA AND RXOIFB)						
$f_{o(IF)}$	IF output frequency	LO > RF	–	200	–	MHz
$R_{L(m)}$	matched load resistance	differential; note 2	–	1	–	kΩ
$G_{conv(p)}$	power conversion gain	into specified matched load resistance; note 1	23	24.5	27	dB
G_{ripple}	gain ripple	over specified frequency range; note 3	–0.5	–	+0.5	dB
$\Delta G/\Delta T$	gain variation with temperature	note 6	–60	–30	–	dBm/K
F	noise figure	for $R_{i(dif)}$; notes 1, 3 and 4	–	3.45	3.85	dB
CP1	–1 dB input compression point referenced to input	note 1				
		at T_{amb} = 25 °C	–23.5	–	–	dBm
		over temperature range	–24.2	–	–	dBm
IP_3	third-order intercept point referenced to input	note 1	–18	–	–	dBm
DES_{3dB}	3 dB desensitization point referenced to input	$\Delta f_{i(RF)}$ = 3 MHz RF input power = –101 dBm; note 1	–25	–	–	dBm

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IR	image rejection	$f_{o(IF)}$ = 200 MHz; note 1	30	35	–	dB
G_{off}	output isolation in off-state	bit LNA = 0; notes 1 and 5	60	70	–	dB
Receiver IF section (AGC and baseband filter); the impedance of the source, input balun, matching network and specified input is 50 Ω						
IF INPUT TO AGC AMPLIFIER (PINS RXIIFA AND RXIIFB)						
$f_{i(IF)}$	IF input frequency		–	200	–	MHz
$R_{i(dif)}$	differential input resistance		–	1	–	kΩ
$P_{i(m)}$	input power matching	note 1	–	–15	–10	dB
BASEBAND INPUT/OUTPUT; RX MODE (PINS IA, IB, QA AND QB)						
$G_{conv(dif)(min)}$	differential voltage conversion gain per channel; gain set to minimum	notes 1 and 7	–2.5	–0.5	+1.5	dB
$G_{conv(dif)(max)}$	differential voltage conversion gain per channel; gain set to maximum		59.5	61.5	63.5	dB
$G_{conv(step)}$	voltage conversion step gain	note 1	–	2	–	dB
ΔG_{I-Q}	gain difference between I and Q paths	note 1	–	–	0.8	dB
$\Delta\varphi$	quadrature-phase error between I and Q paths		–5	–	+5	deg
G_L	gain control linearity	note 1	–2	–	+2	dB
		notes 1 and 11	–3	–	+3	dB
		within any 20 dB gain range	–1	–	+1	dB
F	noise figure	$G_{conv(dif)(max)}$; notes 1 and 9	–	–	9	dB
		$G_{conv(dif)(min)}$; notes 1 and 9	–	–	61	dB
IP_3	third-order intercept point referenced to input	$G_{conv(dif)(max)}$ = 61 dB; note 8	–42	–38	–	dBm
CP1	–1 dB compression point referenced to input	$G_{conv(dif)(min)}$; note 8	–4	0	–	dBm
$CP1_{adjacent}$	–1 dB compression point for adjacent channels referenced to input	G_{conv} = 49 dB; notes 7 and 6 $\Delta f_{mod} = n \times 200$ kHz; n = 1, 2, 3	–45	–40	–	dBm
$B_{bf(-1dB)}$	–1 dB baseband filter bandwidth	note 10	67.7	–	–	kHz
$\Delta t_{d(g)}$	group delay variation	DC < Δf_{mod} < 67.7 kHz	–	1.5	–	µS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{bf5}	baseband filter attenuation (fifth-order Butterworth)	note 10;				
		Δf_{mod} = 140 kHz	8	11	–	dB
		Δf_{mod} = 200 kHz	19	25	–	dB
		Δf_{mod} = 400 kHz	36	55	–	dB
		Δf_{mod} = 600 kHz	44	–	–	dB
$V_{o(pin)(peak)(max)}$	maximum peak output voltage per pin giving a total harmonic distortion of less than 3% at G_{conv} >7	differential resistance between QA/QB or IA/IB > = 180 kΩ; note 1	0.75	–	–	V
V_{OO}	output offset voltage adjustment	G_{conv} = 31 dB	–60	–	+60	mV
LSB_{offset}	LSB offset adjustment		–	50	100	mV
ΔV_{offset}	offset variation	gain from $G_{conv(dif)(min)}$ to $G_{conv(dif)(max)}$	–10	–	+10	mV
Transmit IF section; general conditions: $V_{mod(peak)}$ = 0.25 V; $V_{I(IQ)} = V_{O(IQ)}$ = 1.25 V; f_{mod} = 67.7 kHz						
BASEBAND INPUT/OUT; TX MODE (PINS IA, IB, QA AND QB)						
Δf_{mod}	modulation frequency	gain = –3 dB gain	0	–	2	MHz
$V_{mod(peak)}$	modulation level (peak value)	single-ended	0.225	0.25	0.275	V
DR_i	dynamic input resistance	single-ended per pin	–	12.5	–	kΩ
TRANSMITTER IF LC TUNED CIRCUIT (PINS TXIFA AND TXIFB)						
$f_{o(IF)}$	IF output frequency		–	200	–	MHz
LO_{out}	local oscillator feedthrough level	$f_{o(IF)}$ = 200 MHz	–	–40	–30	dBc
P_o	transmit power without LC tuned circuit	$f_{o(IF)}$ = 200 MHz ± 67.7 kHz; measured through a balun; note 12	–	–16	–	dBm
$IM2_o$	level of second-order image products	$f_{o(IF)}$ = 200 MHz ± 2 × 67.7 kHz; note 12	–	–48	–45	dBc
$IM3_o$	level of third-order image products	$f_{o(IF)}$ = 200 MHz ± 3 × 67.7 kHz; note 12	–	–55	–50	dBc
IM_o	image level	$f_{o(IF)}$ = 200 MHz – 67.7 kHz; note 12	–	–34	–	dBc
φ_N	phase noise output power density	f_{offset} = 400 kHz	–	–	–125	dBc/Hz
		f_{offset} = 10 MHz	–	–140	–133	dBc/Hz
Transmit modulation loop section; General conditions: $V_{mod(peak)}$ = 0.25 V; $V_{I(IQ)} = V_{O(IQ)}$ = 1.25 V; f_{mod} = 67.7 kHz						
OFFSET MIXER; GSM BAND (PINS TXIRFA AND TXIRFB)						
$f_{i(RF)(TX)}$	TX RF VCO input frequency		880	–	915	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{i(pin)}$	input resistance per pin	note 13	–	100	–	Ω
$C_{i(pin)}$	input capacitance per pin		–	1	–	pF
P_i	input power	symmetrical	–14.5	–10	–5.5	dBm
		single-ended	–11.5	–7	–2.5	dBm
S_{11}	input power matching	note 1	–	–15	–10	dB
LO_L	reverse isolation local oscillator leakage		–	–	–40	dBm
OFFSET MIXER; DCS BAND (PINS TXIRFA AND TXIRFB)						
$f_{i(RF)(TX)}$	TX RF VCO input frequency		1710	–	1785	MHz
$R_{i(pin)}$	input resistance per pin	note 13	–	100	–	Ω
$C_{i(pin)}$	input capacitance per pin		–	1	–	pF
P_i	input power	symmetrical	–14.5	–10	–5.5	dBm
		single-ended	–11.5	–7	–2.5	dBm
S_{11}	input power matching	note 1	–	–15	–10	dB
LO_L	reverse isolation local oscillator leakage		–	–	–40	dBm
PHASE DETECTOR; DCS AND GSM BAND (PIN PHDOUT)						
$I_{cp(max)}$	charge pump maximum sink or source current	R = 270 Ω, 1%; $V_O = ½V_{CCPHD}$	2.2	2.4	2.6	mA
G_{PHD}	phase detector gain		–	2	–	mA/rad
ΔG_{PHD}	phase detector gain variation	$V_O = ½V_{CCPHD}$; note 11	–20	–	+20	%
V_O	output voltage		0.5	–	V_{CCPHD} – 0.5	V
R_o	output resistance	$V_O = ½V_{CCPHD}$	–	10	–	kΩ
N_o	output noise current density	20 kHz < f_{offset} < 20 MHz in lock; note 1	–	–	200	pA/√Hz
I_{sweep}	VCO sweeping source current	$V_O = ½V_{CCPHD}$	0.4	0.55	0.7	mA
$R_{o(off)}$	output resistance to ground when powered down	TX mode disabled	–	1	–	kΩ
$SPUR_{4fm}$	level of spurious signal at four times the wanted f_{mod} signal	f_{mod} = 67.7 kHz; $f_{o(RF)(GSM)}$ = 880 MHz to 915 MHz; $f_{o(RF)(DCS)}$ = 1710 MHz to 1785 MHz	–	–	–48	dBc
$SPUR_{8fm}$	level of spurious signal at eight times the wanted f_{mod} signal		–	–	–55	dBc
LO_{out}	local oscillator feedthrough level	at f_{RF}	–	–40	–32	dBc
IM_o	image level	at f_{RF}; note 1	–	–38	–35	dBc

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF LO buffer; measured and guaranteed on evaluation board						
RF LO SOURCE CONNECTED TO PIN RFLOE (see Fig.7)						
R_i	input resistance		–	50	–	Ω
C_i	input capacitance		–	1	–	pF
S_{11}	input power matching		–	–15	–10	dB
$P_{i(LO)}$	input power acceptable from the RF LO source		–7	–3	2	dBm
IF LO; measured and guaranteed on evaluation board						
EXTERNAL RESONATOR CIRCUIT CONNECTED TO PINS IFLOC AND IFLOE						
f_{osc}	oscillation frequency	note 1	–	400	–	MHz
$V_{osc(peak)}$	peak voltage excursion limit at IFLOC (collector)	V_{CCIFLO} = 2.8 V; see Fig.5	1	–	1.5	V
φ_N	phase noise	f_{offset} = 400 kHz; $f_{LO(IF)}$ = 400 MHz	–	–	–125	dBc/Hz
Δf_{TROFF}	frequency variation with supply voltage (pushing)	note 14	–	–	1	MHz/V
Δf_{TRON}	frequency variation between RX on and RX off (pulling)		–	–	10	kHz
IF LO buffer; measured and guaranteed on evaluation board						
IF SOURCE CONNECTED TO PIN IFLOE						
R_i	input resistance		–	50	–	Ω
C_i	input capacitance		–	1	–	pF
$P_{i(m)}$	input power matching		–	–15	–10	dB
P_{IF}	power available from the IF source	see Fig.5	–8	–5	–2	dBm
RF and IF synthesizer VCOs						
REFERENCE FREQUENCY INPUT (PIN REFIN)						
f_{ref}	reference frequency		–	13	–	MHz
$V_{i(fref)(rms)}$	input voltage level (RMS value)		80	–	250	mV
R_i	input resistance	f_{ref} = 13 MHz	–	10	–	kΩ
C_i	input capacitance		–	1	–	pF
RF SYNTHESIZER; GSM AND DCS MODES (PINS RXIRFA, RXIRFB AND CPORF)						
$f_{LO(RF)}$	RF LO frequency		1040	–	1720	MHz
$f_{ph(comp)}$	phase comparator frequency		–	200	–	kHz
$\varphi_{N(GSM)}$	GSM close-in phase noise	within the closed-loop bandwidth P_{xtal} = 0 dBm; $f_{LO(RF)}$ = 1.1 GHz	–	–82	–75	dBc/Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\varphi_{N(DCS)}$	DCS close-in phase noise	within the closed-loop bandwidth P_{xtal} = 0 dBm; $f_{LO(RF)}$ = 1.6 GHz	–	–79	–74	dBc/Hz
$V_{fph(comp)(spur)}$	phase comparator frequency spurii breakthrough level	f_{offset} = 200 kHz; second-order loop filter closed-loop bandwidth = 11 kHz	–	–75	–60	dBc
$I_{o(cp)}$	charge pump output current	sink or source current; at $V_{o(cp)}$	1.8	2.2	2.6	mA
$I_{L(cp)(off)}$	charge pump leakage current in off-state		–5	–	+5	nA
$V_{o(cp)}$	charge pump output voltage	$I_{o(cp)}$ within specified values	0.4	–	V_{CC} – 0.4	V
IF SYNTHESIZER (PINS IFLOC, IFLOE AND CPOIF)						
$f_{LO(IF)}$	IF LO frequency		380	400	440	MHz
$f_{ph(comp)}$	phase comparator frequency		–	1	–	MHz
φ_N	close-in phase noise	within the closed-loop bandwidth P_{xtal} = 0 dBm; $f_{LO(IF)}$ = 400 MHz	–	–95	–85	dBc/Hz
$V_{fph(comp)(spur)}$	phase comparator frequency spurii breakthrough level	f_{offset} = 1 MHz; second order loop filter closed-loop bandwidth = 25 kHz	–	–75	–60	dBc
$I_{o(cp)}$	charge pump output current	sink or source current; at $V_{o(cp)}$	0.75	1.1	1.35	mA
$I_{L(cp)(off)}$	charge pump leakage current in off-state		–5	–	+5	nA
$V_{o(cp)}$	charge pump output voltage		0.4	–	V_{CC} – 0.4	V
Frequency dividers						
$D/D_{fLO(RF)}$	RF frequency programmable divider ratio		5200	–	8600	
$D/D_{fLO(IF)}$	IF frequency programmable divider ratio		–	200	–	
$D/D_{fref(RF)}$	RF reference frequency divider ratio	fixed ratio	–	65	–	
$D/D_{fref(IF)}$	IF reference frequency divider ratio		–	13	–	
General IC specification						
t_{ON}	switch-on time	90% of the final current	–	–	10	µs

Notes

1. Measured and guaranteed only on UAA3522 evaluation board.
2. The IF output has open collectors which are supplied via external inductors. External resistors are also needed to set the output impedance and to match the IF output to the specified load resistance R_L (see Fig.3).
3. Value includes losses due to the printed circuit board and balun.
4. Value is guaranteed only for the $P_{i(LO)}$ typ.
5. For a given RF input power, the value is the difference in the power measured at the IF output when the LNA is switched on and when it is switched off.
6. This value is guaranteed within the temperature range –10 to +70 °C.
7. Voltage gain is defined as the differential baseband output voltage (either at pins IA/IB or pins QA/QB) divided by the differential input voltage at pins RXIIFA and RXIIFB.
8. Value refers to differential voltage at pins RXIIFA and RXIIFB (1 kΩ input impedance).
9. Value includes printed circuit board and balun losses.
10. R_{REFAGC} = 18 kΩ, 1%.
11. Guaranteed at T_{amb} = –30 to +70 °C.
12. With specified LC tuned circuit (33 nH, 15 pF) connected as shown in Fig.4.
13. Defined for the typical input power.
14. Oscillator configured as shown in the evaluation board diagram Fig.7.

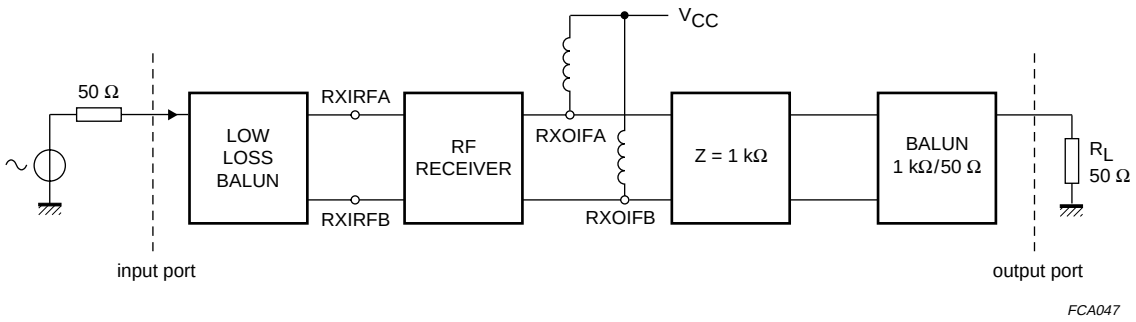


Fig.3 RF receiver test principle.

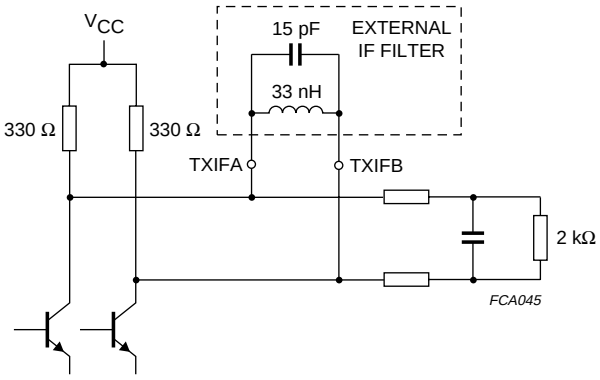


Fig.4 I/Q modulator output.

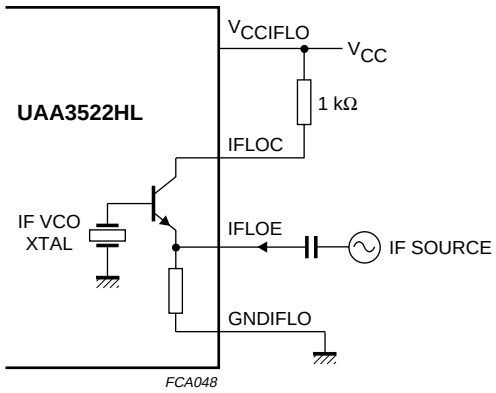


Fig.5 Evaluating IF LO buffer.

SERIAL TIMING CHARACTERISTICS

General conditions: V_{CC} = 2.8 V; T_{amb} = 25 °C; see Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock (pin CLK)					
t_r	rise time	–	10	40	ns
t_f	fall time	–	10	40	ns
$T_{cy(clk)}$	clock cycle time	100	–	–	ns
Enable programming (pin EN)					
$t_{d(ENL-CLKH)}$	delay from enable active to rising clock edge	40	–	–	ns
$t_{d(CLKL-ENH)}$	delay from enable inactive to last falling clock edge	20	–	–	ns
$t_{W(reg)(min)}$	minimum inactive pulse width when consecutively programming two different registers	150	–	–	ns
$t_{W(IFLO)(min)}$	minimum inactive pulse width when consecutively programming two IF divider ratios	150	–	–	ns
$t_{W(RFLO)(min)}$	minimum inactive pulse width when consecutively programming two RF divider ratios	500	–	–	ns
$t_{su(ENH-CLKH)}$	enable set-up time to next rising clock edge	20	–	–	ns
Register serial input data (pin DATA)					
$t_{su(DATA-CLK)}$	set-up time DATA to CLK	20	–	–	ns
$t_{h(DATA-CLK)}$	hold time DATA to CLK	20	–	–	ns

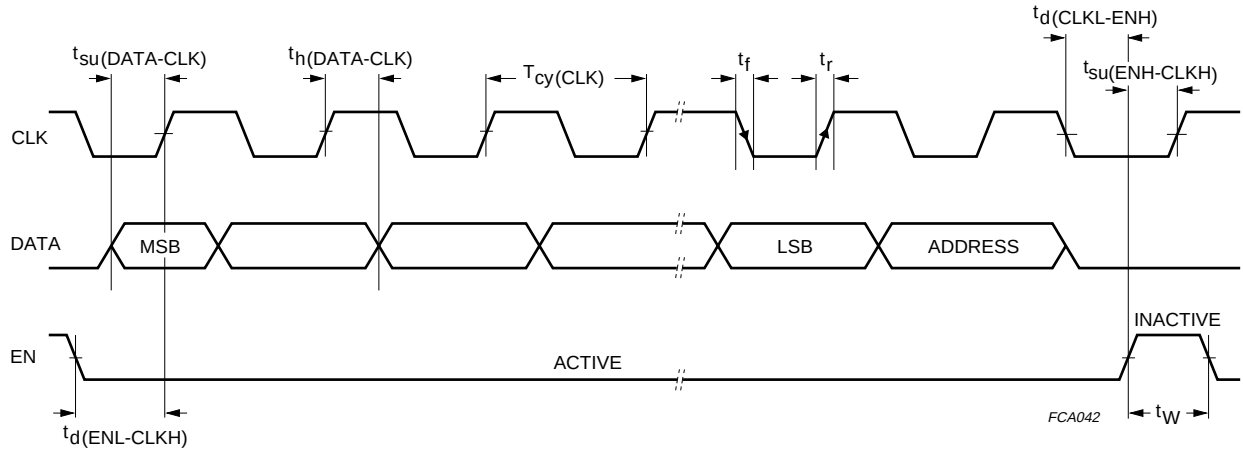
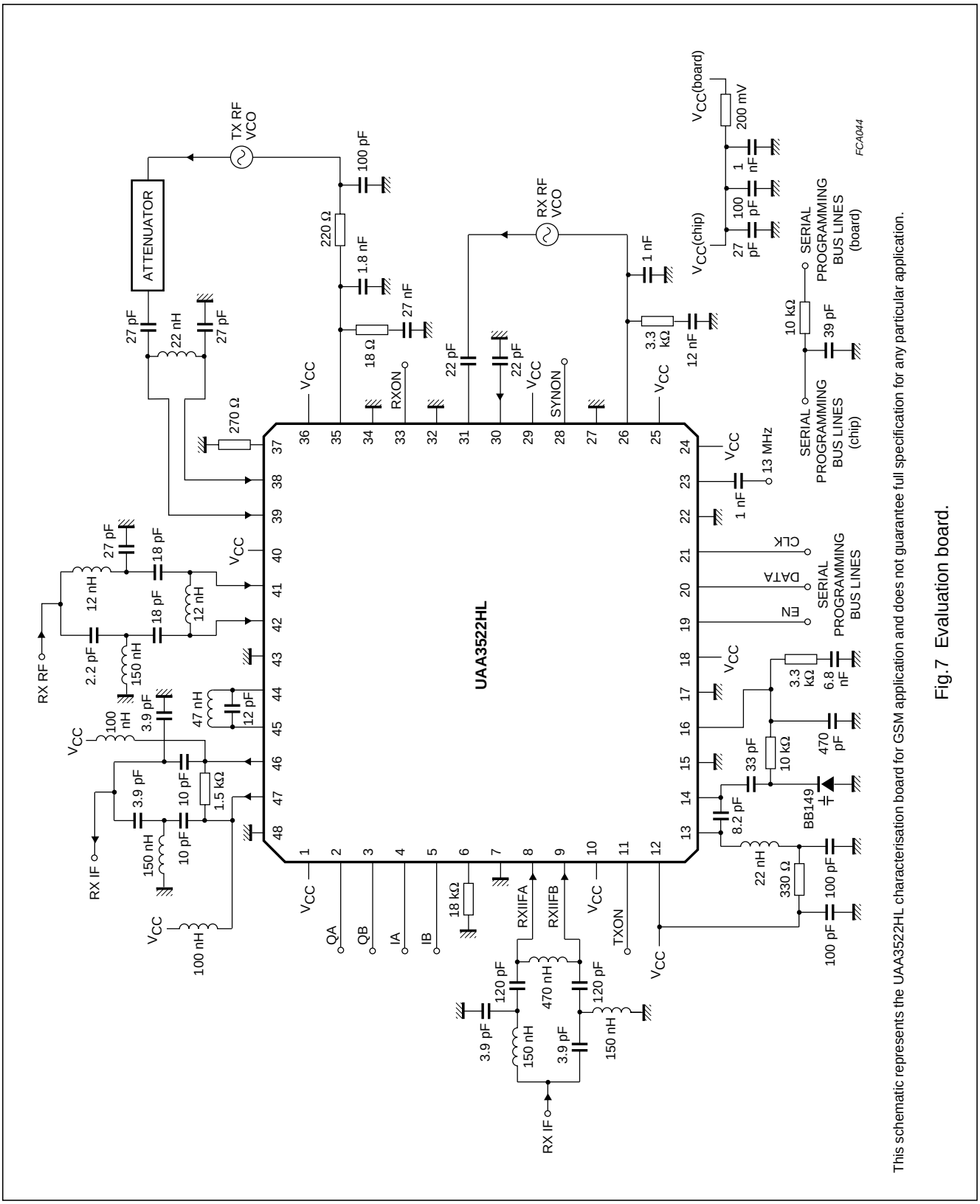


Fig.6 Serial bus timing diagram.

APPLICATION INFORMATION



This schematic represents the UAA3522HL characterisation board for GSM application and does not guarantee full specification for any particular application.

Fig.7 Evaluation board.

Typical application

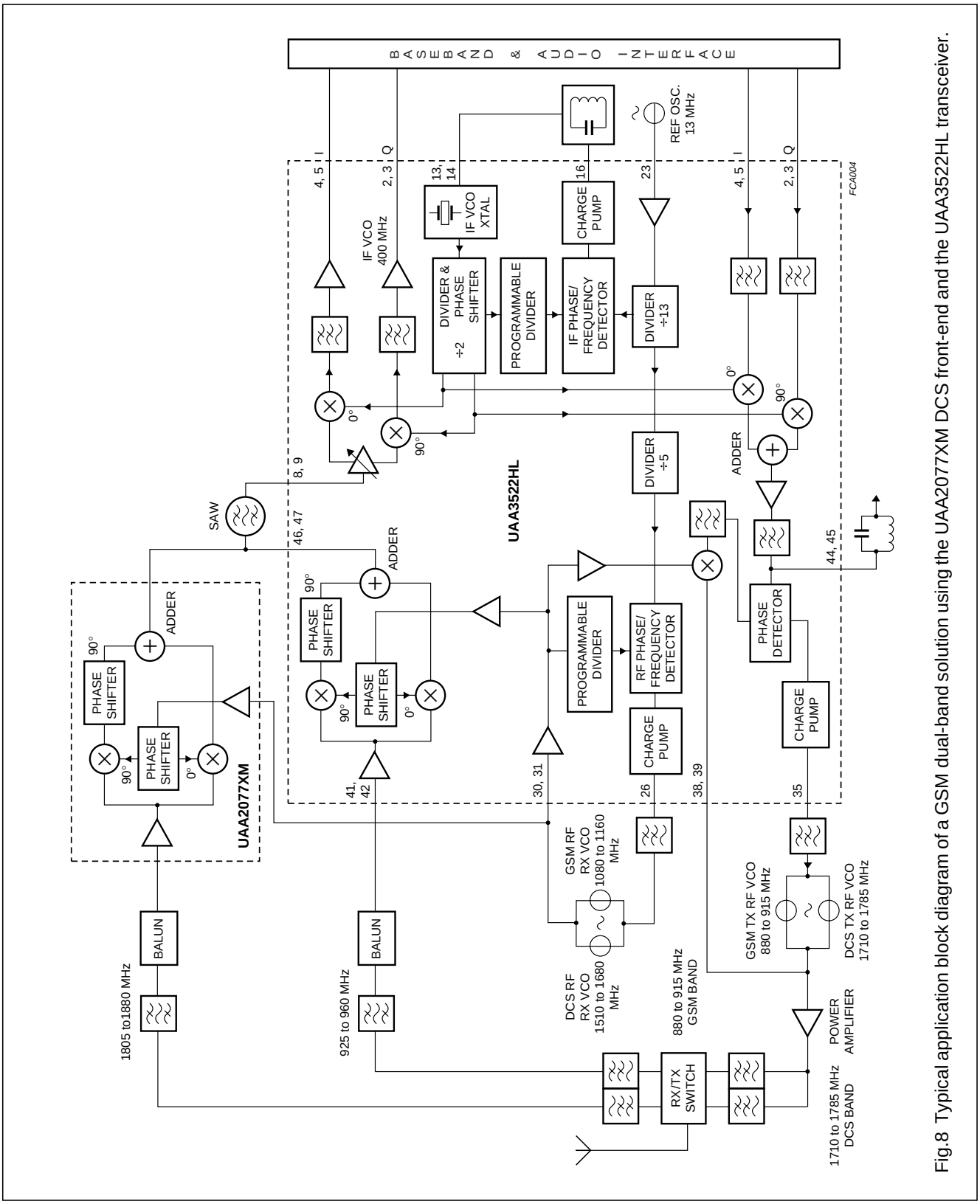
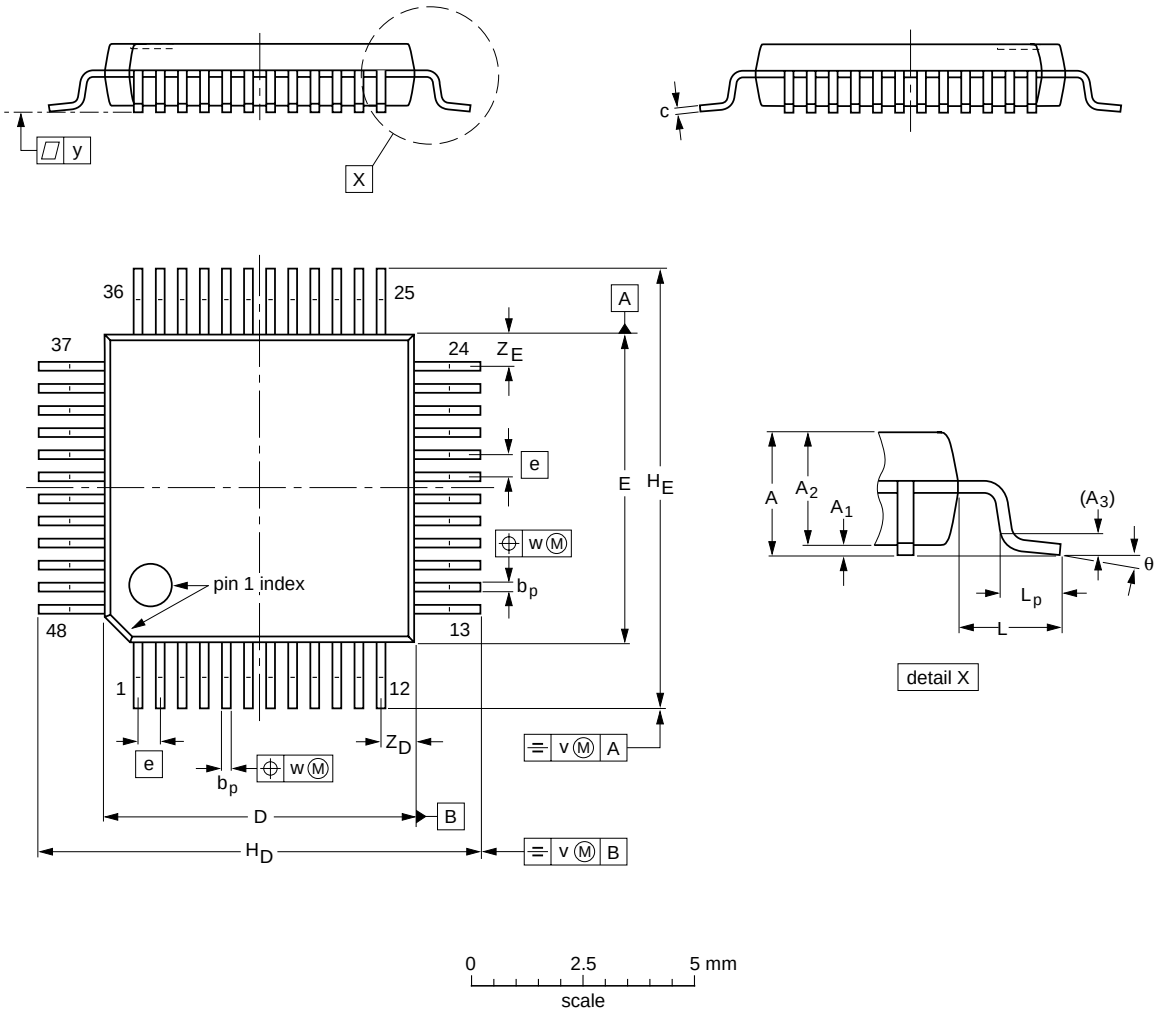


Fig.8 Typical application block diagram of a GSM dual-band solution using the UAA2077XM DCS front-end and the UAA3522HL transceiver.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 3341 299, Fax.+381 11 3342 553

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands 403506/01/pp28 Date of release: 2000 Feb 18 Document order number: 9397 750 06451

Let's make things better.

Philips Semiconductors

PHILIPS

PHILIPS