DATA SHEET

UBA2014
600 V driver IC for HF fluorescent lamps

Product specification

2002 May 16

Philips
Semiconductors

PHILIPS

600 V driver IC for HF fluorescent lamps UBA2014

FEATURES

- Adjustable preheat time
- Adjustable preheat current
- Current controlled operating
- Single ignition attempt
- Adaptive non-overlap time control
- Integrated high-voltage level-shift function
- Power-down function
- Protection against lamp failures or lamp removal
- Capacitive mode protection.

APPLICATIONS

The circuit topology enables a broad range of ballast applications at different mains voltages for driving lamp types from e.g. T8, T5, PLC, T10, T12, PLL and PLT.

GENERAL DESCRIPTION

The IC is a monolithic integrated circuit for driving electronically ballasted fluorescent lamps, with mains voltages up to 277 V (RMS) (nominal value).

The circuit is made in a 650 V BCD power-logic process. It provides the drive function for the 2 discrete power MOSFETs.

Beside the drive function the IC also includes the level-shift circuit, the oscillator function, a lamp voltage monitor, a current control function, a timer function and protections.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA2014T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
UBA2014P	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1

QUICK REFERENCE DATA

All voltages are referenced to GND; V_{DD} = 13 V; $V_{FVDD} - V_{SH}$ = 13 V; T_{amb} = 25 °C; unless otherwise specified; see Chapter “Application information”.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
High-voltage supply						
V_{HS}	high side supply voltage	I_{HS} < 30 μA; t < 1 s	–	–	600	V
Start-up state						
$V_{DD(start)}$	oscillator start voltage		12.4	13.0	13.6	V
$V_{DD(stop)}$	oscillator stop voltage		–	9.1	–	V
$I_{DD(start)}$	start-up current	V_{DD} < $V_{DD(start)}$	–	170	200	μA
Reference voltage						
V_{Vref}	reference voltage	I_L = 10 μA	–	2.95	–	V
Voltage controlled oscillator						
f_{max}	maximum bridge frequency		–	100	–	kHz
f_{min}	minimum bridge frequency		38.9	40.5	42.1	kHz
Output drivers						
$I_{source(GH)}$	output driver source current	$V_{GH} - V_{SH}$ = 0; V_{GL} = 0	–	180	–	mA
$I_{sink(GH)}$	output driver sink current	$V_{GH} - V_{SH}$ = 13 V	–	300	–	mA
Preheat current sensor						
V_{ph}	preheat voltage level		–	0.60	–	V
Lamp voltage sensor						
$V_{lamp(fail)}$	lamp fail voltage level at pin LVS		0.77	0.81	0.85	V
$V_{lamp(max)}$	maximum lamp voltage level at pin LVS		1.44	1.49	1.54	V
Average current sensor						
V_{offset}	offset voltage	V_{CS} = 0 to 2.5 V	–2	0	+2	mV
g_m	transconductance	f = 1 kHz	–	3800	–	μA/mV
Timer						
t_{ph}	preheat time	C_{CT} = 330 nF; R_{IREF} = 33 kΩ	1.6	1.8	2.0	s
$V_{OL(CT)}$	LOW-level output voltage at pin CT		–	1.4	–	V
$V_{OH(CT)}$	HIGH-level output voltage at pin CT		–	3.6	–	V

BLOCK DIAGRAM

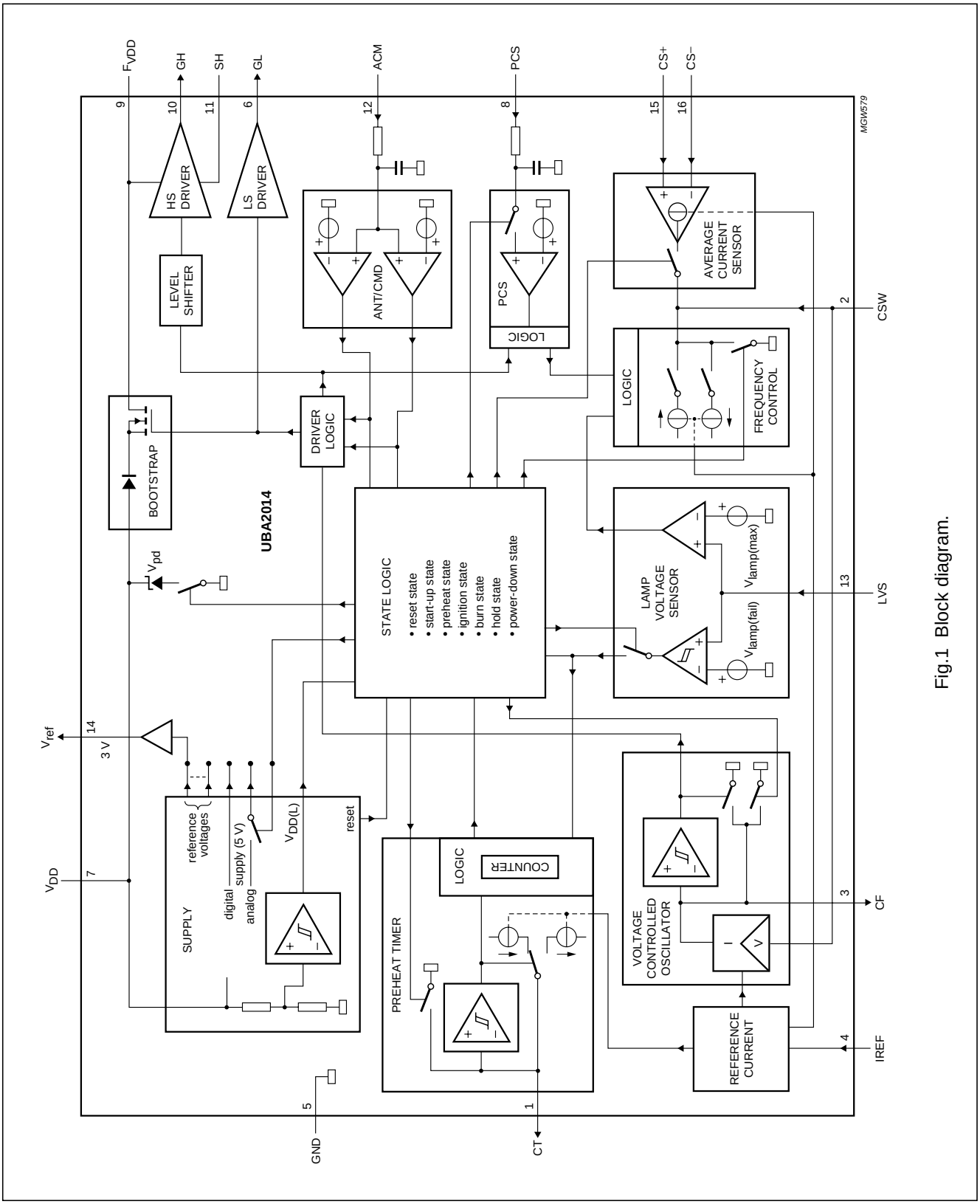


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CT	1	preheat timer output
CSW	2	voltage controlled oscillator input
CF	3	oscillator output
IREF	4	internal reference current input
GND	5	ground
GL	6	gate output for the low-side switch
V_{DD}	7	low-voltage supply
PCS	8	preheat current sensor input
F_{VDD}	9	floating supply, supply for the high-side switch
GH	10	gate output for the high-side switch
SH	11	source of the high-side switch
ACM	12	capacitive mode input
LVS	13	lamp voltage sensor input
V_{ref}	14	reference voltage output
CS+	15	positive input for the average current sensor
CS–	16	negative input for the average current sensor

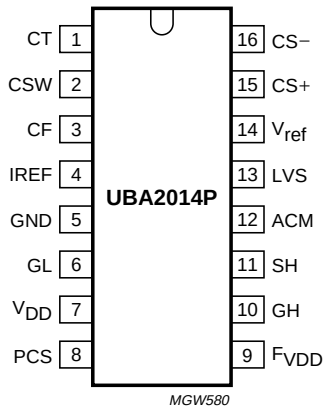


Fig.2 Pin configuration (DIP16).

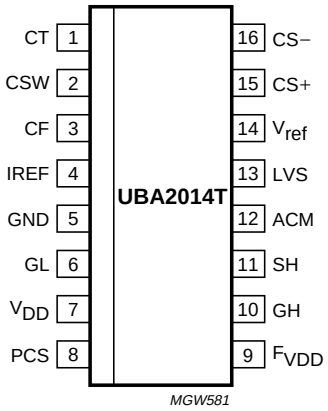


Fig.3 Pin configuration (SO16).

FUNCTIONAL DESCRIPTION

Start-up state

Initial start-up can be achieved by charging the low voltage supply capacitor C7 (see Fig.8) via an external start-up resistor. Start-up of the circuit is achieved under the condition that both half-bridge transistors TR1 and TR2 are non-conductive. The circuit will be reset in the start-up state. If the low voltage supply (V_{DD}) reaches the value of $V_{DD(H)}$ the circuit will start oscillating. A DC reset circuit is incorporated in the High-Side (HS) driver. Below the lock-out voltage at the F_{VDD} pin the output voltage ($V_{GH} - V_{SH}$) is zero. The voltages at pins CF and CT are zero during the start-up state.

Oscillation

The internal oscillator is a Voltage-Controlled Oscillator circuit (VCO) which generates a sawtooth waveform between the CF_{high} level and 0 V. The frequency of the sawtooth is determined by capacitor C_{CF}, resistor R_{IREF}, and the voltage at pin CSW. The minimum and maximum switching frequencies are determined by R_{IREF} and C_{CF}; their ratio is internally fixed. The sawtooth frequency is twice the half-bridge frequency. The UBA2014 brings the transistors TR1 and TR2 into conduction alternately with a duty cycle of approximately 50%. An overview of the oscillator signal and driver signals is illustrated in Fig.4. The oscillator starts oscillating at f_{max}. During the first switching cycle the Low-Side (LS) transistor is switched on. The first conducting time is made extra long to enable the bootstrap capacitor to charge.

Adaptive non-overlap

The non-overlap time is realized with an adaptive non-overlap circuit (ANT). By using an adaptive non-overlap circuit, the application can determine the duration of the non-overlap time and make it optimum for each frequency (see Fig.4). The non-overlap time is determined by the slope of the half-bridge voltage, and is detected by the signal across resistor R16 which is connected directly to pin ACM. The minimum non-overlap time is internally fixed. The maximum non-overlap time is internally fixed at approximately 25% of the bridge period time. An internal filter of 30 ns is included at the ACM pin to increase the noise immunity.

Timing circuit

A timing circuit is included to determine the preheat time and the ignition time. The circuit consists of a clock generator and a counter.

The preheat time is defined by C_{CT} and R_{IREF} and consists of 7 pulses at C_{CT}; the maximum ignition time is 1 pulse at C_{CT}. The timing circuit starts operating after the start-up state, as soon as the low supply voltage (V_{DD}) has reached $V_{DD(H)}$ or when a critical value of the lamp voltage ($V_{lamp(fail)}$) is exceeded. When the timer is not operating C_{CT} is discharged to 0 V at 1 mA.

Preheat state

After starting at f_{max}, the frequency decreases until the momentary value of the voltage across sense resistor R14 reaches the internally fixed preheat voltage level (pin PCS). At crossing the preheat voltage level, the output current of the Preheat Current Sensor circuit (PCS) discharges the capacitor C_{CSW}, thus raising the frequency. The preheat time begins at the moment that the circuit starts oscillating. During the preheat time the Average Current Sensor circuit (ACS) is disabled. An internal filter of 30 ns is included at pin PCS to increase the noise immunity.

Ignition state

After the preheat time the ignition state is entered and the frequency will sweep down due to charging of the capacitor at pin CSW with an internally fixed current; see Fig.5. During this continuous decrease in frequency, the circuit approaches the resonant frequency of the load. This will cause a high voltage across the load, which normally ignites the lamp. The ignition voltage of a lamp is designed above the $V_{lamp(fail)}$ level. If the lamp voltage exceeds the $V_{lamp(fail)}$ level the ignition timer is started.

Burn state

If the lamp voltage does not exceed the $V_{lamp(max)}$ level the voltage at pin CSW will continue to increase until the clamp level at pin CSW is reached; see Fig.5. As a consequence the frequency will decrease until the minimum frequency is reached.

When the frequency reaches its minimum level it is assumed that the lamp has ignited and the circuit enters the burn state. The Average Current Sensor circuit (ACS) will be enabled. As soon as the averaged voltage across sense resistor R14, measured at pin CS–, reaches the reference level at pin CS+, the average current sensor circuit will take over the control of the lamp current. The average current through R14 is transferred to a voltage at the voltage controlled oscillator and regulates the frequency and, as a result, the lamp current.

Lamp failure mode

DURING IGNITION STATE

If the lamp does not ignite, the voltage level increases. When the lamp voltage exceeds the $V_{lamp(max)}$ level, the voltage will be regulated at the $V_{lamp(max)}$ level; see Fig.6. At crossing the $V_{lamp(fail)}$ level the ignition timer was already started. If the voltage at pin LVS is above the $V_{lamp(fail)}$ level at the end of the ignition time the circuit stops oscillating and is forced in a Power-down mode. The circuit will be reset only when the supply voltage is powered-down.

DURING BURN STATE

If the lamp fails during normal operation, the voltage across the lamp will increase and the lamp voltage will exceed the $V_{lamp(fail)}$ level; see Fig.7. At that moment the ignition timer is started. If the lamp voltage increases further it will reach the $V_{lamp(max)}$ level. This forces the circuit to re-enter the ignition state and results in an attempt to re-ignite the lamp. If during restart the lamp still fails, the voltage remains high until the end of the ignition time. At the end of the ignition time the circuit stops oscillating and the circuit will enter in the Power-down mode.

Power-down state

The Power-down state will be entered if, at the end of the ignition time, the voltage at pin LVS is above $V_{lamp(fail)}$. In the Power-down mode the oscillator will be stopped and both TR1 and TR2 will be non-conductive. The V_{DD} supply is internally clamped. The circuit is released from the Power-down state by lowering the low voltage supply below $V_{DD(reset)}$.

Capacitive mode protection

The signal across R16 also gives information about the switching behaviour of the half bridge.

If, after the preheat state, the voltage across the ACM resistor (R16) does not exceed the V_{CMD} level during the non-overlap time, the Capacitive Mode Detection circuit (CMD) assumes that the circuit is in the capacitive mode of operation. As a consequence the frequency will directly be increased to f_{max}. The frequency behaviour is decoupled from the voltage at pin CSW until C_{CSW} has been discharged to zero.

Charge coupling

Due to parasitic capacitive coupling to the high voltage circuitry all pins are burdened with a repetitive charge injection. Given the typical application the pins IREF and CF are sensitive to this charge injection. For charge coupling of ±8 pC, a safe functional operation of the IC is guaranteed, independent of the current level.

Charge coupling at current levels below 50 μA will not interfere with the accuracy of the V_{CS}, V_{PCS} and V_{ACM} levels.

Charge coupling at current levels below 20 μA will not interfere with the accuracy of any parameter.

Design equations

The following design equations are used to calculate the desired preheat time, the maximum ignition time, and the minimum and the maximum switching frequency.

$t_{ph} = 1.7 \times 10^{-4} \times C_{CT} \times R_{IREF}$ (s)

$t_{ign} = 3.1 \times 10^{-5} \times C_{CT} \times R_{IREF}$ (s)

$$f_{min} = \frac{125 \times 10^3}{(C_{CF} \times R_{IREF})} \text{ in kHz}$$

$f_{max} = 2.5 \times f_{min}$ (kHz)

with C_{CT} in nF, R_{IREF} in kΩ, and C_{CF} in pF. Start of ignition is defined as the moment at which the measured lamp voltage crosses the $V_{lamp(fail)}$ level; see Section “Lamp failure mode”.

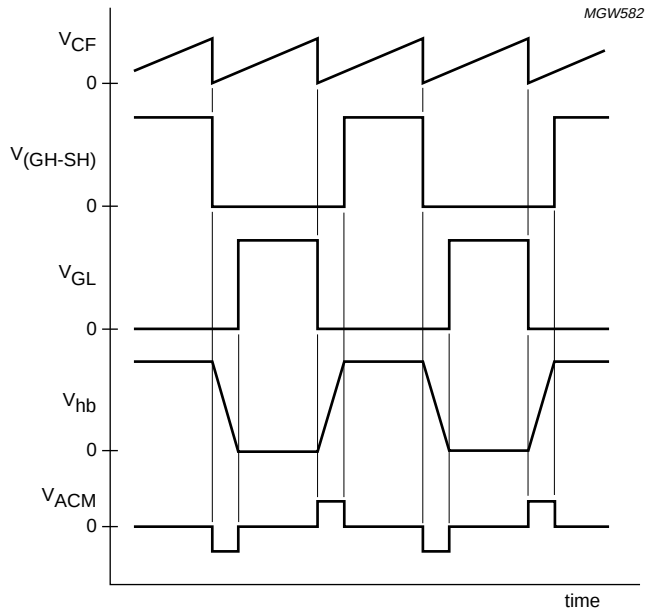


Fig.4 Oscillator and driver signals.

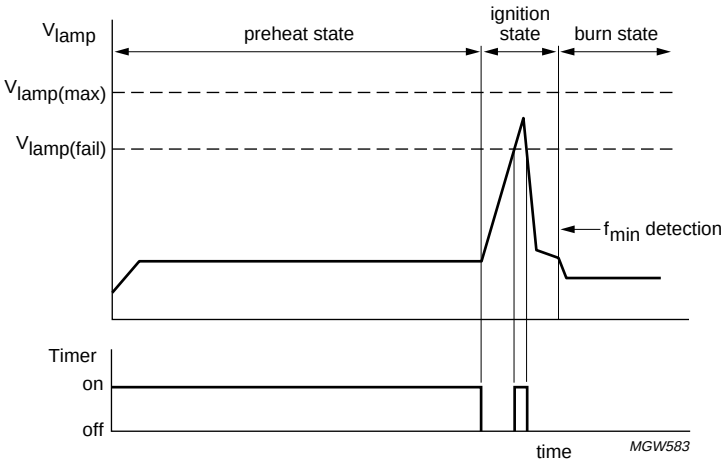


Fig.5 Normal ignition behaviour.

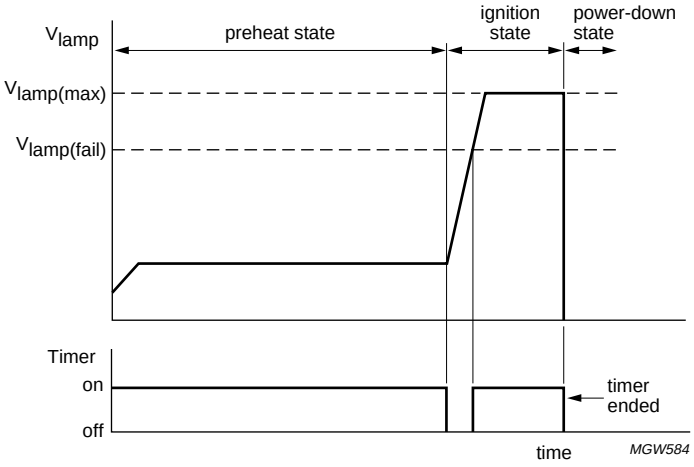


Fig.6 Failure mode during ignition.

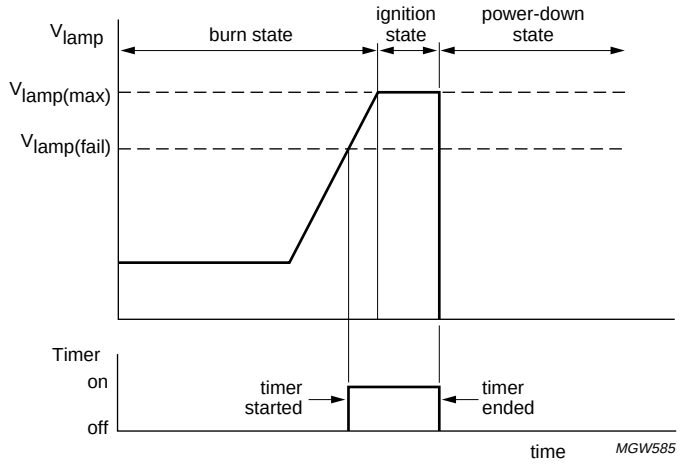


Fig.7 Failure mode during burn.

LIMITING VALUES

In according with the Absolute Maximum Rating System (IEC 60134); voltages with respect to pin GND.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{HS}	high side supply voltage	I_{HS} < 30 μA; t < 1 s	600	–	V
		I_{HS} < 30 μA	510	–	V
$V_{DD(max)}$	maximum voltage at pin V_{DD}		–	14	V
$V_{ACM(max)}$	maximum voltage at pin ACM		–5	+5	V
$V_{PCS(max)}$	maximum voltage at pin PCS		–5	+5	V
$V_{LVS(max)}$	maximum voltage at pin LVS		0	5	V
$V_{CS+(max)}$	maximum voltage at pin CS+		0	5	V
$V_{CS-(max)}$	maximum voltage at pin CS–		–0.3	+5	V
$V_{CSW(max)}$	maximum voltage at pin CSW		0	5	V
T_{amb}	ambient temperature		–25	+80	°C
T_j	junction temperature		–25	+150	°C
T_{stg}	storage temperature		–55	+150	°C
V_{esd}	electrostatic handling voltage	note 1			
	pins F_{VDD}, GH, and SH		–	±1000	V
	pins CT, CSW, CF, IREF, GL, V_{DD}, PCS, CS–, CS+, V_{ref}, LVS, and ACM		–	±2500	V

Note

1. In accordance with the human body model, i.e. equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	SO16		100	K/W
	DIP16		60	K/W
$R_{th(j-pin)}$	thermal resistance from junction to PCB	in free air		
	SO16		50	K/W
	DIP16		30	K/W

QUALITY SPECIFICATION

In accordance with *'SNW-FQ-611-E'*.

CHARACTERISTICS

All voltages referenced to GND; V_{DD} = 13 V; $V_{FVDD} - V_{SH}$ = 13 V; T_{amb} = 25 °C; unless otherwise specified; see Chapter “Application information”.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
High-voltage supply						
I_{leak}	leakage current on high-voltage pins	voltage at pins F_{VDD}, GH and SH = 600 V	–	–	30	µA
Start-up state						
V_{DD}	supply voltage for defined driver output	TR1 = off; TR2 = off	–	–	6	V
$V_{DD(start)}$	oscillator start voltage		12.4	13.0	13.6	V
$V_{DD(low)}$	oscillator stop voltage		8.6	9.1	9.6	V
$V_{DD(hys)}$	start-stop hysteresis		3.5	3.9	4.4	V
$I_{DD(start)}$	start-up current	$V_{DD} < V_{DD(start)}$	–	170	200	µA
$V_{DD(clamp)}$	clamp voltage	Power-down mode	10	11	12	V
I_{pd}	power-down current	V_{DD} = 9 V	–	170	200	µA
$V_{DD(reset)}$	reset voltage	TR1 = off; TR2 = off	4.5	5.5	7.0	V
I_{DD}	operating supply current	f_{bridge} = 40 kHz without gate drive	–	1.5	2.2	mA
Reference voltage						
V_{Vref}	reference voltage	I_L = 10 µA	2.86	2.95	3.04	V
$I_{source(Vref)}$	source current capability		1	–	–	mA
$I_{sink(Vref)}$	sink current capability		1	–	–	mA
Z_{Vref}	output impedance	I_L = 1 mA source	–	3.0	–	Ω
$\Delta V_{Vref}/\Delta T$	temperature coefficient	I_L = 10 µA; T_{amb} = 25 to 150 °C	–	–0.64	–	%/K
Current supply						
V_{IREF}	voltage at pin IREF		–	2.5	–	V
I_{IREF}	reference current range		65	–	95	µA
Voltage controlled oscillator						
V_{CSW}	control voltage		2.7	3.0	3.3	V
V_{clamp}	clamp voltage	burn state	2.8	3.1	3.4	V
$I_{CF(start)}$	output oscillator start current	V_{CF} = 1.5 V	3.8	4.5	5.2	µA
t_{start}	first output oscillator stroke time		–	50	–	µs
$I_{CF(min)}$	minimum output oscillator current	V_{CF} = 1.5 V	–	21	–	µA
$I_{CF(max)}$	maximum output oscillator current	V_{CF} = 1.5 V	–	54	–	µA
f_{max}	maximum bridge frequency		90	100	110	kHz
f_{min}	minimum bridge frequency		38.9	40.5	42.1	kHz
Δf_{stab}	frequency stability	T_{amb} = –20 to +80 °C	–	1.3	–	%
$V_{CF(high)}$	high level output oscillator voltage	$f = f_{min}$	–	2.5	–	V
$t_{nc(min)}$	minimum non-overlap time	GH to GL	0.68	0.90	1.13	µs
		GL to GH	0.75	1.00	1.25	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{no(max)}$	maximum non-overlap time	f_{bridge} = 40 kHz; note 1	–	7.5	–	µs
Output drivers						
$I_{o(source)(GH)}$	high side output source current	$V_{GH} - V_{SH} = 0$	135	180	235	mA
$I_{o(sink)(GH)}$	high side output sink current	$V_{GH} - V_{SH}$ = 13 V	265	330	415	mA
$I_{o(source)(GL)}$	low side output source current	$V_{GL} = 0$	135	200	235	mA
$I_{o(sink)(GL)}$	low side output sink current	V_{GL} = 13 V	265	330	415	mA
$V_{OH(GH)(h)}$	HIGH-level high side output voltage	I_o = 10 mA	12.5	–	–	V
$V_{OL(GH)(h)}$	LOW-level high side output voltage	I_o = 10 mA	–	–	0.5	V
$V_{OH(GL)(l)}$	HIGH-level low side output voltage	I_o = 10 mA	12.5	–	–	V
$V_{OL(GL)(l)}$	LOW-level low side output voltage	I_o = 10 mA	–	–	0.5	V
$R_{HS(on)}$	high side on resistance	I_o = 10 mA	32	39	45	Ω
$R_{HS(off)}$	high side off resistance	I_o = 10 mA	16	21	26	Ω
$R_{LS(on)}$	low side on resistance	I_o = 10 mA	32	39	45	Ω
$R_{LS(off)}$	low side off resistance	I_o = 10 mA	16	21	26	Ω
V_{boot}	bootstrap diode forward drop voltage	I = 5 mA	1.3	1.7	2.1	V
V_{FVDD}	lockout voltage		2.8	3.5	4.2	V
I_{FVDD}	floating well supply current	DC level at $V_{GH} - V_{SH}$ = 13 V	–	35	–	µA
Preheat current sensor						
$I_{i(PCS)}$	input current	V_{PCS} = 0.6 V	–	–	1	µA
V_{ph}	preheat voltage level at pin PCS		0.57	0.60	0.63	V
$I_{o(source)(CSW)}$	output source current	V_{CSW} = 2.0 V	9.0	10	11	µA
$I_{o(sink)(CSW)}$	effective output sink current	V_{CSW} = 2.0 V	–	10	–	µA
Adaptive non-overlap and capacitive mode detection						
$I_{i(ACM)}$	input current	V_{ACM} = 0.6 V	–	–	1	µA
V_{CMD+}	positive capacitive mode detection voltage		80	100	120	mV
V_{CMD-}	negative capacitive mode detection voltage		–68	–85	–102	mV
Lamp voltage sensor						
$I_{i(LVS)}$	input current	V_{LVS} = 0.81 V	–	–	1	µA
$V_{lamp(fail)}$	lamp fail voltage level at pin LVS		0.77	0.81	0.85	V
$V_{lamp(fail)(hys)}$	hysteresis lamp fail voltage level at pin LVS		119	144	169	mV
$V_{lamp(max)}$	maximum lamp voltage level at pin LVS		1.44	1.49	1.54	V
$I_{o(sink)(CSW)}$	output sink current	V_{CSW} = 2.0 V	27	30	33	µA
$I_{o(source)(ign)}$	ignition output source current	V_{CSW} = 2.0 V	9.0	10	11	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Average current sensor						
$I_{i(CS)}$	input current	V_{CS} = 0 V	–	–	1	μA
V_{offset}	offset voltage	V_{CS+} = V_{CS-} = 0 to 2.5 V	–2	0	+2	mV
g_m	transconductance	f = 1 kHz	1900	3800	5700	μA/mV
$I_{o(CSW)}$	output current	source and sink; V_{CSW} = 2 V	85	95	105	μA
Timer						
$I_{o(CT)}$	preheat timer output current	V_{CT} = 2.5 V	5.5	5.9	6.3	μA
$V_{OL(CT)}$	LOW-level preheat timer output voltage		–	1.4	–	V
$V_{OH(CT)}$	HIGH-level preheat timer output voltage		–	3.6	–	V
$V_{hys(CT)}$	preheat timer output hysteresis		2.05	2.20	2.35	V
t_{ph}	preheat time	C_{CT} = 330 nF and R_{IREF} = 33 kΩ	1.6	1.8	2.0	s
t_{ign}	ignition time	C_{CT} = 330 nF and R_{IREF} = 33 kΩ	–	0.26	–	s

Note

1. The maximum non-overlap is determined by the level of the CF signal. If this signal exceeds a level of 1.25 V the non-overlap will end, resulting in a maximum non-overlap time of 7.5 μs at a bridge frequency of 40 kHz.

APPLICATION INFORMATION

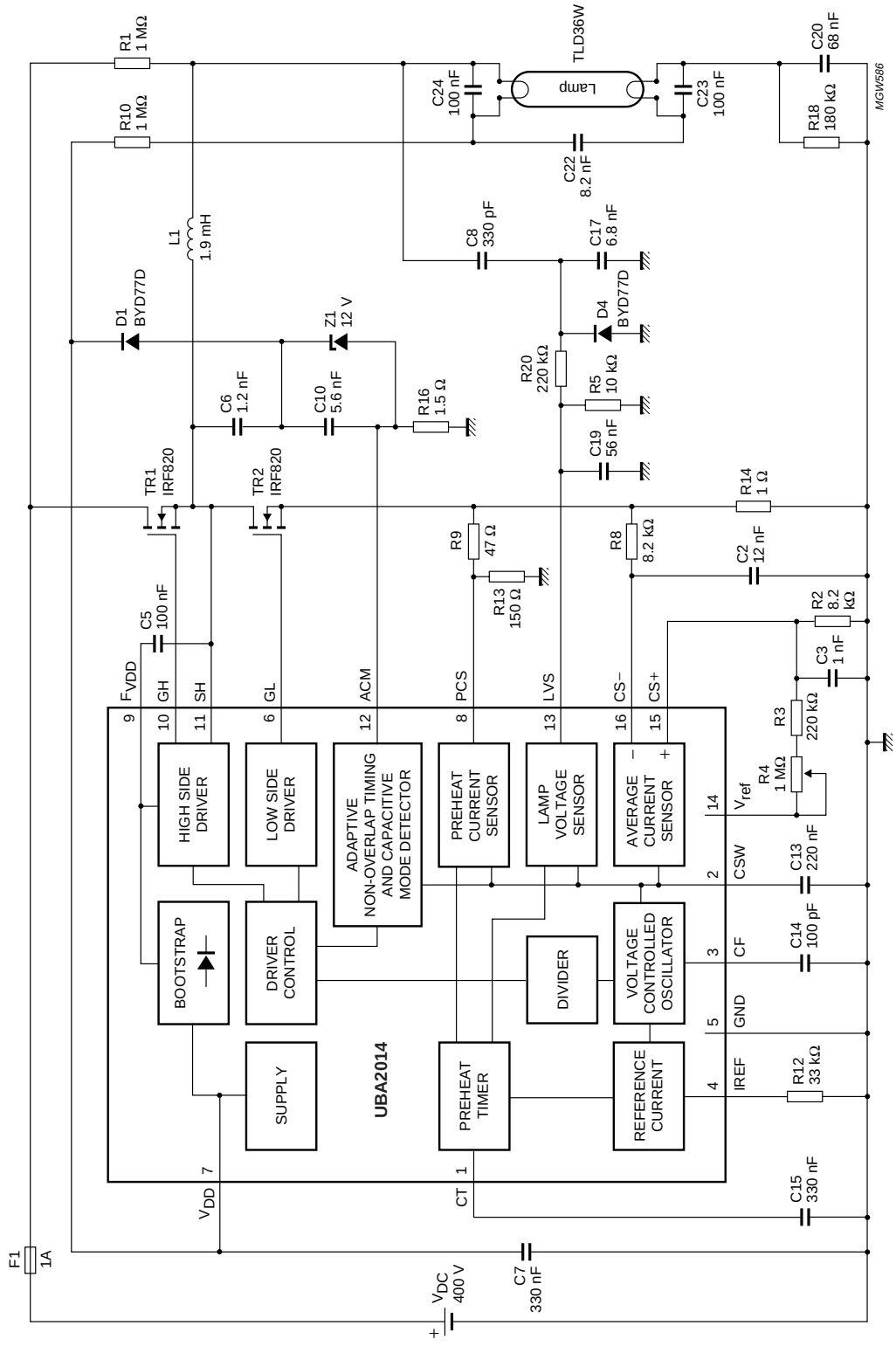
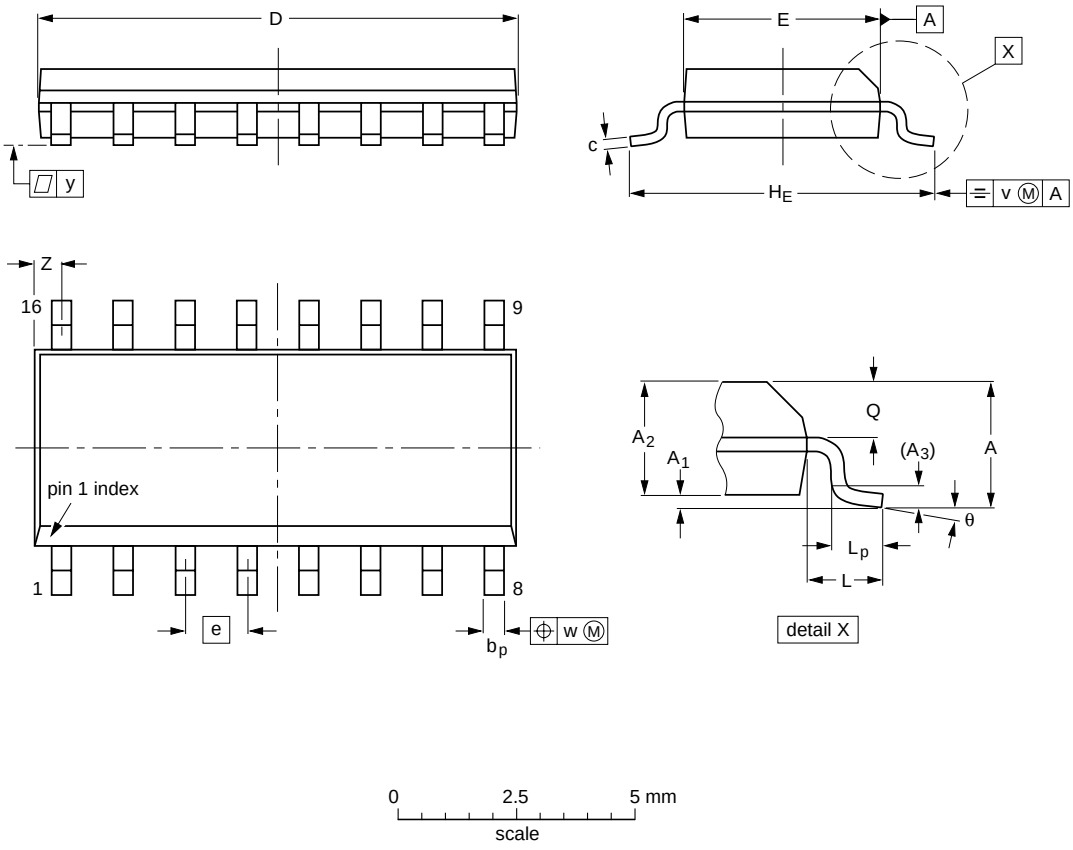


Fig.8 Test and application circuit.

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

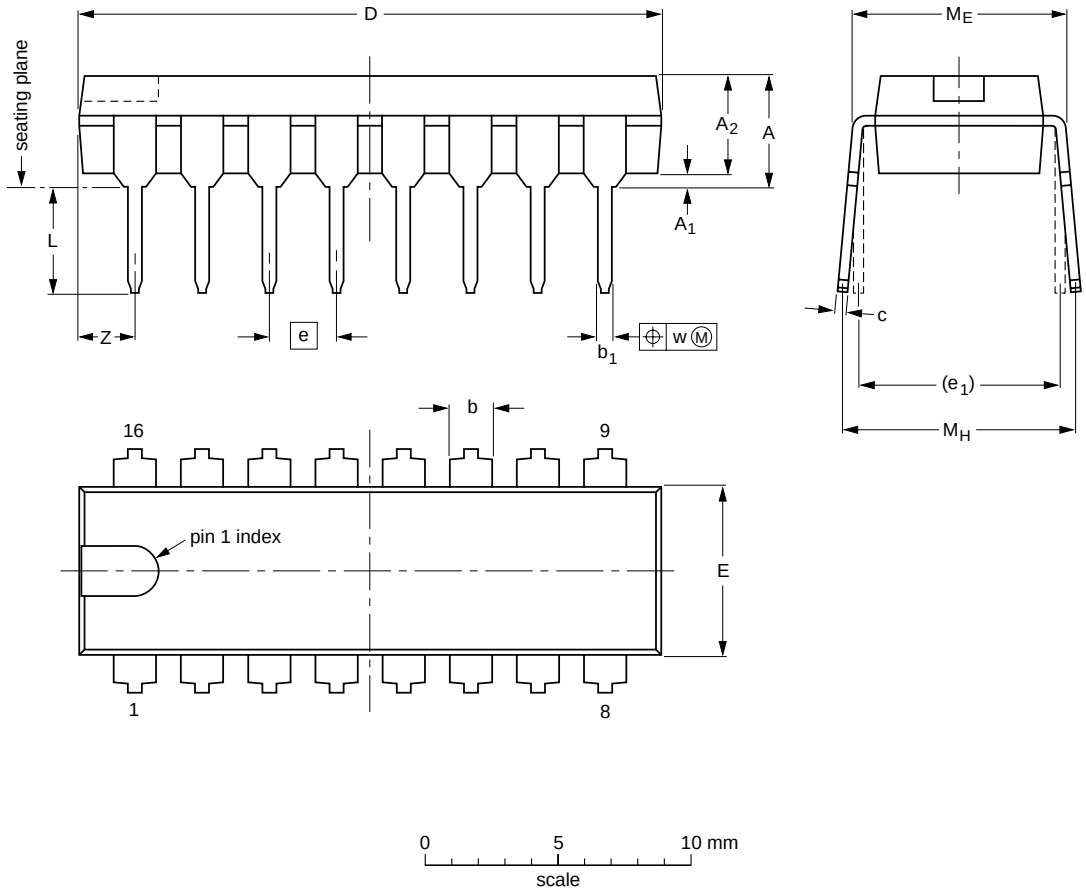
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				~~97-05-22~~ 99-12-27

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001	SC-503-16			~~95-01-19~~ 99-12-27

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (pre-heating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW(1)	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable(2)	–	suitable
Surface mount	BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable	–
	HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(3)	suitable	–
	PLCC(4), SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended(4)(5)	suitable	–
	SSOP, TSSOP, VSO	not recommended(6)	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

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