19-2630; Rev 1; 8/03

MAXIM

6.25Gbps, 1.8V PC Board Equalizer

General Description

The MAX3785 6.25Gbps equalizer operates from a single 1.8V supply and compensates for transmission-medium losses encountered with FR4 transmission lines. Optimized for low-voltage, high-density, DC-coupled interconnections between the line card and switch card, the MAX3785 enables a system upgrade path while maintaining a legacy rate of 2.5Gbps to 3.125Gbps. Roughly the size of two 0603 passive components, the MAX3785 easily provides placement and routing flexibility.

The MAX3785 is comprised of an equalizer, limiting amplifier, and output driver. For data rates of 3.2Gbps and lower, the MAX3785 equalizes signals for spans up to 40in of FR4 board material. For data rates up to 6.25Gbps, the MAX3785 compensates for 30in of FR4 board material. The MAX3785 is coding independent, functioning equally well for 8b/10b or scrambled signals.

The MAX3785 features DC-coupled current-mode logic (CML) data inputs and outputs. It is packaged in a tiny 1.5mm × 1.5mm chip-scale package (USCP™) and a 6-pin TDFN package.

Applications

HSBI for ≤ 6.4Gbps

Double IEEE 802.3ae XAUI

Double STM-16/OC-48

UCSP is a trademark of Maxim Integrated Products, Inc.

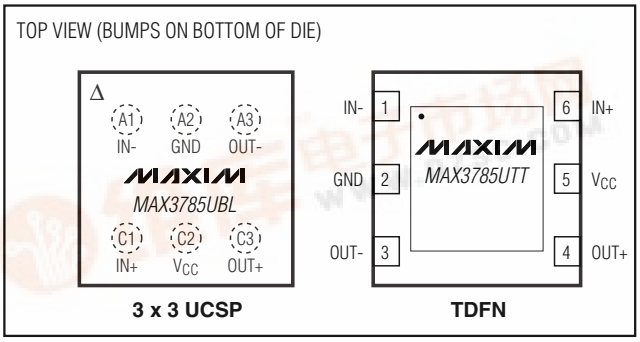
Features

- ♦ **Single 1.8V Supply**
- ♦ **Very Low Power, 60mW**
- ♦ **Spans 30in with FR4 at 6.25Gbps**
- ♦ **Operates from 1.0Gbps to 6.4Gbps**
- ♦ **Coding Independent, 8b/10b or Scrambled**
- ♦ **DC-Coupled CML Inputs and Outputs**
- ♦ **Small 1.5mm × 1.5mm Footprint**

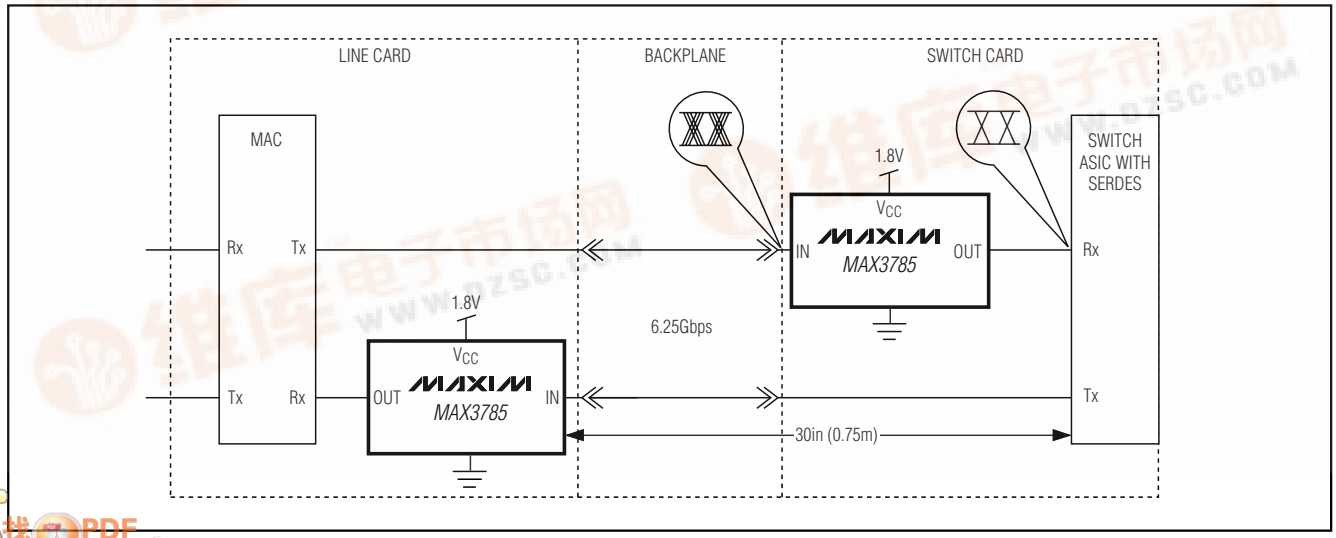
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE
MAX3785UBL	0°C to +85°C	6 UCSP (3 × 3)	—
MAX3785UTT	0°C to +85°C	6 TDFN	T633-1

Pin Configuration



Typical Application Circuit



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} to GND.....-0.5V to +6.0V
Continuous Output Current (OUT+, OUT-) .....-25mA to +25mA
Input Voltage (IN+, IN-).....-0.5V to (V_{CC} + 0.5V)
Operating Ambient Temperature Range ..... 0°C to +85°C
Storage Ambient Temperature Range.....-55°C to +150°C
Continuous Power Dissipation (T_A = +70°C)
6-Pin TDFN (derate 24.4mW above +70°C).....1.95W

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Typical values measured at V_{CC} = 1.8V and T_A= +25°C. Specifications guaranteed over specified operating conditions.) (See *Operating Conditions* table.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current			35	55	mA
Input Swing (IN)	Measured differentially at data source before encountering loss (Point A in Figure 1) (Note 1)	400		1600	mV_{P-P}
Input Common-Mode Voltage Range	(Note 1)	V_{CC} - (IN_{MAX}/4)		V_{CC} - (IN_{MIN}/4)	V
Input Return Loss	100MHz to 3.2GHz, power off		15		dB
Differential Input Resistance	IN+ and IN-	85	100	115	Ω
Output Swing	Measured differentially at OUT+ and OUT- with 50Ω ±1% load at each side	450		800	mV_{P-P}
Output Resistance	OUT+ or OUT-	42	50	58	Ω
Output Return Loss	100MHz to 3.2GHz, IN+ = high		14		dB
Output Transition Time (t_r, t_f)	20% to 80% (Note 2)	30	40	55	ps
Residual Deterministic Jitter (Notes 1, 3, 4)	2.5Gbps, 3.2Gbps, 5.0Gbps; 0in to 30in FR4 400mV_{P-P} ≤ IN ≤ 1600mV_{P-P}		0.10	0.15	UI
	2.5Gbps, 3.2Gbps; 40in FR4 400mV_{P-P} ≤ IN ≤ 1600mV_{P-P}		0.15	0.20	
	6.25Gbps; 0in to 30in FR4 600mV_{P-P} ≤ IN ≤ 1600mV_{P-P}		0.15	0.25	
	6.25Gbps; 0in to 30in FR4 IN = 400mV_{P-P}		0.20	0.30	
Output Random Jitter	(Notes 1, 2)		0.75	1.0	ps_{RMS}
Low-Frequency Cutoff Frequency			50		kHz
Latency			200		ps
Maximum Bit Rate	(Note 1)	6.25	6.4		Gbps
Minimum Bit Rate	(Note 1)		1.0	2.5	Gbps

Note 1: Guaranteed by design and characterization.
Note 2: Using input pattern 0000011111 at 6.25Gbps.
Note 3: Difference in deterministic jitter between data source and equalizer output, evaluated at 2.5Gbps, 3.2Gbps, 5Gbps, and 6.25Gbps. Pattern used: PRBS (2^7), ninety-six 0s, 1, 0, 1, 0, PRBS (2^7), ninety-six 1s, 0, 1, 0, 1.
Note 4: Signal is applied differentially at input to a 6-mil wide, loosely coupled stripline. Deterministic jitter at the output of the transmission line is from media-induced loss, not from clock source modulation (see Figure 1).

Operating Conditions

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})		1.71	1.8	1.89	V
Operating Ambient Temperature		0	25	85	°C
Supply Noise Tolerance	10Hz ≤ f < 100Hz		100		mV_{P-P}
	100Hz ≤ f < 1MHz		40		
	1MHz ≤ f ≤ 1GHz		10		
Bit Rate	NRZ data	2.50		6.25	Gbps

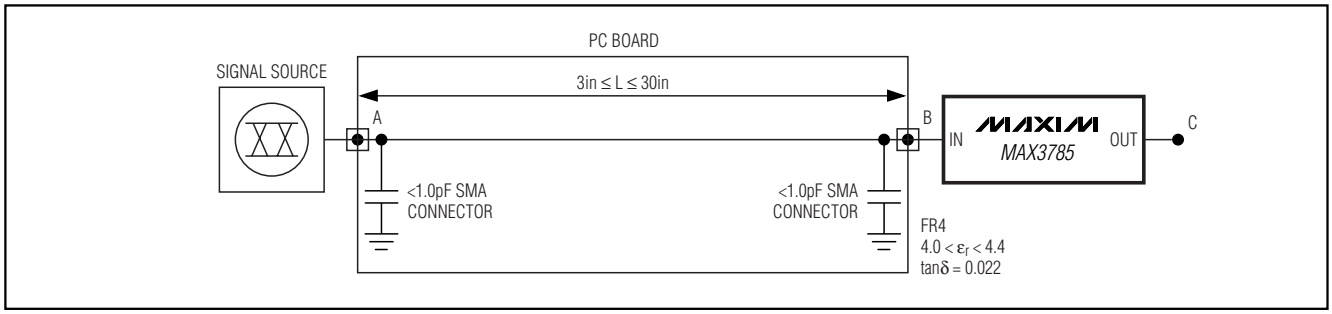
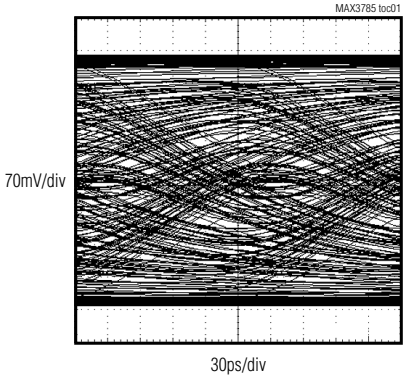


Figure 1. Conditions of Testing

Typical Operating Characteristics

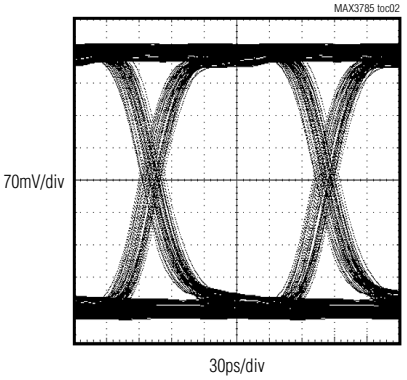
(V_{CC} = +1.8V, T_A = +25°C, unless otherwise noted. Measurements done at 6.25Gbps, 500mV_{P-P} at the source with a test pattern: PRBS (2^7), ninety-six 0s, 1, 0, 1, 0, PRBS (2^7), ninety-six 1s, 0, 1, 0, 1. Deterministic jitter of the MAX3785 and the board was measured using Tektronix's FrameScan™. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams were acquired by FrameScan, which includes system jitter but eliminates random jitter.)

EYE DIAGRAM OF UNEQUALIZED SIGNAL AFTER 30in OF FR4



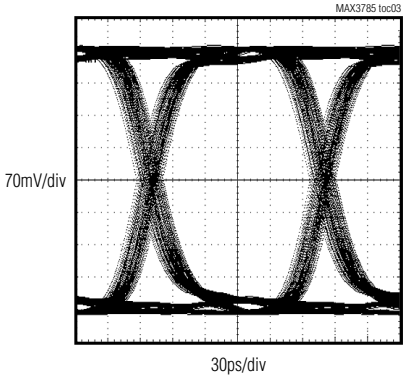
TEST PATTERN, 6.25Gbps,
WITHOUT RANDOM JITTER,
INCLUDING 13ps SYSTEM JITTER

EYE DIAGRAM OF EQUALIZED SIGNAL AFTER 30in OF FR4



TEST PATTERN, 6.25Gbps,
WITHOUT RANDOM JITTER,
INCLUDING 13ps SYSTEM JITTER

EYE DIAGRAM OF EQUALIZED SIGNAL AFTER 30in OF FR4



2^{10} - 1 PRBS, 6.25Gbps,
WITHOUT RANDOM JITTER,
INCLUDING 13ps SYSTEM JITTER

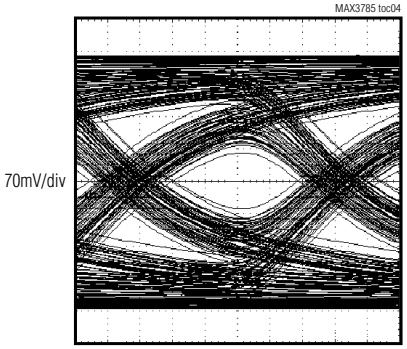
FrameScan is a trademark of Tektronix.

6.25Gbps, 1.8V PC Board Equalizer

Typical Operating Characteristics (continued)

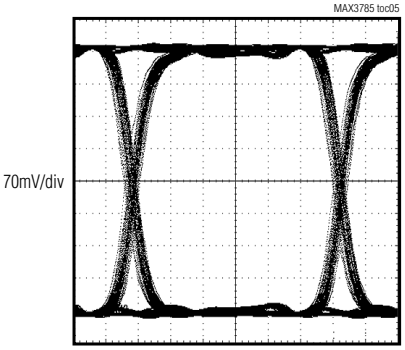
(V_{CC} = +1.8V, T_A = +25°C, unless otherwise noted. Measurements done at 6.25Gbps, 500mV_{P-P} at the source with a test pattern: PRBS (2^7), ninety-six 0s, 1, 0, 1, 0, PRBS (2^7), ninety-six 1s, 0, 1, 0, 1. Deterministic jitter of the MAX3785 and the board was measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams were acquired by FrameScan, which includes system jitter but eliminates random jitter.)

EYE DIAGRAM OF UNEQUALIZED SIGNAL AFTER 30in OF FR4



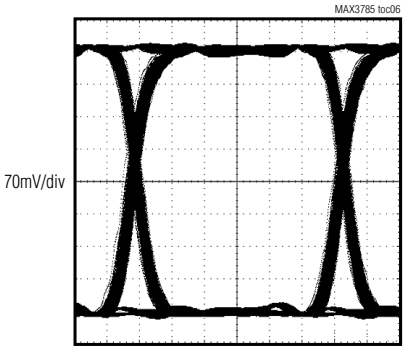
TEST PATTERN, 3.125Gbps,
WITHOUT RANDOM JITTER,
INCLUDING 13ps SYSTEM JITTER

EYE DIAGRAM OF EQUALIZED SIGNAL AFTER 30in OF FR4



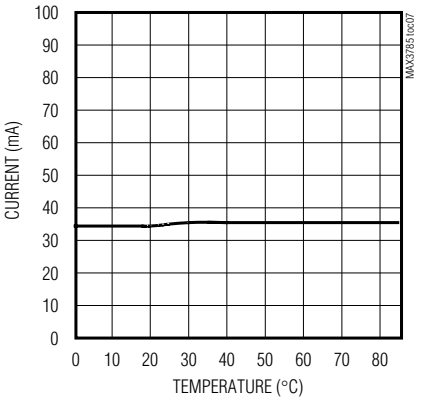
TEST PATTERN, 3.125Gbps,
WITHOUT RANDOM JITTER,
INCLUDING 13ps SYSTEM JITTER

EYE DIAGRAM OF EQUALIZED SIGNAL AFTER 30in OF FR4

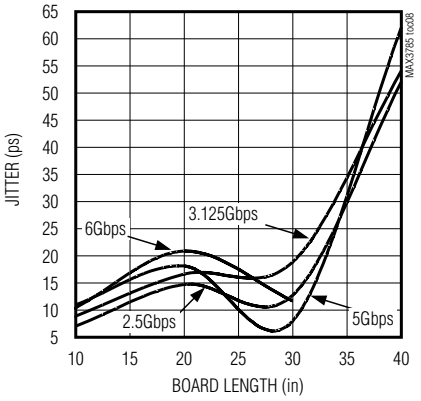


CRPAT, 3.125Gbps,
WITHOUT RANDOM JITTER,
INCLUDING 13ps SYSTEM JITTER

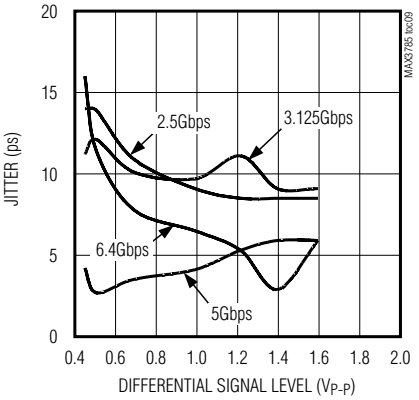
EQUALIZER OPERATING CURRENT vs. TEMPERATURE



DETERMINISTIC JITTER vs. BOARD LENGTH (FR4) (INPUT LEVEL OF 500mV_{P-P}, TEST PATTERN)



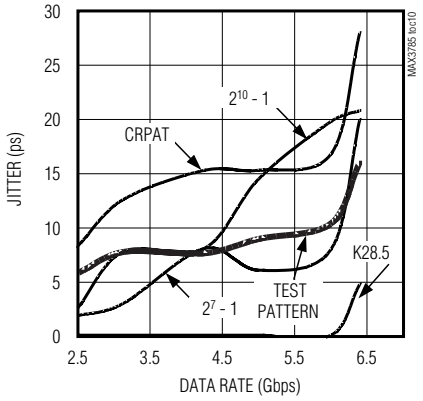
DETERMINISTIC JITTER vs. SIGNAL LEVEL (TEST PATTERN, 30in OF FR4 BOARD)



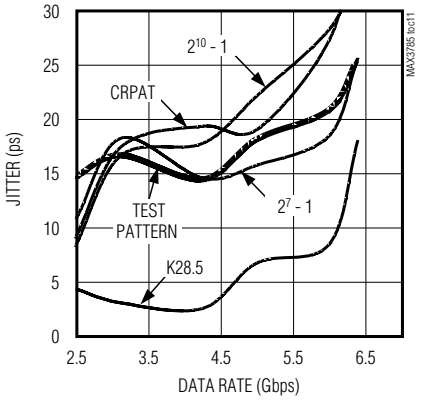
Typical Operating Characteristics (continued)

(V_{CC} = +1.8V, T_A = +25°C, unless otherwise noted. Measurements done at 6.25Gbps, 500mV$_{P-P}$ at the source with a test pattern: PRBS (2^7), ninety-six 0s, 1, 0, 1, 0, PRBS (2^7), ninety-six 1s, 0, 1, 0, 1. Deterministic jitter of the MAX3785 and the board was measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams were acquired by FrameScan, which includes system jitter but eliminates random jitter.)

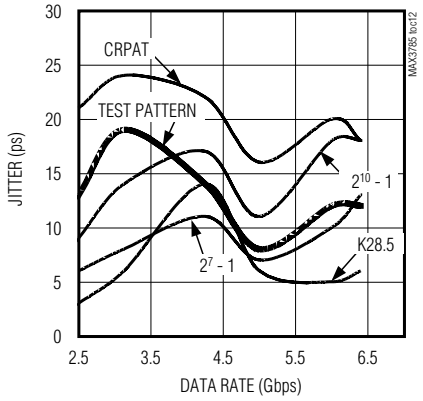
DETERMINISTIC JITTER vs. DATA RATE FOR 10in OF FR4 BOARD (INPUT LEVEL OF 500mV$_{P-P}$)



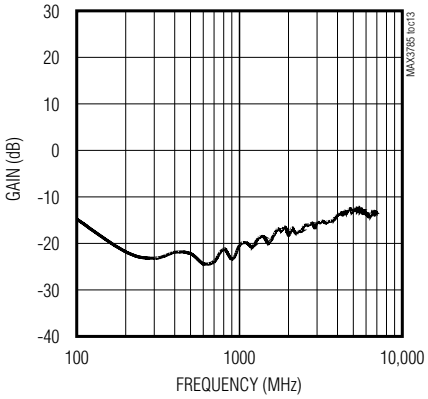
DETERMINISTIC JITTER vs. DATA RATE FOR 20in OF FR4 BOARD (INPUT LEVEL OF 500mV$_{P-P}$)



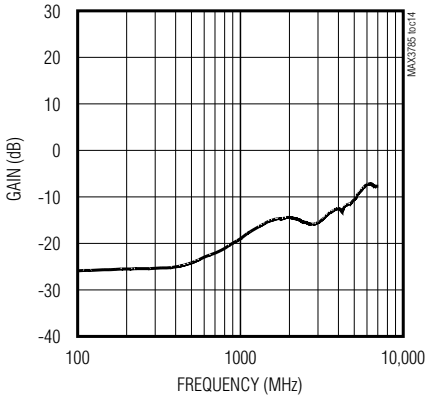
DETERMINISTIC JITTER vs. DATA RATE FOR 30in OF FR4 BOARD (INPUT LEVEL OF 500mV$_{P-P}$)



EQUALIZER INPUT RETURN GAIN (SDD11) (INPUT SIGNAL LEVEL = -40dBm, POWER OFF)



EQUALIZER INPUT RETURN GAIN (SDD22) (INPUT SIGNAL LEVEL = -40dBm, IN+ HIGH)



6.25Gbps, 1.8V PC Board Equalizer

MAX3785UBL Pin Description

PIN	NAME	FUNCTION (MAX3785UBL)
A1	IN-	Negative Data Input, CML
A2	GND	Supply Ground
A3	OUT-	Negative Data Output, CML
C1	IN+	Positive Data Input, CML
C2	V_{CC}	Supply Voltage
C3	OUT+	Positive Data Input, CML

Functional Description

The MAX3785 6.25Gbps PC board equalizer consists of an equalizer, limiting amplifier, offset driver, and offset cancellation circuit (see Figure 2). The equalizer block compensates for the attenuation caused by the PC board. The limiting amplifier squares up the signal at the output of the equalizer block. The offset cancellation circuit corrects for internal offset in the limiting amplifier to minimize pulse-width distortion. This introduces a low-frequency cutoff. The data must achieve a 50% mark/space ratio in less than 100µs. The specified minimum differential input must be maintained to avoid oscillation.

Input and Output Structures

An equivalent DC input circuit is shown in Figure 3. It has an equivalent DC differential input resistance of 100Ω. The output buffer is implemented using current-mode logic (CML), as shown in Figure 4.

Package Description

The chip-scale package (UCSP) has a bump pitch of 0.5mm (19.7 mils) and a bump diameter of 0.3mm (12 mils). Lay out the solder pad spacing on 0.5mm (19.7 mils), a pad size of 0.25mm (10 mils) and a solder mask opening of 0.33mm (13 mils). Round or square pads are permissible. For detailed information on UCSP layout and handling, go to Maxim's website, www.maxim-ic.com. The enclosed package description was accurate at the time of publication. For the MAX3785, all of the balls shown in row B of the drawing are unpopulated. Go to Maxim's website for the latest package information.

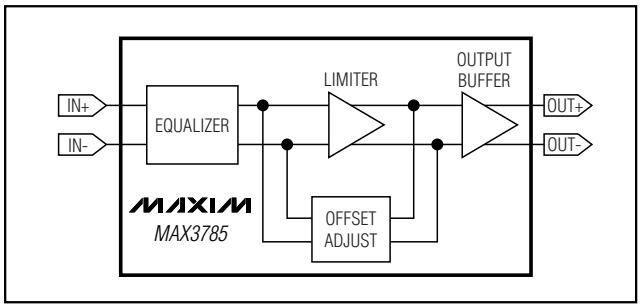


Figure 2. Functional Diagram of the MAX3785

MAX3785UTT Pin Description

PIN	NAME	FUNCTION (MAX3785UTT)
1	IN-	Negative Data Input (CML)
2	GND	Supply Ground
3	OUT-	Negative Data Output (CML)
4	OUT+	Positive Data Output (CML)
5	V_{CC}	Supply Voltage
6	IN+	Positive Data Input (CML)

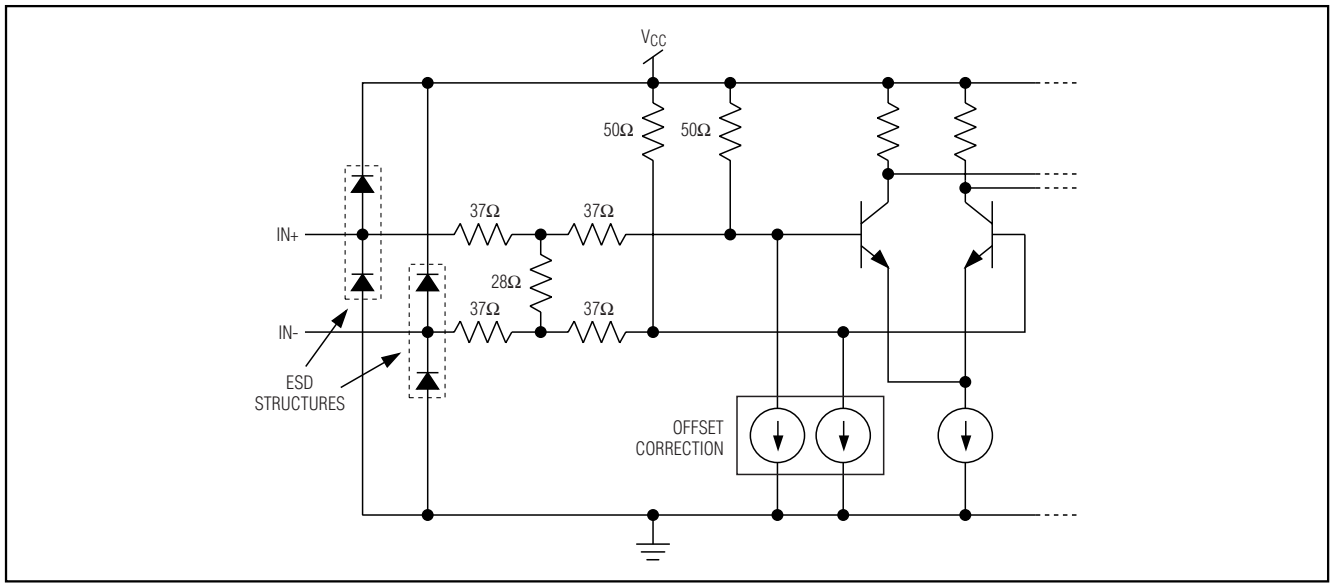


Figure 3. Equalizer Input DC Equivalent Circuit

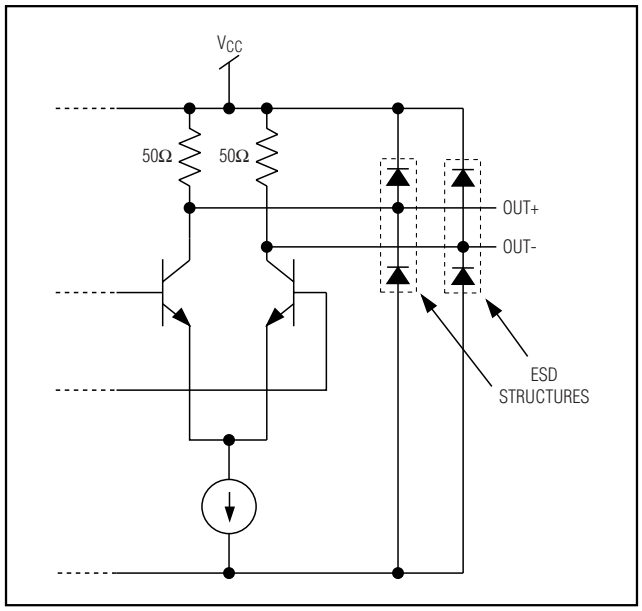
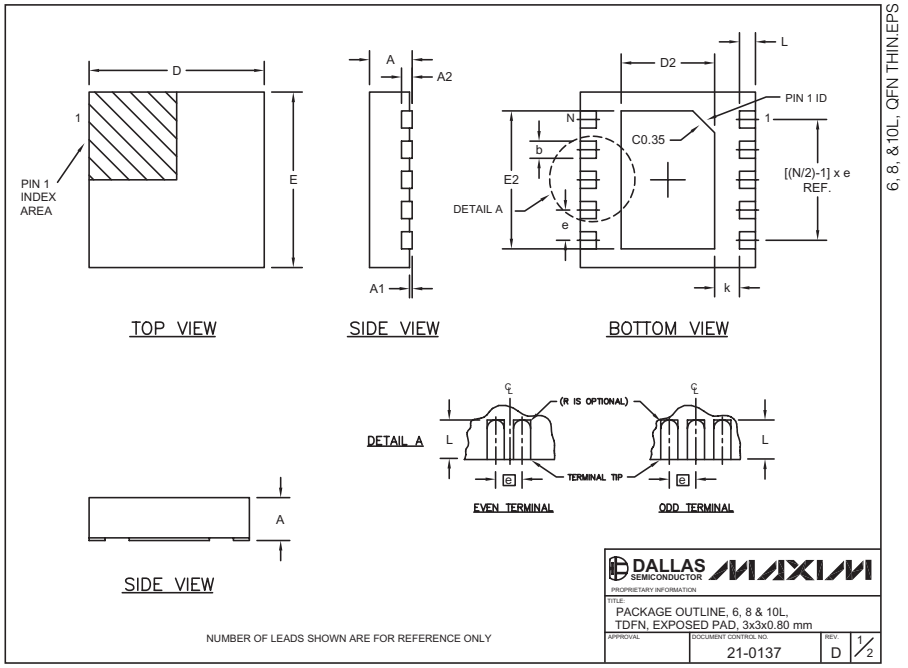


Figure 4. CML Output Equivalent Circuit

6.25Gbps, 1.8V PC Board Equalizer

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Note: For the MAX3785, all of the balls shown in row B of the drawing are unpopulated.

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50–0.10	2.30–0.10	0.95 BSC	MO229 / WEEA	0.40–0.05	1.90 REF
T833-1	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T1033-1	10	1.50–0.10	2.30–0.10	0.50 BSC	MO229 / WEED-3	0.25–0.05	2.00 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2".
6. "N" IS THE TOTAL NUMBER OF LEADS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

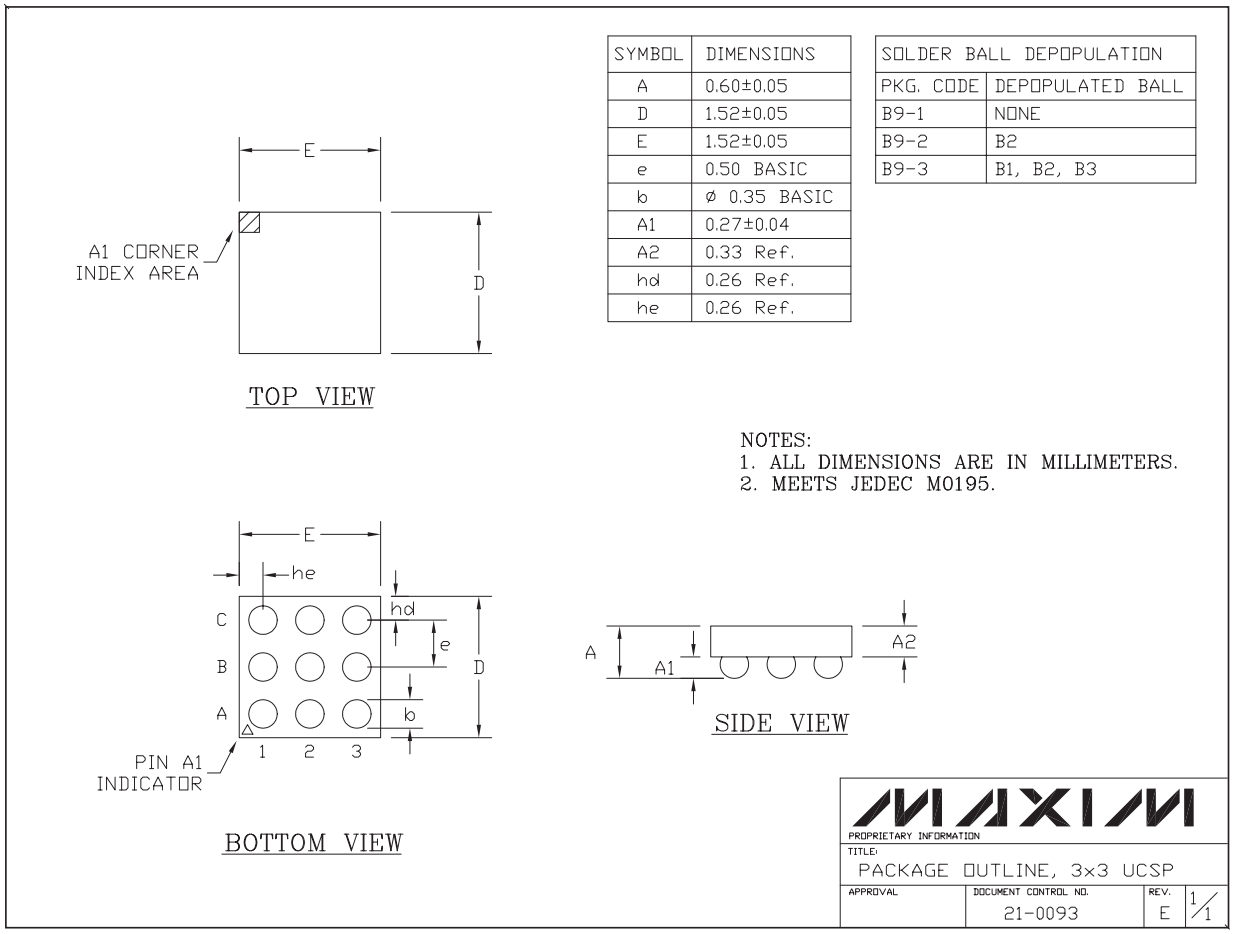
TITLE: PACKAGE OUTLINE, 6, 8 & 10L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	D	2/2

6.25Gbps, 1.8V PC Board Equalizer

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



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