UNITRODE

UC1903
UC2903
UC3903

Quad Supply and Line Monitor

FEATURES

- Inputs for Monitoring up to Four Separate Supply Voltage Levels
- Internal Inverter for Sensing a Negative Supply Voltage
- Line/Switch Sense Input for Early Power Source Failure Warning
- Programmable Under- and Over-Voltage Fault Thresholds with Proportional Hysteresis
- A Precision 2.5V Reference
- General Purpose Op-Amp for Auxiliary Use
- Three High Current, >30mA, Open-Collector Outputs Indicate Over-Voltage, Under-Voltage and Power OK Conditions
- Input Supply Under-Voltage Sensing and Start-Latch Eliminate Erroneous Fault Alerts During Start-Up
- 8-40V Supply Operation with 7mA Stand-By Current

DESCRIPTION

The UC1903 family of quad supply and line monitor integrated circuits will respond to under- and over-voltage conditions on up to four continuously monitored voltage levels. An internal op-amp inverter allows at least one of these levels to be negative. A separate line/switcher sense input is available to provide early warning of line or other power source failures.

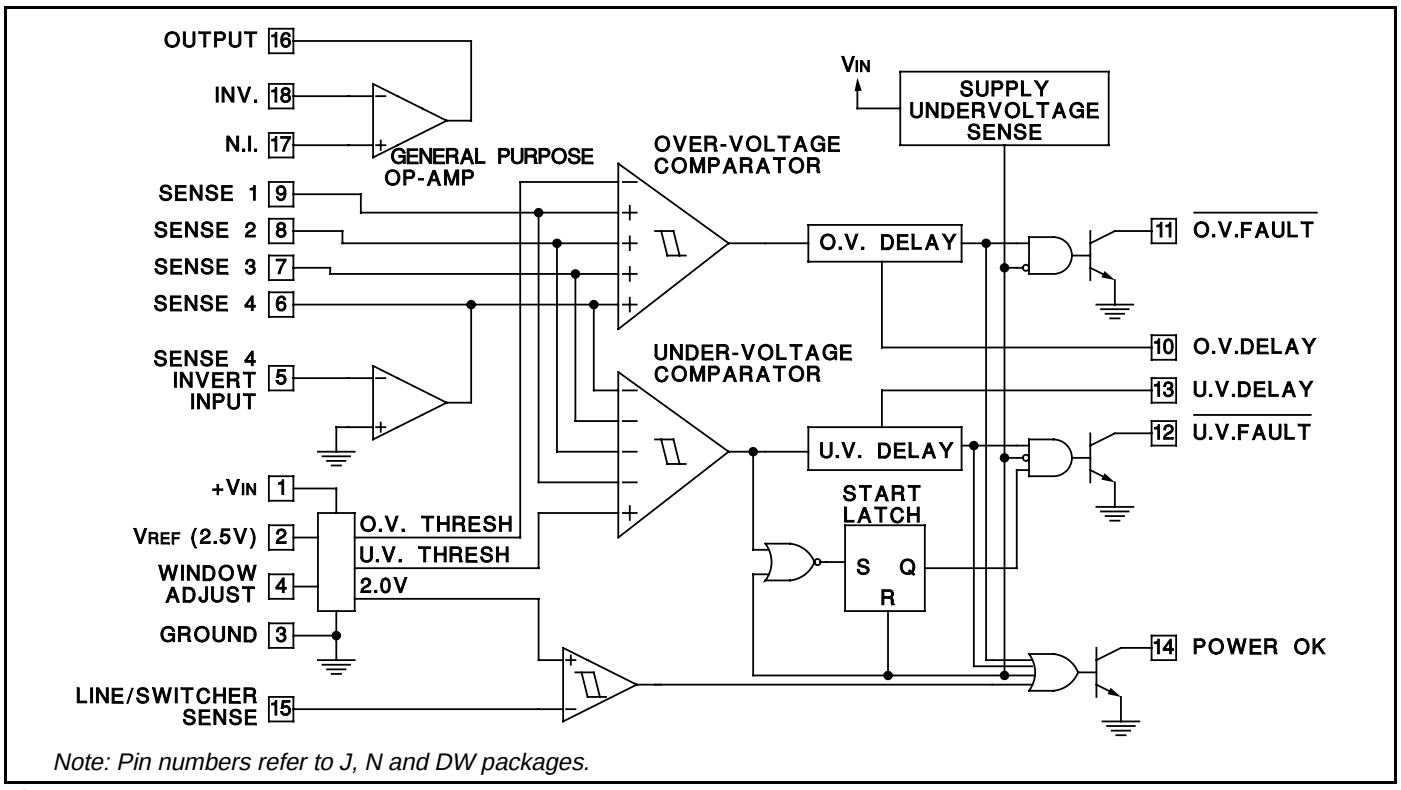
The fault window adjustment circuit on these devices provides easy programming of under- and over-voltage thresholds. The thresholds, centered around a precision 2.5V reference, have an input hysteresis that scales with the window width for precise, glitch-free operation. A reference output pin allows the sense input fault windows to be scaled independently using simple resistive dividers.

The three open collector outputs on these devices will sink in excess of 30mA of load current when active. The under- and over-voltage outputs respond after separate, user defined, delays to respective fault conditions. The third output is active during any fault condition including under- and over-voltage, line/switcher faults, and input supply under-voltage. The off state of this output indicates a "power OK" situation.

An additional, uncommitted, general purpose op-amp is also included. This op-amp, capable of sourcing 20mA of output current, can be used for a number of auxiliary functions including the sensing and amplification of a feedback error signal when the 2.5V output is used as a system reference.

In addition, these ICs are equipped with a start-latch to prevent erroneous under-voltage indications during start-up. These parts operate over an 8V to 40V input supply range and require a typical stand-by current of only 7mA.

BLOCK DIAGRAM

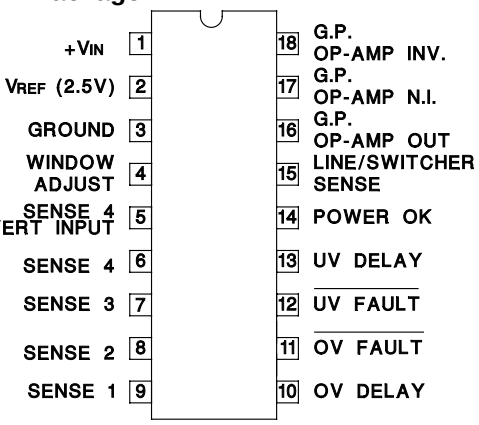


Note: Pin numbers refer to J, N and DW packages.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (+V_{IN}) . . . . . +40V
Open Collector Output Voltages . . . . . +40V
Open Collector Output Currents 50mA
Sense 1-4 Input Voltages . . . . . -0.3V to +20V
Line/Switcher Sense Input Voltage . . . . . -0.3V to +40V
Op-Amp and Inverter Input Voltages . . . . . -0.3V to +40V
Op-Amp and Inverter Output Currents . . . . . -40mA
Window Adjust Voltage . . . . . 0.0V to +10V
Delay Pin Voltages . . . . . 0.0V to +5V
Reference Output Current . . . . . -40mA
Power Dissipation at T_A = 25°C (Note 1) 1000mW
Power Dissipation at T_C = 25°C (Note 1) 2000mW
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

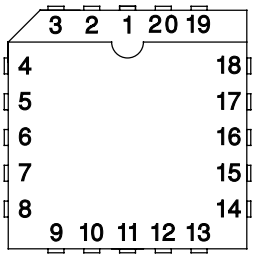
DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



Note 1: Voltages are referenced to ground (Pin 3). Currents are positive into, negative out of, the specified terminals. Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

PLCC-20, LCC-20
(TOP VIEW)
Q, L Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
+VIN	1
V_{REF} (2.5V)	2
GROUND	3
GROUND	4
WINDOW ADJUST	5
N/C	6
SENSE 4 INVERT INPUT	7
SENSE 4	8
SENSE 3	9
SENSE 2	10
SENSE 1	11
OV DELAY	12
$\overline{\text{OV FAULT}}$	13
$\overline{\text{UV FAULT}}$	14
UV DELAY	15
POWER OK	16
LINE/SWITCHER SENSE	17
G.P. OP-AMP OUT	18
G.P. OP-AMP N.I.	19
G.P. OP-AMP INV.	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1903; –40°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; +V_{IN} = 15V; Sense Inputs (Pins 6–9 and Pin 15) = 2.5V; $V_{PIN\ 4}$ = 1.0V, T_A = T_J.

PARAMETERS	TEST CONDITIONS	UC1903 / UC2903			UC3903			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply								
Input Supply Current	No Faults		7	9		7	11	mA
	UV, OV and Line Fault		10	15		10	18	mA
Supply Under Voltage Threshold (V_{SUV})	Fault Outputs Enabled	6.0	7.0	7.5	5.5	7.0	8.0	V
Minimum Supply to Enable Power OK Output			3.0	4.0		3.0	4.0	V
Reference								
Output Voltage (V_{REF})	T_J = 25°C	2.485	2.5	2.515	2.470	2.5	2.530	V
	Over Temperature	2.465		2.535	2.465		2.535	V
Load Regulation	I_L = 0 to 10mA		1	10		1	15	mV
Line Regulation	+V_{IN} = 8 to 40V		1	4		1	8	mV
Short Circuit Current	T_J = 25°C		40			40		mA
Fault Thresholds (Note 4)								
OV Threshold Adj.	Offset from V_{REF} as a function of $V_{PIN\ 4}$ Input = Low to High, 0.5V ≤ $V_{PIN\ 4}$ ≤ 2.5V	.230	.25	.270	.230	.25	.270	V/V
UV Threshold Adj.	Offset from V_{REF} as a function of $V_{PIN\ 4}$ Input = High to Low, 0.5V ≤ $V_{PIN\ 4}$ ≤ 2.5V	-.270	-.25	-.230	-.270	-.25	-.230	V/V

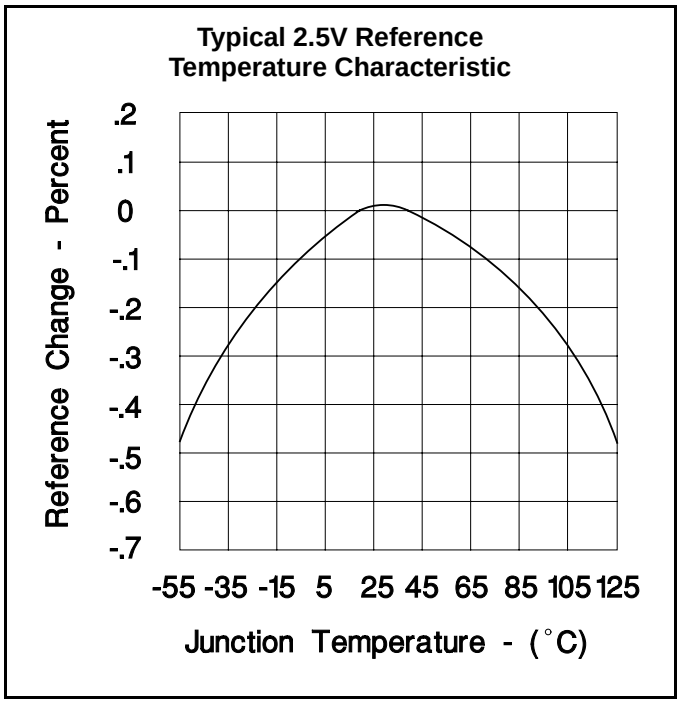
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1903; –40°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; $+V_{IN}$ = 15V; Sense Inputs (Pins 6–9 and Pin 15) = 2.5V; $V_{PIN\ 4}$ = 1.0V, $T_A = T_J$.

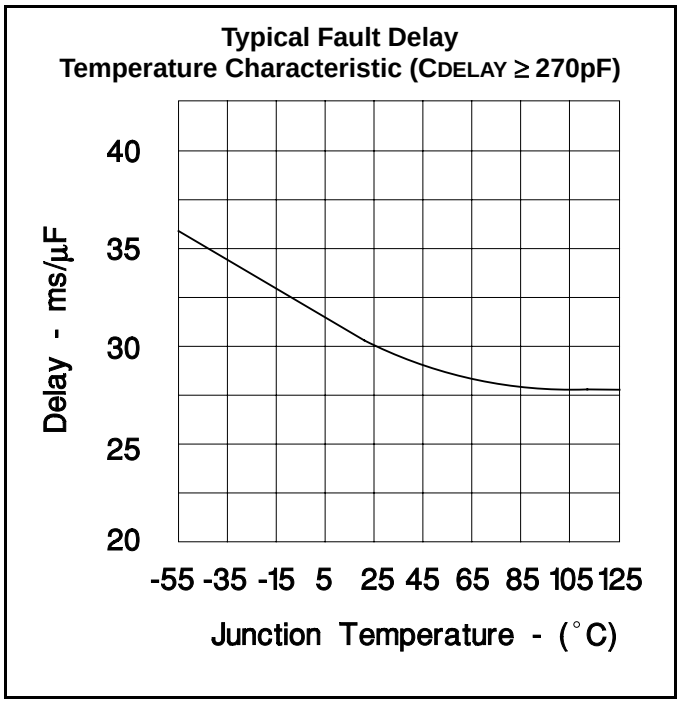
PARAMETERS	TEST CONDITIONS	UC1903/UC2903			UC3903			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Fault Thresholds (cont.)								
OV & UV Threshold Hyst.	$0.5V \le V_{PIN\ 4} \le 2.5V$	10	20	30	10	20	30	mV/V
OV & UV Threshold Supply Sensitivity	$+V_{IN}$ = 8V to 40V		.002	.01		.002	.02	%/V
Adjust Pin (Pin 4) Input Bias Current	$0.5V \le V_{PIN\ 4} \le 2.5V$		±1	±10		±1	±12	µA/V
Line Sense Threshold	Input = High to Low	1.94	2.0	2.06	1.9	2.0	2.1	V
Line Sense Threshold Hyst.		125	175	225	100	175	250	mV
Sense Inputs								
Sense 1-4 Input Bias Current	Input = 2.8V (Note 2)		1	3		1	6	µA
	Input = 2.2 (Note 2)		-1	-3		-1	-6	µA
Line Sense Input Bias Current	Input = 2.3V (Note 2)		1	3		1	6	µA
OV and UV Fault Delay								
Charging Current			60			60		µA
Threshold Voltage	Delay Pin = Low to High		1.8			1.8		V
Threshold Hysteresis	T_J = 25°C		250			250		mV
Delay	Ratio of Threshold Voltage to Charging Current	20	30	50	20	30	50	ms/µF
Fault Outputs ($\overline{OV}$, $\overline{UV}$, & Power 0K)								
Maximum Current	V_{OUT} = 2V	30	70		30	70		mA
Saturation Voltage	I_{OUT} = 12mA		.25	.40		.25	.40	V
Leakage Current	V_{OUT} = 40 V		3	25		3	25	µA
Sense 4 Inverter (Note 3)								
Input Offset Voltage			2	8		2	10	mV
Input Bias Current			.1	2		.1	4	µA
Open Loop Gain		65	80		65	80		dB
PSRR	$+V_{IN}$ = 8 to 40 V	65	100		65	100		dB
Unity Gain Frequency			1			1		MHz
Slew Rate			.4			.4		V/µs
Short Circuit Current	T_J = 25°C		40			40		mA
G.P. Op-Amp (Note 3)								
Input Offset Voltage			1	5		1	8	mV
Input Bias Voltage			.1	2		.1	4	µA
Input Offset Current			.01	.5		.01	1.0	µA
Open Loop Gain		65	120		65	120		dB
CMRR	V_{CM} = 0 to $+V_{IN}$ = 2.0V	65	100		65	100		dB
PSRR	$+V_{IN}$ = 8 to 40V	65	100		65	100		dB
Unity Gain Frequency			1			1		MHz
Slew Rate			.4			.4		V/µs
Short Circuit Current	T_J = 25°C		40			40		mA

Note 2: These currents represent maximum input bias currents required as the sense inputs cross appropriate thresholds.

Note 3: When either the G.P. OP-Amp, or the Sense 4 Inverter, are configured for sensing a negative supply voltage, the divider resistance at the inverting input should be chosen such that the nominal divider current is ≤ 1.4mA. With the divider current at or below this level possible latching of the circuit is avoided. Proper operation for currents at or below 1.4mA is 100% tested in production.

Note 4: Reference to pin numbers in this specification pertain to 18 pin DIL N and J packages and 18 pin SOIC DW package.





OPERATION AND APPLICATION INFORMATION

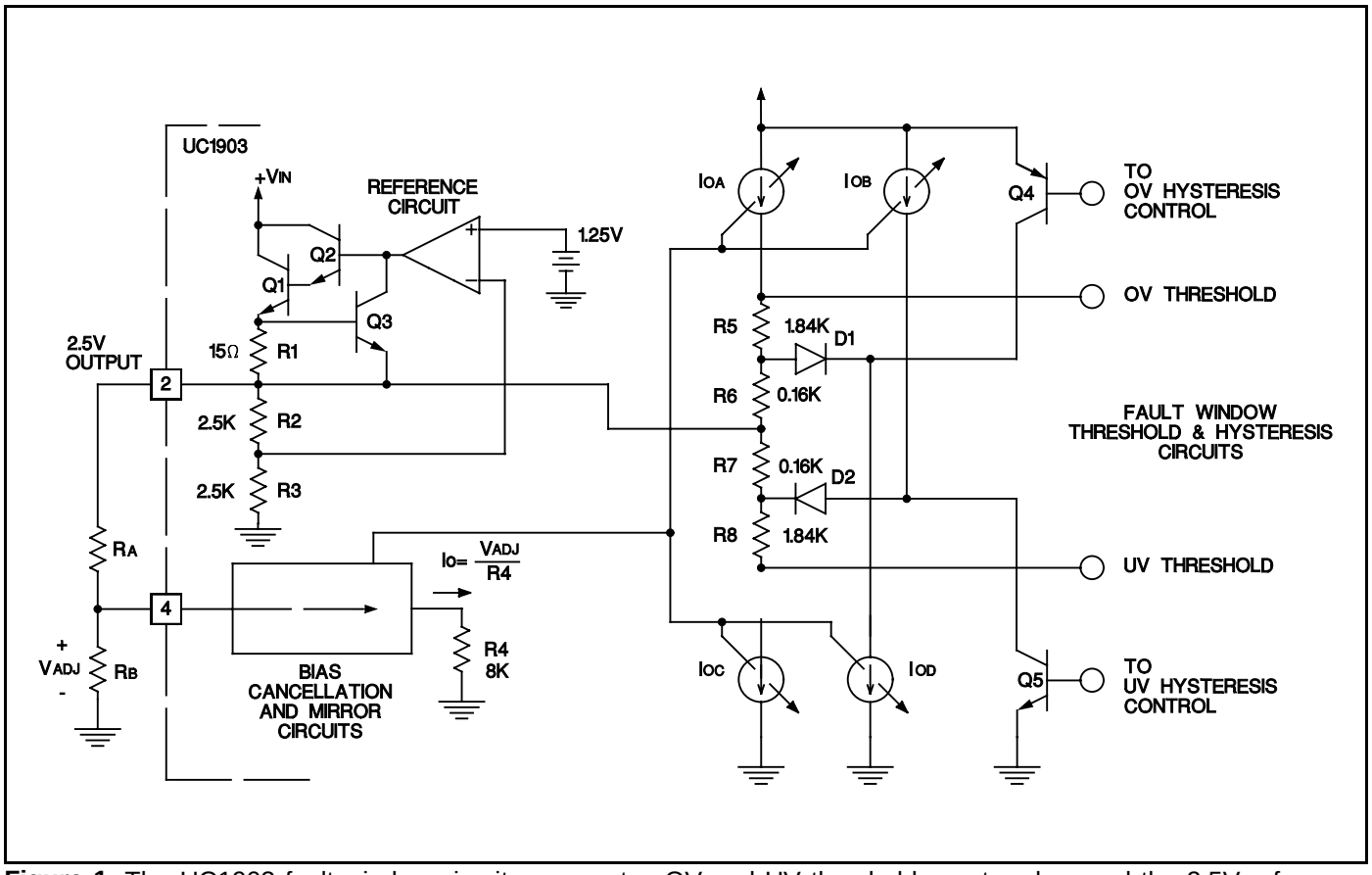


Figure 1. The UC1903 fault window circuitry generates OV and UV thresholds centered around the 2.5V reference. Window magnitude and threshold hysteresis are proportional to the window adjust input voltage at Pin 4.

OPERATION AND APPLICATION INFORMATION

Setting a Fault Window

The fault thresholds on the UC1903 are generated by creating positive and negative offsets, equal in magnitude, that are referenced to the chip's 2.5V reference. The resulting fault window is centered around 2.5V and has a magnitude equal to that of the applied offsets. Simplified schematics of the fault window and reference circuits are shown in Figure 1 (see previous page). The magnitude of the offsets is determined by the voltage applied at the window adjust pin, Pin 4. A bias cancellation circuit keeps the input current required at Pin 4 low, allowing the use of a simple resistive divider off the reference to set the adjust pin voltage.

The adjust voltage at Pin 4 is internally applied across R_4, and an 8k resistor. The resulting current is mirrored four times to generate current sources I_{OA}, I_{OB}, I_{OC}, and I_{OD}, all equal in magnitude. When all four of the sense inputs are inside the fault window, a no-fault condition, Q_4 and Q_5 are turned on. In combination with D_1 and D_2 this prevents L_{OB} and L_{OD} from affecting the fault thresholds. In this case, the OV and UV thresholds are equal to $V_{REF} + I_{OA}(R_5 + R_6)$ and $V_{REF} - I_{OC}(R_7 + R_8)$ respectively. The fault window can be expressed as:

$$(1) \qquad 2.5V \pm \frac{V_{ADJ}}{4}.$$

In terms of a sensed nominal voltage level, V_S, the window as a percent variation is:

$$(2) \qquad V_S \pm (10 \cdot V_{ADJ})\ \%.$$

When a sense input moves outside the fault window given in equation(1), the appropriate hysteresis control signal turns off Q_4 or Q_5. For the under-voltage case, Q_5 is disabled and current source I_{OB} flows through D_2. The net current through R_7 becomes zero as I_{OB} cancels I_{OC}, giving an 8% reduction in the UV threshold offset. The over-voltage case is the same, with Q_4 turning off, allowing I_{OD} to cancel the current flow, I_{OA}, through R_6. The result is a hysteresis at the sense inputs which is always 8% of the window magnitude. This is shown graphically in Figure 2.

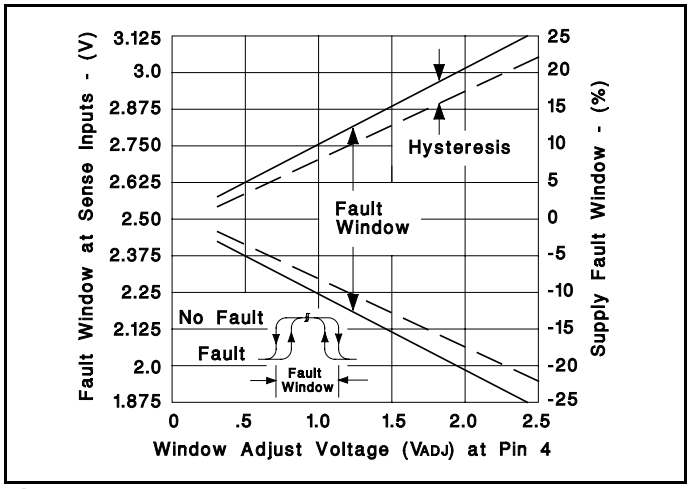


Figure 2. The fault window and threshold hysteresis scale as a function of the voltage applied at Pin 4, the window adjust pin.

Fault Windows Can Be Scaled Independently

In many applications, it may be desirable to monitor various supply voltages, or voltage levels, with varying fault windows. Using the reference output and external resistive dividers this is easily accomplished with the UC1903. Figures 3 and 4 illustrate how the fault window at any sense input can be scaled independently of the remaining inputs.

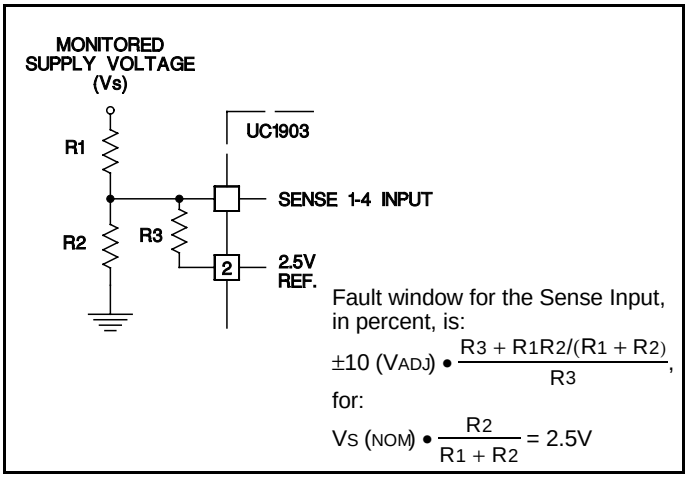


Figure 3. Using the reference output and a resistive divider, a sense input with an independently wider fault window can be generated.

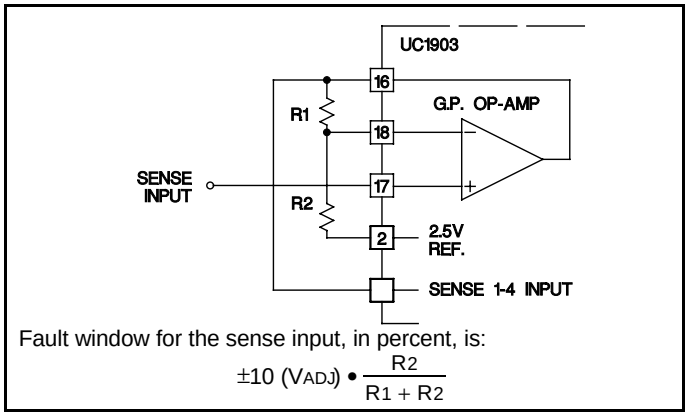


Figure 4. The general purpose op-amp on the UC1903 can be used to create a sense input with an independently tighter fault window.

Figure 4 demonstrates one of many auxiliary functions that the uncommitted op-amp on the UC1903 can be used for. Alternatively, this op-amp can be used to buffer high impedance points, perform logic functions, or for sensing and amplification. For example, the G.P. op-amp, combined with the 2.5V reference, can be used to produce and buffer an optically coupled feedback signal in isolated supplies with primary side control. The output stage of this op-amp is detailed in Figure 5. The NPN emitter follower provides high source current capability. ≥20mA while the substrate device, Q_3, provides good transient sinking capability.

OPERATION AND APPLICATION INFORMATION (continued)

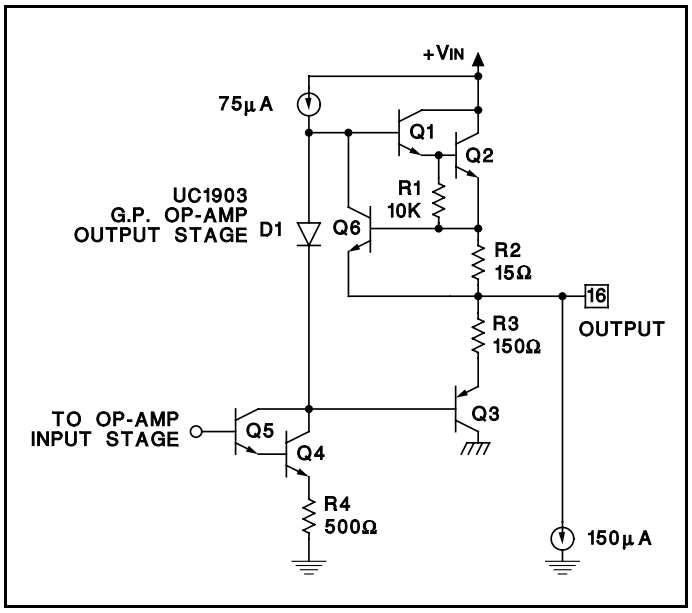


Figure 5. The G.P. op-amp on the UC1903 has a high source current (≥20mA) capability and enhanced transient sinking capability through substrate device Q3.

Sensing a Negative Voltage Level

The UC1903 has a dedicated inverter coupled to the sense 4 input. With this inverter, a negative voltage level can be sensed as shown in Figure 6. The output of the inverter is an unbiased emitter follower. By tying the inverting input, Pin 5, high the output emitter follower will be reverse biased, leaving the sense 4 input in a high impedance state. In this manner, the sense 4 input can be used, as the remaining sense inputs would be, for sensing positive voltage levels.

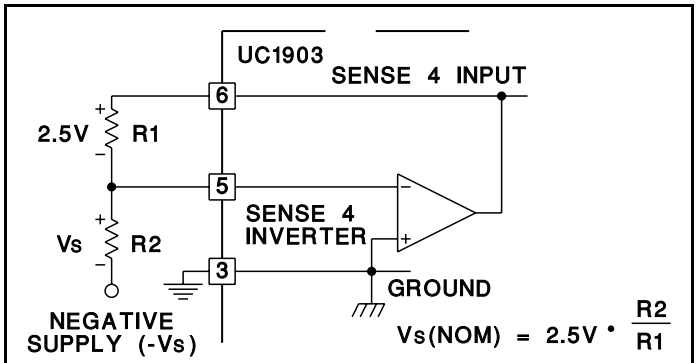


Figure 6. Inverting the sense 4 input for monitoring a negative supply is accommodated with the dedicated inverter.

Using The Line/Switcher Sense Output

The line switcher sense input to the UC1903 can be used for early detection of line, switcher, or other power source, failures. Internally referenced to 2.0V, the line sense comparator will cause the POWER OK output to indicate a fault (active low) condition when the LINE/SWITCHER SENSE input goes from above to below 2.0V. The line sense comparator has approximately 175mV of hysteresis requiring the line/switcher input to reach 2.175V before the POWER OK output device can be turned off, allowing a no-fault indication. In Figure 7 an example showing the use of the LINE/SWITCHER SENSE input for early switcher-fault detection is detailed. A sample signal is taken from the output of the power transformer, rectified and filtered, and used at the line/switcher input. By adjusting the R_2C time constant with respect to the switching frequency of the supply and the hold up time of the output capacitor, switcher faults can be detected before supply outputs are significantly affected.

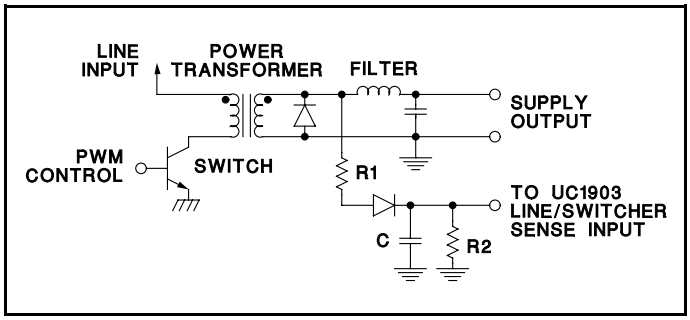


Figure 7. The line/switcher sense input can be used for an early line or switcher fault indication.

OV and UV Comparators Maintain Accurate Thresholds

The structure of the $\overline{OV}$ and $\overline{UV}$ comparators, shown in Figure 8 results in accurate fault thresholds even in the case where multiple sense inputs cross a fault threshold simultaneously. Unused sense inputs can be tied either to the 2.5V reference, or to another, utilized, sense input. The four under- and over-voltage sense inputs on the UC1903 are clamped as detailed on the Sense 1 input in Figure 8. The series 2k resistor, R_1, and zener diode Z_1, prevent extreme under- and over-voltage conditions from inverting the outputs of the fault comparators. A parasitic diode, D_1, is present at the inputs as well. Under normal operation it is advisable to insure that voltage levels at all of the sense inputs stay above -0.3V. The same type of input protection exists at the line sense input, Pin 15, except a 5k series resistor is used.

The fault delay circuitry on the UC1903 is also shown in Figure 8. In the case of an over-voltage condition at one of the sense inputs Q_{20} is turned off, allowing the internal 60µA current source to charge the user-selected delay capacitor. When the capacitor voltage reaches 1.8V, the $\overline{OV}$ and POWER OK outputs become active low. When the fault condition goes away Q_{20} is turned back on, rapidly discharging the delay capacitor. Operation of the under-voltage delay is, with appropriate substitutions, the same.

OPERATION AND APPLICATION INFORMATION (continued)

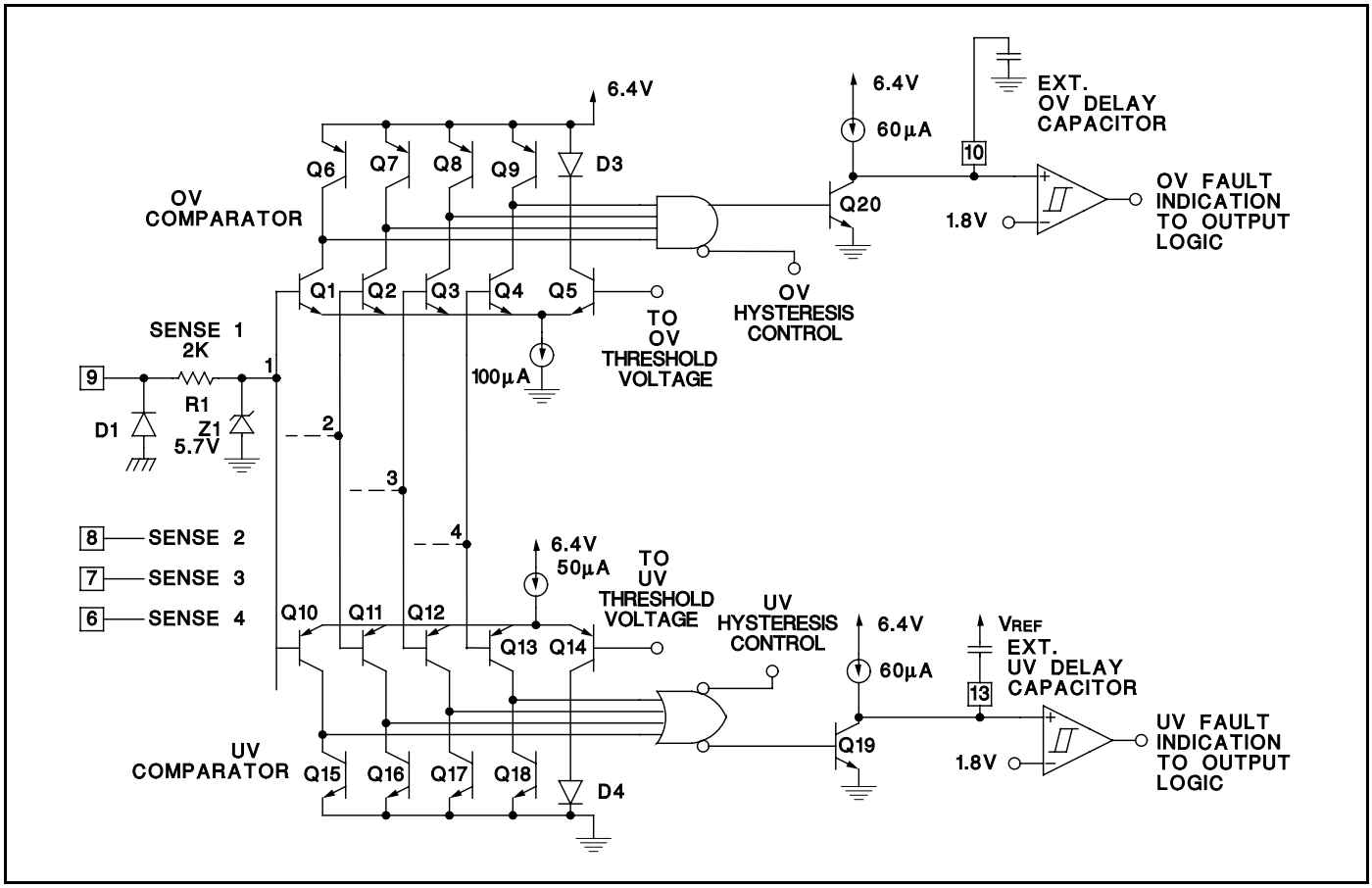


Figure 8. The OV and UV comparators on the UC1903 trigger respective fault delay circuits when one or more of the sense inputs move outside the fault window. Input clamps insure proper operation under extreme fault conditions. Terminating the UV delay capacitor to V_{REF} assures correct logic at power up.

Start Latch and Supply Under-Voltage Sense Allow Predictable Power-Up

The supply under-voltage sense and start-latch circuitry on the UC1903 prevents fault indications during start-up or low input supply ($+V_{IN}$) conditions. When the input supply voltage is below the supply under-voltage threshold the $\overline{OV}$ and $\overline{UV}$ fault outputs are disabled and the POWER OK output is active low. The POWER OK output will remain active until the input supply drops below approximately 3.0V. With $+V_{IN}$ below this level, all of the open collector outputs will be off.

When the input supply is low, the under-voltage sense circuitry resets the start-latch. With the start-latch reset, the UV fault output will remain disabled until the input supply rises to its normal operating level (8-40V), and all of the sense inputs are above the under-voltage threshold. This allows slow starting, or supply sequencing, without an artificial under-voltage fault indication. Once the latch is set, the UV fault output will respond if any of the sense inputs drop below the under-voltage threshold.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-88697012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8869701VA	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	N / A for Pkg Type
UC1903J	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	N / A for Pkg Type
UC1903J883B	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	N / A for Pkg Type
UC1903L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC1903L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC2903DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2903DWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2903DWTR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2903DWTRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2903J	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	N / A for Pkg Type
UC2903N	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2903NG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2903Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC2903QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC2903QTR	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC2903QTRG3	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3903DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3903DWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3903DWTR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3903DWTRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3903J	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	N / A for Pkg Type
UC3903N	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3903NG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3903Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3903QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3903QTRG3	ACTIVE	PLCC	FN	20		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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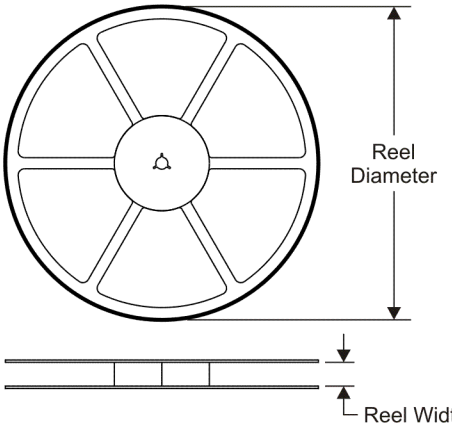
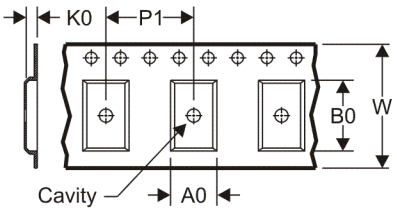
TAPE AND REEL INFORMATION

REEL DIMENSIONS

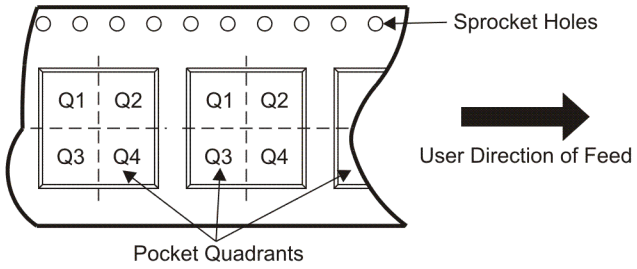


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

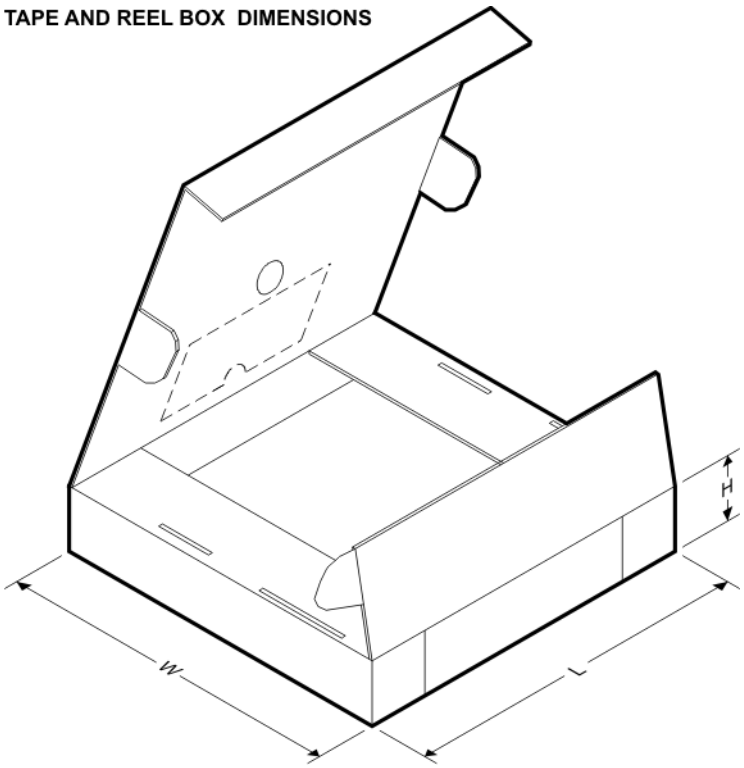
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2903DWTR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1
UC3903DWTR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2903DWTR	SOIC	DW	18	2000	346.0	346.0	41.0
UC3903DWTR	SOIC	DW	18	2000	346.0	346.0	41.0

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