Dual Channel Power Driver

FEATURES

- Two independent Drivers

- 1.5A Totem Pole Outputs

- Inverting and Non-Inverting Inputs

- 40ns Rise and Fall into 1000pF

- High-Speed, Power MOSFET Compatible

- Low Cross-Conduction Current Spike

- Analog Shutdown with Optional Latch

- Low Quiescent Current

- 5V to 40V Operation

- Thermal Shutdown Protection

- 16-Pin Dual-In-Line Package

- 20-Pin PLCC and CLCC Package

DESCRIPTION

The UC1707 family of power drivers is made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFETs. These devices contain two independent channels, each of which can be activated by either a high or low input logic level signal. Each output can source or sink up to 1.5A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, it can be forced low in common through the action either of a digital high signal at the Shutdown terminal or a differential low-level analog signal. The Shutdown command from either source can either be latching or not, depending on the status of the Latch Disable pin.

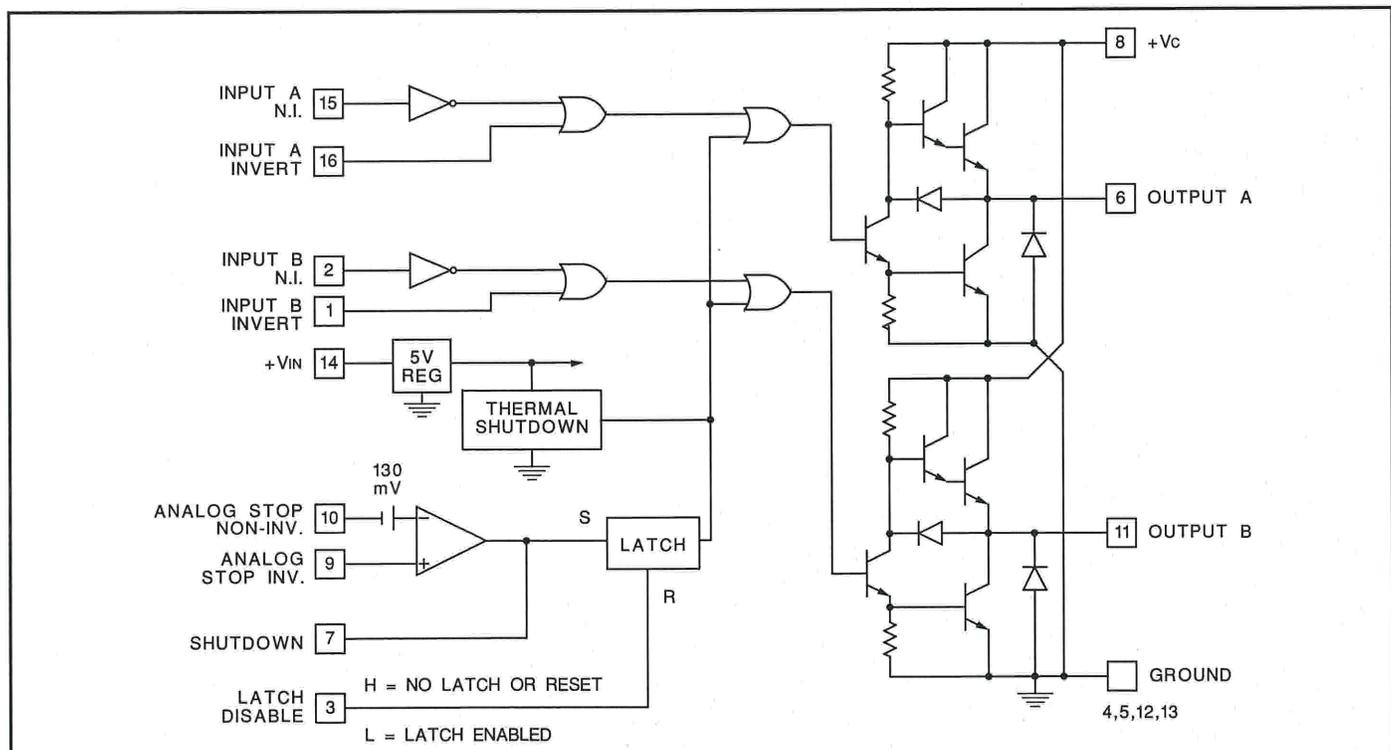Supply voltage for both VIN and VC can independently range from 5V to 40V.

These devices are available in two-watt plastic "bat-wing" DIP for operation over a 0°C to 70°C temperature range and, with reduced power, in a hermetically sealed cerdip for −55°C to +125°C operation. Also available in surface mount DW, Q, L packages.

TRUTH TABLE (Each Channel)

INV.	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

$OUT = \overline{INV}$ and N.I.

$\overline{OUT} = INV$ or N.I.

BLOCK DIAGRAM

INPUT A N.I. [15]
INPUT A INVERT [16]
INPUT B N.I. [2]
INPUT B INVERT [1]
+VIN [14] — 5V REG
THERMAL SHUTDOWN
130 mV
ANALOG STOP NON-INV. [10]
ANALOG STOP INV. [9]
SHUTDOWN [7]
LATCH DISABLE [3]
S — LATCH — R
H = NO LATCH OR RESET
L = LATCH ENABLED

[8] +Vc
[6] OUTPUT A
[11] OUTPUT B
GROUND 4,5,12,13

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VIN, N/J-Pkg 40V
Collector Supply Voltage, VC, N/J-Pkg 40V
Output Current (Each Output, Source or Sink) Steady-State,
    N/J-Pkg . . . . ±500mA
 Peak Transient
    N-Pkg . . . . ±1.5A
    J-Pkg . . . . ±1.0A
 Capacitive Discharge Energy
    N-Pkg 20mJ
    J-Pkg 15mJ
Digital Inputs (See Note), N/J-Pkg 5.5V
Analog Stop Inputs, N/J-Pkg . . . . VIN
Power Dissipation at T_A = 25°C (See Note)
    N-Pkg 2W
    J-Pkg 1W
Power Dissipation at T (Leads/Case) = 25°C (See Note)
    N-Pkg 5W
    J-Pkg 2W
Operating Temperature Range . . . . –55°C to +125°C
Storage Temperature Range . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . 300°C

Note: All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal. Digital Drive can exceed 5.5V if input current is limited to 10mA. Consult Packaging section of Databook for thermal limitations and considerations of package.
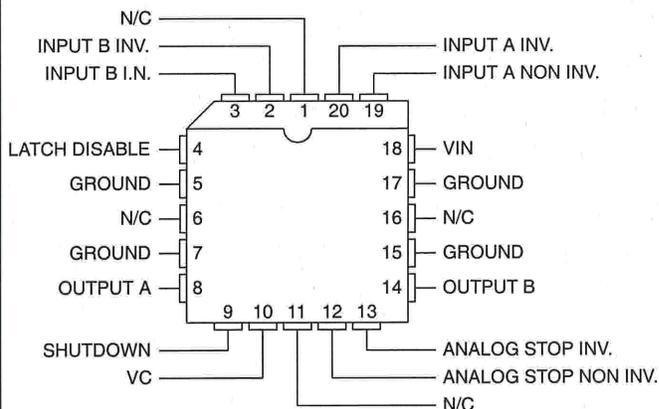
CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N Package,

INPUT B INV.	1	16 INPUT A INV.
INPUT B N.I.	2	15 INPUT A N.I.
LATCH DISABLE	3	14 +VIN
GROUND	4	13 GROUND
GROUND	5	12 GROUND
OUTPUT A	6	11 OUTPUT B
SHUTDOWN	7	10 ANALOG STOP NON-INV.
+Vc	8	9 ANALOG STOP INV.
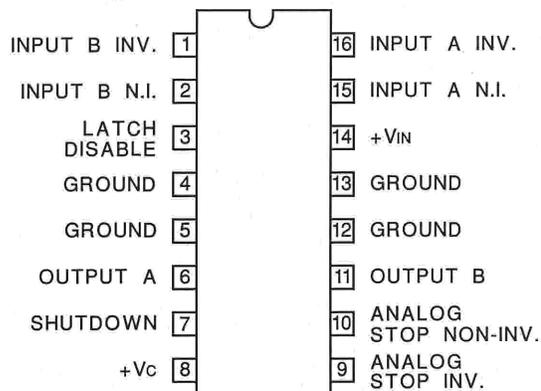
Note: All four ground pins must be connected to a common ground.

PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages

N/C
INPUT B INV.
INPUT B I.N.

INPUT A INV.
INPUT A NON INV.

LATCH DISABLE 4	18 VIN
GROUND 5	17 GROUND
N/C 6	16 N/C
GROUND 7	15 GROUND
OUTPUT A 8	14 OUTPUT B

3 2 1 20 19

9 10 11 12 13

SHUTDOWN
VC

ANALOG STOP INV.
ANALOG STOP NON INV.
N/C

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1707, –25°C to +85°C for the UC2707 and 0°C to +70°C for the UC3707; V_{IN} = V_C = 20V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	V_{IN} = 40V		12	15	mA
V_C Supply Current	V_C = 40V, Outputs Low		5.2	7.5	mA
V_C Leakage Current	V_{IN} =0, VC =30V, No Load		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		–0.06	–1.0	mA
Input Leakage	V_I = 5V		.05	0.1	mA
Output High Sat., V_C-V_O	I_O = –50mA			2.0	V
	I_O = –500mA			2.5	V
Output Low Sat., V_O	I_O = –50mA			0.4	V
	I_O = –500mA			2.5	V
Analog Threshold	V_{CM} = 0 to 15V	100	130	160	mV
Input Bias Current	V_{CM} = 0		–10	–20	μA
Thermal Shutdown			155		°C
Shutdown Threshold	Pin 7 Input	0.4	1.0	2.2	V
Latch Disable Threshold	Pin 3 Input	0.8	1.2	2.2	V

TYPICAL SWITCHING CHARACTERISTICS: V_{IN} = V_C = 20V, T_A = 25°C. Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT CL =			UNITS
From Inv. Input to Output		open	1.0	2.2	nF
Rise Time Delay		40	50	60	ns
10% to 90% Rise		25	40	50	ns
Fall Time Delay		30	40	50	ns
90% to 10% Fall		25	40	50	ns
From N.I. Input to Output					
Rise Time Delay		30	40	50	ns
10% to 90% Rise		25	40	50	ns
Fall Time Delay		45	55	65	ns
90% to 10% Fall		25	40	50	ns
V_C Cross-Conduction	Output Rise	25			ns
Current Spike Duration	Output Fall	0			ns
Analog Shutdown Delay	Stop non-Inv. = 0V	180			ns
	Stop Inv. = 0 to 0.5V	180			ns
Digital Shutdown Delay	2V Input on Pin 7	50			ns

SIMPLIFIED INTERNAL CIRCUITRY

The input common-mode voltage range is from ground to (VIN-3V). When not used both inputs should be grounded. Activate time is a function of overdrive with a typical value of 180ns. Pin 7 serves both as a comparator output and as a common digital shutdown input. A high signal here will accomplish the fastest turn off of both outputs. Note that "OFF" is defined as the outputs low. Pulling shutdown low defeats the latch operation regardless of its status.

Figure 1. Typical digital input gate.

The input zener may be used to clamp input signal voltages higher than 5V as long as the zener current is limited to 10mA max. External pull-up resistors are not required.
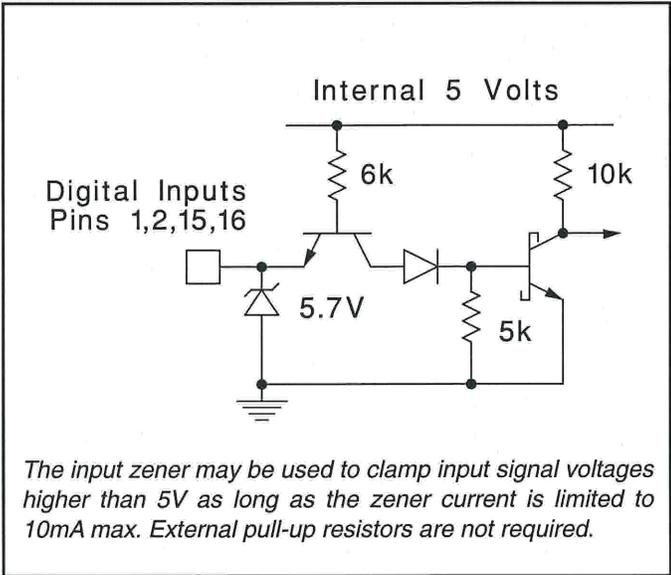
Figure 2. Typical digital input gate.

The Shutdown latch is disabled when pin 3 is open. An impedance of 4k or less from pin 3 to ground will allow a shutdown signal to set the latch which can then be reset by either recycling the VIN supply or by momentarily (>200ns) raising pin 3 high.
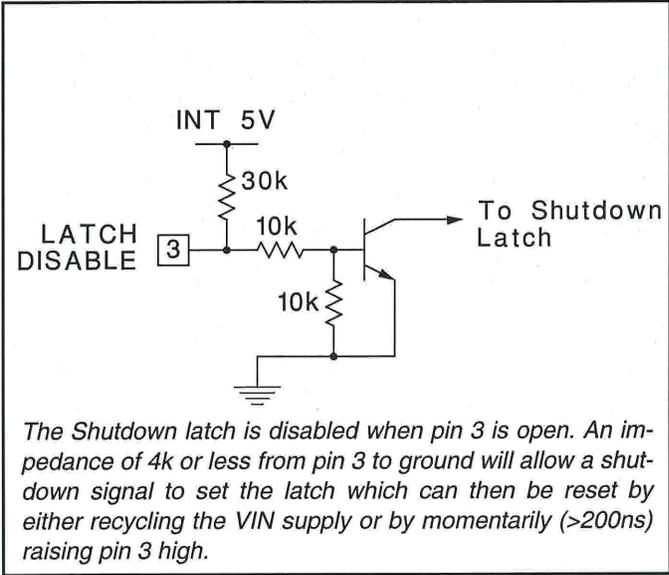
Figure 3. Latch disable.

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SIMPLIFIED INTERNAL CIRCUITRY (cont.)
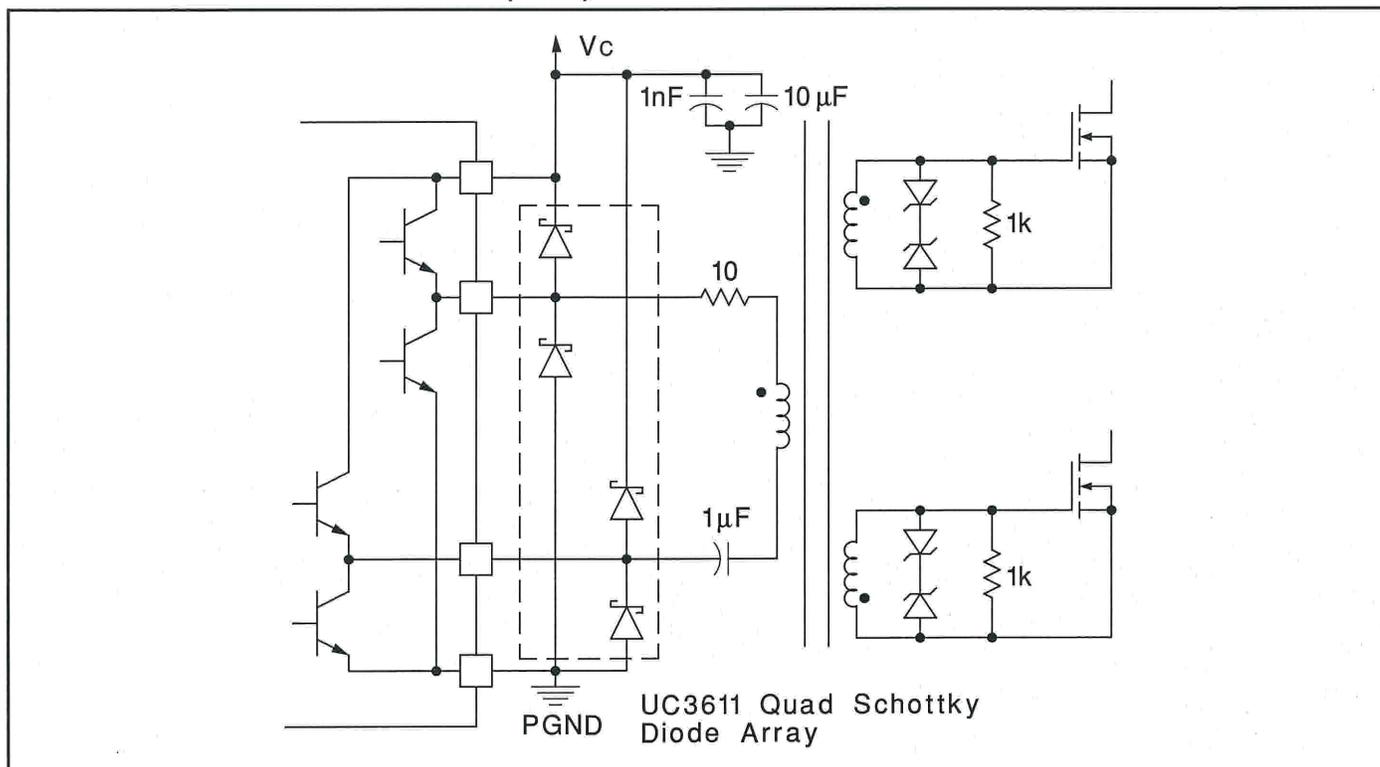
Figure 4. Transformer coupled push-pull MOSFET drive circuit.
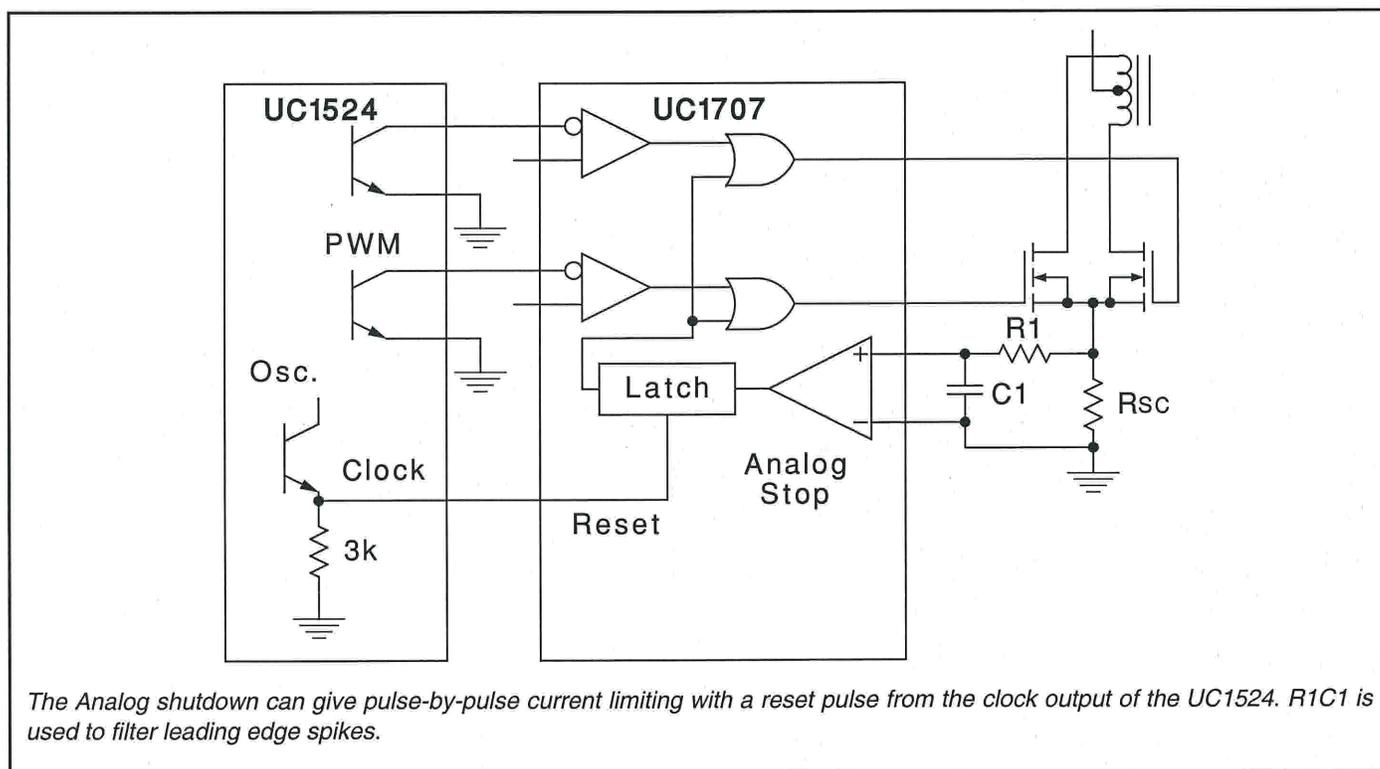
The Analog shutdown can give pulse-by-pulse current limiting with a reset pulse from the clock output of the UC1524. R1C1 is used to filter leading edge spikes.

Figure 5. Current limiting.

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APPLICATIONS

With an external reference, the shutdown comparator can be used for over-voltage protection. R1 and R2 set the shutdown level while R3 adds positive feedback for hysteresis.
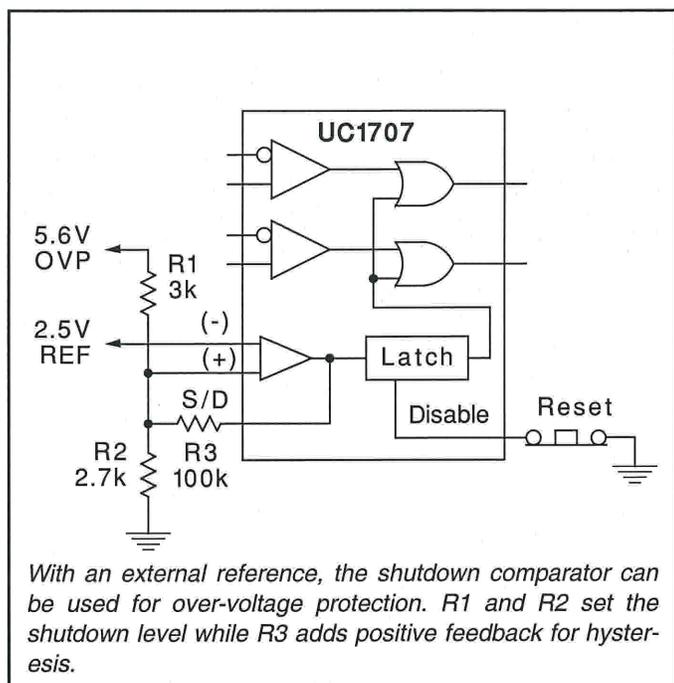
Figure 6. Over-voltage protection.

D1, D2: UC3611 Schottky Diodes

Figure 7. Power MOSFET drive circuit.

When driven with a TTL square wave drive, the low output impedance of the UC1707 allows ready implementation of charge pump voltage converters.

Figure 8. Charge pump circuits.

D1, D2: UC3611 Schottky Diodes
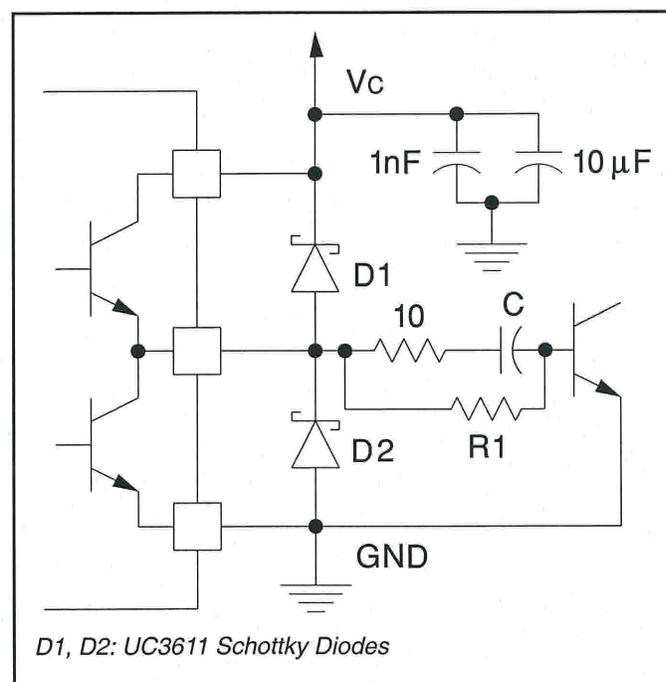
Figure 9. Power bipolar drive circuit.

TRANSFORMER COUPLING

D1, D2: UC3611 Schottky Diode
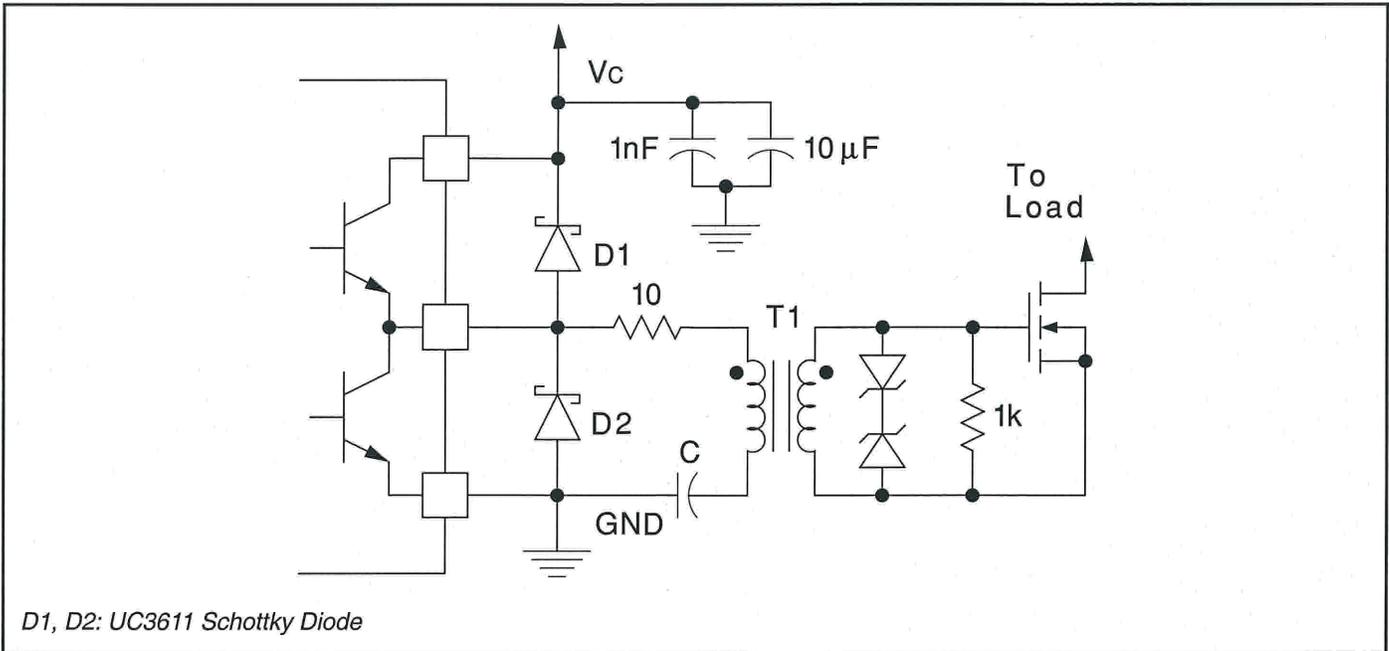
Figure 10. Transformer coupled MOSFET drive circuit.

D1, D2: UC3611 Schottky Diode
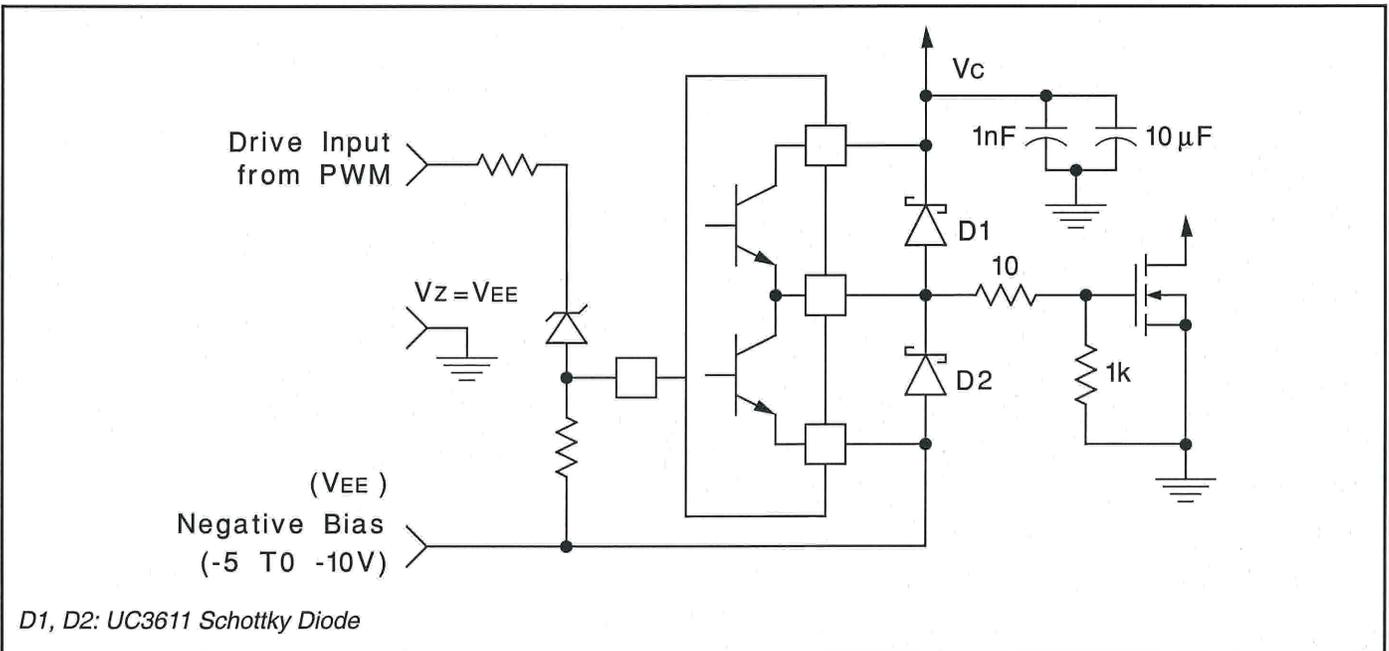
Figure 11. Power MOSFET drive circuit using negative bias voltage and level shifting to ground reference PWM.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-87619012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8761901EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8761901V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8761901VEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
UC1707J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC1707J/80313	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC1707J883B	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC1707JQMLV	ACTIVE	CDIP	J	16		TBD	Call TI	Call TI
UC1707L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC1707L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC2707DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2707DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2707DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2707DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2707N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2707NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2707Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC2707QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3707DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3707DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3707DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3707DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3707J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC3707N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3707NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3707Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3707QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in

a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check
http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements
for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered
at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and
package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS
compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame
retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder
temperature.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
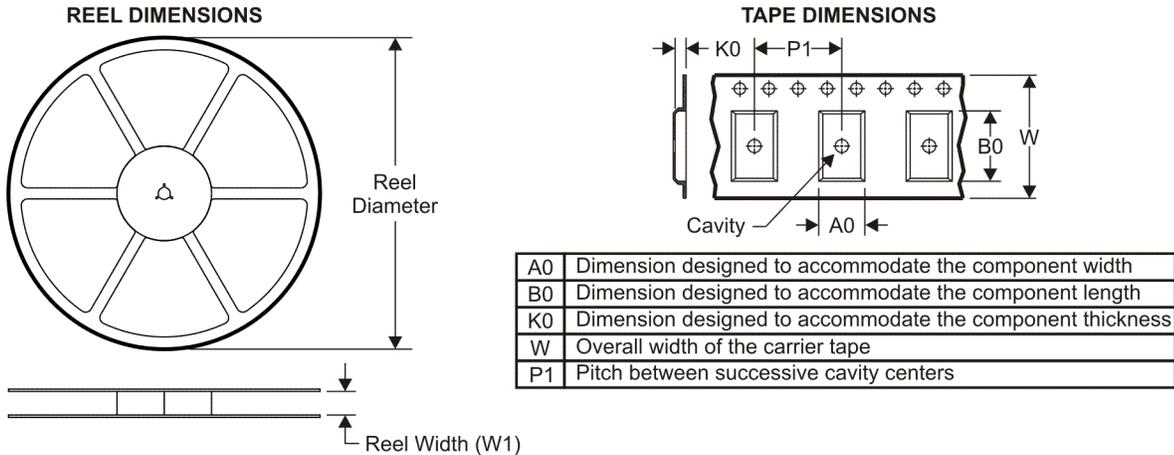
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
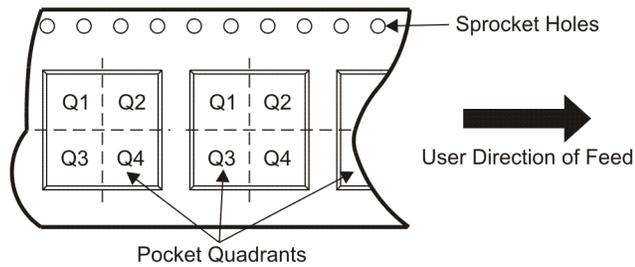
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2707DWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1
UC3707DWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS
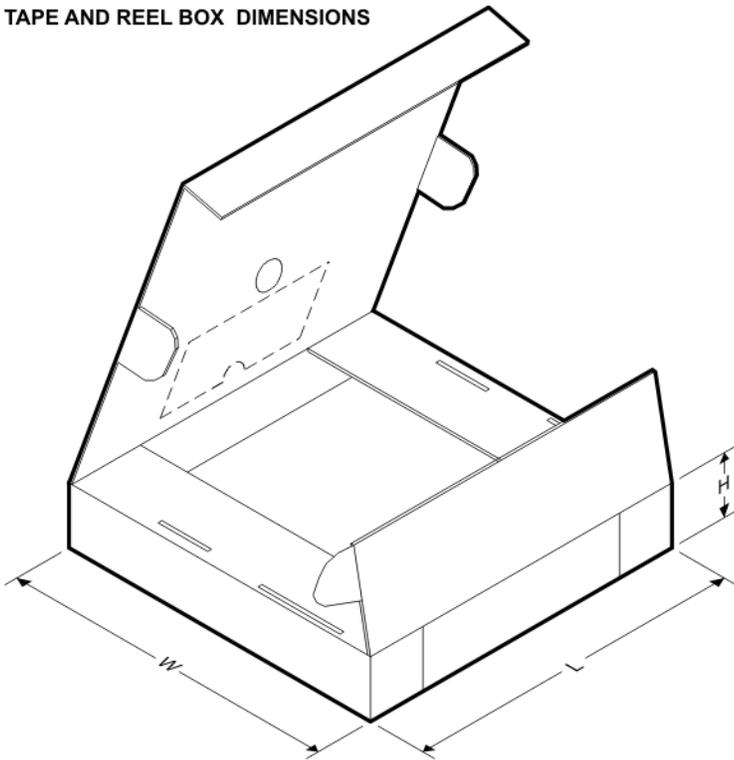
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2707DWTR	SOIC	DW	16	2000	346.0	346.0	33.0
UC3707DWTR	SOIC	DW	16	2000	346.0	346.0	33.0