UNITRODE

UC1901
UC2901
UC3901

Isolated Feedback Generator

FEATURES

- An Amplitude-Modulation System for Transformer Coupling an Isolated Feedback Error Signal
- Low-Cost Alternative to Optical Couplers
- Internal 1% Reference and Error Amplifier
- Internal Carrier Oscillator Usable to 5MHz
- Modulator Synchronizable to an External Clock
- Loop Status Monitor

DESCRIPTION

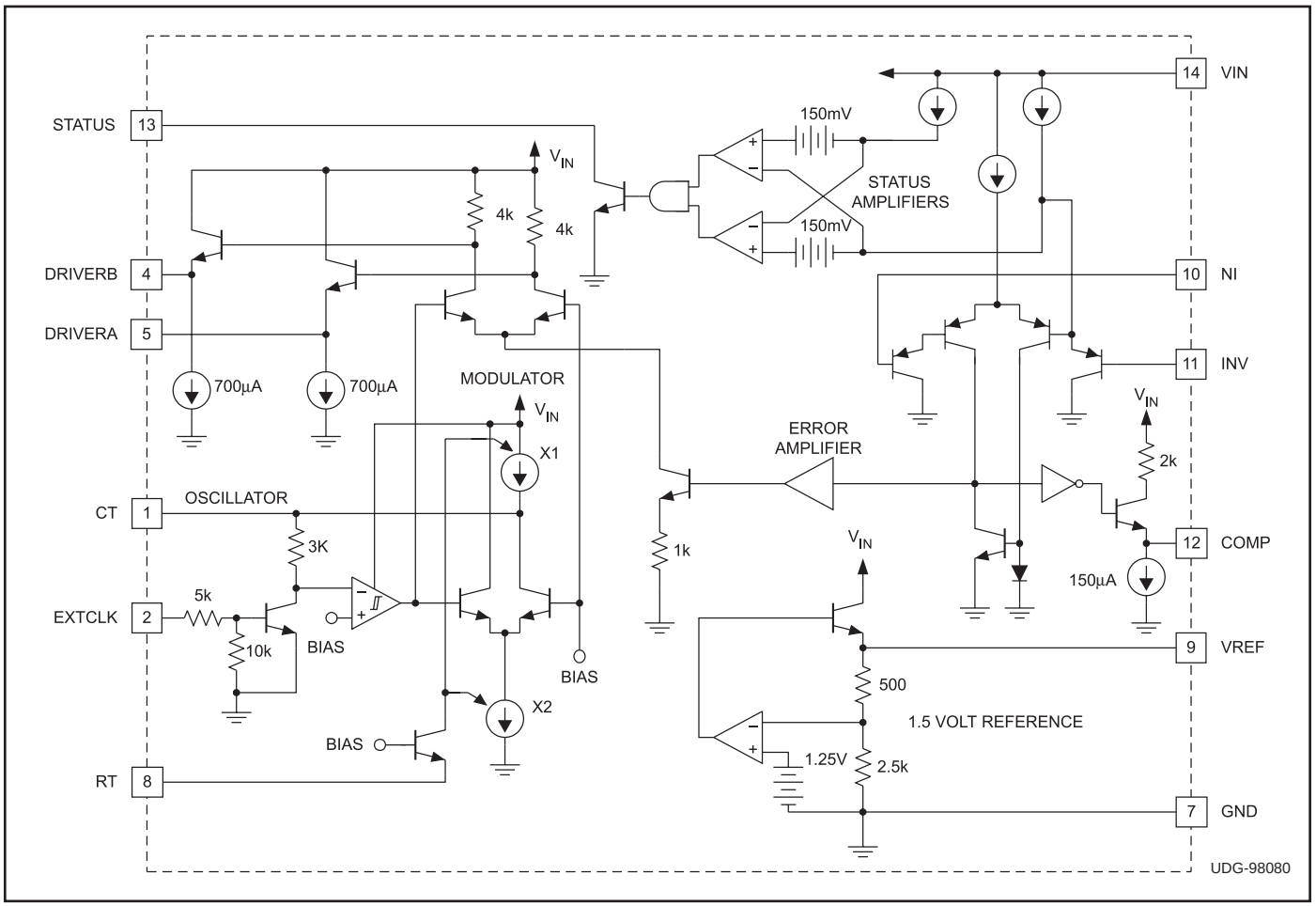
The UC1901 family is designed to solve many of the problems associated with closing a feedback control loop across a voltage isolation boundary. As a stable and reliable alternative to an optical coupler, these devices feature an amplitude modulation system which allows a loop error signal to be coupled with a small RF transformer or capacitor.

The programmable, high-frequency oscillator within the UC1901 series permits the use of smaller, less expensive transformers which can readily be built to meet the isolation requirements of today's line-operated power systems. As an alternative to RF operation, the external clock input to these devices allows synchronization to a system clock or to the switching frequency of a SMPS.

An additional feature is a status monitoring circuit which provides an active-low output when the sensed error voltage is within ±10% of the reference. The DRIVERA output, DRIVERB output, and STATUS output are disabled until the input supply has reached a sufficient level to allow proper operation of the device.

Since these devices can also be used as a DC driver for optical couplers, the benefits of 4.5 to 40V supply operation, a 1% accurate reference, and a high gain general purpose amplifier offer advantages even though an AC system may not be desired.

UC1901 SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS *(Note 1)*

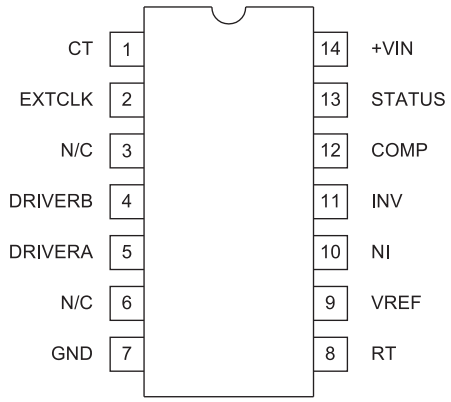
Input Supply Voltage, V_{IN} 40V
Reference Output Current . . . . . –10mA
Driver Output Currents . . . . . –35mA
Status Indicator Voltage 40V
Status Indicator Current 20mA
Ext. Clock Input 40V
Error Amplifier Inputs . . . . . –0.5V to +35V
Power Dissipation at T_A = 25°C 1000mW
Power Dissipation at T_C = 25°C 2000mW
Operating Junction Temperature . . . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

Note 1*: Voltages are referenced to ground, Pin 7. Currents are positive into, negative out of the specified terminal.*

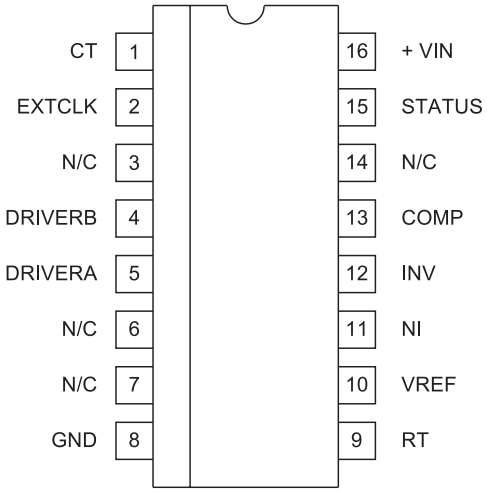
Note 2*: Consult Packaging section of Databook for thermal limitations and considerations of package.*

CONNECTION DIAGRAMS

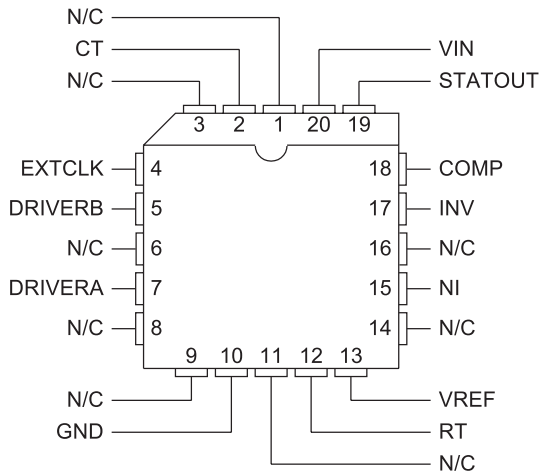
DIL-14, SOIC-14 (TOP VIEW)
J or N Package, D Package



SOIC-16 Wide (TOP VIEW)
DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



TEMPERATURE AND PACKAGE SELECTION GUIDE

	TEMPERATURE RANGE	AVAILABLE PACKAGES
UC1901	–55°C to +125°C	J, L
UC2901	–40°C to +85°C	D, DW, J, N, Q
UC3901	0°C to +70°C	D, DW, J, N, Q

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for V_{IN} = 10V, R_T = 10kΩ, C_T = 820pF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1901/UC2901			UC3901			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_{MIN} \le T_J \le T_{MAX}$	1.470	1.5	1.530	1.455	1.5	1.545	
Line Regulation	V_{IN} = 4.5 to 35V		2	10		2	15	mV
Load Regulation	I_{OUT} = 0 to 5mA		4	10		4	15	mV
Short Circuit Current	T_J = 25°C		–35	–55		–35	–55	mV
Error Amplifier Section (To Compensation Terminal)								
Input Offset Voltage	V_{CM} = 1.5V		1	4		1	8	mV
Input Bias Current	V_{CM} = 1.5V		–1	–3		–1	–6	µA
Input Offset Current	V_{CM} = 1.5V		0.1	1		0.1	2	µA
Small Signal Open Loop Gain		40	60		40	60		dB
CMRR	V_{CM} = 0.5 to 7.5V	60	80		60	80		dB
PSRR	V_{IN} = 2 to 25V	80	100		80	100		dB
Output Swing, Δ V_O		0.4	0.7		0.4	0.7		V
Maximum Sink Current		90	150		90	150		µA
Maximum Source Current		–2	–3		–2	–3		mA
Gain Band Width Product			1			1		MHz
Slew Rate			0.3			0.3		V/µS
Modulators/Drivers Section (From Compensation Terminal)								
Voltage Gain		11	12	13	10	12	14	dB
Output Swing		±1.6	±2.8		±1.6	±2.8		V
Driver Sink Current		500	700		500	700		µA
Driver Source Current		–15	–35		–15	–35		mA
Gain Band Width Product			25			25		MHz
Oscillator Section								
Initial Accuracy	T_J = 25°C	140	150	160	130	150	170	kHz
	$T_{MIN} \le T_J \le T_{MAX}$	130		170	120		180	kHz
Line Sensitivity	V_{IN} = 5 to 35V		.15	.35		.15	.60	%/V
Maximum Frequency	R_T = 10k, C_T = 10pF		5			5		MHz
Ext. Clock Low Threshold	Pin 1 (C_T) = V_{IN}	0.5			0.5			V
Ext. Clock High Threshold	Pin 1 (C_T) = V_{IN}			1.6			1.6	V
Status Indicator Section								
Input Voltage Window	@ E/A Inputs, V_{CM} = 1.5V	±135	±150	±165	±130	±150	±170	mV
Saturation Voltage	E/A Δ Input = 0V, I_{SINK} = 1.6mA			0.45			0.45	V
Max. Output Current	Pin 13 = 3V, E/A Δ Input = 0.0V	8	15		8	15		mA
Leakage Current	Pin 13 = 40V, E/A ΔInput = 0.2V		.05	1		.05	5	µA
Supply Current	V_{IN} = 35V		5	8		5	10	mA
UVLO Section								
Drivers Enabled Threshold	At Input Supply V_{IN}		3.9	4.5		3.9	4.5	V
Status Output Enabled Threshold	At Input Supply V_{IN}		3.9	4.5		3.9	4.5	V
Change in Reference Output	When V_{IN} Reaches UVLO Threshold		–2	–30		–2	–30	mV

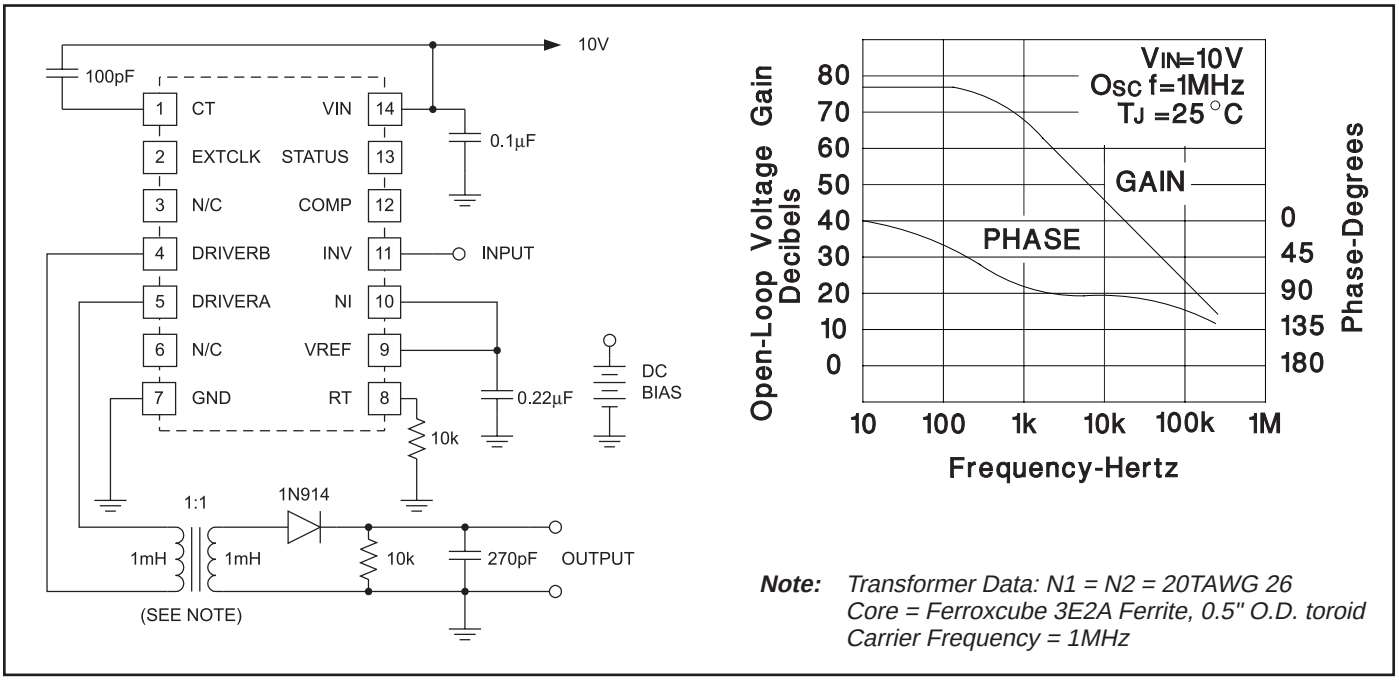


Figure 1. Transformer Coupled Open Loop Transfer Function

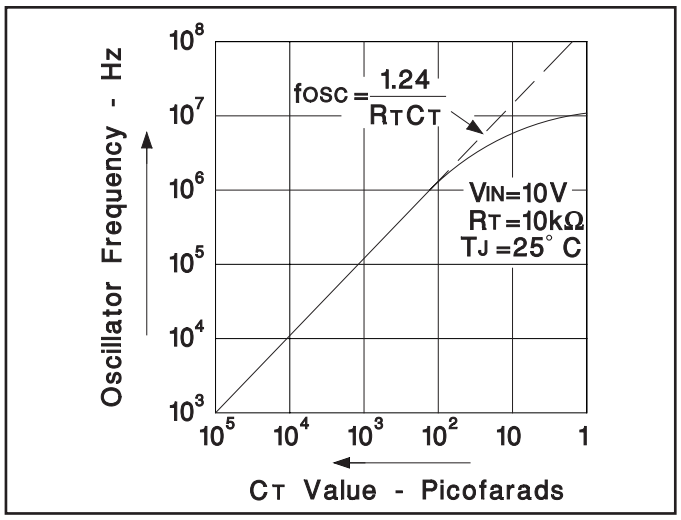


Figure 2. Oscillator Frequency

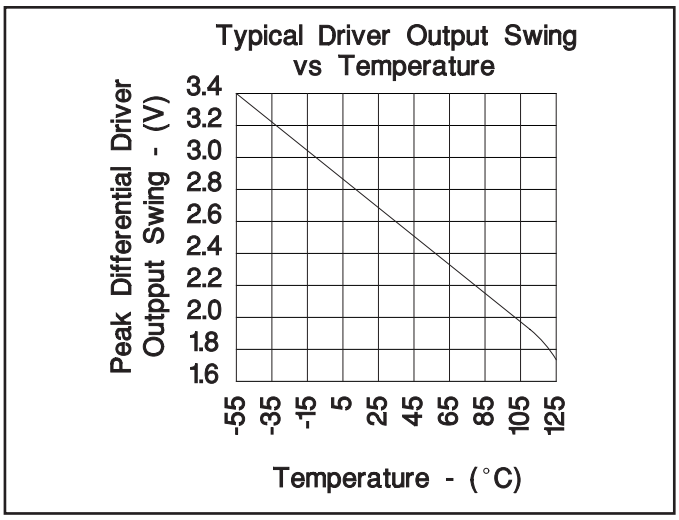


Figure 3. Typical Driver Output Swing vs Temperature

APPLICATION INFORMATION

The error amplifier compensation terminal, Pin 12, is intended as a source of feedback to the amplifier's inverting input at Pin 11. For most applications, a series DC blocking capacitor should be part of the feedback network. The amplifier is internally compensated for unity feedback.

The waveform at the driver outputs is a squarewave with an amplitude that is proportional to the error amplifier input signal. There is a fixed 12dB of gain from the error amplifier compensation pin to the modulator driver outputs. The frequency of the output waveform is controlled by either the internal oscillator or an external clock signal. With the internal oscillator the squarewave will have a fixed 50% duty cycle. If the internal oscillator is disabled by connecting Pin 1, C_R, to V_{IN} then the frequency and duty cycle of the output will be determined by the input clock waveform at Pin 2. If the oscillator remains disabled and there is not clock input at Pin 2, there will be a linear 12dB of signal gain to one or the other of the driver outputs depending on the DC state of Pin 2.

The driver outputs are emitter followers which will source a minimum of 15mA of current. The sink current, internally limited at 700µA, can be increased by adding resistors to ground at the driver outputs.

APPLICATION INFORMATION (continued)

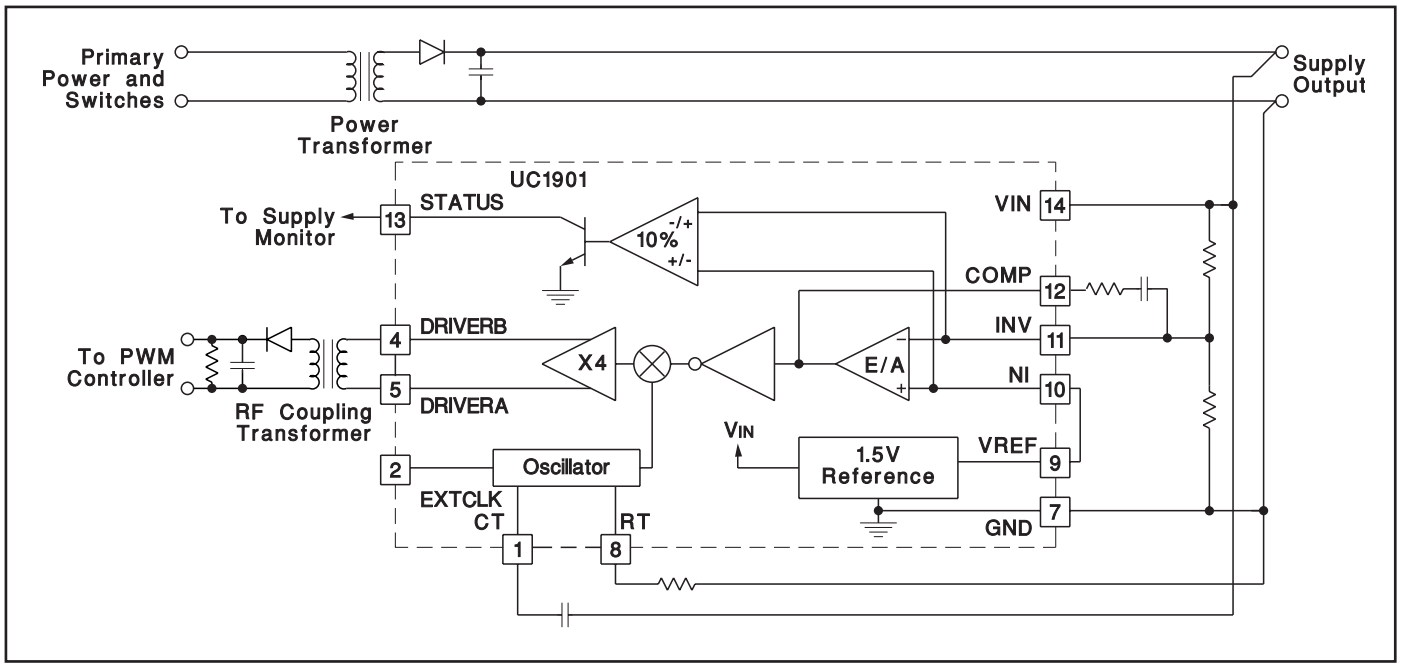


Figure 4. R.F. Transformer Coupled Feedback

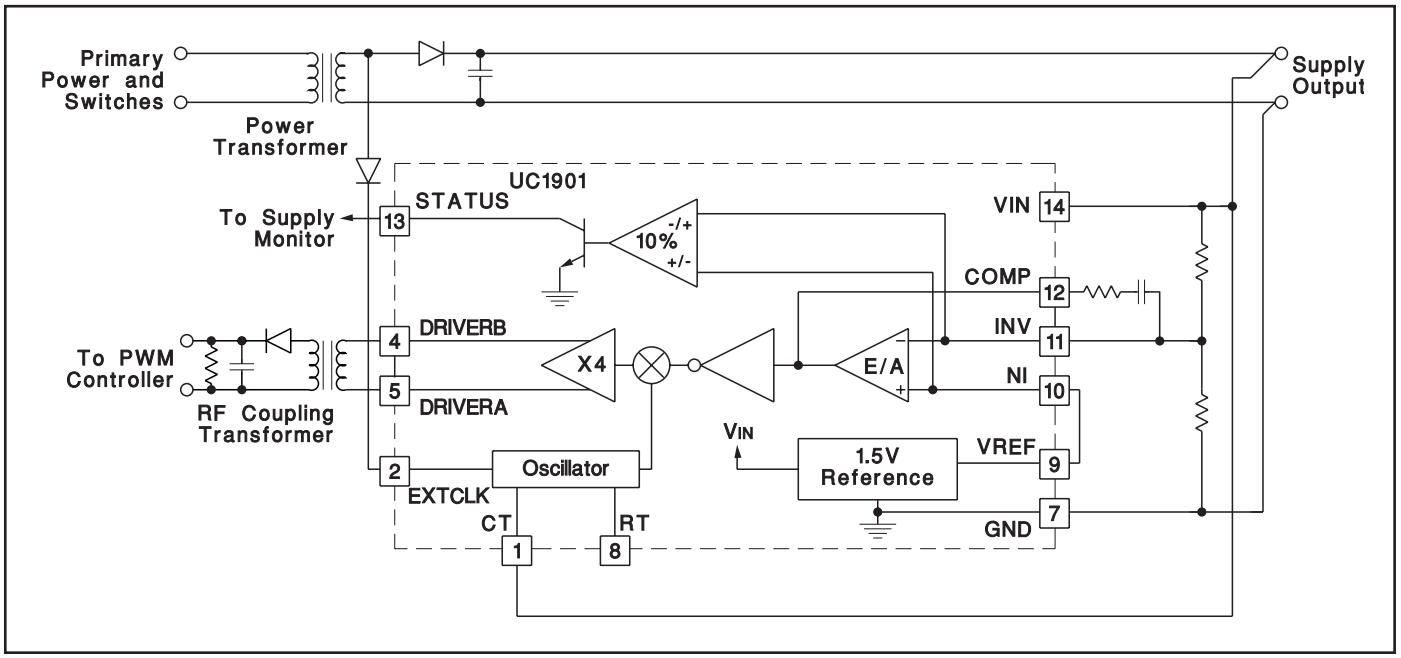


Figure 5. Feedback Coupled at Switching Frequency

TYPICAL APPLICATION

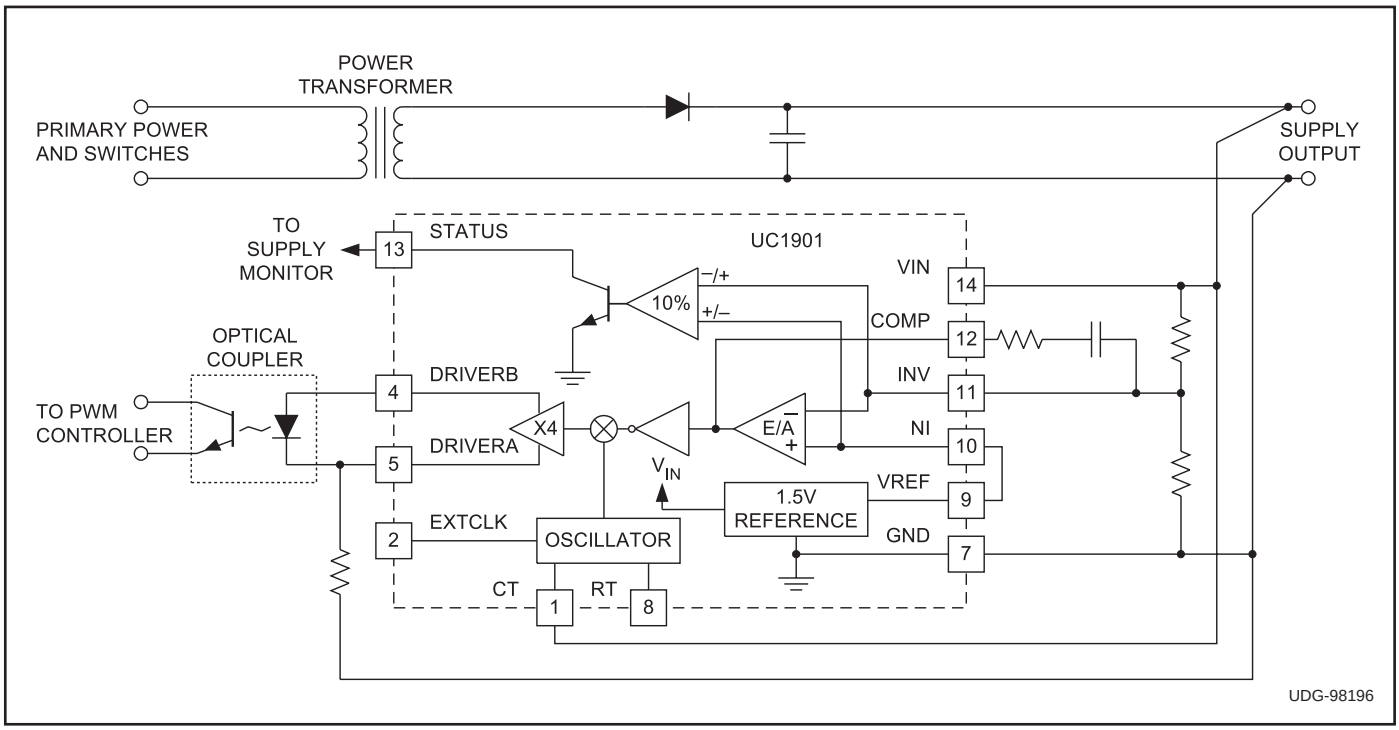


Figure 6. Optically Coupled DC Feedback

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-89441012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-8944101CA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
5962-8944101VCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
UC1901J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1901J883B	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1901L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
UC1901L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
UC2901D	ACTIVE	SOIC	D	14	50	TBD	CU NIPDAU	Level-1-220C-UNLIM
UC2901DTR	ACTIVE	SOIC	D	14	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
UC2901DW	ACTIVE	SOIC	DW	16	40	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC2901DWTR	ACTIVE	SOIC	DW	16	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC2901J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
UC2901N	ACTIVE	PDIP	N	14	25	TBD	CU NIPDAU	Level-NA-NA-NA
UC2901Q	ACTIVE	PLCC	FN	20	46	TBD	CU SNPB	Level-2-220C-1 YEAR
UC2901QTR	ACTIVE	PLCC	FN	20	1000	TBD	CU SNPB	Level-2-220C-1 YEAR
UC3901D	ACTIVE	SOIC	D	14	50	TBD	CU NIPDAU	Level-1-220C-UNLIM
UC3901DTR	ACTIVE	SOIC	D	14	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
UC3901DW	ACTIVE	SOIC	DW	16	40	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC3901DWTR	ACTIVE	SOIC	DW	16	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC3901DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3901J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
UC3901N	ACTIVE	PDIP	N	14	25	TBD	CU NIPDAU	Level-NA-NA-NA
UC3901Q	ACTIVE	PLCC	FN	20	46	TBD	CU SNPB	Level-2-220C-1 YEAR
UC3901QTR	ACTIVE	PLCC	FN	20	1000	TBD	CU SNPB	Level-2-220C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
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(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGING INFORMATION

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5962-89441012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8944101CA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8944101VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
UC1901J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
UC1901J883B	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
UC1901L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC1901L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC2901D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2901DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2901DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2901DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2901DWG4	ACTIVE	SOIC	DW	16		TBD	Call TI	Call TI
UC2901DWTRG4	ACTIVE	SOIC	DW	16		TBD	Call TI	Call TI
UC2901J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
UC2901N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2901NG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2901Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC2901QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3901D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3901DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3901DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3901DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3901DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3901DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3901DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3901DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3901N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3901NG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3901Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
UC3901QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3901QTR	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3901QTRG3	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR

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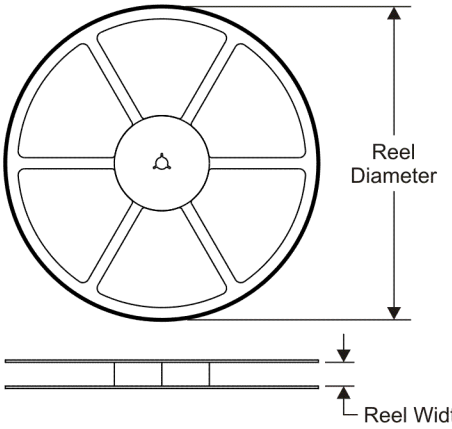
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

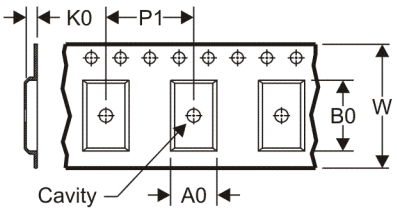
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

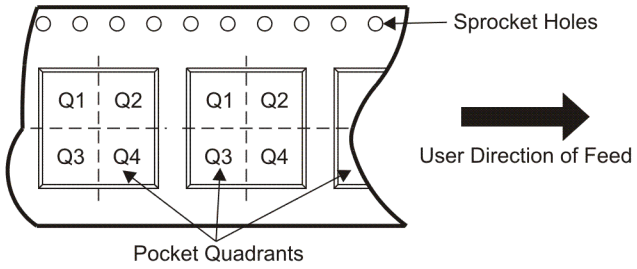


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

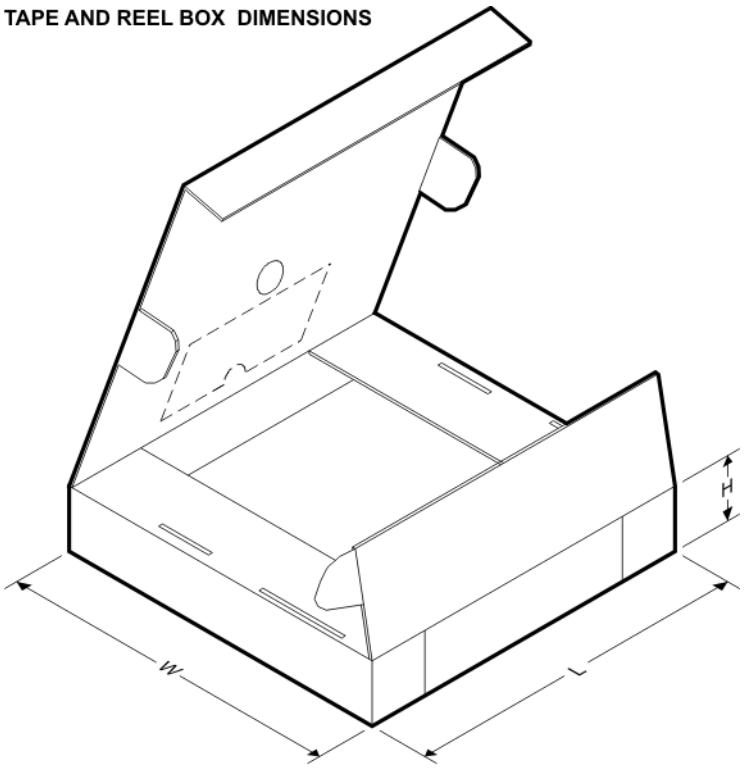
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2901DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3901DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3901DWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2901DTR	SOIC	D	14	2500	346.0	346.0	33.0
UC3901DTR	SOIC	D	14	2500	346.0	346.0	33.0
UC3901DWTR	SOIC	DW	16	2000	346.0	346.0	33.0

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