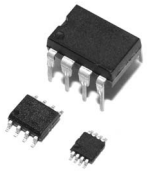


SLUS545B − NOVEMBER 2002 − REVISED NOVEMBER 2004

DUAL 4-A HIGH SPEED LOW−SIDE MOSFET DRIVERS WITH ENABLE

FEATURES

- **Industry-Standard Pin-Out**
- **Enable Functions for Each Driver**
- **High Current Drive Capability of ±4 A**
- **Unique BiPolar and CMOS True Drive Output Stage Provides High Current at MOSFET Miller Thresholds**
- **TTL/CMOS Compatible Inputs Independent of Supply Voltage**
- **20-ns Typical Rise and 15-ns Typical Fall Times with 1.8-nF Load**
- **Typical Propagation Delay Times of 25 ns with Input Falling and 35 ns with Input Rising**
- **4-V to 15-V Supply Voltage**
- **Dual Outputs Can Be Paralleled for Higher Drive Current**
- **Available in Thermally Enhanced MSOP PowerPAD™ Package with 4.7°C/W θjc**
- **Rated From –40°C to 105°C**

APPLICATIONS

- **Switch Mode Power Supplies**
- **DC/DC Converters**
- **Motor Controllers**
- **Line Drivers**
- **Class D Switching Amplifiers**

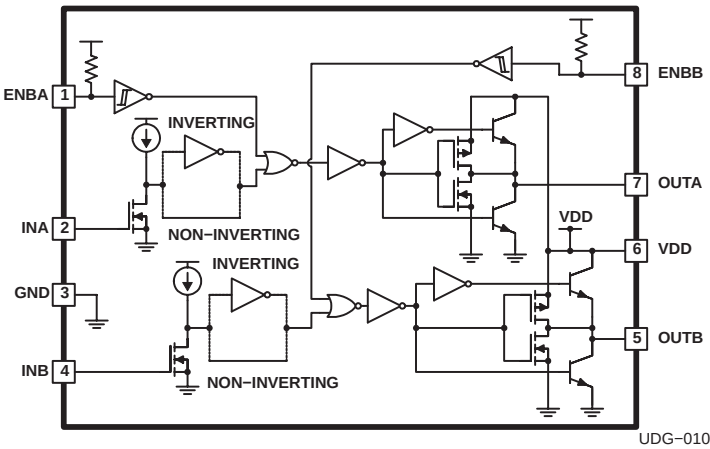
DESCRIPTION

The UCC27423/4/5 family of high-speed dual MOSFET drivers can deliver large peak currents into capacitive loads.Three standard logic options are offered – dual-inverting, dual-noninverting and one-inverting and one-noninverting driver. The thermally enhanced 8-pin PowerPAD™ MSOP package (DGN) drastically lowers the thermal resistance to improve long-term reliability. It is also offered in the standard SOIC-8 (D) or PDIP-8 (P) packages.

Using a design that inherently minimizes shoot-through current, these drivers deliver 4-A of current where it is needed most at the Miller plateau region during the MOSFET switching transition. A unique BiPolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing and sinking at low supply voltages.

The UCC27423/4/5 provides enable (ENBL) functions to have better control of the operation of the driver applications. ENBA and ENBB are implemented on pins 1 and 8 which were previously left unused in the industry standard pin-out. They are internally pulled up to Vdd for active high logic and can be left open for standard operation.

BLOCK DIAGRAM



UDG−01063

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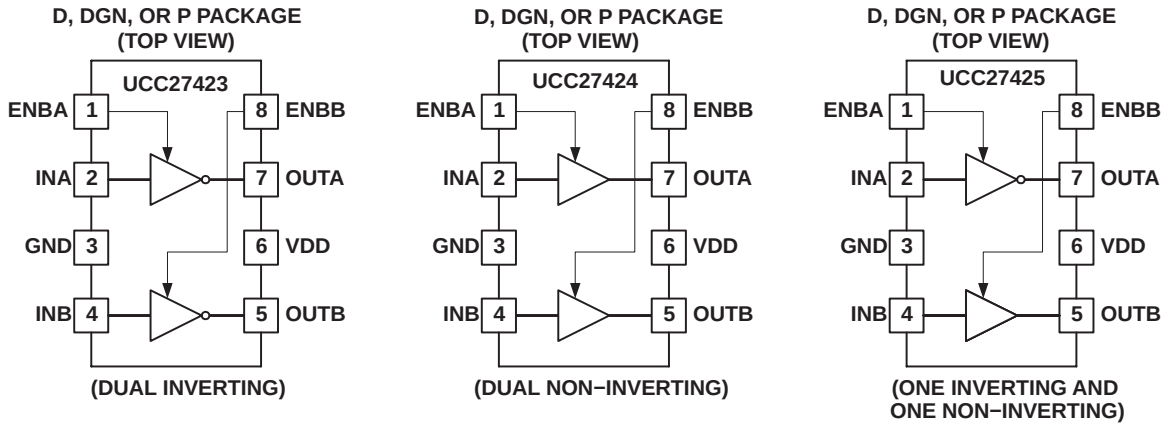
ORDERING INFORMATION

OUTPUT CONFIGURATION	TEMPERATURE RANGE $T_A = T_J$	PACKAGED DEVICES		
		SOIC-8 (D)	MSOP-8 PowerPAD (DGN)‡	PDIP-8 (P)
Dual inverting	−40°C to +105°C	UCC27423D	UCC27423DGN	UCC27423P
Dual nonInverting	−40°C to +105°C	UCC27424D	UCC27424DGN	UCC27424P
One inverting, one noninverting	−40°C to +105°C	UCC27425D	UCC27425DGN	UCC27425P

† D (SOIC−8) and DGN (PowerPAD−MSOP) packages are available taped and reeled. Add R suffix to device type (e.g. UCC27423DR, UCC27424DGNR) to order quantities of 2,500 devices per reel for D or 1,000 devices per reel for DGN package.

‡ The PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device.



power dissipation rating table

PACKAGE	SUFFIX	Θjc (°C/W)	Θja (°C/W)	Power Rating (mW) T_A = 70°C See Note 1	Derating Factor Above 70°C (mW/°C) See Note 1
SOIC-8	D	42	84 – 160‡	344−655 See Note 2	6.25 − 11.9 See Note 2
PDIP-8	P	49	110	500	9
MSOP PowerPAD-8 See Note 3	DGN	4.7	50 − 59‡	1370	17.1

Notes: 1. 125°C operating junction temperature is used for power rating calculations

2. The range of values indicates the effect of pc−board. These values are intended to give the system designer an indication of the best and worst case conditions. In general, the system designer should attempt to use larger traces on the pc−board where possible in order to spread the heat away form the device more effectively. For information on the PowerPAD™ package, refer to Technical Brief, *PowerPad Thermally Enhanced Package*, Texas Instrument s Literature No. SLMA002 and Application Brief, *PowerPad Made Easy*, Texas Instruments Literature No. SLMA004.
3. The PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device.

Table 1. Input/Output Table

		INPUTS (VIN_L, VIN_H)		UCC27423		UCC27424		UCC27425	
ENBA	ENBB	INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
H	H	L	L	H	H	L	L	H	L
H	H	L	H	H	L	L	H	H	H
H	H	H	L	L	H	H	L	L	L
H	H	H	H	L	L	H	H	L	H
L	L	X	X	L	L	L	L	L	L

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

Supply voltage, V_{DD} . . . . . −0.3 V to 16 V
Output current (OUTA, OUTB) DC, I_{OUT_DC} . . . . . 0.3 A
Pulsed, (0.5 µs), I_{OUT_PULSED} . . . . . 4.5 A
Input voltage (INA, INB), V_{IN} . . . . . −5 V to 6 V or V_{DD}+0.3 (whichever is larger)
Enable voltage (ENBA, ENBB) . . . . . −0.3 V to 6 V or V_{DD}+0.3 (whichever is larger)
Power dissipation at T_A = 25°C (DGN package) . . . . . 3 W
(D package) . . . . . 650 mW
(P package) . . . . . 350 mW
Junction operating temperature, T_J . . . . . −55°C to 150°C
Storage temperature, T_{stg} . . . . . −65°C to 150°C
Lead temperature (soldering, 10 sec.), ... 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 V to 15 V, TA = −40°C to 105°C, $T_A = T_J$, (unless otherwise noted)

PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNITS
Input (INA, INB)							
V_{IN_H}, logic 1 input threshold				2			V
V_{IN_L}, logic 0 input threshold						1	V
Input current	0 V <= V_{IN} <= V_{DD}			−10	0	10	µA
Output (OUTA, OUTB)							
Output current	V_{DD} = 14 V,	See Note 1,	See Note 2		4		A
V_{OH}, high-level output voltage	V_{OH} = V_{DD} – V_{OUT},		I_{OUT} = −10 mA		330	450	mV
V_{OL}, low-level output level	I_{OUT} = 10 mA				22	40	mV
Output resistance high	T_A = 25°C, See Note 3	I_{OUT} = −10 mA,	V_{DD} = 14 V,	25	30	35	Ω
	T_A = full range, See Note 3	I_{OUT} = −10 mA,	V_{DD} = 14 V,	18		45	Ω
Output resistance low	T_A = 25°C, See Note 3	I_{OUT} = 10 mA,	V_{DD} = 14 V,	1.9	2.2	2.5	Ω
	T_A = full range See Note 3	I_{OUT} = 10 mA,	V_{DD} = 14 V,	1.2		4.0	Ω
Latch-up protection	See Note 1			500			mA

NOTES: 1. Ensured by design. Not tested in production.
2. The pullup / pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The pulsed output current rating is the combined current from the bipolar and MOSFET transistors.
3. The pullup / pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 V to 15 V, TA = −40°C to 105°C, $T_A = T_J$, (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Switching Time						
t_R, rise time (OUTA, OUTB)		C_{LOAD} = 1.8 nF,(1)		20	40	ns
t_F, fall time (OUTA, OUTB)		C_{LOAD} = 1.8 nF,(1)		15	40	
t_{D1}, delay, IN rising (IN to OUT)		C_{LOAD} = 1.8 nF,(1)		25	40	
t_{D2}, delay, IN falling (IN to OUT)		C_{LOAD} = 1.8 nF,(1)		35	50	
Enable (ENBA, ENBB)						
V_{IN_H}, high-level input voltage		LO to HI transition	1.7	2.4	2.9	V
V_{IN_L}, low-level input voltage		HI to LO transition	1.1	1.8	2.2	V
Hysteresis			0.15	0.55	0.90	
R_{ENBL}, enable impedance		V_{DD} = 14 V, ENBL = GND	75	100	140	kΩ
t_{D3}, propagation delay time(4)		C_{LOAD} = 1.8 nF(1)		30	60	ns
t_{D4}, propagation delay time(4)		C_{LOAD} = 1.8 nF(1)		100	150	
Overall						
I_{DD}, static operating current, V_{DD} = 15 V, ENBA = ENBB = 15 V	UCC27423	INA = 0 V, INB = 0 V		900	1350	µA
		INA = 0 V, INB = HIGH		750	1100	
		INA = HIGH, INB = 0 V		750	1100	
		INA = HIGH, INB = HIGH		600	900	
	UCC27424	INA = 0 V, INB = 0 V		300	450	
		INA = 0 V, INB = HIGH		750	1100	
		INA = HIGH, INB = 0 V		750	1100	
		INA = HIGH, INB = HIGH		1200	1800	
	UCC27425	INA = 0 V, INB = 0 V		600	900	
		INA = 0 V, INB = HIGH		1050	1600	
		INA = HIGH, INB = 0 V		450	700	
		INA = HIGH, INB = HIGH		900	1350	
I_{DD}, disabled, V_{DD} = 15 V, ENBA = ENBB = 0 V	All	INA = 0 V, INB = 0 V		300	450	
		INA = 0 V, INB = HIGH		450	700	
		INA = HIGH, INB = 0 V		450	700	
		INA = HIGH, INB = HIGH		600	900	

NOTES: 1. Ensured by design. Not production.
2. The pullup / pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors.
3. The pullup / pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.
4. See Figure 2.

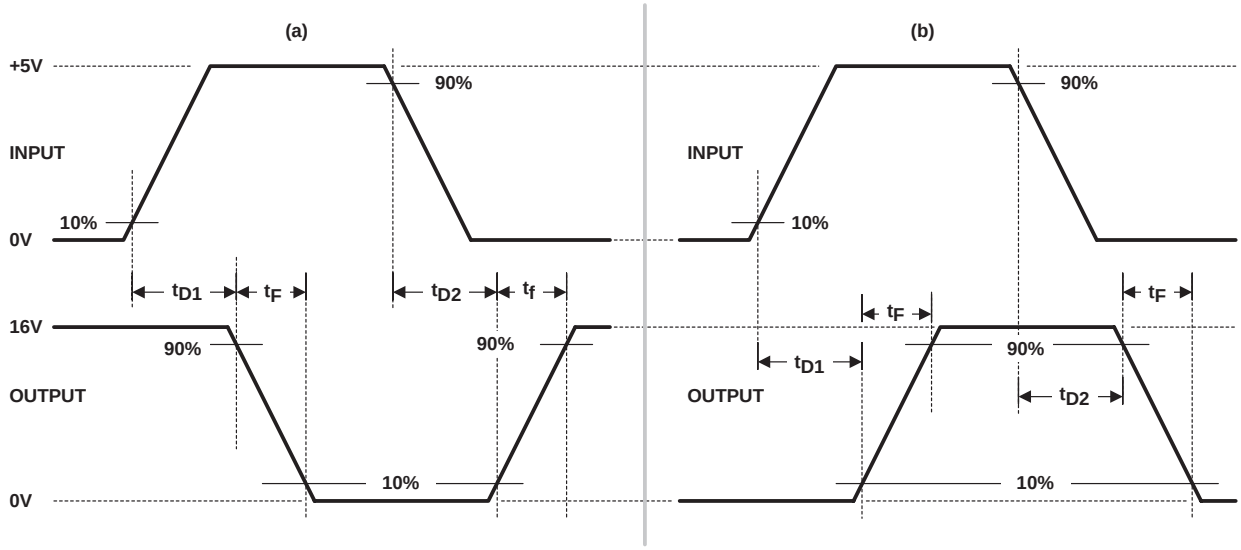


Figure 1. Switching Waveforms for (a) Inverting Driver and (b) Noninverting Driver

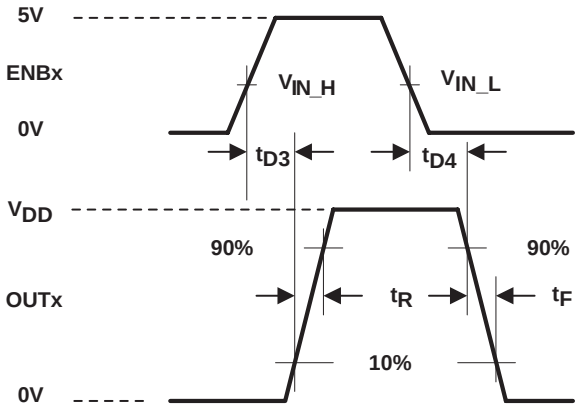


Figure 2. Switching Waveform for Enable to Output

NOTE:

The 10% and 90% thresholds depict the dynamics of the BiPolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Terminal Functions

TERMINAL			FUNCTION
NO.	NAME	I/O	
1	ENBA	I	Enable input for the driver A with logic compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to V_{DD} with 100-kΩ resistor for active high operation. The output state when the device is disabled will be low regardless of the input state.
2	INA	I	Input A. Input signal of the A driver which has logic compatible threshold and hysteresis. If not used, this input should be tied to either VDD or GND. It should not be left floating.
3	GND	−	Common ground. This ground should be connected very closely to the source of the power MOSFET which the driver is driving.
4	INB	I	Input B. Input signal of the A driver which has logic compatible threshold and hysteresis. If not used, this input should be tied to either VDD or GND. It should not be left floating.
5	OUTB	O	Driver output B. The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
6	VDD	I	Supply. Supply voltage and the power input connection for this device.
7	OUTA	O	Driver output A. The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
8	ENBB	I	Enable input for the driver B with logic compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to V_{DD} with 100-kΩ resistor for active high operation. The output state when the device is disabled will be low regardless of the input state.

APPLICATION INFORMATION

General Information

High frequency power supplies often require high-speed, high-current drivers such as the UCC27423/4/5 family. A leading application is the need to provide a high power buffer stage between the PWM output of the control IC and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the driver IC is utilized to drive the power device gates through a drive transformer. Synchronous rectification supplies also have the need to simultaneously drive multiple devices which can present an extremely large load to the control circuitry.

Driver ICs are utilized when it is not feasible to have the primary PWM regulator IC directly drive the switching devices for one or more reasons. The PWM IC may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases there may be a desire to minimize the effect of high frequency switching noise by placing the high current driver physically close to the load. Also, newer ICs that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high impedance input to a driver such as the UCC27423/4/5. Finally, the control IC may be under thermal stress due to power dissipation, and an external driver can help by moving the heat from the controller to an external package.

APPLICATION INFORMATION

Input Stage

The input thresholds have a 3.3-V logic sensitivity over the full range of V_{DD} voltages; yet it is equally compatible with 0 to V_{DD} signals. The inputs of UCC27423/4/5 family of drivers are designed to withstand 500-mA reverse current without either damage to the IC for logic upset. The input stage of each driver should be driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The input stages to the drivers function as a digital gate, and they are not intended for applications where a slow changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limiting the rise or fall times to the power device is desired, limit the rise or fall times to the power device, then an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor may also help remove power dissipation from the devoce package, as discussed in the section on Thermal Considerations.

Output Stage

Inverting outputs of the UCC27423 and OUTA of the UCC27425 are intended to drive external P-channel MOSFETs. Noninverting outputs of the UCC27424 and OUTB of the UCC27425 are intended to drive external N-channel MOSFETs.

Each output stage is capable of supplying ±4-A peak current pulses and swings to both VDD and GND. The pullup/ pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the external MOSFET. This means that in many cases, external-schottky-clamp diodes are not required.

The UCC27423 family delivers 4-A of gate drive where it is most needed during the MOSFET switching transition – at the Miller plateau region – providing improved efficiency gains. A unique BiPolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing at low supply voltages.

APPLICATION INFORMATION

Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC27423/4/5 drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver device. [1]

Two circuits are used to test the current capabilities of the UCC27423 driver. In each case external circuitry is added to clamp the output near 5 V while the IC is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test there is a transient period where the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient.

The first circuit in Figure 2 is used to verify the current sink capability when the output of the driver is clamped around 5 V, a typical value of gate-source voltage during the Miller plateau region. The UCC27423 is found to sink 4.5 A at V_{DD} = 15 V and 4.28 A at V_{DD} = 12 V.

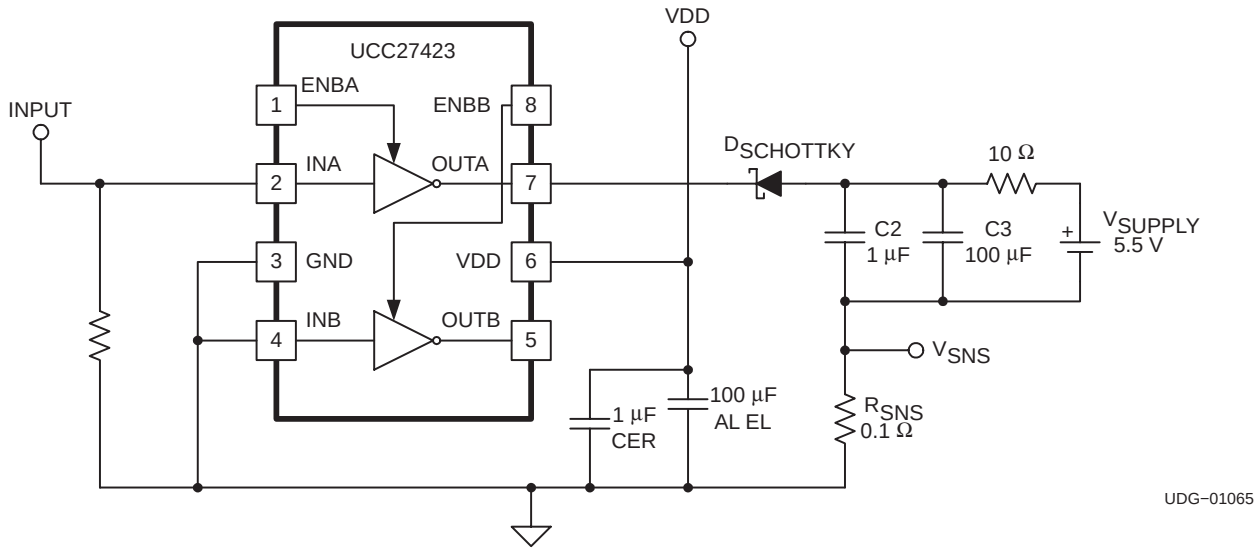


Figure 3.

APPLICATION INFORMATION

The circuit shown in Figure 3 is used to test the current source capability with the output clamped to around 5 V with a string of Zener diodes. The UCC27423 is found to source 4.8 A at V_{DD} = 15 V and 3.7 A at V_{DD} = 12 V.

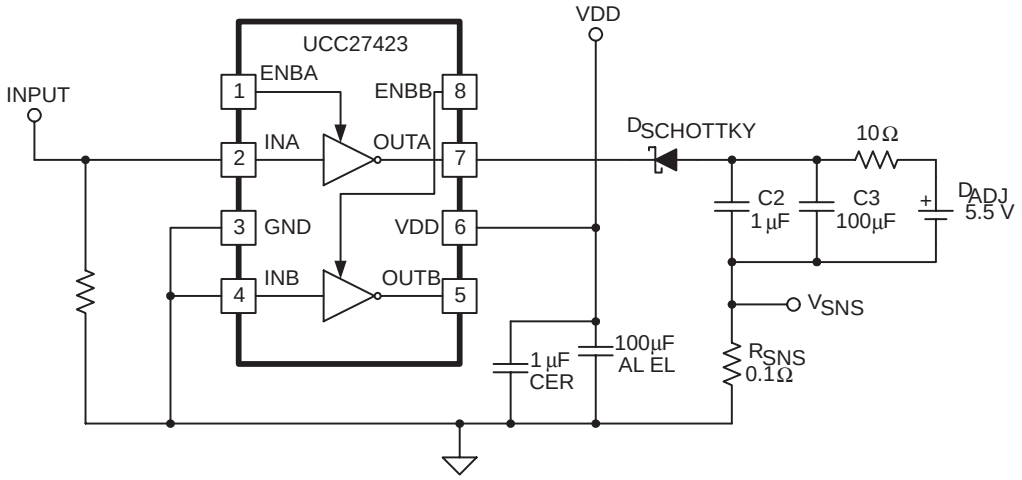


Figure 4.

It should be noted that the current sink capability is slightly stronger than the current source capability at lower VDD. This is due to the differences in the structure of the bipolar-MOSFET power output section, where the current source is a P-channel MOSFET and the current sink has an N-channel MOSFET.

In a large majority of applications it is advantageous that the turn-off capability of a driver is stronger than the turn-on capability. This helps to ensure that the MOSFET is held OFF during common power supply transients which may turn the device back ON.

Parallel Outputs

The A and B drivers may be combined into a single driver by connecting the INA/INB inputs together and the OUTA/OUTB outputs together. Then, a single signal can control the paralleled combination as shown in Figure 4.

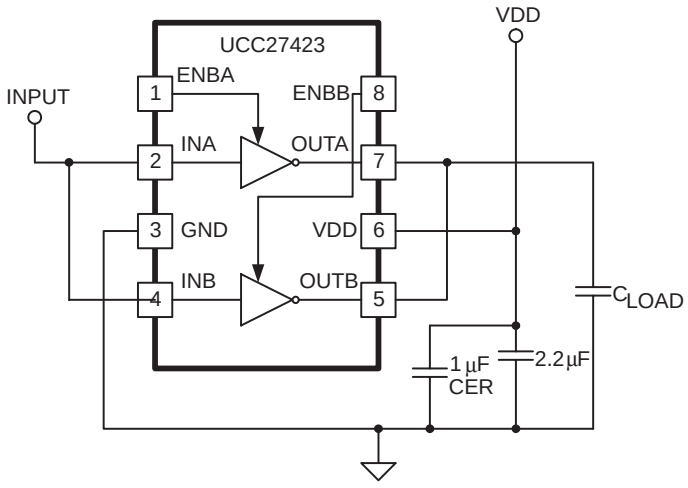


Figure 5.

APPLICATION INFORMATION

Operational Waveforms and Circuit Layout

Figure 5 shows the circuit performance achievable with a single driver (1/2 of the 8-pin IC) driving a 10-nF load. The input pulsewidth (not shown) is set to 300 ns to show both transitions in the output waveform. Note the linear rise and fall edges of the switching waveforms. This is due to the constant output current characteristic of the driver as opposed to the resistive output impedance of traditional MOSFET-based gate drivers.

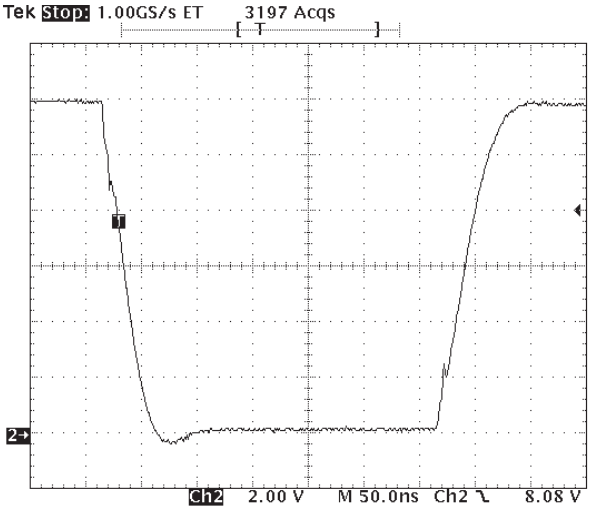


Figure 6.

In a power driver operating at high frequency, it is a significant challenge to get clean waveforms without much overshoot/undershoot and ringing. The low output impedance of these drivers produces waveforms with high di/dt. This tends to induce ringing in the parasitic inductances. Utmost care must be used in the circuit layout. It is advantageous to connect the driver IC as close as possible to the leads. The driver IC layout has ground on the opposite side of the output, so the ground should be connected to the bypass capacitors and the load with copper trace as wide as possible. These connections should also be made with a small enclosed loop area to minimize the inductance.

VDD

Although quiescent VDD current is very low, total supply current will be higher, depending on OUTA and OUTB current and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from:

I_{OUT} = Qg x f, where f is frequency

For the best high-speed circuit performance, two V_{DD} bypass capacitors are recommended tp prevent noise problems. The use of surface mount components is highly recommended. A 0.1-µF ceramic capacitor should be located closest to the VDD to ground connection. In addition, a larger capacitor (such as 1-µF) with relatively low ESR should be connected in parallel, to help deliver the high current peaks to the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels in the driver application.

APPLICATION INFORMATION

Drive Current and Power Requirements

The UCC27423/4/5 family of drivers are capable of delivering 4-A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. A MOSFET is used in this discussion because it is the most common type of switching device used in high frequency power conversion equipment.

References 1 and 2 discuss the current required to drive a power MOSFET and other capacitive-input switching devices. Reference 2 includes information on the previous generation of bipolar IC gate drivers.

When a driver IC is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$E = \frac{1}{2}CV^2$, where C is the load capacitor and V is the bias voltage feeding the driver.

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by the following:

$P = 2 \times \frac{1}{2}CV^2f$, where f is the switching frequency.

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as:

$P = 10\ nF \times (12)^2 \times (300\ kHz) = 0.432\ W$

With a 12-V supply, this would equate to a current of:

$$I = \frac{P}{V} = \frac{0.432\ W}{12\ V} = 0.036\ A$$

The actual current measured from the supply was 0.037 A, and is very close to the predicted value. But, the I_{DD} current that is due to the IC internal consumption should be considered. With no load the IC current draw is 0.0027 A. Under this condition the output rise and fall times are faster than with a load. This could lead to an almost insignificant, yet measurable current due to cross-conduction in the output stages of the driver. However, these small current differences are buried in the high frequency switching spikes, and are beyond the measurement capabilities of a basic lab setup. The measured current with 10-nF load is reasonably close to that expected.

APPLICATION INFORMATION

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence Qg = CeffV to provide the following equation for power:

$$P = C \times V^2 \times f = Q_g \times f$$

This equation allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

Enable

UCC27423/4/5 provides dual Enable inputs for improved control of each driver channel operation. The inputs incorporate logic compatible thresholds with hysteresis. They are internally pulled up to V_{DD} with 100-kΩ resistor for active high operation. When ENBA and ENBB are driven high, the drivers are enabled and when ENBA and ENBB are low, the drivers are disabled. The default state of the Enable pin is to enable the driver and therefore can be left open for standard operation. The output states when the drivers are disabled is low regardless of the input state. See the truth table of Table 1 for the operation using enable logic.

Enable input are compatible with both logic signals and slow changing analog signals. They can be directly driven or a power−up delay can be programmed with a capacitor between ENBA, ENBB and AGND. ENBA and ENBB control input A and input B respectively.

THERMAL INFORMATION

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the IC package. In order for a power driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC27423/4/5 family of drivers is available in three different packages to cover a range of application requirements.

As shown in the power dissipation rating table, the SOIC-8 (D) and PDIP-8 (P) packages each have a power rating of around 0.5 W with T_A = 70°C. This limit is imposed in conjunction with the power derating factor also given in the table. Note that the power dissipation in our earlier example is 0.432 W with a 10-nF load, 12 VDD, switched at 300 kHz. Thus, only one load of this size could be driven using the D or P package, even if the two onboard drivers are paralleled. The difficulties with heat removal limit the drive available in the older packages.

The MSOP PowerPAD-8 (DGN) package significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As illustrated in Reference 3, the PowerPAD packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board directly underneath the IC package, reducing the Θjc down to 4.7°C/W. Data is presented in Reference 3 to show that the power dissipation can be quadrupled in the PowerPAD configuration when compared to the standard packages. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference 4. This allows a significant improvement in heatsinking over that available in the D or P packages, and is shown to more than double the power capability of the D and P packages. Note that the PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device.

References

1. Power Supply Seminar SEM−1400 Topic 2: *Design And Application Guide For High Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, Texas Instruments Literature No. SLUP133.
2. Application Note, *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits*, by Bill Andreycak, Texas Instruments Literature No. SLUA105
3. Technical Brief, *PowerPad Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002
4. Application Brief, *PowerPAD Made Easy*, Texas Instruments Literature No. SLMA004

Related Products

Product	Description	Packages
UCC37323/4/5	Dual 4-A Low-Side Drivers	MSOP-8 PowerPAD, SOIC-8, PDIP-8
UCC37321/2	Single 9-A Low-Side Driver with Enable	MSOP-8 PowerPAD, SOIC-8, PDIP-8
TPS2811/12/13	Dual 2-A Low-Side Drivers with Internal Regulator	TSSOP-8, SOIC-8, PDIP-8
TPS2814/15	Dual 2-A Low-Side Drivers with Two Inputs per Channel	TSSOP-8, SOIC-8, PDIP-8
TPS2816/17/18/19	Single 2-A Low-Side Driver with Internal Regulator	5-Pin SOT−23
TPS2828/29	Single 2-A Low-Side Driver	5-Pin SOT−23

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY (VDD = 4.5 V)

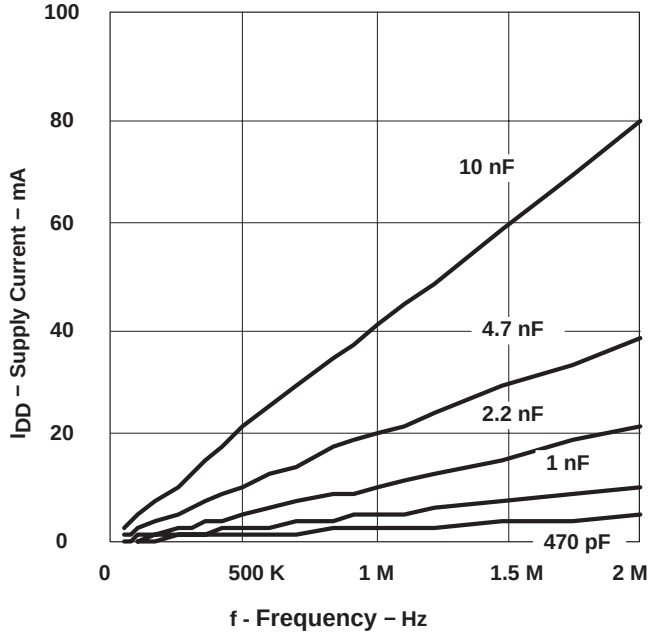


Figure 7

SUPPLY CURRENT vs FREQUENCY (VDD = 8.0 V)

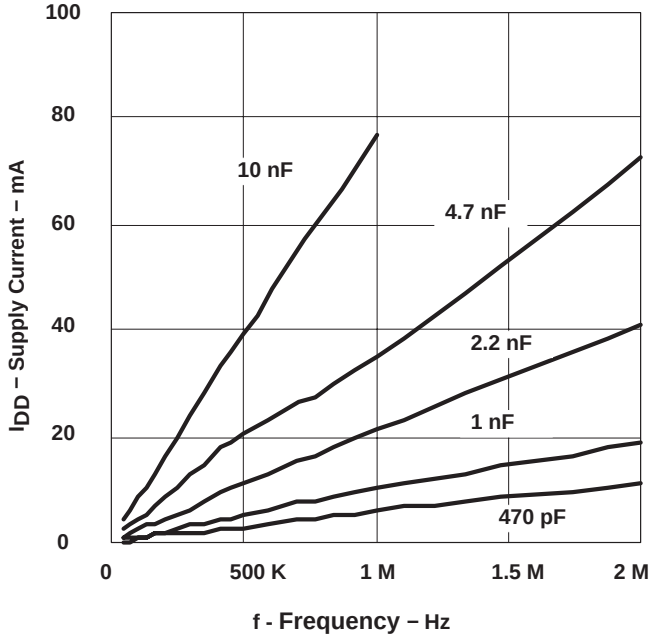


Figure 8

SUPPLY CURRENT vs FREQUENCY (VDD = 12 V)

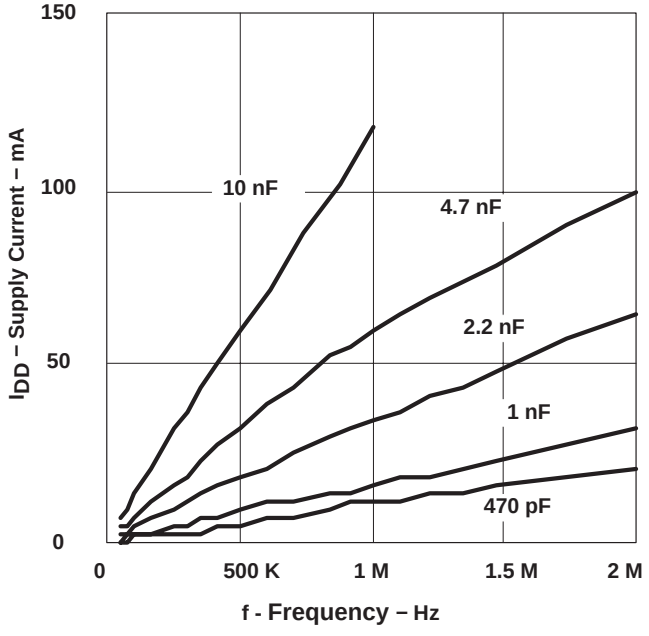


Figure 9

SUPPLY CURRENT vs FREQUENCY (VDD = 15 V)

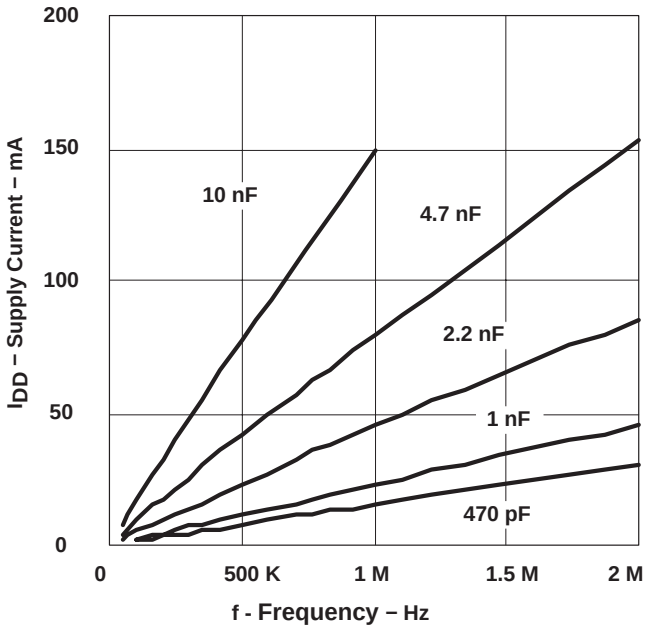


Figure 10

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE (C_{LOAD} = 2.2 nF)

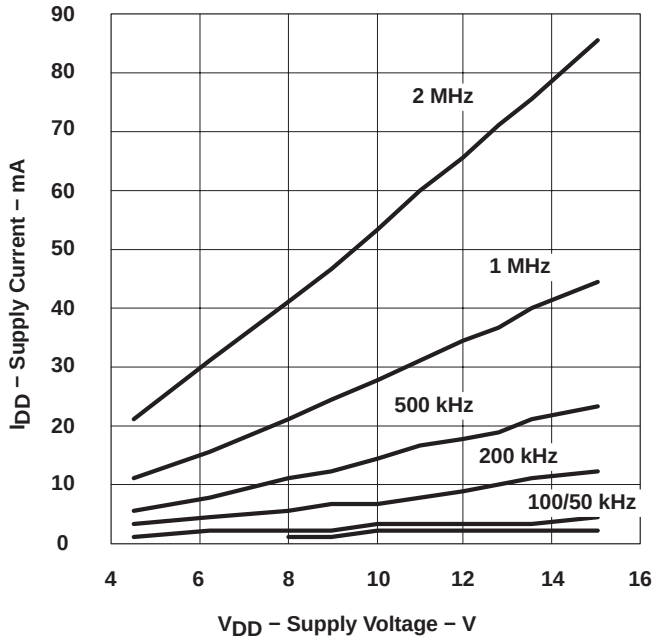


Figure 11

SUPPLY CURRENT vs SUPPLY VOLTAGE (C_{LOAD} = 4.7 nF)

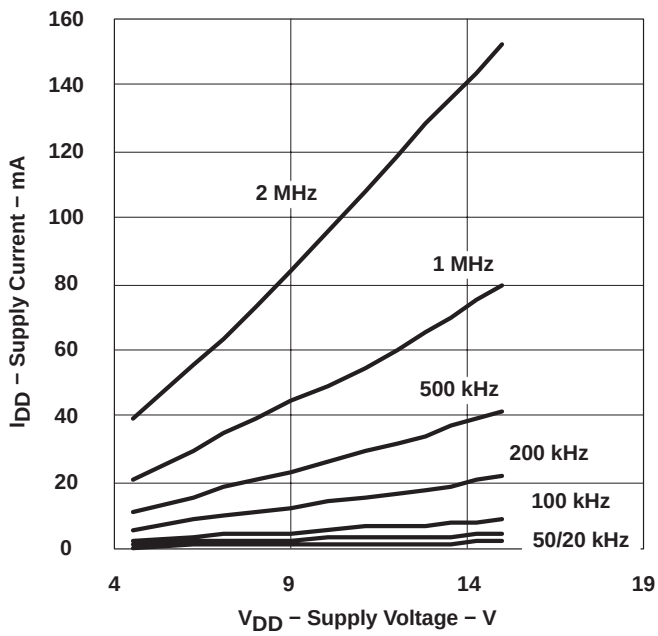


Figure 12

SUPPLY CURRENT vs SUPPLY VOLTAGE (UCC27423)

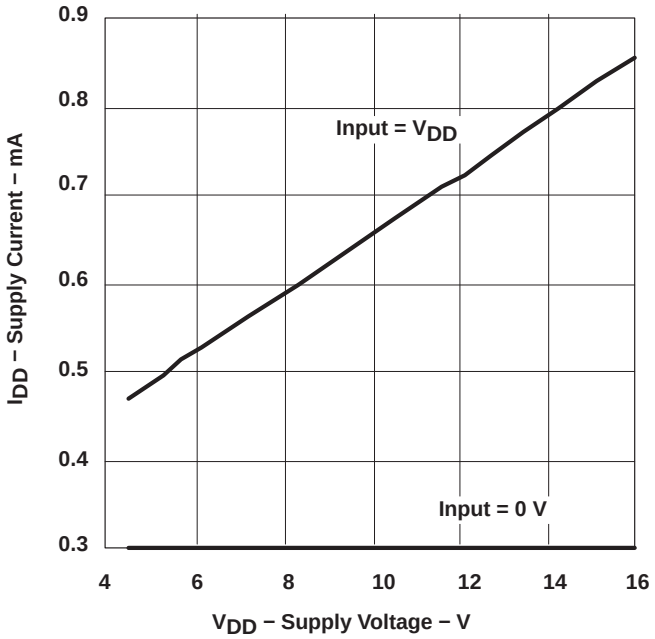


Figure 13

SUPPLY CURRENT vs SUPPLY VOLTAGE (UCC27424)

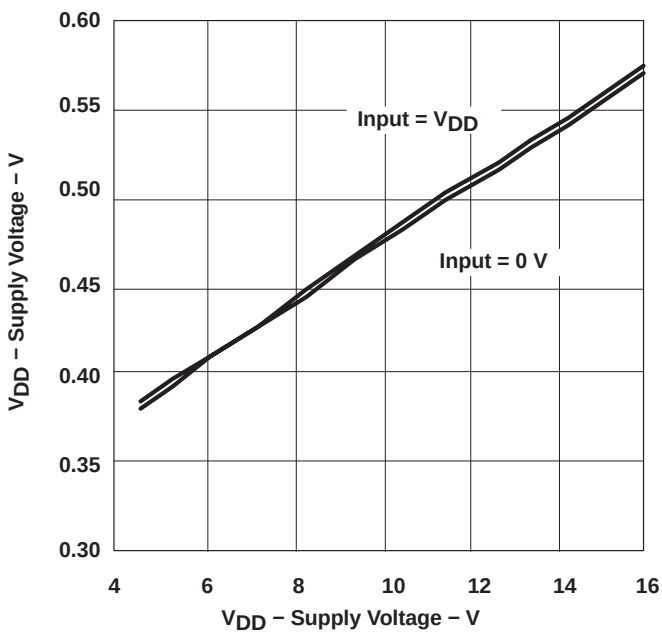


Figure 14

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE (UCC27425)

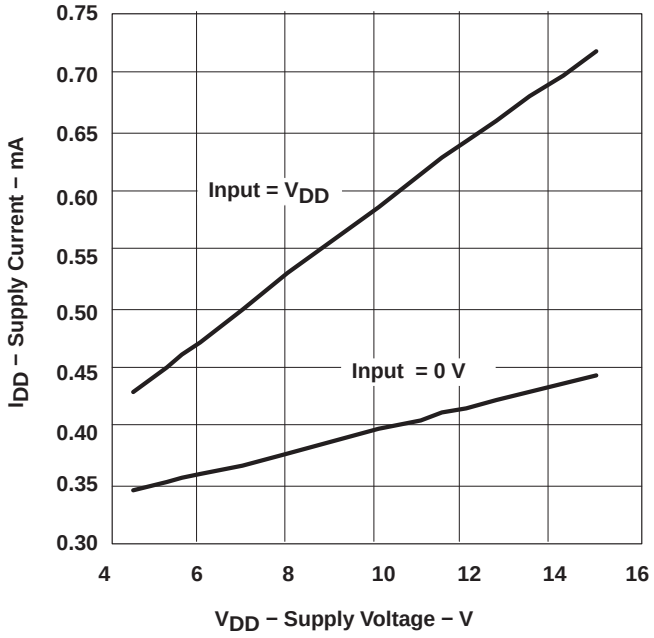


Figure 15

RISE TIME/FALL TIME vs TEMPERATURE (UCC27423)

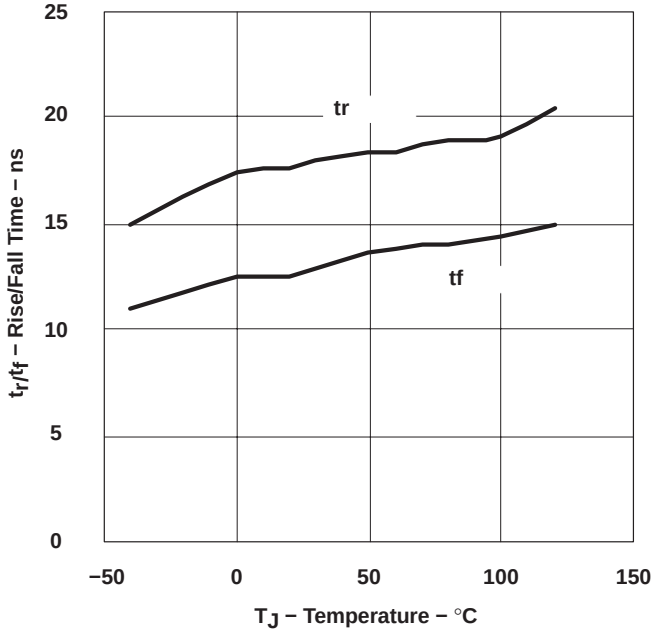


Figure 16

RISE TIME vs SUPPLY VOLTAGE

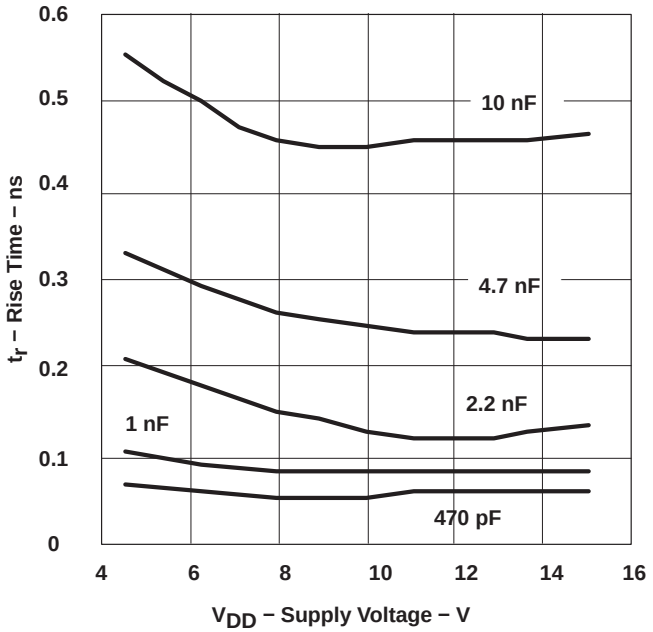


Figure 17

FALL TIME vs SUPPLY VOLTAGE

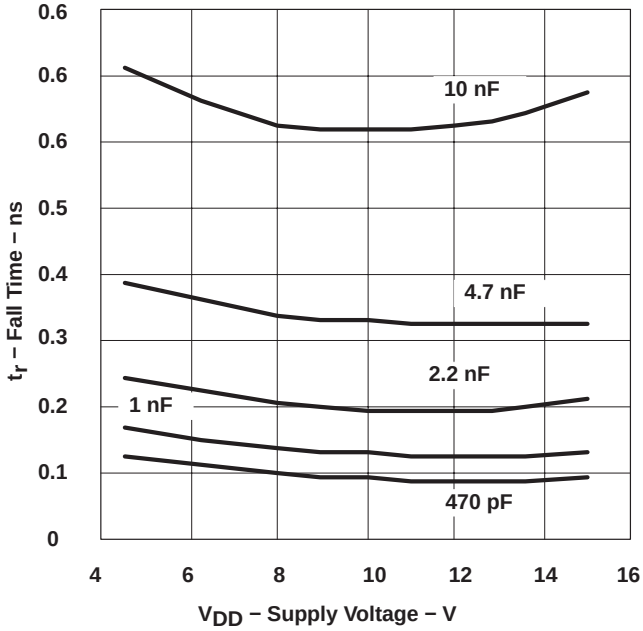


Figure 18

TYPICAL CHARACTERISTICS

DELAY TIME (t_D1)
vs
SUPPLY VOLTAGE (UCC27423)

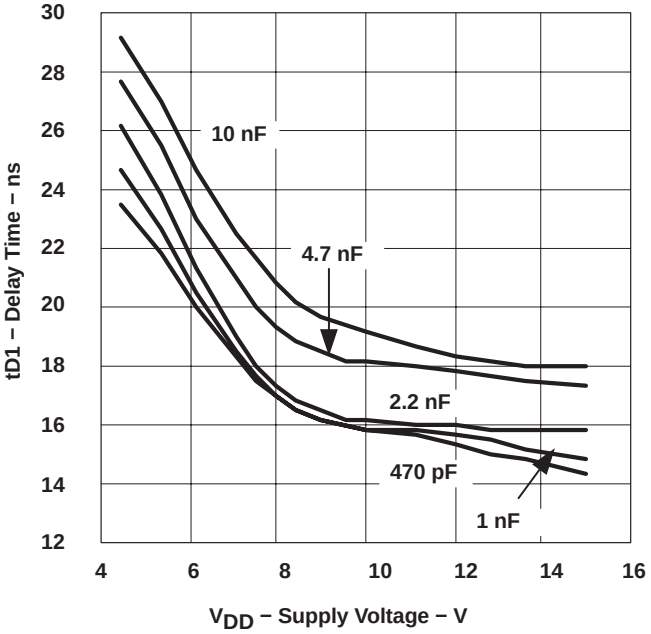


Figure 19

DELAY TIME (t_D2)
vs
SUPPLY VOLTAGE (UCC27423)

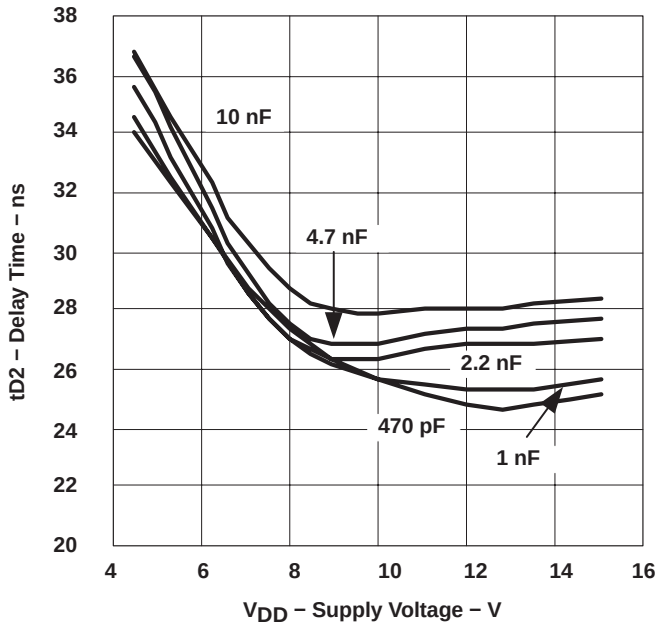


Figure 20

ENABLE THRESHOLD AND HYSTERESIS
vs
TEMPERATURE

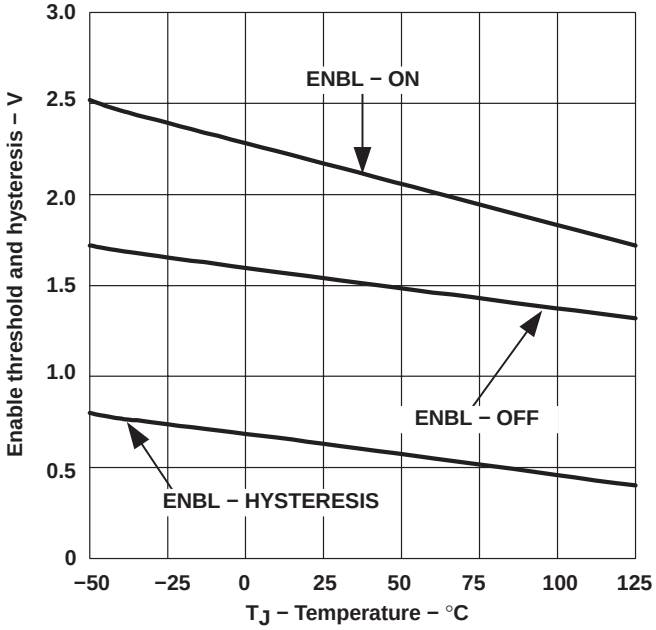


Figure 21

ENABLE RESISTANCE
vs
TEMPERATURE

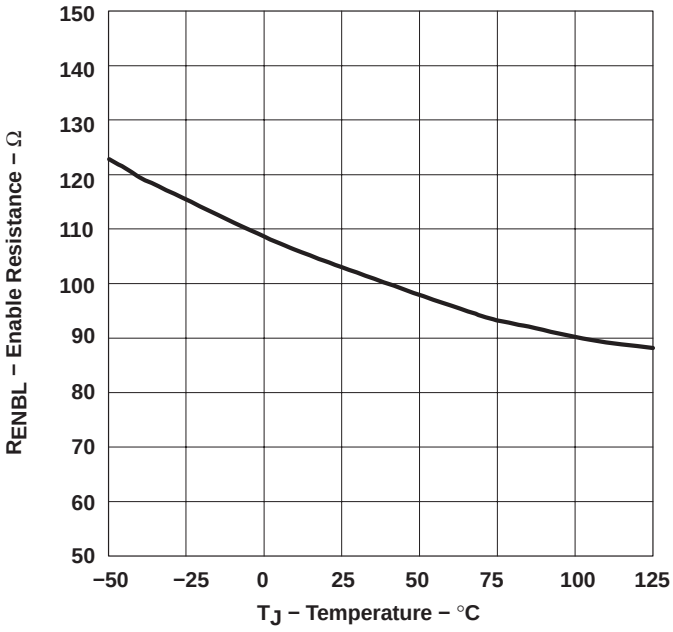


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT BEHAVIOR vs SUPPLY VOLTAGE (INVERTING)

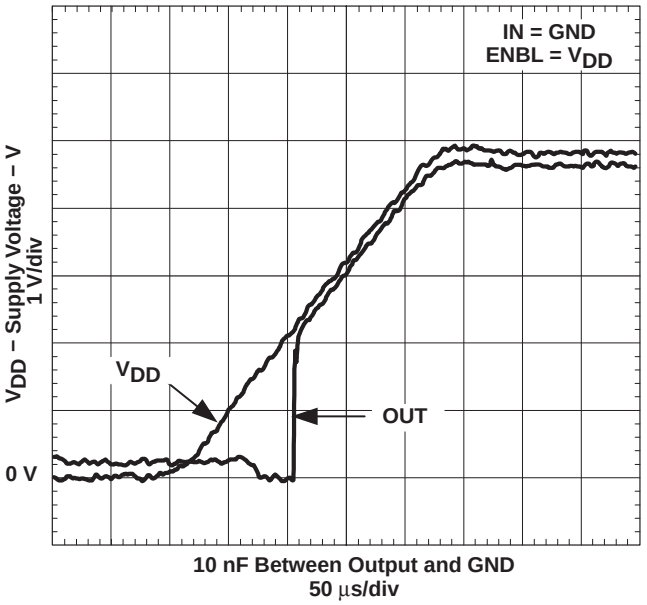


Figure 23

OUTPUT BEHAVIOR vs SUPPLY VOLTAGE (INVERTING)

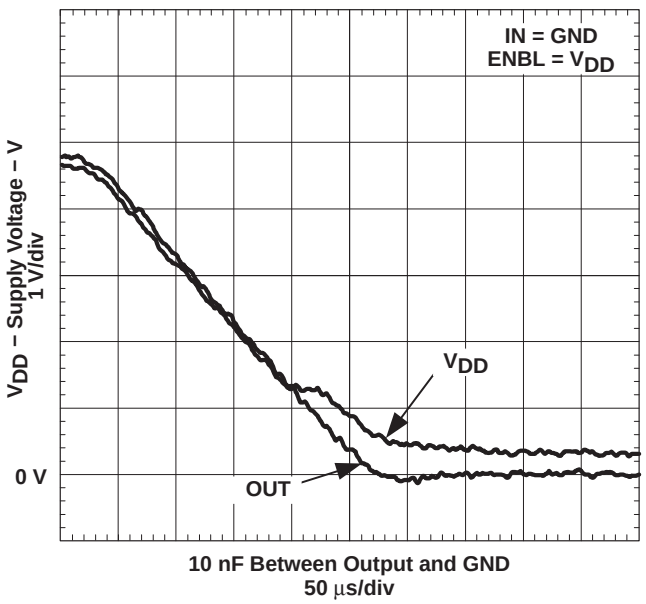


Figure 24

OUTPUT BEHAVIOR vs VDD (INVERTING)

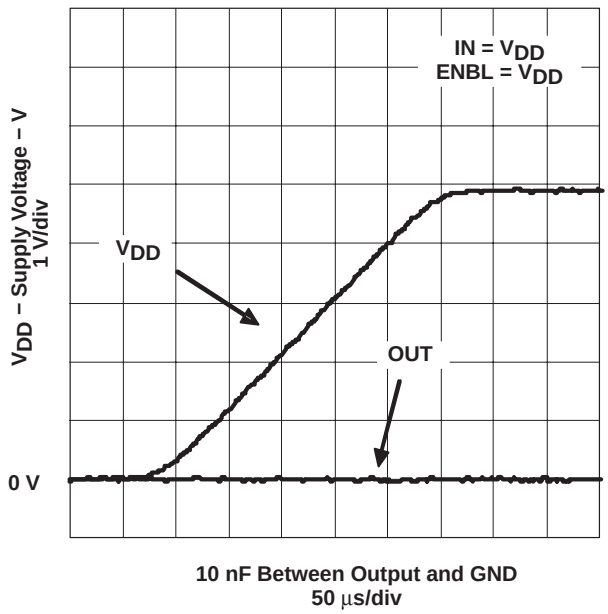


Figure 25

OUTPUT BEHAVIOR vs VDD (INVERTING)

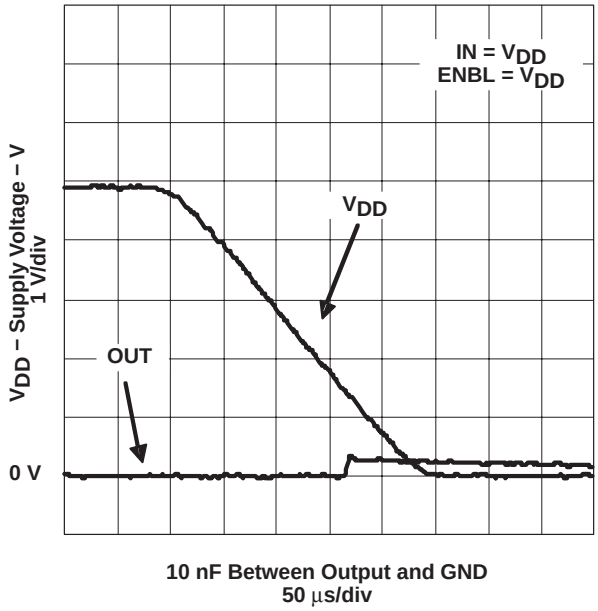


Figure 26

TYPICAL CHARACTERISTICS

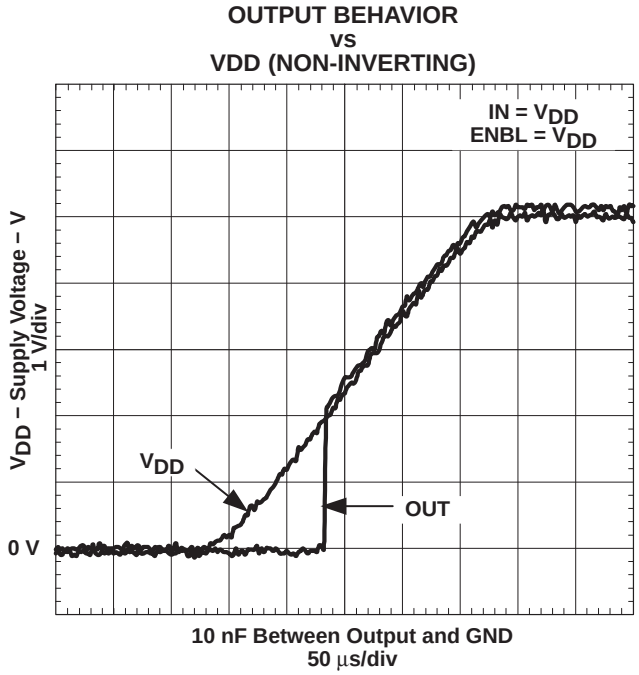


Figure 27

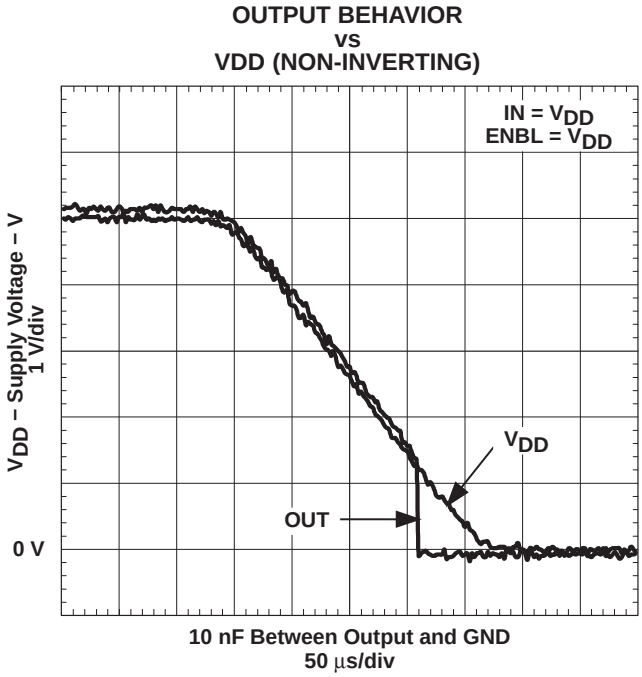


Figure 28

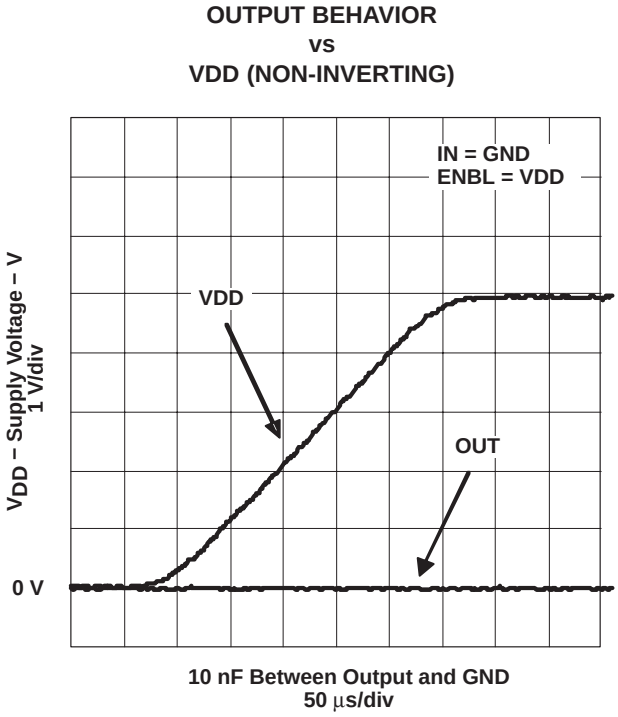


Figure 29

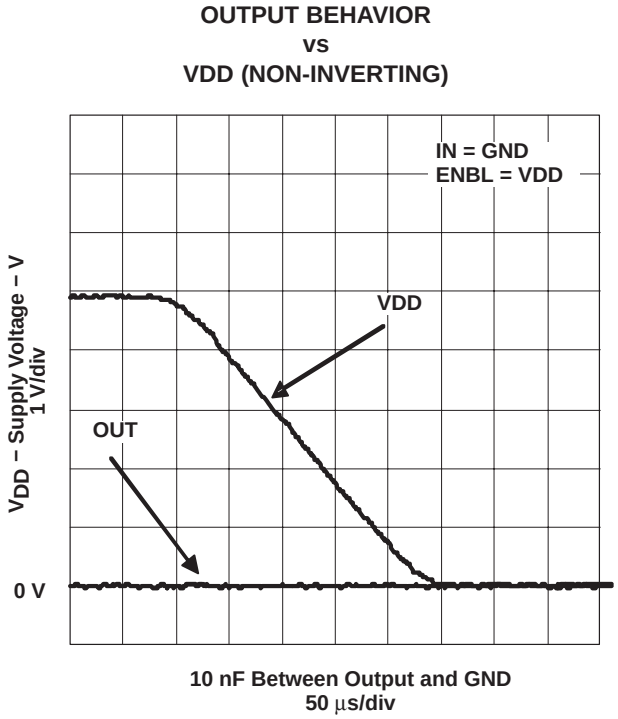


Figure 30

TYPICAL CHARACTERISTICS

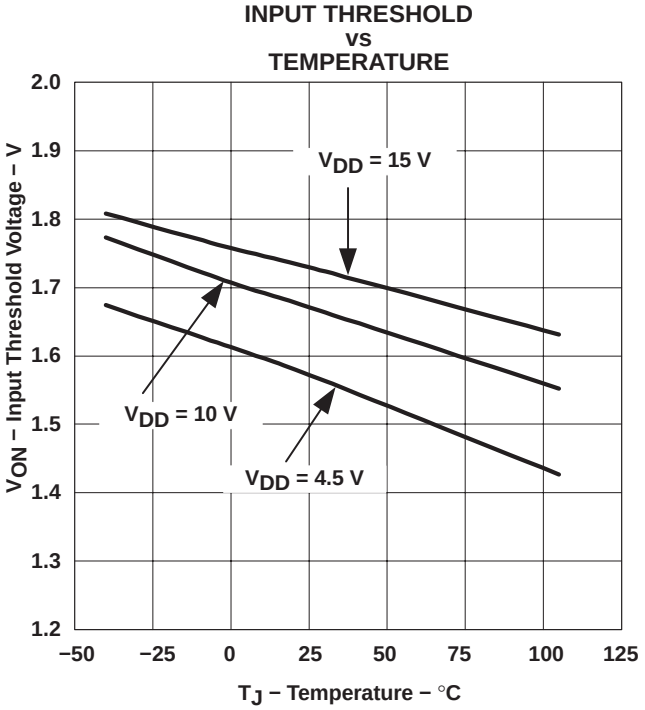
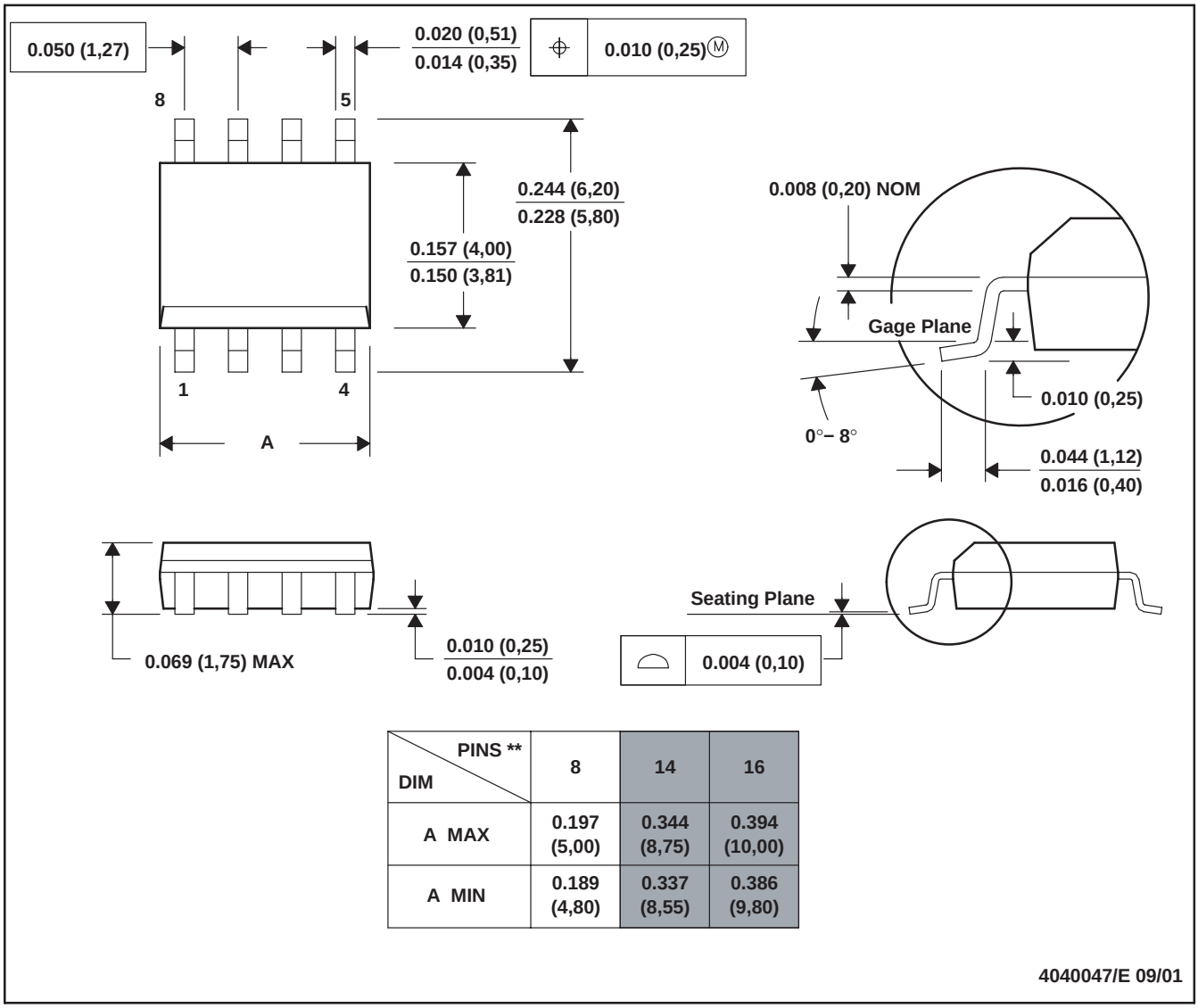


Figure 31

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN



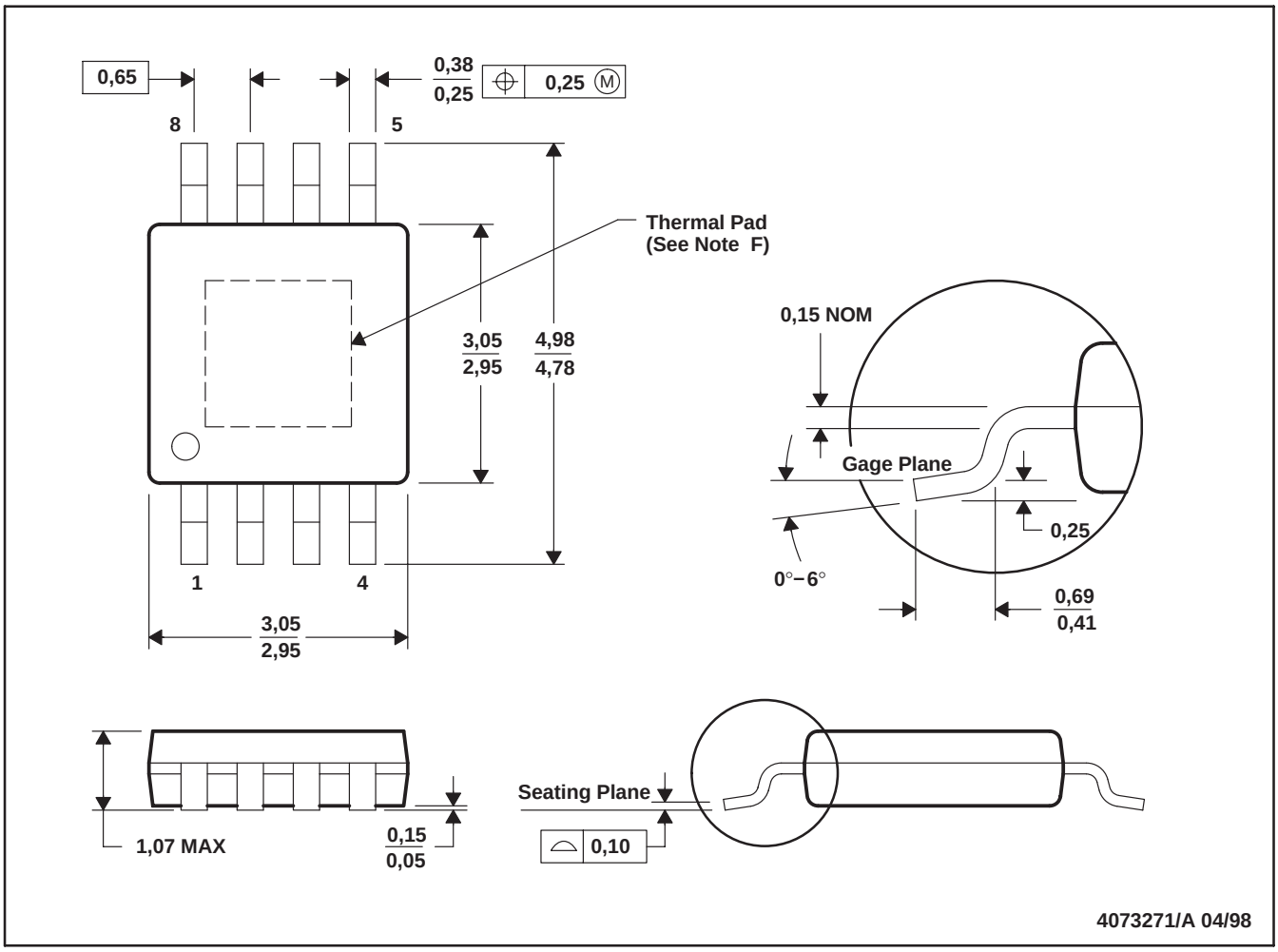
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

DGN (MSOP) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

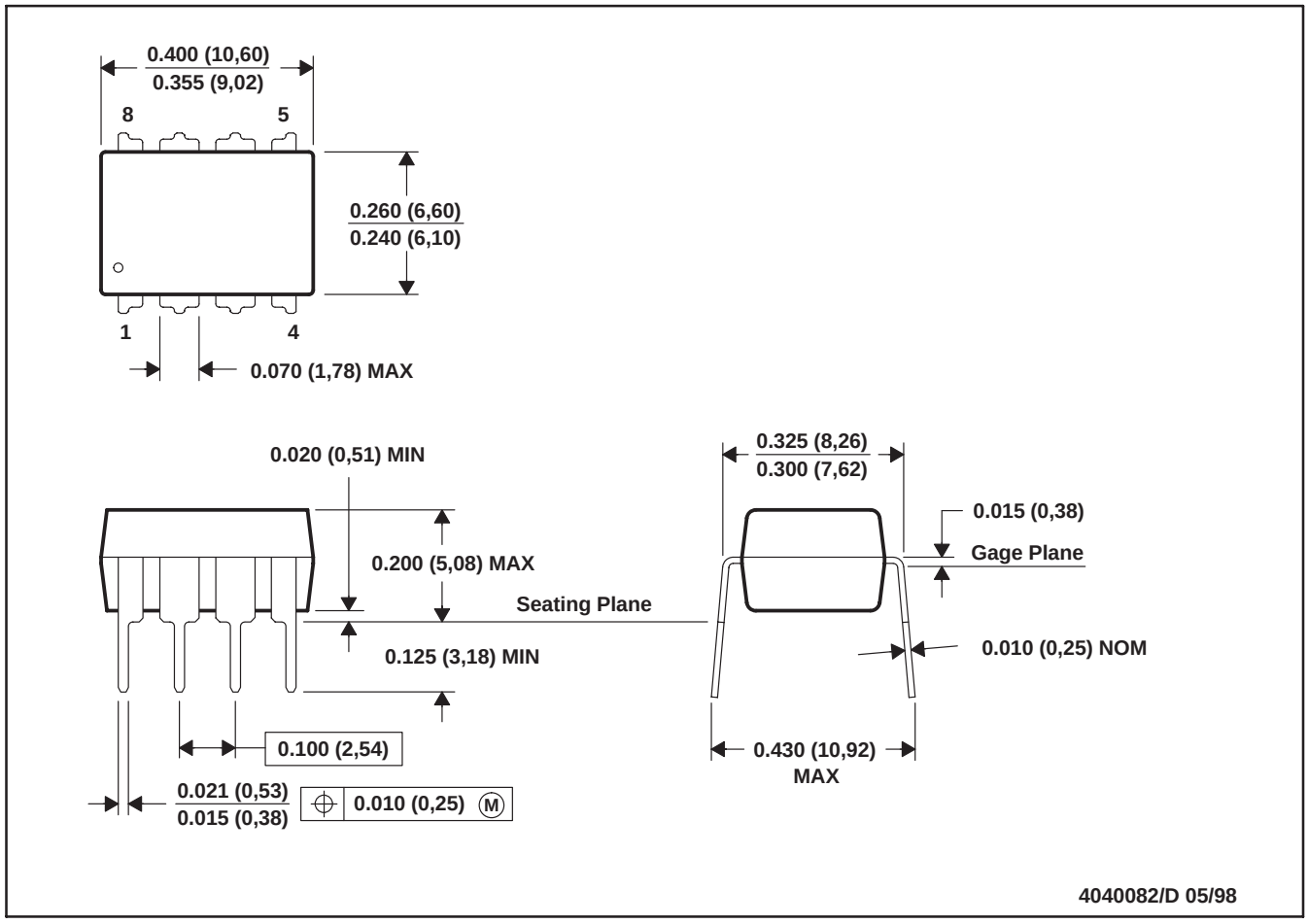


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. Falls within JEDEC MO-187
E. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad.
F. The PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device. The exposed pad dimension is 1.3 mm x 1.7 mm. However, the tolerances can be +1.05/−0.05 mm (+ 41 / −2 mils) due to position and mold flow variation.
G. For additional information on the PowerPAD™ package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPad Thermally Enhanced Package*, Texas Instrument s Literature No. SLMA002 and Application Brief, *PowerPad Made Easy*, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

PowerPAD™ is a trademark of Texas Instruments Incorporated.

MECHANICAL DATA

P (PDIP) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC27423D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27423DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27423DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27423DGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27423DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27423DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27423DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27423DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27423P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
UCC27423PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
UCC27424D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27424DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27424DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27424DGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27424DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27424DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27424DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27424DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27424P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
UCC27424PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
UCC27425D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27425DG4	ACTIVE	SOIC	D	8	75	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
						no Sb/Br)		
UCC27425DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27425DGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27425DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27425DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27425DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27425DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC27425P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
UCC27425PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

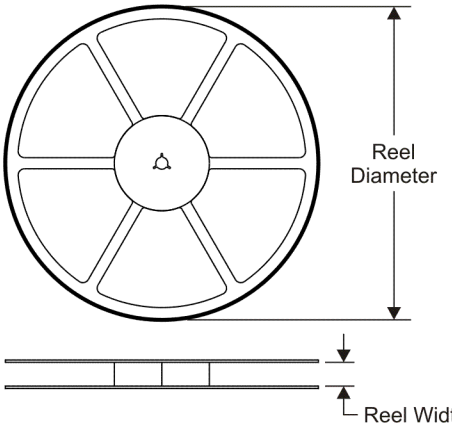
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

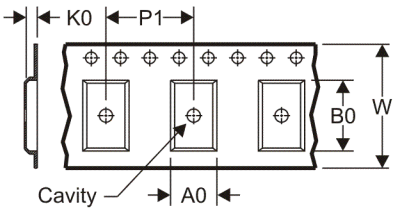
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

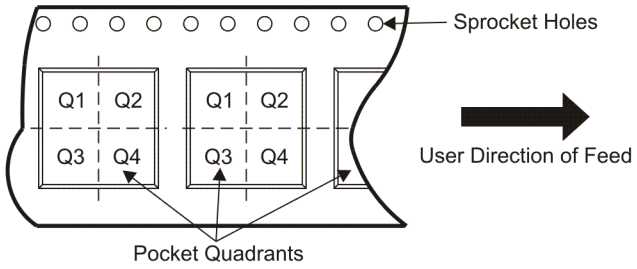


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

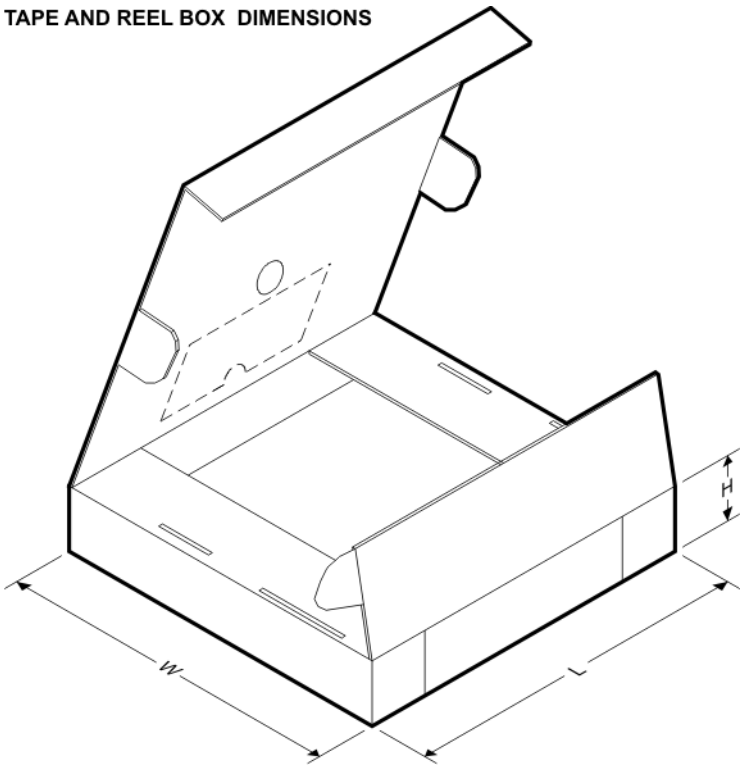
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27423DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27423DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27424DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27424DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27425DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27425DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

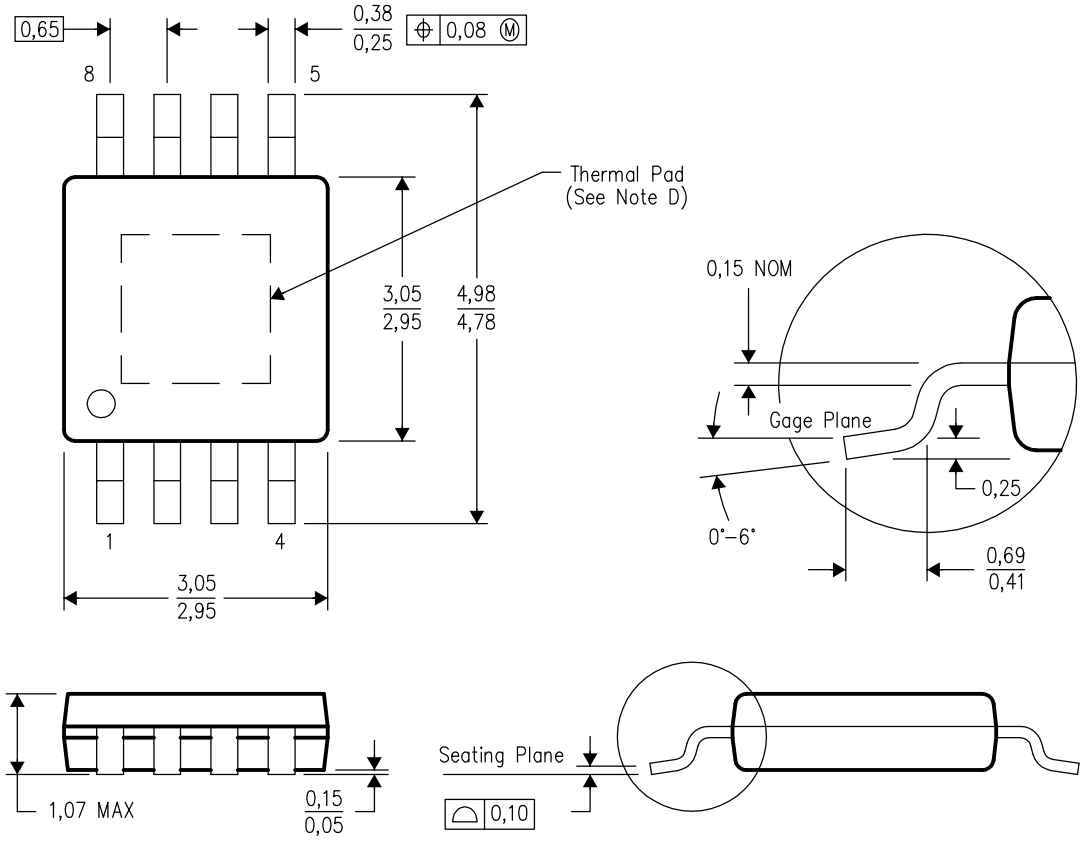
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27423DGNR	MSOP-PowerPAD	DGN	8	2500	346.0	346.0	29.0
UCC27423DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC27424DGNR	MSOP-PowerPAD	DGN	8	2500	346.0	346.0	29.0
UCC27424DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC27425DGNR	MSOP-PowerPAD	DGN	8	2500	346.0	346.0	29.0
UCC27425DR	SOIC	D	8	2500	340.5	338.1	20.6

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–187

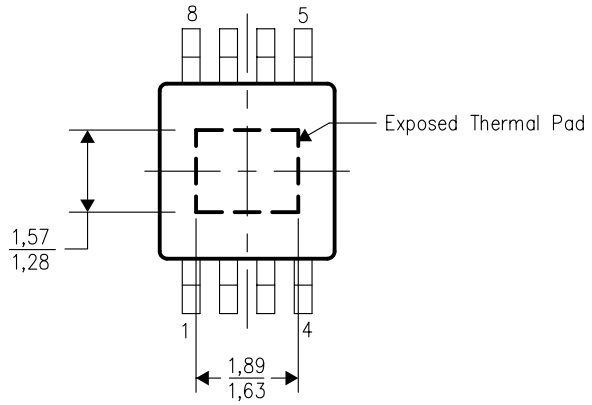
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

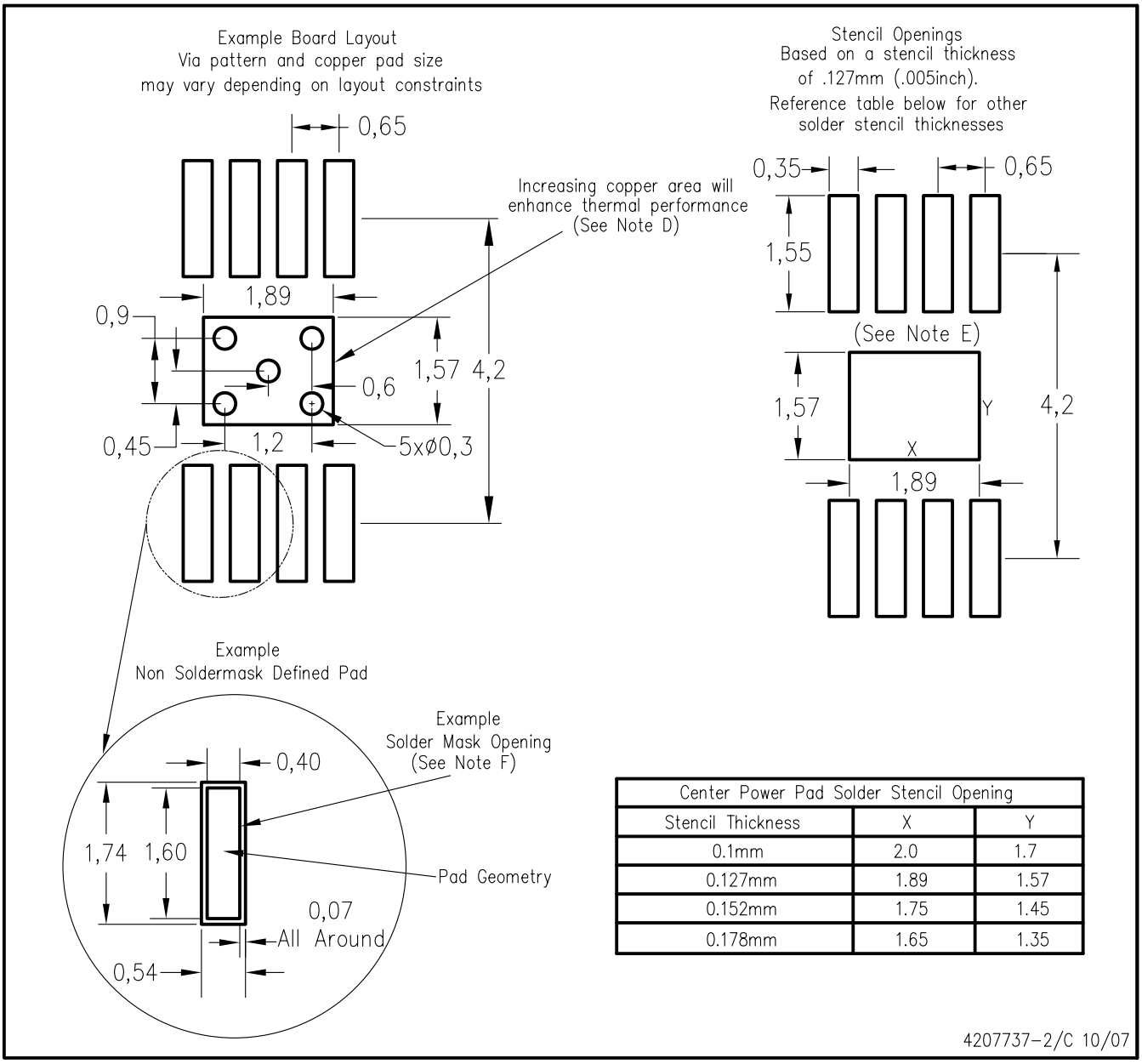


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

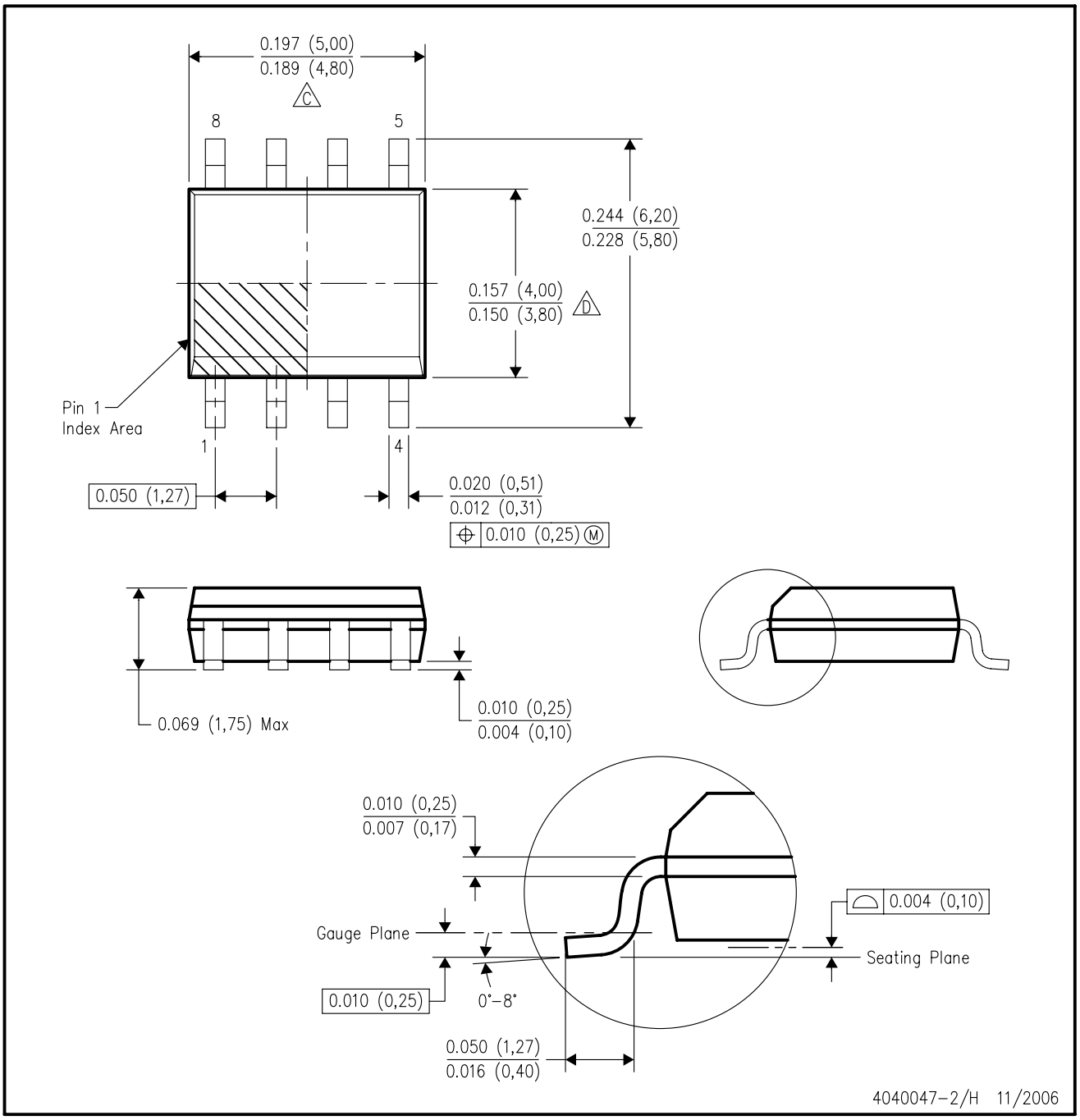
DGN (R–PDSO–G8) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

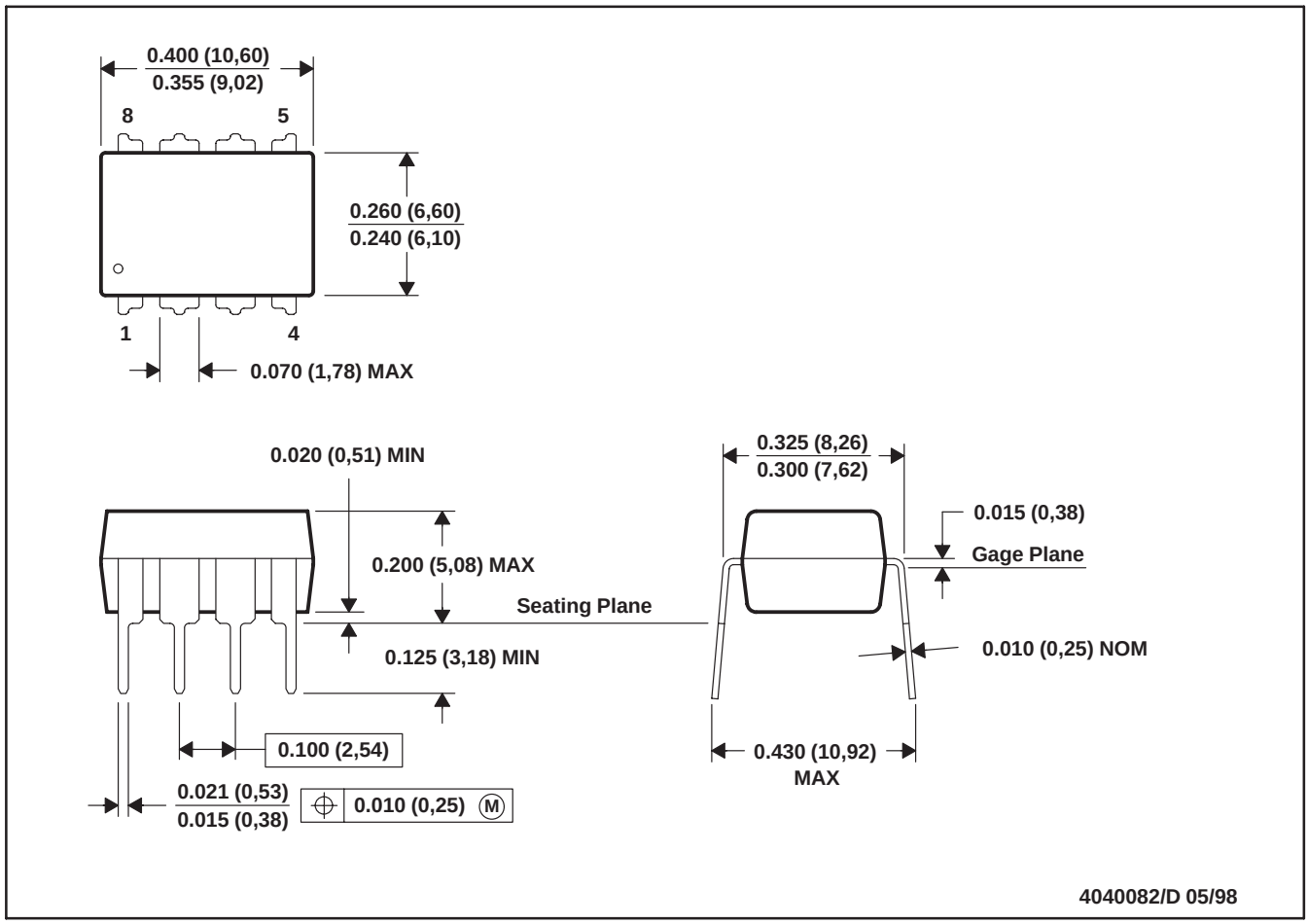
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

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