PROGRAMMABLE MAXIMUM DUTY CYCLE PWM CONTROLLER

FEATURES

- **User Programmable Maximum PWM Duty Cycle**
- **100-A Startup Current**
- **Operation to 1 MHz**
- **Internal Full Cycle Soft Start**
- **Internal Leading Edge Blanking of Current Sense Signal**
- **1-A Totem Pole Output**

ORDERING INFORMATION

PART NUMBER	TURN-ON THRESHOLD	TURN-OFF THRESHOLD	PACKAGES
UCCx807-1	7.2 V	6.9 V	J
UCCx807-2	12.5 V	8.3 V	N, D
UCCx807-3	4.3 V	4.1 V	N, D, PW

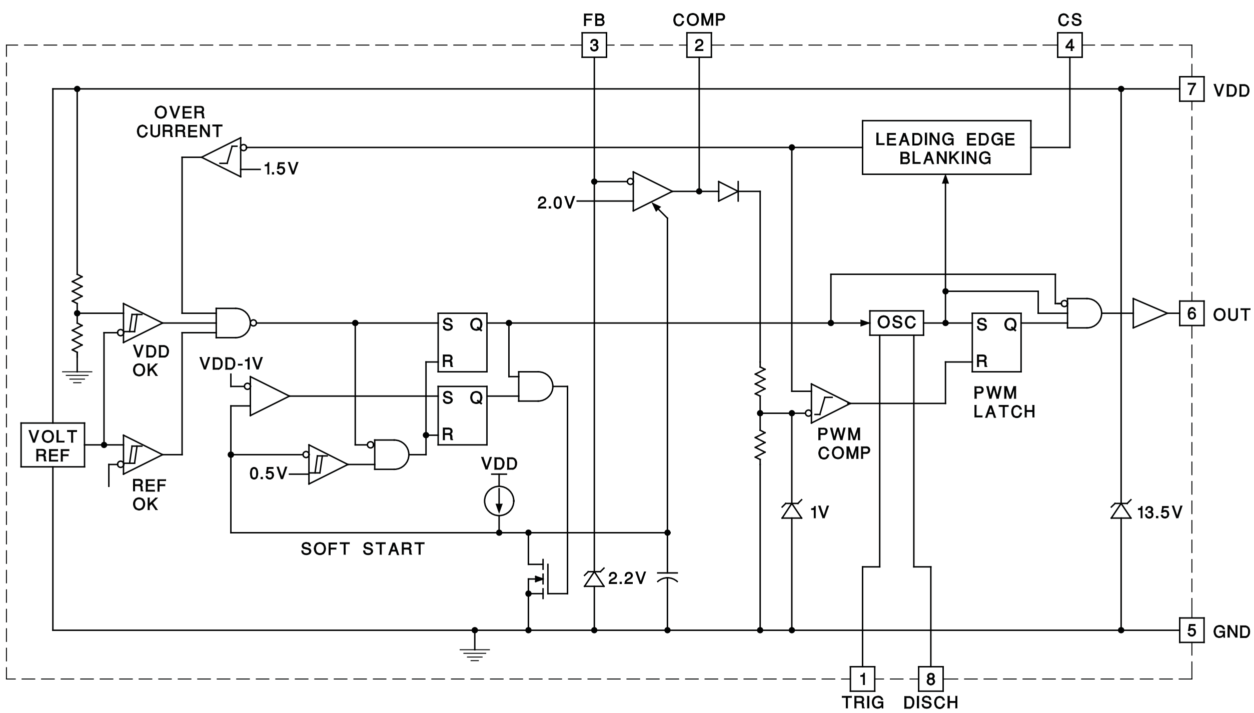
DESCRIPTION

The UCC3807 family of high speed, low power integrated circuits contains all of the control and drive circuitry required for off-line and dc-to-dc fixed frequency current mode switching power supplies with minimal external parts count.

These devices are similar to the UCC3800 family, but with the added feature of a user programmable maximum duty cycle. Oscillator frequency and maximum duty cycle are programmed with two resistors and a capacitor. The UCC3807 family also features internal full cycle soft start and internal leading edge blanking of the current sense input.

The UCC3807 family offers a variety of package options, temperature range options, and choice of critical voltage levels. The family has UVLO thresholds and hysteresis levels for off-line and battery powered systems. Thresholds are shown in the table below.

BLOCK DIAGRAM



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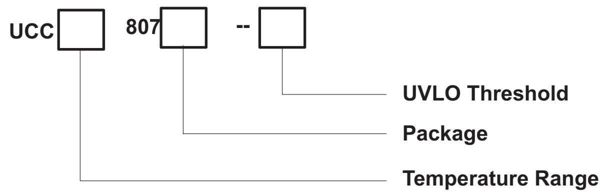
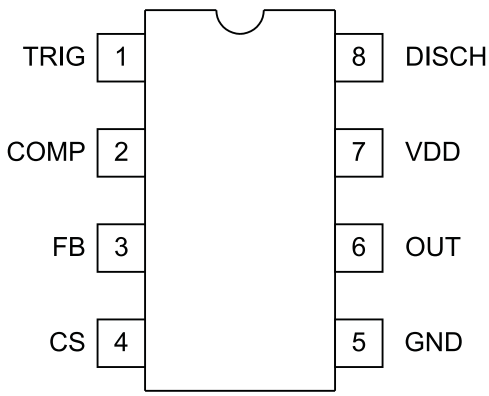
ORDERING INFORMATION

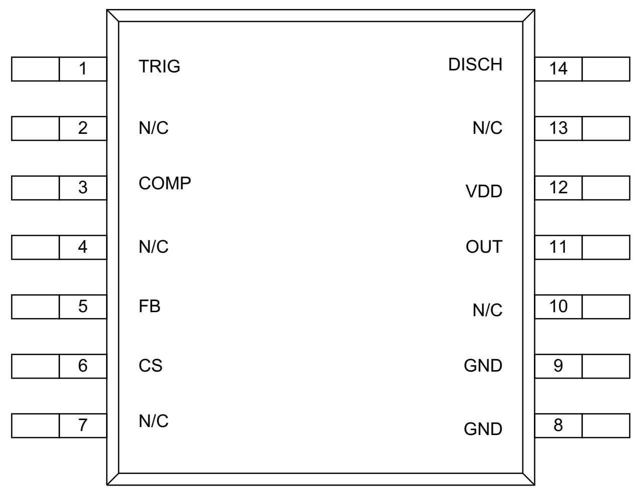


CONNECTION DIAGRAMS

DIL-8, SOIC-8 (Top View) J, N or D Packages



TSSOP-14 (Top View) PW Package (UCC2807-3 only)



NOTE

Specified thermal resistance is θ_{JL} (junction to lead) on TSSOP-14 pin 8 and 9.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PACKAGE	θ_{JA}	θ_{JC}
DIL-8, J	125-160	28 (1)
DIL-8, N	110 (2)	50
SOIC-8, D	84-160 (2)	42
TSSOP-14	132-158 (3)	15 (3)

(1) θ_{JC} data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states that "The baseline values shown are worst case (mean + 2s) for a 60 x 60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die size greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack, 10°C/W; pin grid array, 10°C/W".
(2) Specified θ_{JC} (junction to ambient) is for devices mounted to 5 in2 FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 in2 aluminum PC board. Test PWB was 0.062 inch thick and typically used 0.635 mm trace widths for power packages and 1.3 mm trace widths for non-power packages with 100 x 100 mil probe land area at the end of each trace.
(3) Modeled Data. If value range given for θ_{JA}, lower value is for 3 x 3 in., 1 ounce internal copper ground plane, higher value is for 1 x 1 inch ground plane. All model data assumes only one trace for each non-fused lead.

ABSOLUTE MAXIMUM RATINGS[(1)(2)]

		UNIT
Supply voltage (I_{DD} 10 mA)		13.5 V
Supply current		30 mA
OUT current		±1 A
Analog inputs (FB, CS)		–0.3 V to (V_{DD} + 0.3 V)
Power dissipation	T_A +25°C (N or J packages)	1 W
	T_A +25°C (D package)	0.65 W
Storage temperature		–65°C to 150°C
Junction temperature		–65°C to 150°C
Lead temperature (soldering, 10 sec.)		300°C

(1) All currents are positive into, negative out of the specified terminal.
(2) The UCCx807-2 is designed to be operated in a system that uses as external high voltage source to provide a startup current to a large capacitor from VDD to GND. The worse case current from this source should be less thanthe current needed to run the device in normal operation. The capacitor is needed to provide the reservoir of energy to allow the completion of the startup process before the UVLO voltage is encountered. Once started the converter should be designed so that it is self powered from a controlled voltage source of a lower voltage, one between 9.5 V and 11.5 V. The device is not designed to have the VDD clamp active during normal operation. The VDD voltage is always less than the clamp voltage. The upper limit of the input voltage is applicable to the whole family of UCCx807-1/-2 or -3.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated these specifications apply for T_A = –55°C to 125°C for UCC1807-1/-2/-3; –40°C to 85°C for UCC2807-1/-2/-3; and 0°C to 70°C for UCC3807-1/-2/-3; V_{DD} = 10 V[(1)], R_A = 12 kΩ , R_B = 4.7 kΩ, C_T = 330 pF, 1.0 µF capacitor from V_{DD} to GND, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Oscillator					
Frequency		175	202	228	kHz
Temperature stability	See [(2)]		2.5%		
Amplitude	See [(3)]		1/3VDD		V
Error Amplifier					
Input voltage	COMP = 2.0 V	1.95	2.00	2.05	V
Input bias current		–1		1	A
Open loop voltage gain		60	80		dB
COMP sink current	FB = 2.2 V, COMP = 1.0 V	0.3	2.5		mA
COMP source current	FB = 1.3 V, COMP = 4.0 V	–0.2	–0.5		
PWM					
Maximum duty cycle		75%	78%	81%	
Minimum duty cycle	COMP = 0 V			0%	
Current Sense					
Gain	See [(4)]	1.1	1.65	1.8	V/V
Maximum input signal	COMP = 5.0 V [(5)]	0.9	1.0	1.1	V
Input bias current		–200		200	nA
CS blank time		50	100	150	ns
Overcurrent threshold		1.4	1.5	1.6	V
COMP to CS offset	CS = 0 V	0.55	1.1	1.65	

(1) Adjust VDD above the start threshold before setting at 10 V for UCC3807-2.
(2) Ensured by design. Not 100% tested in production.
(3) Measured at TRIG; signal minimum = 1/3 VDD, maximum = 2/3 VDD.
(4) Gain is defined by: $A \; \frac{V_{COMP}}{V_{CS}}, \; 0 \; V_{CS} \; 0.8\ V$
(5) Parameter measured at trip point of latch with FB at 0 V.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated these specifications apply for T_A = –55°C to 125°C for UCC1807-1/-2/-3; –40°C to 85°C for UCC2807-1/-2/-3; and 0°C to 70°C for UCC3807-1/-2/-3; V_{DD} = 10 V, R_A = 12 kΩ , R_B = 4.7 kΩ, C_T = 330 pF, 1.0 µF capacitor from V_{DD} to GND, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output					
OUT low level	I = 100 mA		0.4	1	V
OUT high level	I = 100 mA, VDD – OUT		0.4	1	
Rise/fall time			20	100	ns
Undervoltage Lockout					
Start threshold	UCCx807-1 (6)	6.6	7.2	7.8	V
	UCCx807-2	11.5	12.5	13.5	
	UCCx807-3	4.1	4.3	4.5	
Minimum operating voltage after start	UCCx807-1 (6)	6.3	6.9	7.5	V
	UCCx807-2	7.6	8.3	9.0	
	UCCx807-3	3.9	4.1	4.3	
Hysteresis	UCCx807-1	0.1	0.3	0.5	V
	UCCx807-2	3.5	4.2	5.1	
	UCCx807-3	0.1	0.2	0.3	
Soft Start					
COMP rise time	FB = 1.8 V, From 0.5 V to 4.0 V		4		
Overall					
Startup current	VDD < Start Threshold (UCCx807-1,-3)		0.1	0.2	mA
	VDD < Start Threshold (UCCx807-2)		0.15	0.25	
Operating supply current	FB = 0 V, CS = 0 V, No Load (7)		1.3	2.1	
VDD zener shunt voltage	I_{DD} = 10 mA	12.0	13.5	15.0	V
Shunt to start difference		0.5	10		V

(6) Start Threshold and Zener Shunt thresholds track one another.
(7) Does not include current in external timing RC network.

PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC3807 is a low output impedance, 2 MHz operational amplifier. COMP can both source and sink current. The error amplifier is internally current limited, which allows zero duty cycle by externally forcing COMP to GND.

The UCC3807 family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

CS: Current sense input. There are two current sense comparators on the chip, the PWM comparator and an overcurrent comparator.

The UCC3807 also contains a leading edge blanking circuit, which disconnects the external CS signal from the current sense comparator during the 100 ns interval immediately following the rising edge of the signal at the OUT pin. In most applications, no analog filtering is required on CS. Compared to an external RC filtering technique, leading edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero on-time of the OUT signal is directly affected by the leading edge blanking and the CS to OUT propagation delay.

The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft start cycle.

FB: The inverting input to the error amplifier. For best stability, keep connections to FB as short as possible and stray capacitance as small as possible.

GND: Reference ground and power ground for all functions of the part.

OUT: The output of a high current power driver capable of driving the gate of a power MOSFET with peak currents exceeding 1A. OUT is actively held low when VDD is below the UVLO threshold.

The high current power driver consists of MOSFET output devices in a totem pole configuration. This allows the output to switch from VDD to GND. The output stage also provides a very low impedance which minimizes overshoot and undershoot. In most cases, external Schottky clamp diodes are not required.

TRIG/DISCH: Oscillator control pins. Trig is the oscillator timing input, which has an RC-type charge/discharge signal controlling the chip's internal oscillator. DISCH is the pin which provides the low impedance discharge path for the external RC network during normal operation. Oscillator frequency and maximum duty cycle are computed as follows:

$$\text{frequency} \; \frac{1.4}{R_A \; 2R_B \; C_T}$$

$$\text{duty cycle} \; \frac{R_A \; R_B}{R_A \; 2R_B} \qquad (1)$$

as shown in Figure 1.

For best performance, keep the lead from C_T to GND as short as possible. A separate ground connection for C_T is desirable. The minimum value of R_A is 10 kΩ , the minimum value of R_B is 2.2 kΩ, and the minimum value of C_T is 47 pF.

VDD: The power input connection for this device. Total VDD current is the sum of quiescent current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from

I_{OUT} = Qg F, where F is frequency.

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible in parallel with an electrolytic capacitor. Once started and operating properly the V_{DD} voltage should be below the clamp voltage of the device.

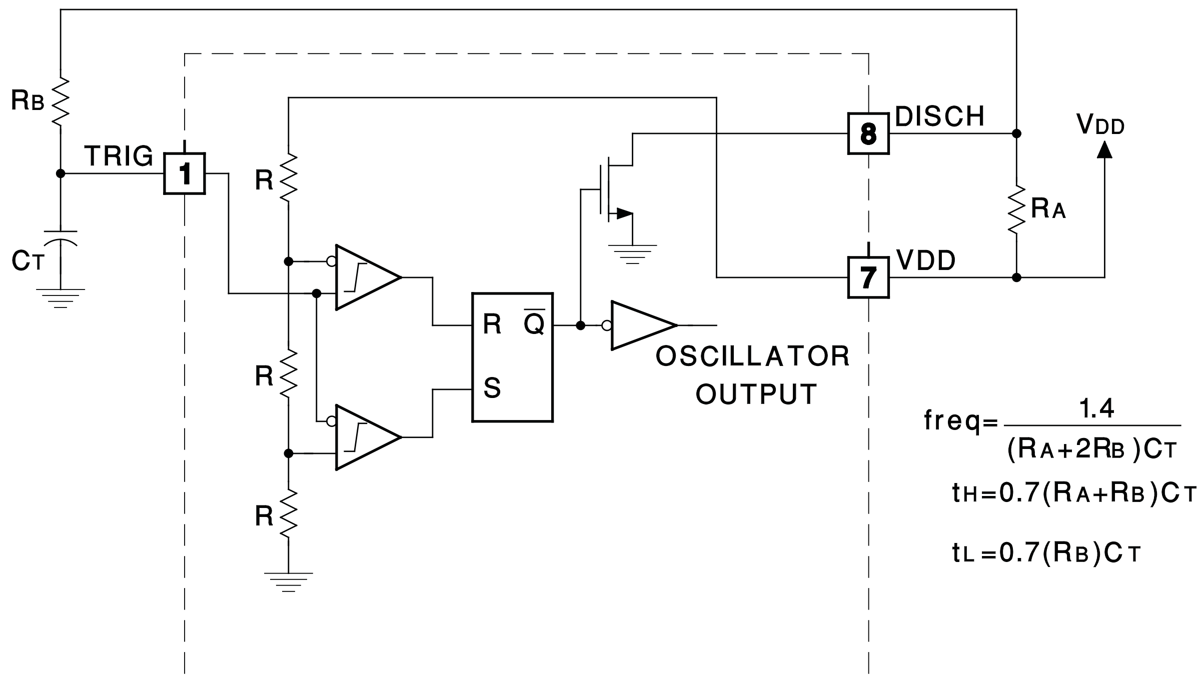


Figure 1. Oscillator Block Diagram

APPLICATION INFORMATION

The circuit shown in Figure 2 illustrates the use of the UCC3807 in a typical off-line application. The 100-W, 200-kHz, universal input forward converter produces a regulated 12VDC at 8 Amps. The programmable maximum duty cycle of the UCC3807 allows operation down to 80VRMS and up to 265VRMS with a simple RCD clamp to limit the MOSFET voltage and provide core reset. In this application the maximum duty cycle is set to about 65%. Another feature of the design is the use of a flyback winding on the output filter choke for both bootstrapping and voltage regulation. This method of loop closure eliminates the optocoupler and secondary side regulator, common to most off-line designs, while providing good line and load regulation.

Winding Information

T1:	
Core	Magnetics Inc. #P-42625-UG (ungapped)
Primary:	28 turns of 2x #26AWG
Secondary:	6 turns of 50x0.2 mm Litz wire
L1:	
Core:	Magnetics Inc. #P-42625-SG-37 (0.020" gap)
Main Winding:	13 turns of 2x #18AWG
Second Winding:	11 turns of #26AWG
Magnetics Inc.	
900 E. Butler Road P.O. Box 391 Butler, PA 16003 Tel: (412) 282-8282 Fax: (412) 282-6955	

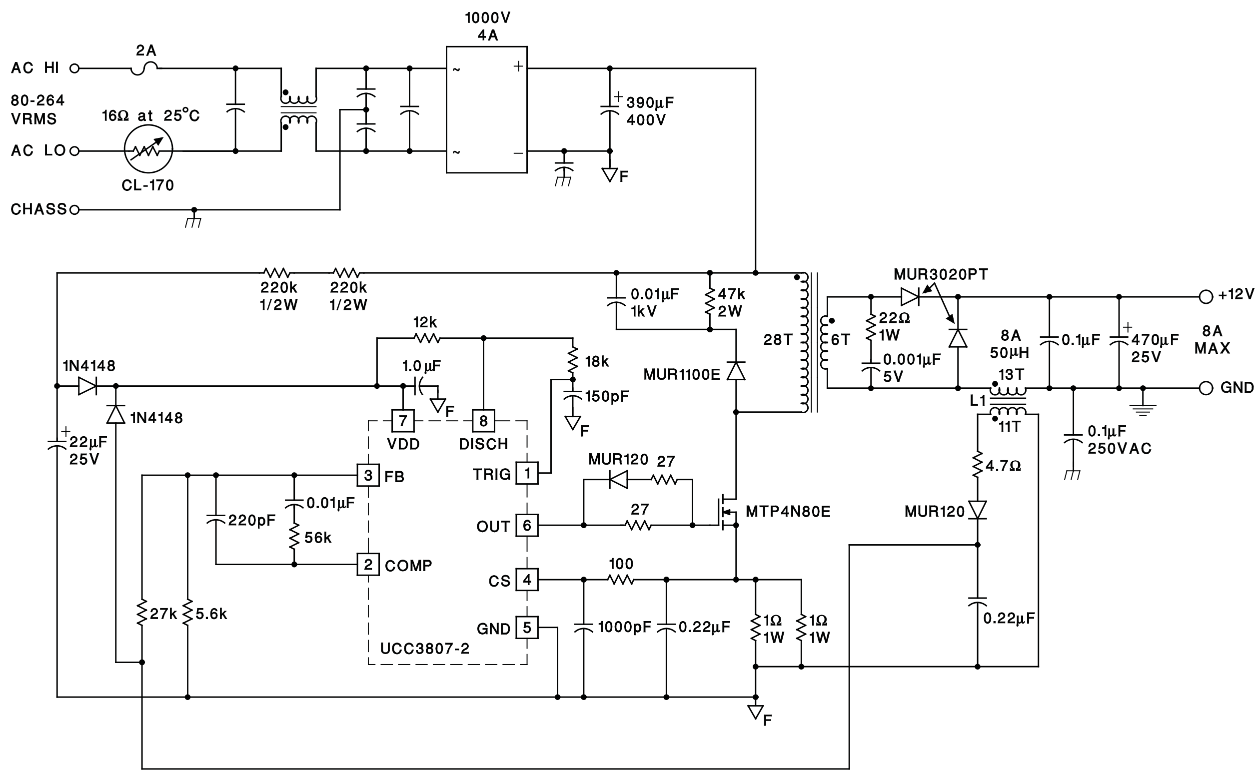


Figure 2. Typical Off-Line Application Using UCC3807-2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC2807D-1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2807D-1G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2807D-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2807D-2G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2807D-3	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2807D-3G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2807DTR-1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2807DTR-1G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2807DTR-2	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2807DTR-2G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2807DTR-3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2807DTR-3G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2807N-1	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC2807N-1G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC2807N-2	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC2807N-2G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC2807PW-3G4	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI
UCC2807PWTR-3G4	ACTIVE	TSSOP	PW	14		TBD	Call TI	Call TI
UCC3807D-1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3807D-1G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3807D-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3807D-2G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3807D-3	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3807D-3G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3807DTR-1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3807DTR-1G4	ACTIVE	SOIC	D	8	2500	Green (RoHS &	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
						no Sb/Br)		
UCC3807DTR-2G4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI
UCC3807DTR-3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3807DTR-3G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3807N-1	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3807N-1G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3807N-2	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3807N-2G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3807N-3	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3807N-3G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3807PWTR-3	PREVIEW	TSSOP	PW	14	2000	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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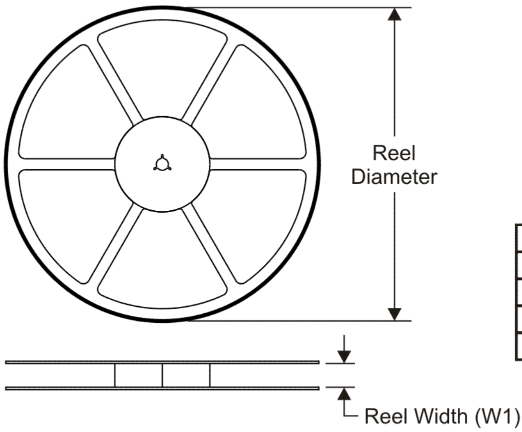
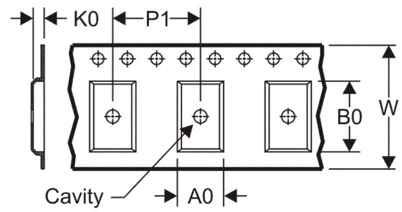
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

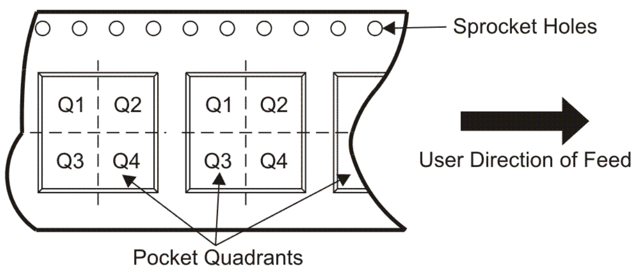


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

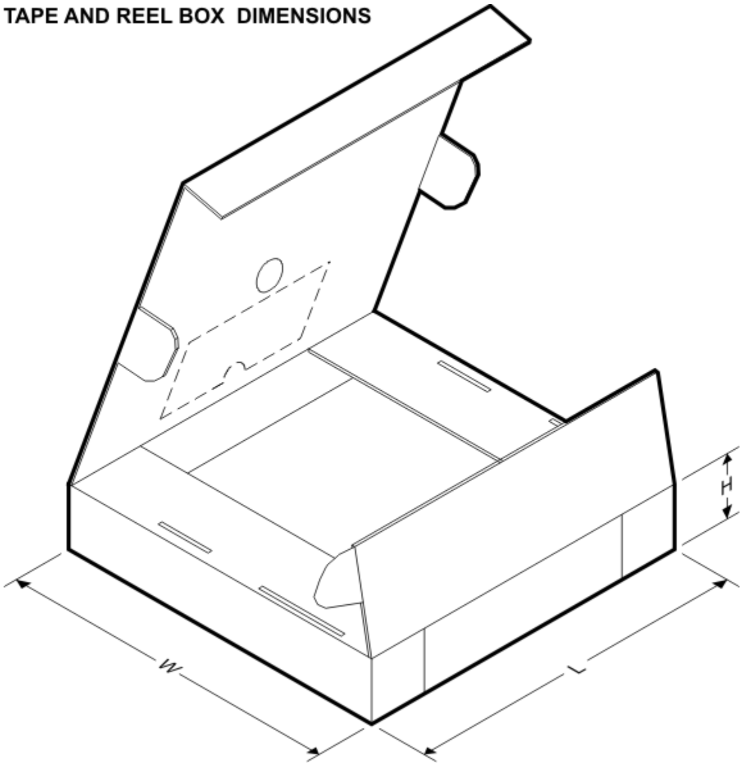
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2807DTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2807DTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2807DTR-3	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3807DTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3807DTR-3	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

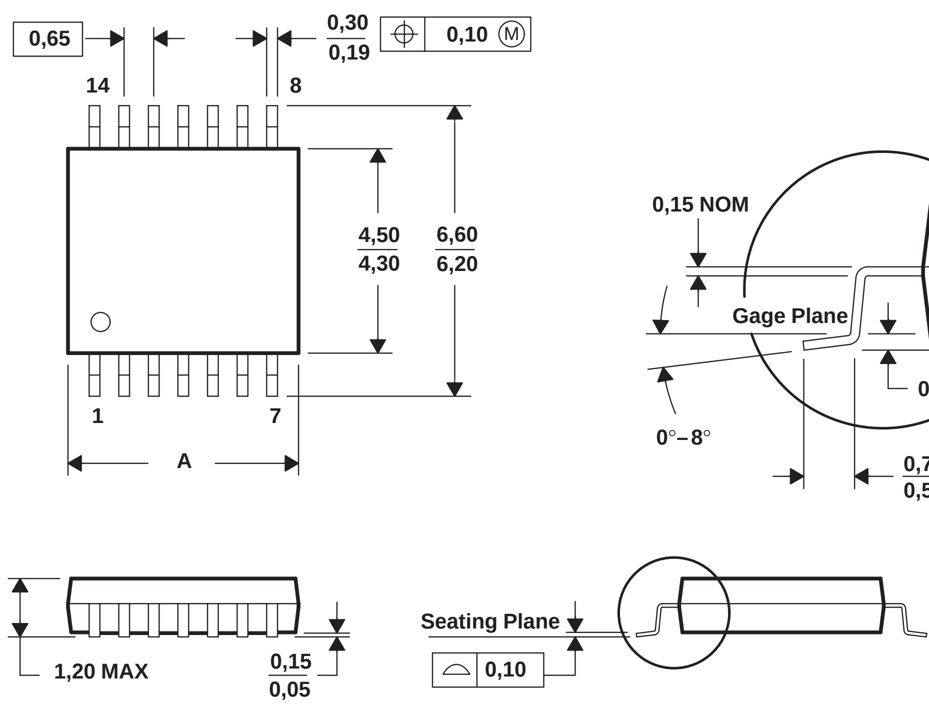


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2807DTR-1	SOIC	D	8	2500	346.0	346.0	29.0
UCC2807DTR-2	SOIC	D	8	2500	346.0	346.0	29.0
UCC2807DTR-3	SOIC	D	8	2500	346.0	346.0	29.0
UCC3807DTR-1	SOIC	D	8	2500	346.0	346.0	29.0
UCC3807DTR-3	SOIC	D	8	2500	346.0	346.0	29.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

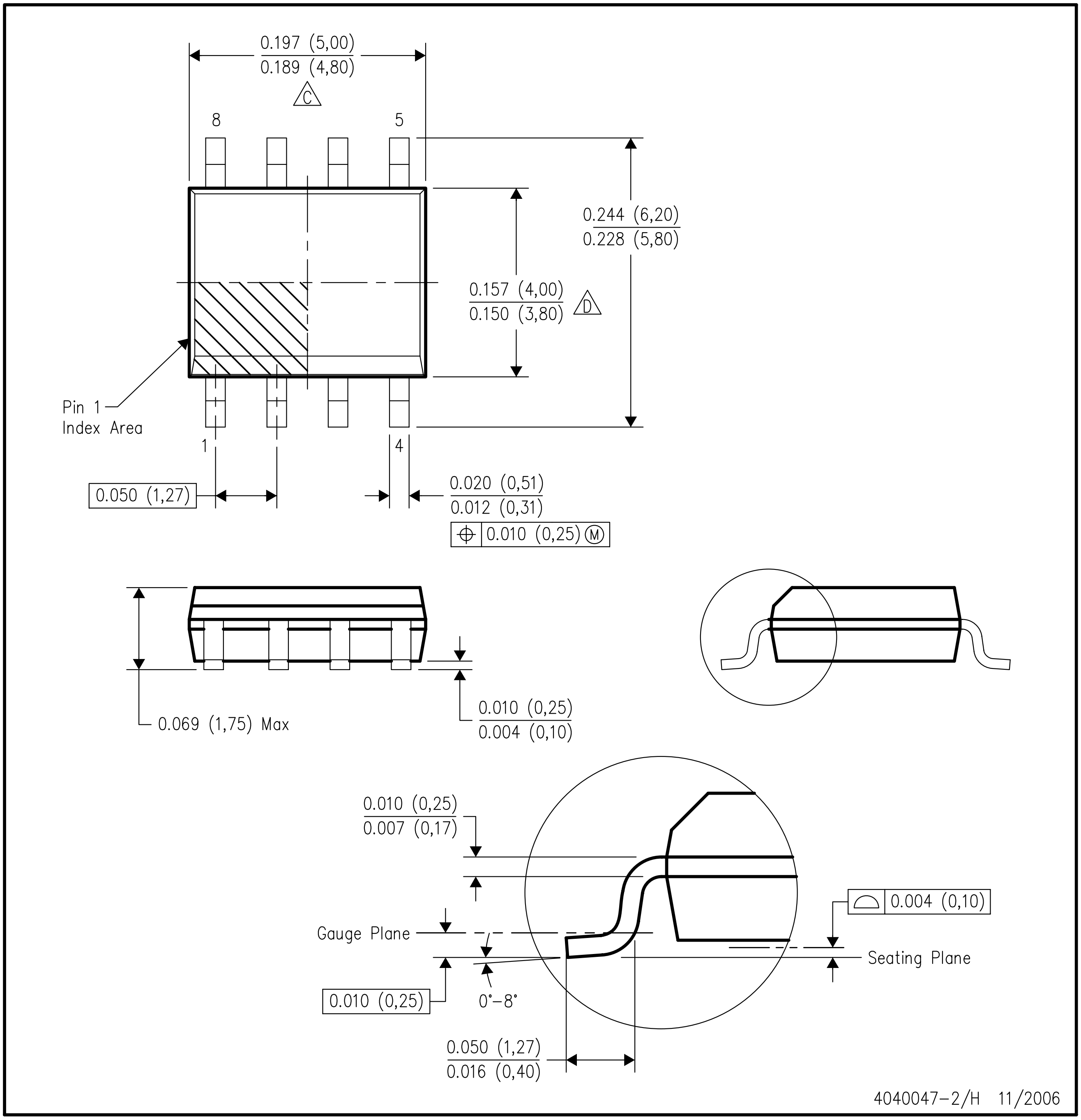


PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

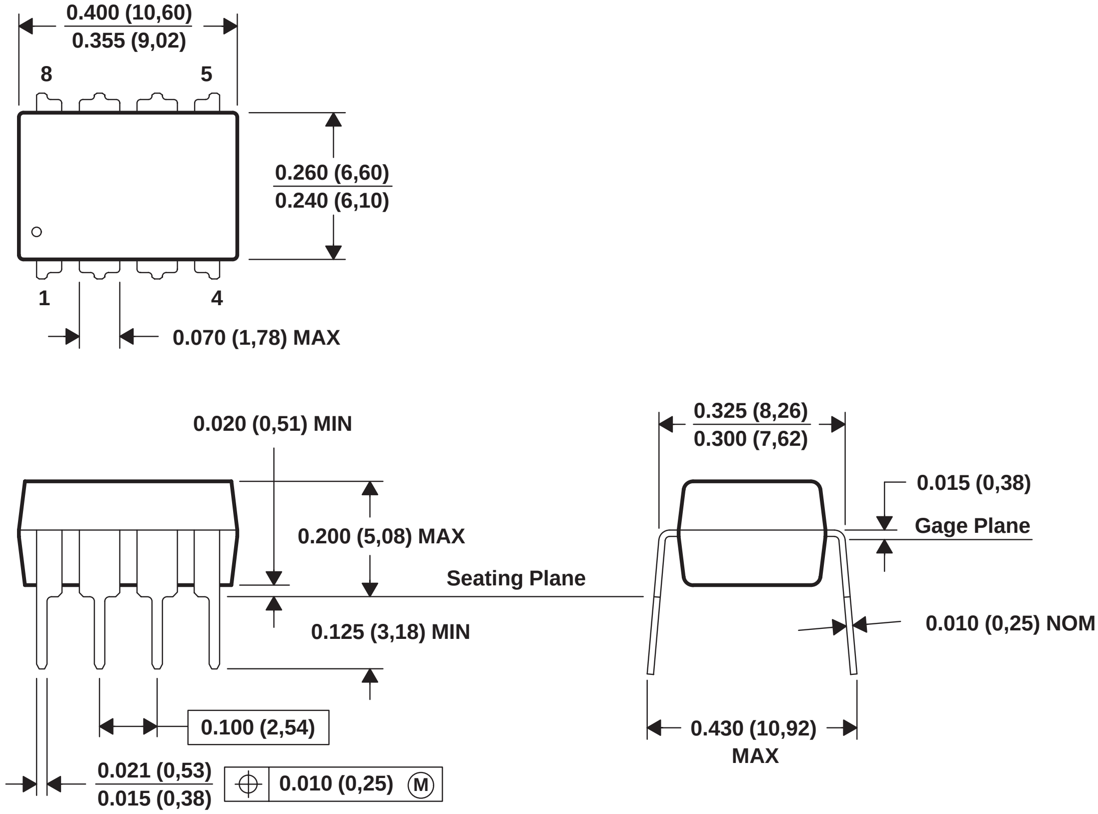
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

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