UNITRODE

Multimode (LVD/SE) SCSI 9 Line Terminator

FEATURES

- Auto Selection Multi-Mode Single Ended or Low Voltage Differential Termination
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Built-in SPI-3 Mode Change Filter/ Delay
- Meets SCSI-1, SCSI-2, Ultra2 (SPI-2 LVD) and Ultra3/Ultra160 Standards
- Supports Active Negation
- 3pF Channel Capacitance
- Reversed Disconnect Polarity

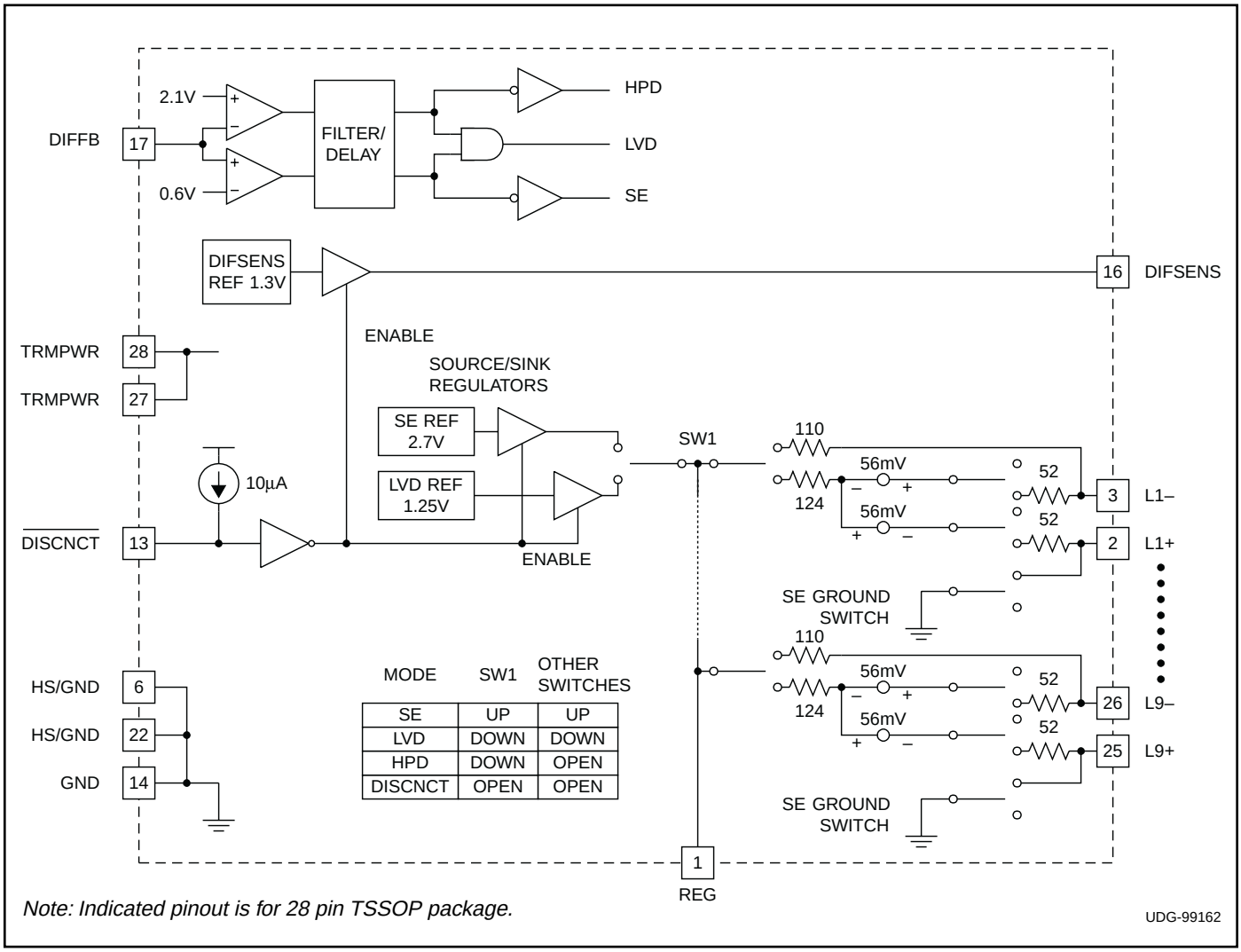
DESCRIPTION

The UCC5673 Multi-Mode Low Voltage Differential and Single Ended Terminator is both a single ended terminator and a low voltage differential terminator for the transition to the next generation SCSI Parallel Interface (SPI-3). The low voltage differential is a requirement for the higher speeds at a reasonable cost and is the only way to have adequate skew budgets.

The automatic mode select/change feature switches the terminator between Single Ended or LVD Termination, depending on the bus mode. If the bus is in High Voltage Differential Mode, the terminator lines transition into a High Impedance state.

The UCC5673 is SPI-3, SPI-2, and SCSI-2 compliant. This device is offered in a 28 pin TSSOP package to minimize the footprint. The UCC5673 is also available in a 36 pin MWP package.

BLOCK DIAGRAM



Note: Indicated pinout is for 28 pin TSSOP package.

ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage 6V
Signal Line Voltage . . . . . 0V to 5V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

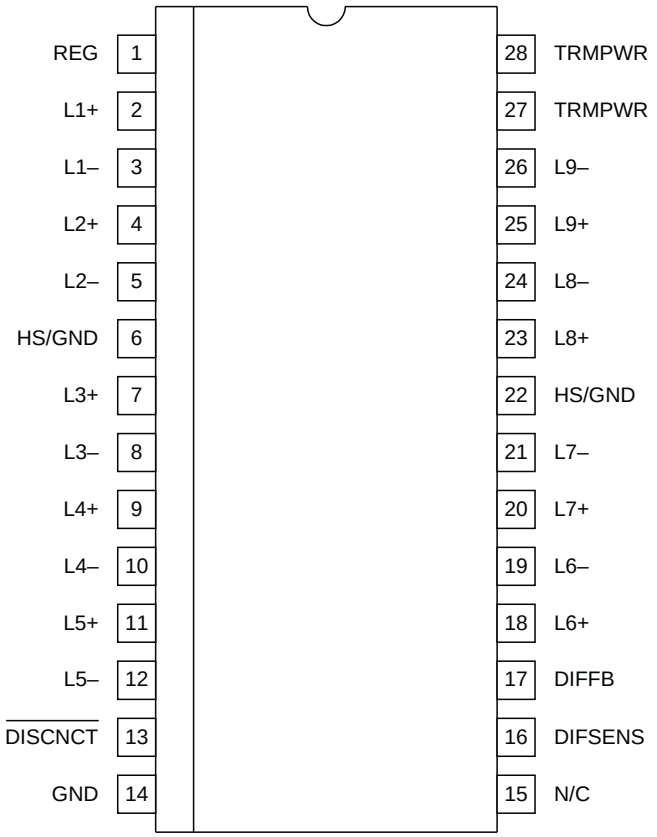
All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

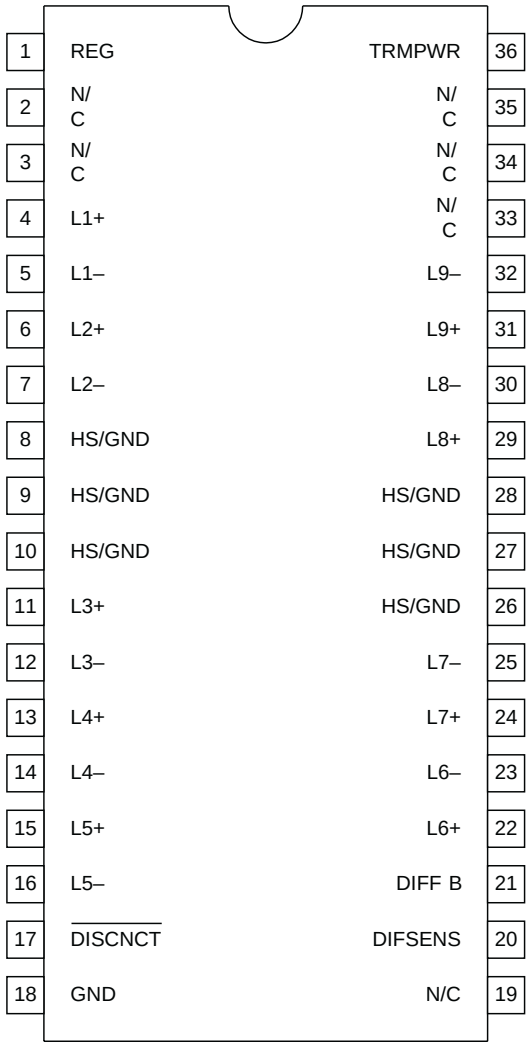
TRMPWR Voltage . . . . . 2.7V to 5.25V

CONNECTION DIAGRAM

TSSOP-28 (TOP VIEW)
PWP Package



QSOP-36 (TOP VIEW)
MWP Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 2.7V to 5.25V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current	LVD Mode		23	35	mA
	SE Mode		14	25	mA
	$\overline{\text{DISCNCT}}$ Mode		250	500	µA
Regulator Section					
1.25V Regulator Output Voltage	LVD Mode	1.15	1.25	1.35	V
1.25V Regulator Source Current	V_{REG}= 0V	–800	–420	–225	mA
1.25V Regulator Sink Current	V_{REG}= 3.3V	100	180	420	mA
2.7V Regulator Output Voltage	SE Mode	2.5	2.7	3.0	V
2.7V Regulator Source Current	V_{REG}= 0V	–800	–420	–225	mA
2.7V Regulator Sink Current	V_{REG}= 3.3V	100	180	420	mA
Diff Sense Driver (DIFSENS) Section					
1.3V DIFSENS Output Voltage	DIFSENS	1.2	1.3	1.4	V
1.3V DIFSENS Source Current	$V_{DIFSENS}$ = 0V	–15		–5	mA
1.3V DIFSENS Sink Current	$V_{DIFSENS}$ = 2.75V	50		200	µA
Differential Termination Section					
Differential Impedance		100	105	110	Ω
Common Mode Impedance	(Note 2)	110	150	165	Ω
Differential Bias Voltage		100		125	mV
Common Mode Bias		1.15	1.25	1.35	V
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended Termination Section					
Impedance	$Z = (VL_X - 0.2V) / IL_X$, (Note 3)	100	108	116	Ω
Termination Current	Signal Level 0.2V, All Lines Low	–25.4	–23	–20	mA
	Signal Level 0.5V	–22.4		–17	mA
Output Leakage				400	nA
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended GND SE Impedance	I = 10mA		20	60	Ω
Disconnect ($\overline{\text{DISCNCT}}$) and Diff Buffer (DIFFB) Input Section					
$\overline{\text{DISCNCT}}$ Threshold		0.8		2.0	V
$\overline{\text{DISCNCT}}$ Input Current		–30	–10		µA
DIFFB SE to LVD Threshold		0.5		0.7	V
DIFFB LVD to HPD Threshold		1.9		2.4	V
DIFFB Input Current		–1		1	µA

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 2.7V to 5.25V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Time Delay/Filter Section					
Mode Change Delay	A new mode change can start any time after a previous mode change has been detected. (Note 4)	100	180	300	ms

Note 1: *Guaranteed by design. Not 100% tested in production.*

Note 2: $Z_{CM} = \frac{1.2V}{I_{(V_{CM}+0.6V)} - I_{(V_{CM}-0.6V)}}$;

Where VCM = Voltage measured with L+ tied to L– and zero current applied;

Note 3: *VL_X= Output voltage for each terminator minus output pin (L1– through L9–) with each pin unloaded.*
IL_X = Output current for each terminator minus output pin (L1– through L9–) with the minus output pin forced to 0.2V.

Note 4: *Noise on DIFFB will not cause a false mode change. The time delay is that same for a change from any mode to any other mode. Within 300ms after power is applied the mode is defined by the voltage of DIFFB.*

PIN DESCRIPTIONS

DIFFB: Input pin for the comparators that select SE, LVD, or HIPD modes of operation. This pin should be decoupled with a 0.1µF capacitor to ground and then coupled to the DIFSENS pin through a 20kΩ resistor.

DIFSENS: Connects to the Diff Sense line of the SCSI bus. The bus mode is controlled by the voltage level on this pin.

$\overline{\text{DISCNCT}}$: Input pin used to shut down the terminator if the terminator is not connected at the end of the bus. Connect this pin to ground to disable the terminator or open pin to activate the terminator.

HS/GND: Heat sink ground pins. These should be connected to large ground area PC board traces to increase the power dissipation capability.

GND: Power Supply return.

L1– thru L9–: Termination lines. These are the active lines in SE mode and are the negative lines for LVD mode. In HIPD mode, these lines are high impedance.

L1+ thru L9+: Termination lines. These lines switch to ground in SE mode and are the positive lines for LVD mode. In HIPD mode, these lines are high impedance.

TRMPWR: 2.7V to 5.25V power input pin.

APPLICATION INFORMATION

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI devices are present on the bus.

The UCC5673 is used in multi-mode active termination applications, where single ended (SE) and low voltage differential (LVD) devices might coexist. The UCC5673 has both SE and LVD termination networks integrated into a single monolithic component. The correct termination network is automatically determined by the SCSI bus "DIFSENS" signal.

The SCSI bus DIFSENS signal line is used to identify which types of SCSI devices are present on the bus. On power-up, the UCC5673 DIFSENS drivers will try to deliver 1.3V to the DIFSENS line. If only LVD devices are present, the DIFSENS line will be successfully driven to 1.3V and the terminators will configure for LVD operation. If any single ended devices are present, they will present a short to ground on the DIFSENS line, signaling the UCC5673(s) to configure into the SE mode, accommodating the SE devices. Or, if any high voltage differential (HVD) devices are present, the DIFSENS line is pulled high and the terminator will enter a high impedance state, effectively disconnecting from the bus.

The DIFSENS line is monitored by each terminator through a 50Hz noise filter at the DIFFB input pin. A set of comparators detect and select the appropriate termination for the bus as follows. If the DIFSENS signal is be-

APPLICATION INFORMATION (cont.)

low 0.5V, the termination network is SE. Between 0.7V and 1.9V, the termination network switches to LVD, and above 2.4V is HVD, causing the terminators to disconnect from the bus. The thresholds accommodate differences in ground potential that can occur with long lines.

Three UCC5673 multi-mode parts are required at each end of the bus to terminate 27 (18 data, plus 9 control) lines. Each part includes a DIFSENS driver, but only one is necessary to drive the line. The DIFFB inputs on all three parts are connected together, allowing them to share the same 50Hz noise filter. This multi-mode terminator operates in full specification down to 2.7V TRMPWR voltage. This accommodates 3.3V systems, with allowance for the 3.3V supply tolerance (+/- 10%), a unidirectional fusing device and cable drop. In 3.3V

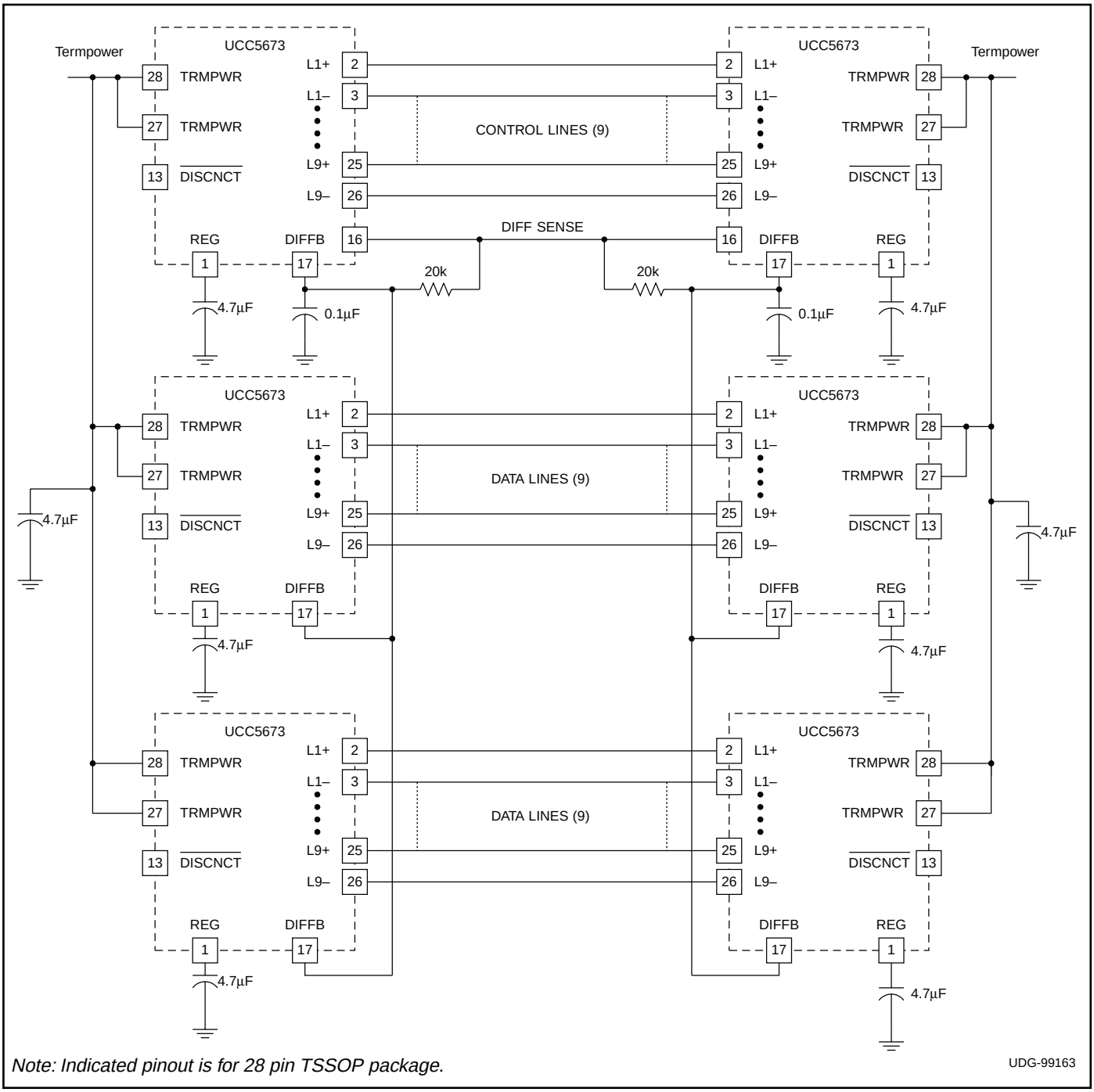


Figure 1. Application diagram.

APPLICATION INFORMATION (cont.)

TRMPWR systems, the UCC3918 is recommended in place of the fuse and diode. The UCC3918's lower voltage drop allows additional margin over the fuse and diode, for the far end terminator.

Layout is critical for Ultra2 and Ultra3 systems. The SPI-2 standard for capacitance loading is 10pF maximum from each positive and negative signal line to ground, and a maximum of 5pF between the positive and negative signal lines of each pair is allowed. These maximum capacitances apply to differential bus termination circuitry that is not part of a SCSI device, (e.g. a cable terminator). If the termination circuitry is included as part of a SCSI device, (e.g., a host adaptor, disk or tape drive), then the corresponding requirements are 30pF maximum from each positive and negative signal line to ground and 15pF maximum between the positive and negative signal lines of each pair.

The SPI-2 standard for capacitance balance of each pair and balance between pairs is more stringent. The standard is 0.75pF maximum difference from the positive and negative signal lines of each pair to ground. An additional requirement is a maximum difference of 2pF when comparing pair to pair. These requirements apply to differential bus termination circuitry that is not part of a SCSI device. If the termination circuitry is included as part of a device, then the corresponding balance requirements are 2.25pF maximum difference within a pair, and 3pF from pair to pair.

Feed-throughs, through-hole connections, and etch lengths need to be carefully balanced. Standard multi-layer power and ground plane spacing add about 1pF to each plane. Each feed-through will add about 2.5pF to 3.5pF. Enlarging the clearance holes on both power and ground planes will reduce the capacitance. Similarly, opening up the power and ground planes under the connector will reduce the capacitance for through-hole connector applications. Capacitance will also be affected by components, in close proximity, above and below the circuit board.

Unitrode multi-mode terminators are designed with very tight balance, typically 0.1pF between pins in a pair and 0.3pF between pairs. At each L+ pin, a ground driver drives the pin to ground, while in single ended mode. The ground driver is specially designed to not effect the capacitive balance of the bus when the device is in LVD or disconnect mode.

Multi-layer boards need to adhere to the 120Ω impedance standard, including the connectors and feed-throughs. This is normally done on the outer layers with 4 mil etch and 4 mil spacing between runs within a pair, and a minimum of 8 mil spacing to the adjacent pairs to reduce crosstalk. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50Ω rather than 120Ω differential systems. Careful consideration must be given to the issue of heat management. A multi-mode terminator, operating in SE mode, will dissipate as much as 130mW of instantaneous power per active line with TRMPWR = 5.25V. The UCC5673 is offered in a 28 pin TSSOP. This package includes two heat sink ground pins. These heat sink/ground pins are directly connected to the die mount paddle under the die and conduct heat from the die to reduce the junction temperature. Both of the HS/GND pins need to be connected to etch area or four feed-through per pin connecting to the ground plane layer on a multi-layer board.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC5673MWP	NRND	SSOP	DCE	36	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC5673MWPG4	ACTIVE	SSOP	DCE	36	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC5673PWP	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC5673PWPG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC5673PWPTR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC5673PWPTRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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