UNITRODE

UCC18500/1/2/3
UCC28500/1/2/3
UCC38500/1/2/3
PRELIMINARY

BiCMOS PFC/PWM Combination Controller

FEATURES

- Combines PFC and 2nd Stage Down Converter Function
- Controls Boost PWM to Near-unity Power Factor
- Accurate Power Limiting
- Average Current Mode Control in PFC Stage
- Peak Current Mode Control in Second Stage
- Programmable Oscillator
- Leading Edge/Trailing Edge Modulation for Reduced Output Ripple Using SmartSync™
- Low Startup Supply Current
- Synchronized Second Stage Start-up, with Programmable Soft-start
- Programmable Second Stage Shut-down

DESCRIPTION

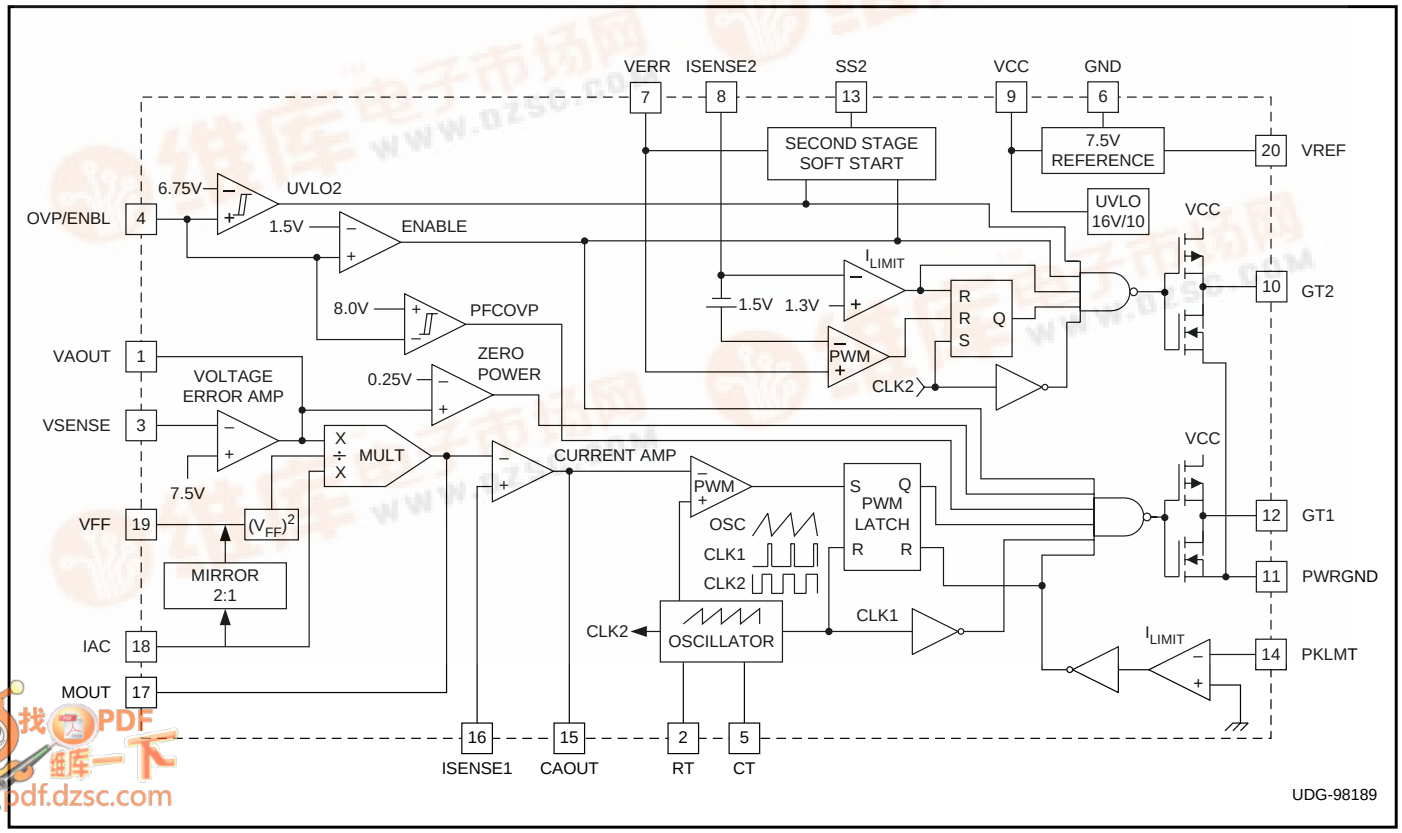
The UCC18500 family provides all of the functions necessary for an active power factor corrected preregulator and a second stage DC-to-DC converter. The controller achieves near-unity power factor by shaping the AC input line current waveform to correspond to the AC input line voltage using average current mode control. The DC-to-DC converter uses peak current mode control to perform the step down power conversion.

The PFC stage is leading edge modulated while the second stage is trailing edge synchronized to allow for minimum overlap between the boost and PWM switches. This reduces ripple current in the bulk output capacitor.

In order to operate with a three to one range of input line voltages, a line feedforward (V_{FF}) in used to keep input power constant with varying input voltage. Generation of V_{FF} is done using I_{AC} in conjunction with an external single pole filter. This not only reduces external parts count, but avoids the use of high voltage components offering a lower cost solution. The multiplier then divides the line current by the square of V_{FF}.

(continued)

BLOCK DIAGRAM



DESCRIPTION (cont.)

The UCC18500 PFC section incorporates a low offset voltage amplifier with 7.5V reference, a highly linear multiplier capable of a wide current range, a high bandwidth, low offset current amplifier, with a novel noise attenuation configuration, PWM comparator and latch and a high current output driver. Additional PFC features include over-voltage protection, zero power detection to turn-off the output when VAOUT is below 0.25V and peak current and power limiting.

The DC-to-DC section relies on an error signal generated on secondary-side and processes it by performing peak current mode control. The DC-to-DC section also features current limiting, a controlled soft-start, preset operating range with selectable options, and 50% maximum duty cycle.

The UCC38500 and UCC38502 have a wide PFC-UVLO threshold (16.5V/10V) for bootstrap bias supply operation. The UCC38501 and UCC38503 are designed with a narrow UVLO range (10.5V/10V) more suitable for fixed bias operation. The UCC38500 and UCC38501 have a narrow UVLO threshold for PWM stage (to allow operation down to 75% of nominal bulk voltage), while the UCC38502 and UCC38503 are configured for a much wider operation range for the PWM stage (down to 50% of bulk nominal voltage).

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} 18V
Gate Drive Current
  Continuous 0.2A
  50% Duty Cycle 1A
Input Voltage
  I_{SENSE1}, I_{SENSE2} MOUT,V_{SENSE}, OVP, ENBL, ... 11V
  PKLMT 5V
Input Current, R_{SET}, I_{AC}, PKLMT, ENA 10mA
Maximum Negative Voltage, GT1, GT2,
  PKLMT, MOUT . . . . . –0.5V
Power Dissipation 1W

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

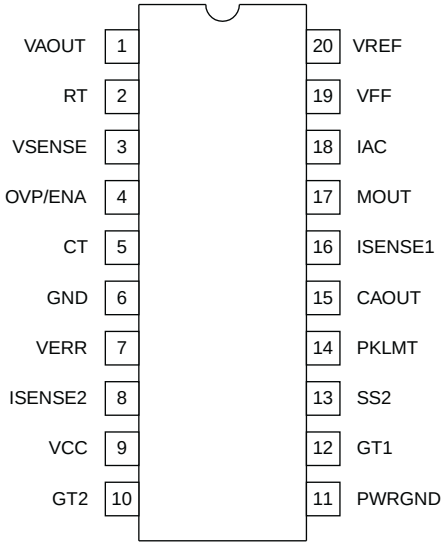
ORDERING INFORMATION

UCC □850□□

- PACKAGE
- PRODUCT OPTION
- TEMPERATURE RANGE

CONNECTION DIAGRAMS

DIL-20, SOIC-20 (TOP VIEW)
N, DW and J Packages



PACKAGE INFORMATION

	TEMPERATURE RANGE	PRODUCT OPTION		PACKAGE
		UVLO	UVLO2 HYSTERESIS	
UCC18500	–55° C to +125° C	16	1.2	J-CDIP N-PDIP DW-SOIC
UCC18501		10.5	1.2	
UCC18502		16	3.0	
UCC18503		10.5	3.0	
UCC28500	–40° C to +85° C	16	1.2	N-PDIP DW-SOIC
UCC28501		10.5	1.2	
UCC28502		16	3.0	
UCC28503		10.5	3.0	
UCC38500	0° C to +70° C	16	1.2	
UCC38501		10.5	1.2	
UCC38502		16	3.0	
UCC38503		10.5	3.0	

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these specifications hold for T_A=0°C to 70°C for the UCC3850X, –40°C to +85°C for the UCC2850X, and –55°C to +125°C for the UCC1850X, $T_A = T_J$. VCC = 12V, RT = 22k, CT = 330pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Supply Current, Off	VCC = 12V (VCC Turn-on Threshold –300mV)		150	300	µA
Supply Current, On	VCC = 12V		4	6	mA
UVLO Section					
VCC Turn-On Threshold (UCCX8500/502)		15.4	16	16.6	V
UVLO Hysteresis (UCCX8500/502)		5.4	6	6.2	V
Shunt Voltage (UCCX8500/502)	I_{VCC} = 10mA		17	17.5	V
VCC Turn-On Threshold (UCCX8501/503)		10.2	10.5	10.8	V
UVLO Hysteresis (UCCX8501/503)		0.4	0.5	0.6	V
Voltage Amplifier Section					
Input Voltage	T_A = 0°C to 70°C	7.388	7.500	7.613	V
	T_A = –40°C to 85°C	7.369	7.500	7.631	V
	T_A = –55°C to125°C	7.313	7.500	7.687	V
V_{SENSE} Bias Current			50		nA
Open Loop Gain	VAOUT = 2V to 5V		80		dB
V_{OUT} High	I_{LOAD} = –150µA	5.4	5.5	5.6	V
V_{OUT} Low	I_{LOAD} = 150µA		0.05	0.10	V
Over Voltage Protection and Enable Section					
Over Voltage Reference		7.8	8.0	8.2	V
Hysteresis		400	500	600	mV
Enable Threshold		1	1.5	2	V
Current Amplifier Section					
Input Offset Voltage	V_{CM} = 0V, V_{CAOUT} = 3V	–5	0	5	mV
Input Bias Current	V_{CM} = 0V, V_{CAOUT} = 3V		–50		nA
Input Offset Current	V_{CM} = 0V, V_{CAOUT} = 3V		25		nA
Open Loop Gain	V_{CM} = 0V, V_{CAOUT} = 2V to 5V		90		dB
CMRR	V_{CM} = 0V to 1.5V, V_{CAOUT} = 3V		80		dB
V_{OUT} High	I_{LOAD} = –120µA		6.3		V
V_{OUT} Low	I_{LOAD} = 1mA		0.2		V
Gain Bandwidth Product	(Note 1)		2.5		MHz
Voltage Reference Section					
Input Voltage	TA = 0° C to 70° C	7.388	7.500	7.613	V
	TA = –40° C to 85° C	7.369	7.500	7.631	V
	TA = –55° C to 125° C	7.313	7.500	7.687	V
Load Regulation	I_{REF} = 1mA to 2mA		5	10	mV
Line Regulation	VCC = 12V to 16V		10	20	mV
Short Circuit Current	VREF = 0V		–25		mA
Oscillator Section					
Initial Accuracy	T_A = 25°C	85	100	115	kHz
Voltage Stability	VCC = 10.8V to 15V		1		%
Total Variation	Line, Temp	80		120	kHz
Ramp Peak Voltage		4.5	5	5.5	V
Ramp Amplitude Voltage (peak to peak)			4		V

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these specifications hold for T_A=0°C to 70°C for the UCC3850X, –40°C to +85°C for the UCC2850X, and –55°C to +125°C for the UCC1850X, $T_A = T_J$. VCC = 12V, RT = 22k, CT = 330pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Peak Current Limit Section					
PKLMT Reference Voltage		–15	0	15	mV
PKLMT Propogation Delay			300		ns
Multiplier Section					
High Line, Low Power	I_{AC} = 500µA, VFF = 4.7V, VAOUT = 1.25V		–6		µA
High Line, High Power	I_{AC} = 500µA, VFF = 4.7V, VAOUT = 5V		–90		µA
Low Line, Low Power	I_{AC} = 150µA, VFF = 1.4V, VAOUT = 1.25V		–19		µA
Low Line, High Power	I_{AC} = 150µA, VFF = 1.4V, VAOUT = 5V		–300		µA
IAC Limited	I_{AC} = 150µA, VFF = 1.3V, VAOUT = 5V		–300		µA
Gain Constant (K)	I_{AC} = 300µA, VFF = 2.8V, VAOUT = 2.5V		1		1/V
Zero Current	I_{AC} = 150µA, VFF = 1.4V, VAOUT = 0.25V		0	–2	µA
	I_{AC} = 500µA, VFF = 4.7V, VAOUT = 0.25V		0	–2	µA
	I_{AC} = 500µA, VFF = 4.7V, VAOUT = 0.5V			–3	µA
Power Limit	I_{AC} = 150µA, VFF = 1.4V, VAOUT = 5V		–420		µW
Zero Power Section					
Zero Power Comparator Threshold	Measured on VAOUT	0.10	0.25	0.40	V
PFC Gate Driver Section					
GT1 Pull Up Resistance	I_{OUT} = –100mA		7		Ω
GT1 Pull Down Resistance	I_{OUT} = 100mA		3		Ω
GT1 Output Rise Time	C_{LOAD} = 1nF, R_{LOAD} = 10Ω		25		ns
GT1 Output Fall Time	C_{LOAD} = 1nF, R_{LOAD} = 10Ω		10		ns
Maximum Duty Cycle			94		%
Second Stage UVLO (UVLO2)					
PWM Turn-on Reference (UCCX8500/501)		6.30	6.75	7.30	V
Hysteresis (UCCX8500/501)			1.2		V
PWM Turn-on Reference (UCCX8502/503)		6.30	6.75	7.30	V
Hysteresis (UCCX8502/503)			3		V
Second Stage Soft Start Section					
SS2 Charge Current		–7.5	–10	–12.5	µA
VERR	I_{VERR} = 2mA, UVLO = Low			300	mV
SS2 Discharge Current	ENA = High, UVLO = Low, SS2 = 2.5V	3		10	mA
Second Stage Duty Cycle Clamp Section					
Maximum Duty Cycle		44		50	%
Second Stage Pulse by Pulse Current Sense Section					
Current Sense Comparator Threshold	VERR = 2.5V, Measured on ISENSE2	.95	1.05	1.15	V
Second Stage Over Current Limit Section					
Peak Current Comparator Threshold		1.15	1.30	1.45	V
Input Bias Current			50		nA
Second Stage Gate Driver Section					
GT2 Pull Up Resistance	I_{OUT} = –200mA		7		Ω
GT2 Pull Down Resistance	I_{OUT} = 100mA		3		Ω
GT2 Output Rise Time	C_{LOAD} = 1nF, R_{LOAD} = 10Ω		25		ns
GT2 Output Fall Time	C_{LOAD} = 1nF, R_{LOAD} = 10Ω		25		ns

Note 1: Guaranteed by design, not 100% tested in production.

PIN DESCRIPTIONS

CAOUT: (current amplifier output) This is the output of a wide bandwidth op amp that senses line current and commands the PFC pulse width modulator (PWM) to force the correct current. This output can swing close to GND, allowing the PWM to force zero duty cycle when necessary.

CT: (Oscillator timing capacitor) A capacitor from CT to GND will set the oscillator frequency according to:

$$f = \frac{0.725}{(RT \bullet CT)}$$

GND: (ground) All voltages measured with respect to ground. VCC and VREF should be bypassed directly to GND with a 0.1µF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing capacitor to GND should be as short and direct as possible.

GT1: (gate drive) The output drive for the PFC stage is a totem pole MOSFET gate driver on GT1. Use a series gate resistor of at least 5 ohms to prevent interaction between the gate impedance and the GT1 output driver that might cause the GT1 to overshoot excessively. Some overshoot of the GT1 output is always expected when driving a capacitive load.

GT2: (gate drive) Same as output GT1 for the second stage output drive. Limited to 50% maximum duty cycle.

IAC: (input ac current) This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (I_{AC}) to MOUT, so this is the only multiplier input which should be used for sensing instantaneous line voltage. Recommended maximum I_{AC} is 500µA.

ISENSE1: (current sense) This is the non-inverting input to the current amplifier. This input and the inverting input MOUT remain functional down to and below GND.

ISENSE2: (current sense) A resistor from the source of the lower FET to ground generates the input signal for the peak limit control of the second stage. The oscillator ramp can also be summed into this pin, for slope compensation.

MOUT: (multiplier output and current sense amplifier inverting input) The output of the analog multiplier and the inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high impedance input so the amplifier can be configured as a differential amplifier to reject ground noise. Multiplier output current is given by:

$$I_{MO} = \frac{(VAOUT - 1.0) \bullet I_{AC}}{K \bullet V_{FF}{}^2}$$

Connect current loop compensation components between MOUT and CAOUT.

OVP/ENBL: (over-voltage/enable) A window comparator input which will disable the PFC output driver if the boost output is 6.67% above nominal or will disable both the PFC and second stage output drivers and reset SS2 if pulled below 1.5V. This input is also used to determine the active range of the second stage PWM.

PKLMT: (PFC peak current limit) The threshold for peak limit is 0V. Use a resistor divider from the negative side of the current sense resistor to VREF to level-shift this signal to a voltage corresponding to the desired overcurrent threshold across the current sense resistor.

PWRGND: Ground for totem pole output drivers.

RT: (oscillator charging current) A resistor from RT to GND is used to program oscillator charging current. A resistor between 10kΩ and 100kΩ is recommended.

SS2: (soft start for PWM) SS2 is at ground for either enable low or OVP/ENBL below the UVLO2 threshold conditions. When enabled, SS2 will charge an external capacitor with a current source. This voltage will be used as the voltage error signal during start-up, enabling the PWM duty cycle to increase slowly. In the event of a disable command or a UVLO2 dropout, SS2 will quickly discharge to disable the PWM.

VAOUT: (voltage amplifier output) This is the output of the opamp that regulates output voltage. The voltage amplifier output is internally limited to approximately 5.5V to prevent overshoot.

VCC: (positive supply voltage) Connect to a stable source of at least 20mA between 12V and 17V for normal operation. Bypass VCC directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate Gate Drive signals, the output devices will be inhibited unless VCC exceeds the upper under-voltage lockout threshold and remains above the lower threshold.

VERR: Voltage amp error signal for the second stage. The error signal is generated by an external amplifier which drives this pin.

VFF: (RMS feed forward signal) VFF signal generated at this pin by mirroring Iac into a single pole external filter.

PIN DESCRIPTIONS

$$R_{VFF} = \frac{VFF_{MAX}}{\sqrt{2} \bullet \frac{IAC_{MAX}}{2} \bullet 0.9}$$

VSENSE: (voltage amplifier inverting input) This is normally connected to a compensation network and to the boost converter output through a divider network.

VREF: (voltage reference output) VREF is the output of an accurate 7.5V voltage reference. This output is capable of delivering 10mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled and will remain at 0V when VCC is below the UVLO threshold. Bypass VREF to GND with a 0.1µF or larger ceramic capacitor for best stability.

APPLICATION INFORMATION

The UCC38500 is designed to incorporate all the control functions required for a power factor correction circuit and a second stage dc-dc converter. The PFC function is implemented as a full feature, average current mode controller Integrated Circuit for excellent performance. In addition, the input voltage feedforward function is implemented in a simplified manner. Current from IAC is mirrored over to the V_{FF} pin. By simply adding a resistor and capacitor (to attenuate 120Hz ripple) a voltage is developed which is proportional to line voltage. This eliminates several components normally connected to the line.

The UCC38500 uses leading edge modulation for the PFC stage and trailing edge modulation for the dc-dc stage. This reduces ripple current in the output capacitor by reducing the overlap in conduction time of the PFC and dc-dc switches. In addition to the reduced ripple current, noise immunity is improved through the current error amplifier implementation.

The UCC38500 is optimized to control a boost PFC stage operating in continuous conduction mode, followed by a dc-dc converter (typically a forward topology). It is usual that the dc-dc converter is transformer isolated and therefore its error amplifier will be located on the secondary side. The UCC38500 is configured without an internal error amplifier. The externally generated error signal is fed into the VERR pin.

The UCC38500 can be configured for voltage mode or current mode control of the second stage. The application figure shows a typical current mode configuration. For voltage mode control the ramp generated by CT is simply fed into the ISENSE2 pin.

One of the main system challenges in designing systems with a PFC front end is coordinating the turn-on and turn-off on the dc-dc converter. If the dc-dc converter is allowed to turn on before the boost converter is operational, it must operate at a much-reduced voltage and therefore can represent a large current draw to the boost converter. This start-up sequencing is handled internally by the UCC38500. The UCC38500 monitors the output voltage of the PFC converter and holds the dc-dc converter off until the output is within 10% of its regulation point. Once the trip point is reached the dc-dc section goes through a soft start sequence for a controlled, low stress start-up. Similarly if the output voltage drops too low (2 voltage options are available) the dc-dc converter shuts down thereby preventing overstress of the converter.

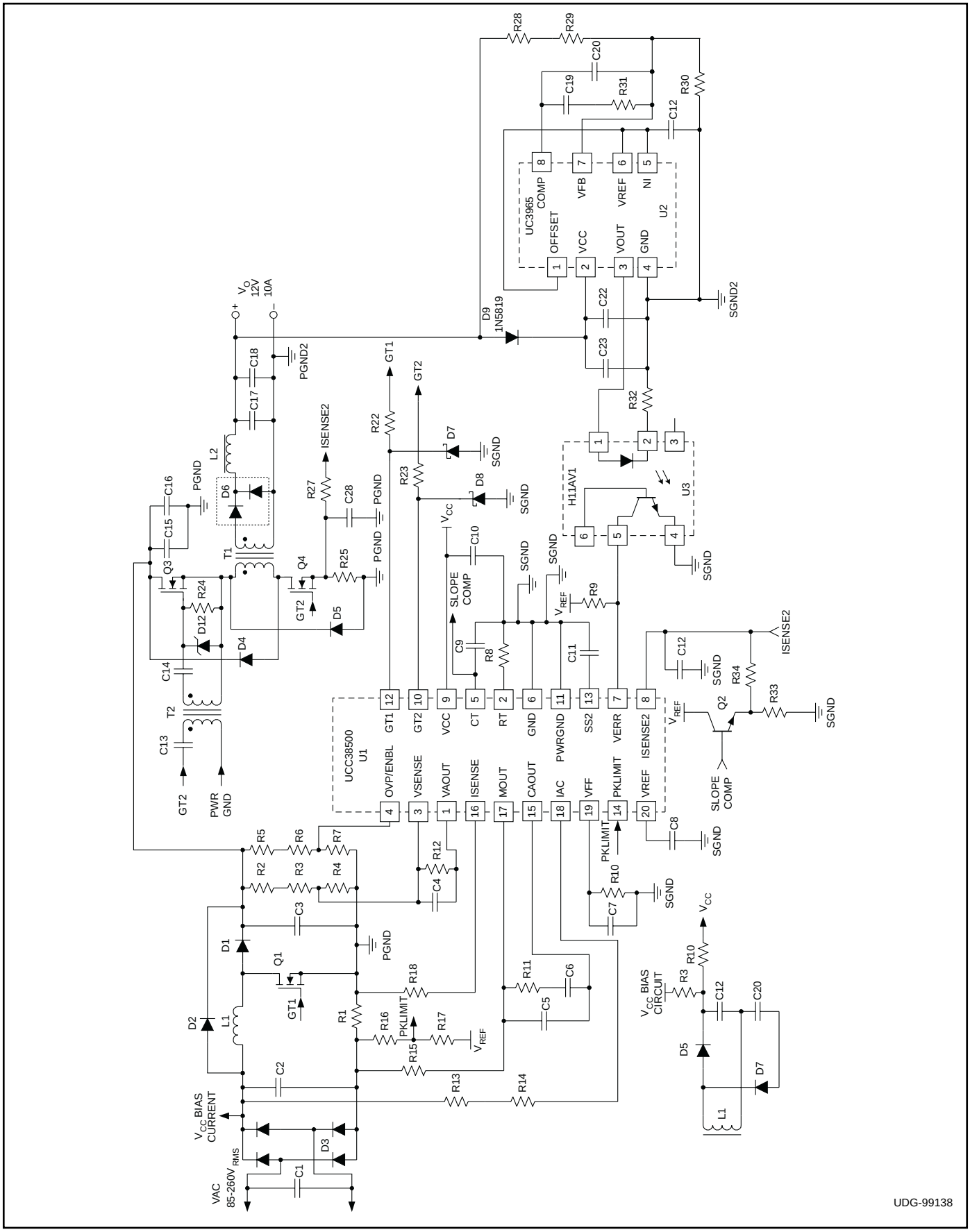
Design details of the PFC section can be found in several references shown below.

- UCC3817 data sheet
- High Power Factor Preregulator for Off-Line Power Supplies, SEM-800
- Optimizing the Design of a High Power Factor Switching Regulator, SEM-800

A design example for a 2 switch forward converter can be found in:

- 250W Off-Line Forward Converter Design Review, SEM-500

TYPICAL APPLICATION CIRCUIT



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