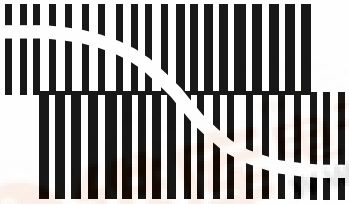
DATA SHEET



UDA1320ATS
Low-cost stereo filter DAC

Preliminary specification
Supersedes data of 1999 Oct 11
File under Integrated Circuits, IC01

2000 Jan 10

Philips Semiconductors

CONTENTS

1 FEATURES

1.1 General

- Low power consumption.
- 2.7 to 3.6 V power supply.
- Selectable control via L3 microcontroller interface or via static pin control.
- 256, 384 and 512f_s system clock (f_{sys}), selectable via the L3 interface or 256 and 384f_s clock mode via static pin control
- supports sampling frequencies from 16kHz to 48kHz.
- Integrated digital filter plus non inverting DAC Digital-to-Analog Converter (DAC).
- Easy application and no analog post filtering required for DAC.
- Slave mode only applications.
- Small package size (SSOP16).

1.2 Multiple format input interface

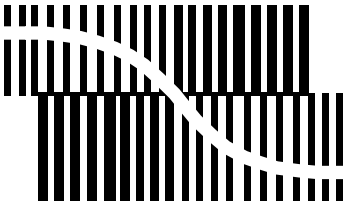
- I^2S-bus, MSB-justified and LSB-justified 16,18 and 20 bits format compatible (in L3-mode).
- I^2S-bus and LSB-justified 16,18 and 20 bits format compatible in static mode.
- 1f_s input format data rate.

1.3 DAC digital sound processing

- Digital logarithmic volume control via L3.
- Digital de-emphasis for 32, 44.1 and 48 kHz f_s via L3 or 44.1 kHz f_s via static pin control.
- Soft mute via static pin control or via L3 interface.

1.4 Advanced audio configuration

- Stereo line output (under L3 volume control)
- High linearity, wide dynamic range, low distortion.



2 APPLICATIONS

- Portable digital audio equipment, see Fig.8.
- Set-top boxes

3 GENERAL DESCRIPTION

The UDA1320ATS/N2 is a single-chip non inverting stereo DAC employing bitstream conversion techniques. The low power consumption and low voltage requirements make the device eminently suitable for use in digital audio equipment which incorporates playback functions.

The UDA1320ATS/N2 supports the I^2S-bus data format with word lengths of up to 20 bits, the MSB-justified data format with word lengths of up to 20 bits and the LSB-justified serial data format with word lengths of 16, 18 and 20 bits.

The UDA1320ATS/N2 can be used in two modes, either L3-mode or static pin mode.

In the L3-mode, all digital sound processing features must be controlled via the L3 interface, including the selection of the system clock setting.

In the two static-modes, the UDA1320ATS/N2 can be operated in the 256f_s and 384f_s system clock mode. The mute, de-emphasis for 44.1 kHz and 4 digital input formats (I^2S and 16, 18, 20 bits LSB formats) can be selected via static pins. The L3 interface cannot be used in this application mode, also, volume control is not available in this mode.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1320ATS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		2.7	3.3	3.6	V
V_{DDD}	digital supply voltage		2.7	3.3	3.6	V
I_{DDA}	DAC supply current		–	6.5	–	mA
I_{DDD}	digital supply current		–	3.0	–	mA
T_{amb}	ambient temperature		–40	–	+85	°C
DAC						
$V_{o(rms)}$	output voltage (RMS value)	note 1, 2	–	1.0	–	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–90	–85	dB
		at –60 dB; A-weighted	–	–38	–35	dB
S/N	signal-to-noise ratio	code = 0; A-weighted	–	100	95	dB
α_{cs}	channel separation		–	100	–	dB
T_{amb}	ambient temperature		–40	–	+85	°C

Notes

1. the output voltage has been changed with respect to the UDA1320TZ/N1.
2. the output voltage scales linearly with the power supply voltage.

6 BLOCK DIAGRAM

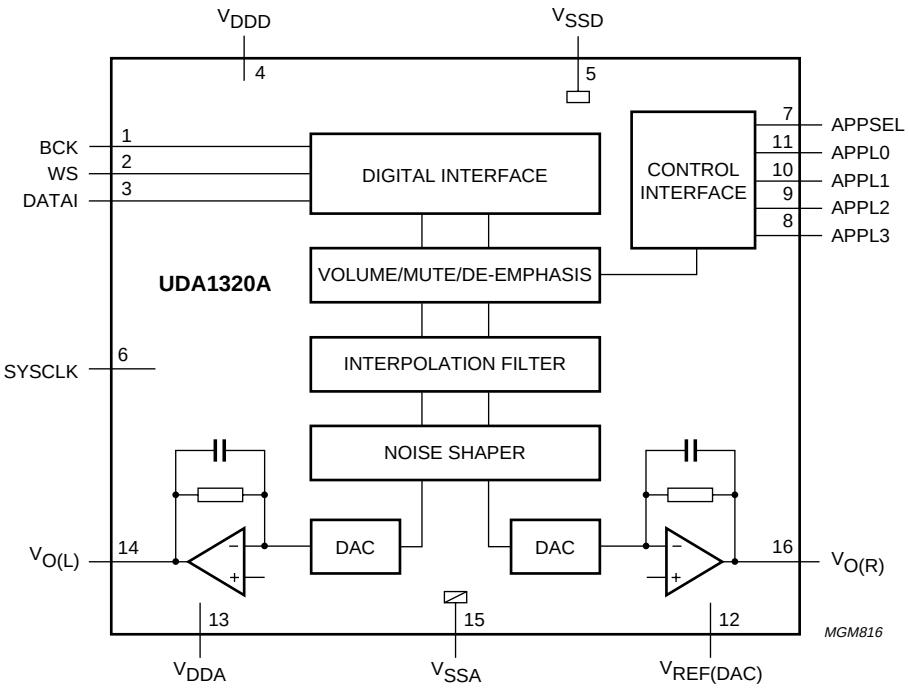


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock
WS	2	word select
DATAI	3	data input
V_{DDD}	4	digital power supply
V_{SSD}	5	digital ground
SYSCLK	6	system clock: $256f_s$, $384f_s$, $512f_s$
APPSEL	7	application mode select
APPL3	8	application pin 3
APPL2	9	application pin 2
APPL1	10	application pin 1
APPL0	11	application pin 0
$V_{REF(DAC)}$	12	DAC reference voltage
V_{DDA}	13	analog supply voltage
$V_{O(L)}$	14	left output voltage
V_{SSA}	15	analog ground
$V_{O(R)}$	16	right output voltage

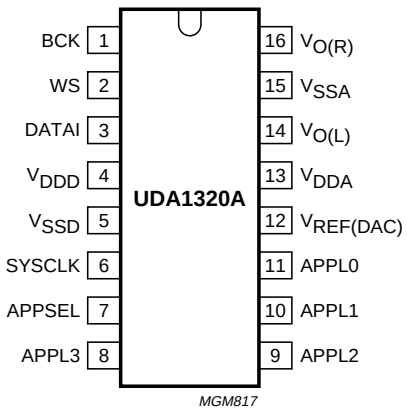


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 System clock

The UDA1320ATS/N2 operates in slave mode only. This means in all applications the system devices must provide the system clock. The system frequency is selectable and depends on the mode of operation.

The options are $256f_s$, $384f_s$ and $512f_s$ for the L3 mode and $256f_s$ plus $384f_s$ for the static mode. The system clock must be locked in frequency to the digital interface input signals.

The UDA1320ATS/N2 supports sampling frequencies from 16kHz up to 48kHz

8.2 Application modes

The application mode can be set with the tri-value APPSEL pin, to L3 mode (APPSEL = V_{SSD}) or to either of two static modes (APPSEL = $0.5V_{DDD}$ or APPSEL = V_{DDD}). See Table 1 for APPL0 to APPL3 pin functions (active = HIGH).

Table 1 Selection modes via APPSEL (note 1)

PIN	APPSEL		
	V_{SSD}	$0.5V_{DDD}$ ($384f_s$)	V_{DDD} ($256f_s$)
APPL0	TEST	MUTE	MUTE
APPL1	L3CLOCK	DEEM	DEEM
APPL2	L3MODE	SF0	SF0
APPL3	L3DATA	SF1	SF1

For example, in static pin control mode, the output signal can be soft muted by setting APPL0 HIGH. De-emphasis can be switched on for 44.1 kHz by setting APPL1 HIGH. APPL1 LOW will disable de-emphasis.

Note that when L3 interface is used, an L3 initialisation must be done when the IC is powered up!

In L3 mode pin APPL0 must be set to LOW.

8.3 Multiple format input interface

L3 mode:

- I^2S-bus with data word length of up to 20 bits
- MSB-justified format with data word length up to 20 bits
- LSB-justified format with data word length of 16, 18 or 20 bits.

8.4 Static pin mode

The UDA1320ATS/N2 supports the following data input name formats in the static pin mode (via SF0 and SF1):

- I^2S bus with data word length of up to 20 bits
- LSB-justified format with data word length of 16, 18 or 20 bits.

See Table 2, for the static pin codes of the 4 formats, selectable via SF0 and SF1.

The UDA1320ATS/N2 also accepts double speed data for double speed data monitoring purposes.

Table 2 Input format selection using SF0 and SF1

FORMAT	SF0	SF1
I^2S	0	0
LSB-justified 16 bits	0	1
LSB-justified 18 bits	1	0
LSB-justified 20 bits	1	1

The formats are illustrated in Fig.3. Left and right data-channel words are time multiplexed. The WS signal must have 50% duty-factor for all LSB-justified modes.

For BCK and WS holds that the BCK frequency must be equal or smaller then 64 times WS, or $f_{BCK} =< 64*f_{WS}$ in both L3 and static mode.

8.5 Pin compatibility

In L3 interface mode the UDA1320ATS/N2 can be used on boards that are designed for the UDA1322. The software for UDA1322 can be used for the UDA1320ATS/N2 to control de-emphasis, volume control and mute and also the status settings like system clock setting and input data format.

IMPORTANT: UDA1320ATS/N2 differs from the UDA1320TZ/N1 with respect to:

- in the static mode 384fs is supported instead of 512fs.
- the output voltage of the DAC. In the UDA1320TZ/N1 this is 800mVrms at 3.0V, now it is 1Vrms at 3.3V power supply

8.6 Interpolation filter (DAC)

The digital filter interpolates from 1 to $128f_s$ by cascading a recursive filter and a FIR filter, see Table 3.

Table 3 Interpolation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	0 to $0.45f_s$	±0.1
Stop band	$>0.55f_s$	−50
Dynamic range	0 to $0.45f_s$	108

8.7 Noise shaper

The 3rd-order noise shaper operates at $128f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter-Stream DAC (FSDAC).

8.8 Filter-Stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to be analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales linearly with the power supply voltage.

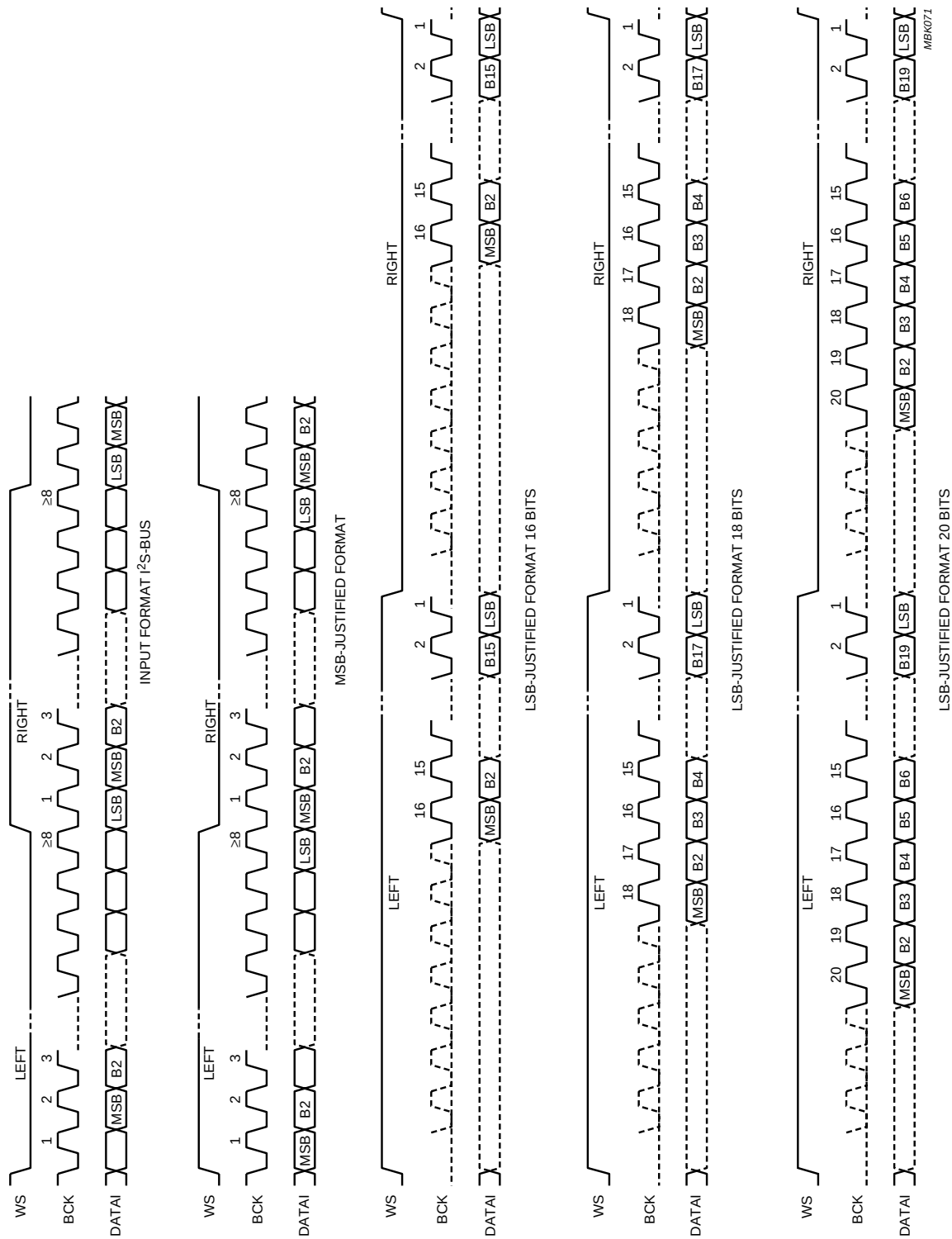


Fig.3 Serial interface; input format I²S-bus.

9 L3 INTERFACE DESCRIPTION

9.1 The L3 interface

The following system and digital sound processing features can be controlled in the microcontroller mode of the UDA1320ATS/N2:

- System clock frequency
- Data input format
- De-emphasis for 32 kHz, 44.1 kHz and 48 kHz
- Volume
- Soft mute.

The exchange of data and control information between the microcontroller and the UDA1320ATS/N2 is accomplished through a serial hardware interface comprising the following pins:

- L3DATA
- L3MODE
- L3CLOCK.

Information transfer through the microcontroller bus is organized in accordance with the L3 format, in which two different modes of operation can be distinguished; address mode and data transfer mode (see Figs 4 and 6).

The address mode is required to select a device communicating via the L3 bus and to define the destination registers for the data transfer mode.

Data transfer can only be in one direction, consisting of input to the UDA1320ATS/N2 to program sound processing and other functional features.

Data bits 7 to 2 represent a 6-bit device address, bit 7 being the MSB. The address of the UDA1320ATS/N2 is 000101 (bit 7 to bit 2). If the UDA1320ATS/N2 receives a different address, it will deselect its microcontroller interface logic.

9.2 Data transfer mode

The selected address remains active during subsequent data transfers until the UDA1320ATS/N2 receives a new address command. The fundamental timing of data transfers is essentially the same as in the address mode, see Fig.6. The maximum input clock and data rate is 64 f_s. All transfers are by 8-bit bytes. Data will be stored in the UDA1320ATS/N2 after reception of a complete byte. See Fig.5 for a multi-byte transfer.

Table 4 Selection of data transfer

BIT 1	BIT 0	TRANSFER
0	0	DATA (volume, de-emphasis, mute)
0	1	not used
1	0	STATUS (system clock frequency, data input format)
1	1	not used

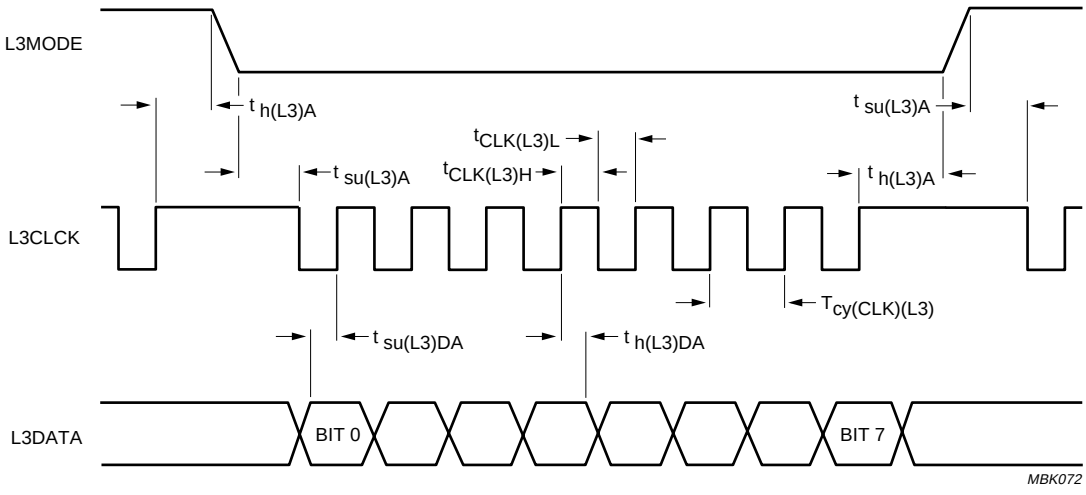


Fig.4 Timing address mode.

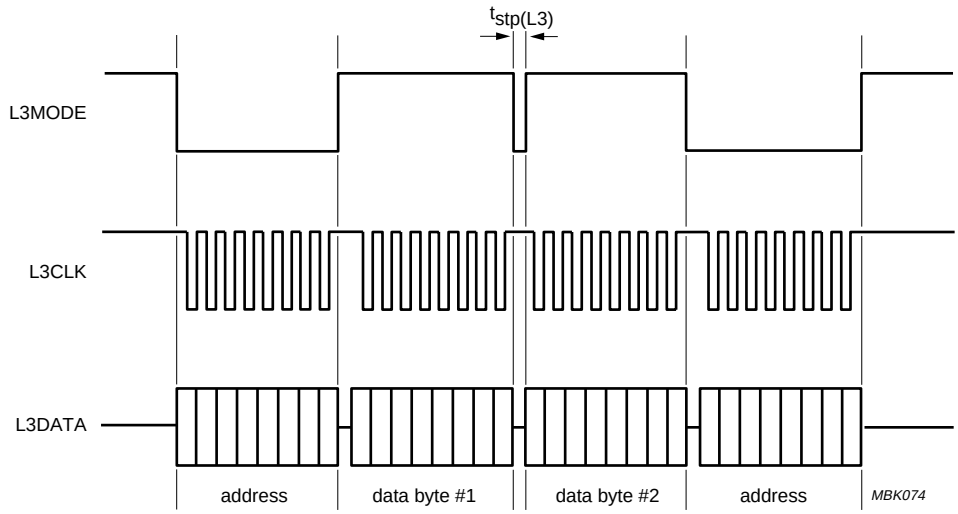


Fig.5 Multi-byte transfer.

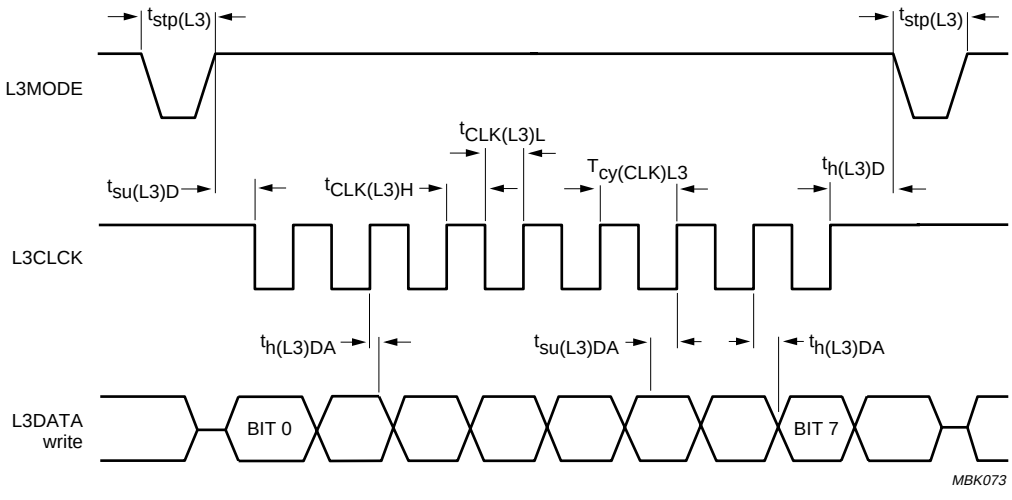


Fig.6 Timing for data transfer mode.

The sound feature values are stored in independent registers. The first selection of the registers is achieved by the choice of data type that is transferred (‘STATUS’ or ‘DATA’ transfer). This is performed in the address mode using bit 1 and bit 0, see Table 4,. The settings that can be controlled with ‘STATUS’ transfer are given in table 5, and the settings that can be controlled using ‘DATA’ transfer are given in table 6.

The second selection is performed by the 2 MSBs of the data byte (bit 7 and bit 6). The other bits in the data byte (bit 5 to bit 0) is the value that is placed in the selected registers.

Table 5 Data transfer of type ‘status’

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	0	SC1	SC0	IF2	IF1	IF0	0	System Clock frequency (1 : 0); data Input Format (2 : 0)
1	0	0	0	0	0	0	0	reserved

Table 6 Data transfer of type ‘data’

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	0	VC5	VC4	VC3	VC2	VC1	VC0	Volume Control (5 : 0)
0	1	0	0	0	0	0	0	reserved
1	0	0	DE1	DE0	MT	0	0	DE-emphasis (1 : 0); MuTe
1	1	0	0	0	0	0	1	default setting

9.3 Programming the features

When the data transfer of type ‘STATUS’ is selected, the features SYSTEM CLOCK FREQUENCY and DATA INPUT FORMAT can be controlled.

System clock frequency: a 2-bit value to select the used external clock frequency.

Table 7 System clock settings

SC1	SC0	FUNCTION
0	0	$512f_s$
0	1	$384f_s$
1	0	$256f_s$
1	1	not used

Data input format: a 3-bit value to select the data format.

Table 8 Data input format settings

IF2	IF1	IF0	FUNCTION
0	0	0	I^2S bus
0	0	1	LSB-justified, 16 bits
0	1	0	LSB -justified, 18 bits
0	1	1	LSB-justified, 20 bits
1	0	0	MSB-justified
1	0	1	not used
1	1	0	not used
1	1	1	not used

When the data transfer of type ‘DATA’ is selected, the features VOLUME, DE-EMPHASIS and MUTE can be controlled.

Volume control: a 6-bit value to program the volume attenuation (VC5 to VC0), 0 to −∞ dB in steps of 1 dB.

Table 9 Volume settings

VC5	VC4	VC3	VC2	VC1	VC0	VOLUME (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	−1
0	0	0	0	1	1	−2
:	:	:	:	:	:	:
1	1	1	1	0	1	−60
1	1	1	1	1	1	−∞

De-emphasis: a 2-bit value to enable the digital de-emphasis filter.

Table 10 De-emphasis settings

DE1	DE0	FUNCTION
0	0	no de-emphasis
0	1	de-emphasis, 32 kHz
1	0	de-emphasis, 44.1 kHz
1	1	de-emphasis, 48 kHz

Mute: a 1-bit value to enable the digital mute.

Table 11 Mute setting

MT	FUNCTION
0	no muting
1	muting

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	–	5.0	V
V_{DDA}	analog supply voltage	note 1	–	5.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		−65	+125	°C
T_{amb}	ambient temperature		−40	+85	°C
V_{es}	electrostatic handling	note 2	−3000	+3000	V
		note 3	−300	+300	V

Notes

1. All supply connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor, except pin 14 which must be specified to −2500V (MIN) and +2500V (MAX).
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

12 QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611-E”*. The number of the quality specification can be found in the *“Quality Reference Handbook”*. The handbook can be ordered using the code 9397 750 00192.

13 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	190	K/W

14 DC CHARACTERISTICS

V_{DDD} = V_{DDA} = 3.3 V; T_{amb} = 25 °C; R_L = 5 kΩ. All voltages referenced to ground (pins 5 and 15) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
Supply						
V_{DDA}	DAC analog supply voltage	note 1	2.7	3.3	3.6	V
V_{DDD}	digital supply voltage	note 1	2.7	3.3	3.6	V
I_{DDA}	analog supply current	operation mode	–	6.5	–	mA
I_{DDD}	digital supply current	operation mode	–	3.0	–	mA
Digital input pins						
V_{IH}	HIGH-level input voltage		$0.8V_{DDD}$	–	–	V
V_{IL}	LOW-level input voltage		–	–	$0.2V_{DDD}$	V
$\lvert I_{LI} \rvert$	input leakage current		–	–	1	μA
C_i	input capacitance		–	–	10	pF
V_{IH}	HIGH-level input voltage		–	–	V_{DDD} + 0.5	V
V_{IL}	LOW-level input voltage		–0.5	–	–	V
DAC						
V_{ref}	reference voltage	with respect to V_{SSA}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$I_{o(max)}$	maximum output current	(THD + N)/S < 0.1% R_L = 5 kΩ	–	0.22	–	mA
R_{out}	output resistance		–	0.15	2.0	Ω
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance	note 2	–	–	50	pF

Notes

1. All supply connections must be made to the same external power supply unit.
2. When the DAC drives a capacitive load above 50 pF, a series resistance of 100 Ω must be used to prevent oscillations in the output operational amplifier.

15 AC CHARACTERISTICS

15.1 Analog

$V_{DDD} = V_{DDA} = 3.3$ V; $f_i = 1$ kHz; $T_{amb} = 25$ °C; $R_L = 5$ kΩ. All voltages referenced to ground (pins 5 and 15) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DAC						
$V_{o(rms)}$	output voltage (RMS value)		–	1.0	–	V
ΔV_o	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–90	–85	dB
		at –60 dB; A-weighted	–	–38	-35	dB
S/N	signal-to-noise ratio	code = 0; A-weighted	–	100	95	dB
α_{cs}	channel separation		–	100	–	dB
PSRR	power supply ripple rejection ratio	f_{ripple} = 1 kHz; $V_{ripple(p-p)}$ = 100 mV	–	50	–	dB

15.2 Digital

V_{DDD} = V_{DDA} = 2.7 to 3.6 V; T_{amb} = −20 to +85 °C; R_L = 5 kΩ. All voltages referenced to ground (pins 5 and 15); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{sys}	system clock cycle	$f_{sys} = 256f_s$	78	88	244	ns
		$f_{sys} = 384f_s$	52	59	162	ns
		$f_{sys} = 512f_s$	39	44	122	ns
t_{CWL}	LOW-level system clock pulse width	f_{sys} < 19.2 MHz	30	–	70	$\%T_{sys}$
		$f_{sys} \geq$ 19.2 MHz	40	–	60	$\%T_{sys}$
t_{CWH}	HIGH-level system clock pulse width	f_{sys} < 19.2 MHz	30	–	70	$\%T_{sys}$
		$f_{sys} \geq$ 19.2 MHz	40	–	60	$\%T_{sys}$
Serial input data timing (see Fig.7)						
$T_{cy(CLK)(bit)}$	bit clock period		300	–	–	ns
$t_{CLKH(bit)}$	bit clock HIGH time		100	–	–	ns
$t_{CLKL(bit)}$	bit clock LOW time		100	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{su(i)(D)}$	data input set-up time		20	–	–	ns
$t_{h(i)(D)}$	data input hold time		0	–	–	ns
$t_{su(WS)}$	word selection set-up time		20	–	–	ns
$t_{h(WS)}$	word selection hold time		10	–	–	ns
Microcontroller interface timing (see Figs 4 and 6)						
$T_{cy(CLK)(L3)}$	L3CLK		500	–	–	ns
$t_{CLK(L3)H}$	L3CLK HIGH period		250	–	–	ns
$t_{CLK(L3)L}$	L3CLK LOW period		250	–	–	ns
$t_{su(L3)A}$	L3MODE set-up time	addressing mode	190	–	–	ns
$t_{h(L3)A}$	L3MODE hold time	addressing mode	190	–	–	ns
$t_{su(L3)D}$	L3MODE set-up time	data transfer mode	190	–	–	ns
$t_{h(L3)D}$	L3MODE hold time	data transfer mode	190	–	–	ns
$t_{su(L3)DA}$	L3DATA set-up time	data transfer and addressing mode	190	–	–	ns
$t_{h(L3)DA}$	L3DATA hold time	data transfer and addressing mode	30	–	–	ns
$t_{stp(L3)}$	L3MODE halt time		190	–	–	ns

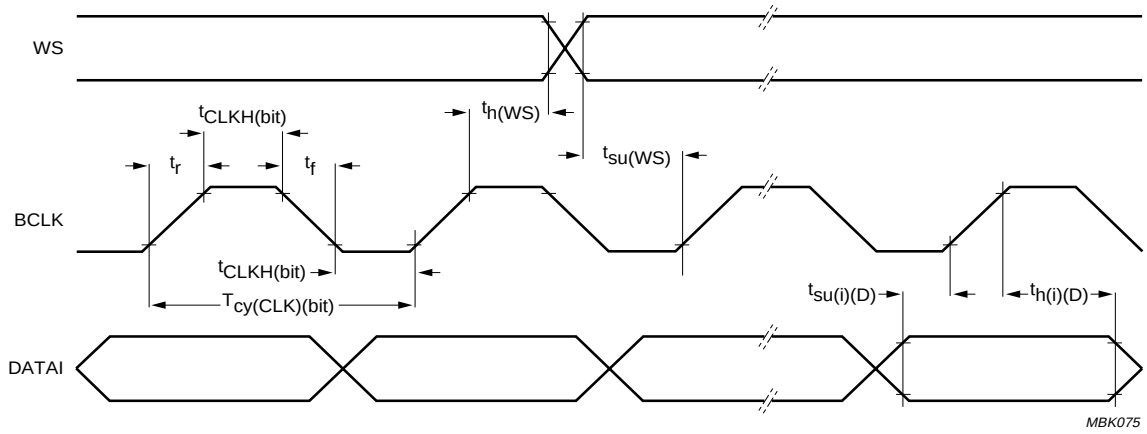


Fig.7 Serial interface timing.

16 APPLICATION INFORMATION

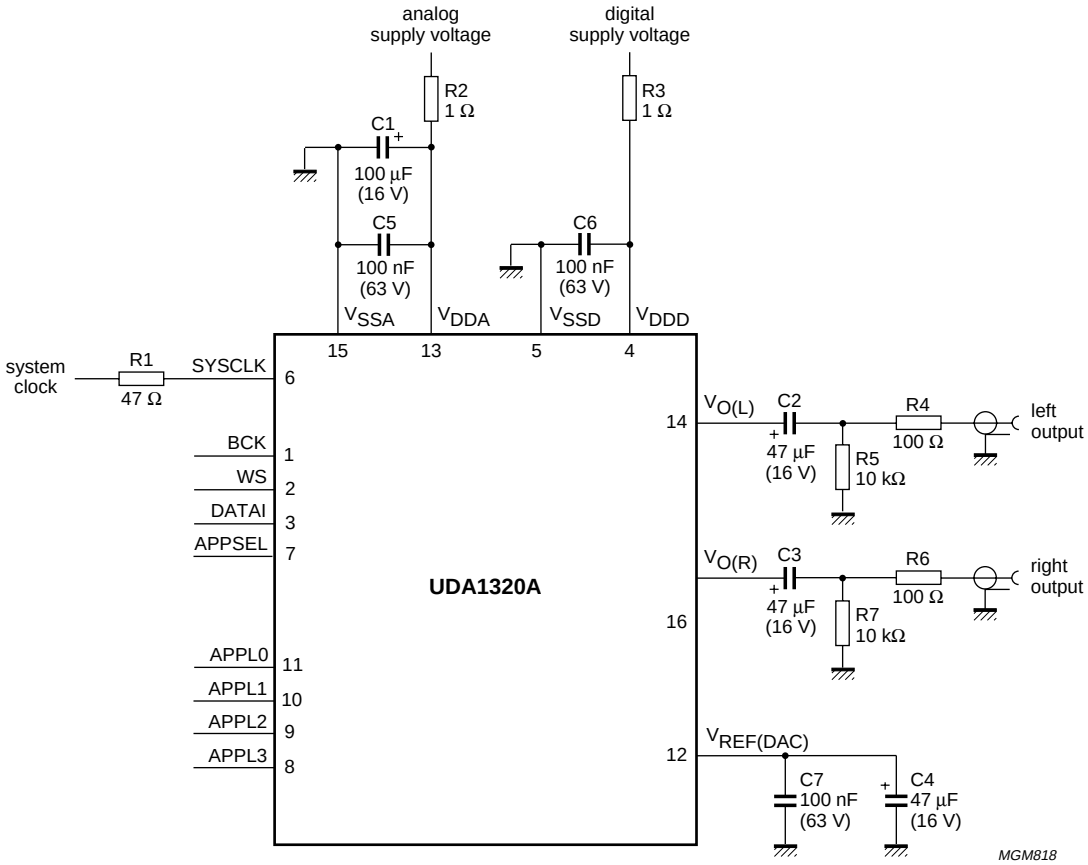
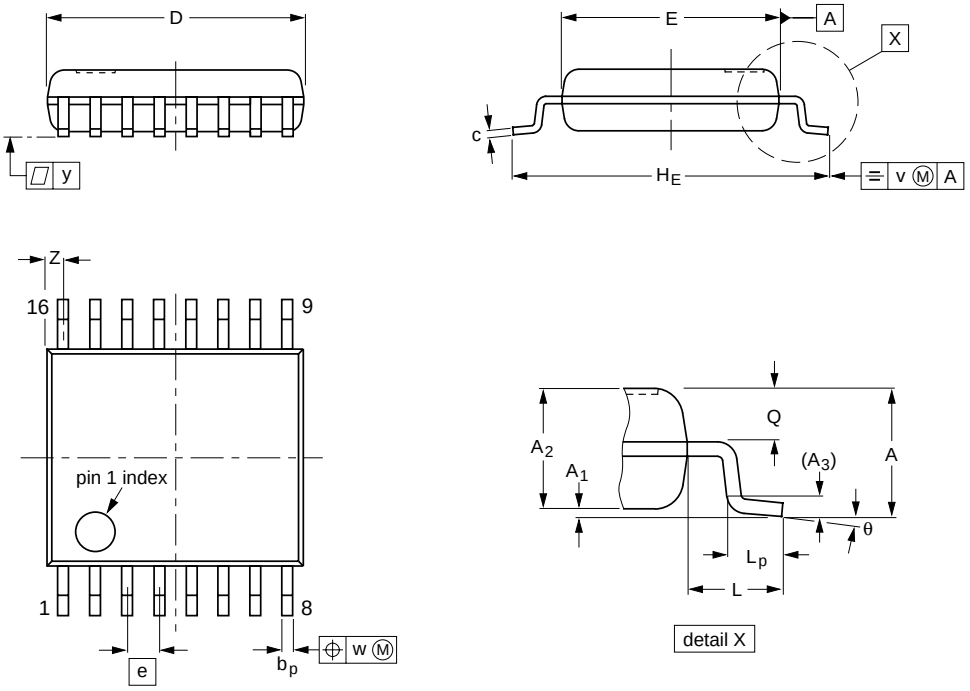
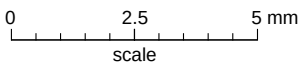


Fig.8 Application schematic.

17 PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm **SOT369-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1		MO-152				~~95-02-04~~ 99-12-27

18 SOLDERING

18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

18.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

19 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

20 LIFE SUPPORT APPLICATIONS

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