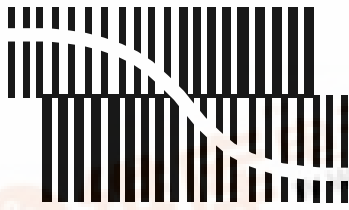


**INTEGRATED CIRCUITS**

# DATA SHEET



BITSTREAM CONVERSION

## **UDA1334TS** Low power audio DAC

Preliminary specification  
File under Integrated Circuits, IC01

1999 Nov 11

**Low power audio DAC****UDA1334TS****CONTENTS**

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# Low power audio DAC

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## 1 FEATURES

### 1.1 General

- 1.8 to 3.6 V power supply voltage
- Integrated digital filter plus DAC
- Supports sample frequencies from 8 to 100 kHz
- Automatic system clock versus sample rate detection
- Low power consumption
- No analog post filtering required for DAC
- Slave mode only applications
- Easy application
- SSOP16 package.

### 1.2 Multiple format data interface

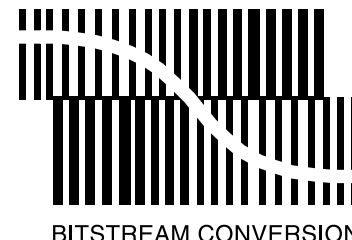
- I<sup>2</sup>S-bus and LSB-justified format compatible
- 1f<sub>s</sub> input data rate.

### 1.3 DAC digital sound processing

- Digital de-emphasis for 44.1 kHz sampling rate
- Mute function.

### 1.4 Advanced audio configuration

- High linearity, wide dynamic range and low distortion
- Standby or Sleep mode in which the DAC is powered down.



## 2 APPLICATIONS

This audio DAC is excellently suitable for digital audio portable application, such as portable MD, MP3 and DVD players.

## 3 GENERAL DESCRIPTION

The UDA1334TS supports the I<sup>2</sup>S-bus data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 20 and 24 bits.

The UDA1334TS has basic features such as de-emphasis (at 44.1 kHz sampling rate) and mute.

## 4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1334TS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

## Low power audio DAC

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## 5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_{DDA}$	DAC analog supply voltage		1.8	2.0	3.6	V
$V_{DDD}$	digital supply voltage		1.8	2.0	3.6	V
$I_{DDA}$	DAC analog supply current	normal operation	–	2.1	–	mA
		Sleep mode	–	150	–	$\mu$ A
$I_{DDD}$	digital supply current	normal operation	–	1.2	–	mA
		Sleep mode	–	50	–	$\mu$ A
$T_{amb}$	ambient temperature		–20	–	+85	$^{\circ}$ C
<b>Digital-to-analog convertor (<math>V_{DDA} = V_{DDD} = 2.0</math> V)</b>						
$V_{o(rms)}$	output voltage (RMS value)	at 0 dB (FS) digital input; note 1	–	500	–	mV
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	$f_s = 44.1$ kHz; at 0 dB	–	–80	–	dB
		$f_s = 44.1$ kHz; at –60 dB; A-weighted	–	–37	–	dB
		$f_s = 96$ kHz; at 0 dB	–	–75	–	dB
		$f_s = 96$ kHz; at –60 dB; A-weighted	–	–35	–	dB
S/N	signal-to-noise ratio	$f_s = 44.1$ kHz; code = 0; A-weighted	–	97	–	dB
		$f_s = 96$ kHz; code = 0; A-weighted	–	95	–	dB
		MUTE = HIGH; A-weighted	–	110	–	dB
$\alpha_{cs}$	channel separation		–	100	–	dB
<b>Digital-to-analog convertor (<math>V_{DDA} = V_{DDD} = 3.0</math> V)</b>						
$V_{o(rms)}$	output voltage (RMS value)	at 0 dB (FS) digital input; note 1	–	750	–	mV
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	$f_s = 44.1$ kHz; at 0 dB	–	–90	–	dB
		$f_s = 44.1$ kHz; at –60 dB; A-weighted	–	–40	–	dB
		$f_s = 96$ kHz; at 0 dB	–	–85	–	dB
		$f_s = 96$ kHz; at –60 dB; A-weighted	–	–37	–	dB
S/N	signal-to-noise ratio	$f_s = 44.1$ kHz; code = 0; A-weighted	–	100	–	dB
		$f_s = 96$ kHz; code = 0; A-weighted	–	98	–	dB
		MUTE = HIGH; A-weighted	–	110	–	dB
$\alpha_{cs}$	channel separation		–	100	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Power dissipation (at <math>f_s = 44.1</math> kHz)</b>						
P	power dissipation	play-back mode; at 2.0 V supply voltage	–	7.0	–	mW
		play-back mode; at 3.0 V supply voltage	–	17	–	mW
		Sleep mode	–	0.5	–	mW

**Note**

1. The DAC output voltage scales proportional to the power supply voltage.

**6 BLOCK DIAGRAM**

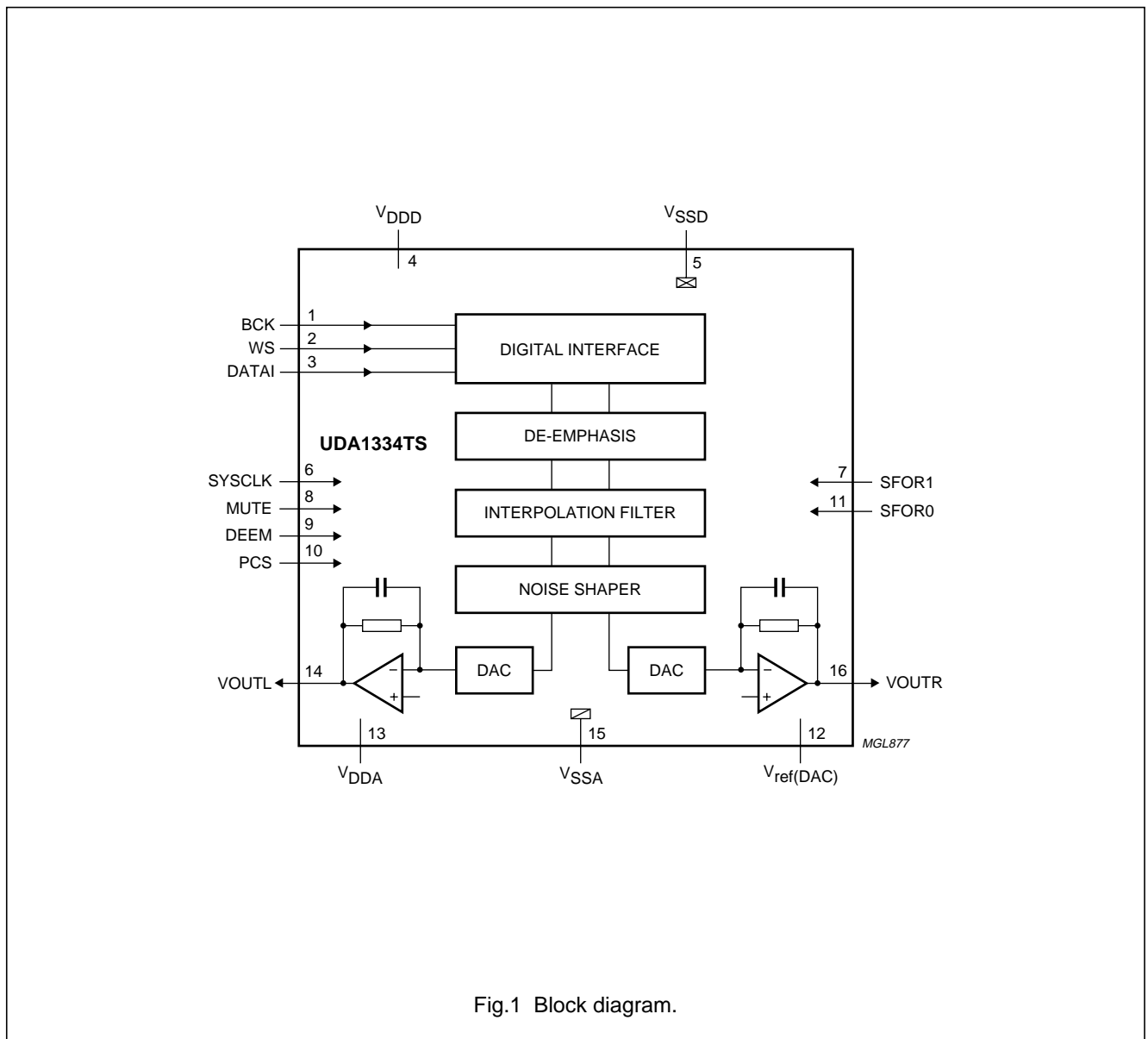


Fig.1 Block diagram.

## Low power audio DAC

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## 7 PINNING

SYMBOL	PIN	PAD TYPE	DESCRIPTION
BCK	1	5 V tolerant digital input pad; note 1	bit clock input
WS	2	5 V tolerant digital input pad; note 1	word select input
DATAI	3	5 V tolerant digital input pad; note 1	serial data input
V <sub>DDD</sub>	4	digital supply pad	digital supply voltage
V <sub>SSD</sub>	5	digital ground pad	digital ground
SYSCLK	6	5 V tolerant digital input pad; note 1	system clock input
SFOR1	7	5 V tolerant digital input pad; note 1	serial format select 1
MUTE	8	5 V tolerant digital input pad; note 1	mute control
DEEM	9	5 V tolerant digital input pad; note 1	de-emphasis control
PCS	10	3-level input pad; note 2	power control and sampling frequency select
SFOR0	11	digital input pad; note 2	serial format select 0
V <sub>ref(DAC)</sub>	12	analog pad	DAC reference voltage
V <sub>DDA</sub>	13	analog supply pad	DAC analog supply voltage
VOUTL	14	analog output pad	DAC output left
V <sub>SSA</sub>	15	analog ground pad	DAC analog ground
VOUTR	16	analog output pad	DAC output right

## Notes

- 5 V tolerant is only supported if the power supply voltage is between 2.7 and 3.6 V. For lower power supply voltages this is maximum 3.3 V tolerant.
- Because of test issues these pads are not 5 V tolerant and they should be at power supply voltage level or at a maximum of 0.5 V above that level.

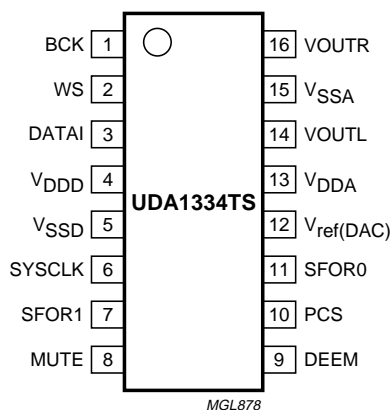


Fig.2 Pin configuration.

## Low power audio DAC

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## 8 FUNCTIONAL DESCRIPTION

## 8.1 System clock

The UDA1334TS operates in slave mode only; this means that in all applications the system must provide the system clock and the digital audio interface signals (BCK and WS).

The system clock must be locked in frequency to the digital interface signals.

The UDA1334TS automatically detects the ratio between the SYSCLK and WS frequencies.

The BCK clock can be up to  $64f_s$ , or in other words the BCK frequency is 64 times the Word Select (WS) frequency or less:  $f_{BCK} \leq 64 \times f_{WS}$ .

**Important:** the WS edge MUST fall on the negative edge of the BCK at all times for proper operation of the digital I/O data interface.

The modes which are supported are given in Table 1.

**Table 1** Supported sampling ranges

CLOCK MODE	SAMPLING RANGE
$768f_s$	8 to 55 kHz
$512f_s$	8 to 100 kHz
$384f_s$	8 to 100 kHz
$256f_s$	8 to 100 kHz
$192f_s$	8 to 100 kHz <sup>(1)(2)</sup>
$128f_s$	8 to 100 kHz <sup>(2)</sup>

## Notes

1. This mode can only be supported for power supply voltages down to 2.4 V. For lower voltages, in  $192f_s$  mode the sampling frequency should be limited to 55 kHz.
2. Not supported in low-sampling frequency mode.

An example is given in Table 2 for a 12.228 MHz system clock input.

**Table 2** Example using a 12.228 MHz system clock

SAMPLING FREQUENCY	CLOCK MODE
96 kHz	$128f_s$
64 kHz <sup>(1)</sup>	$192f_s$
48 kHz	$256f_s$
32 kHz	$384f_s$
24 kHz	$512f_s$
16 kHz	$768f_s$

## Note

1. This mode can only be supported for power supply voltages down to 2.4 V. For lower voltages, in  $192f_s$  mode the sampling frequency should be limited to 55 kHz.

## 8.2 Interpolation filter

The interpolation digital filter interpolates from  $1f_s$  to  $64f_s$  by cascading FIR filters (see Table 3).

**Table 3** Interpolation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	0 to $0.45f_s$	$\pm 0.02$
Stop band	$>0.55f_s$	-50
Dynamic range	0 to $0.45f_s$	$>114$

## 8.3 Noise shaper

The 5th-order noise shaper operates at  $64f_s$ . It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using an Filter Stream DAC (FSDAC).

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### 8.4 Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. No post-filter is needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportional with the power supply voltage.

### 8.5 Feature settings

The features of the UDA1334TS can be set by control pins SFOR1, SFOR0, MUTE, DEEM and PCS.

#### 8.5.1 DIGITAL INTERFACE FORMAT SELECT

The digital audio interface formats (see Fig.3) can be selected via the pins SFOR1 and SFOR0 as shown in Table 4.

The BCK frequency for the digital audio interface can be maximum 64 times the WS frequency:  $f_{BCK} \leq 64f_{WS}$ .

**Table 4** Data format selection

SFOR1	SFOR0	INPUT FORMAT
LOW	LOW	I <sup>2</sup> S-bus input
LOW	HIGH	LSB-justified 16 bits input
HIGH	LOW	LSB-justified 20 bits input
HIGH	HIGH	LSB-justified 24 bits input

#### 8.5.2 MUTE CONTROL

The output signal can be soft muted by setting pin MUTE to HIGH level as shown in Table 5.

**Table 5** Mute control

MUTE	FUNCTION
LOW	mute off
HIGH	mute on

When the output signal is fully muted (pin MUTE at HIGH level), a silence switch inside the FSDAC is activated. In this way a very high signal-to-noise ratio can be achieved in case the output is muted.

#### 8.5.3 DE-EMPHASIS CONTROL

De-emphasis can be switched on for  $f_s = 44.1$  kHz by setting pin DEEM at HIGH level. The function description of pin DEEM is given in Table 6.

**Table 6** De-emphasis control

DEEM	FUNCTION
LOW	de-emphasis off
HIGH	de-emphasis on

#### 8.5.4 POWER CONTROL AND SAMPLING FREQUENCY SELECT

Pin PCS is a 3-level pin and is used to set the mode of the UDA1334TS. The definition is given in Table 7.

**Table 7** PCS function definition

PCS	FUNCTION
LOW	normal operating mode
MID	low sampling frequency mode
HIGH	Power-down or Sleep mode

The low sampling frequency mode is required to have a higher oversampling rate in the noise shaper in order to improve the signal-to-noise ratio. In this mode the oversampling ratio of the noise shaper will be  $128f_s$  instead of  $64f_s$ .



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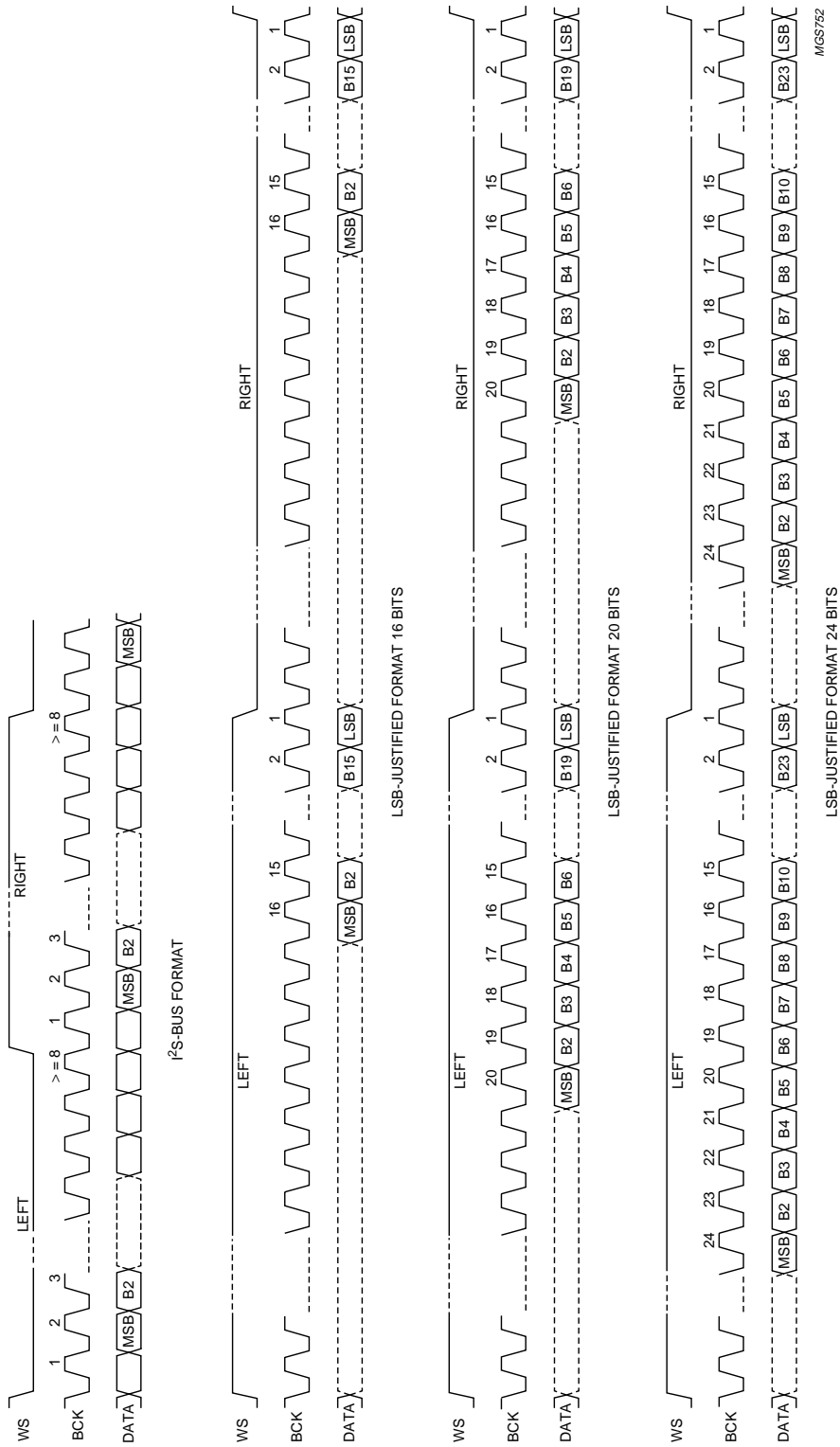


Fig.3 Digital audio formats.

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**9 LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DD}$	supply voltage	note 1	–	4.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
$T_{stg}$	storage temperature		–65	+125	°C
$T_{amb}$	ambient temperature		–20	+85	°C
$V_{es}$	electrostatic handling voltage	human body model	–2000	+2000	V
		machine model	–200	+200	V

**Note**

- All supply connections must be made to the same power supply.

**10 HANDLING**

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices.

**11 THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	145	K/W

**12 QUALITY SPECIFICATION**

In accordance with “SNW-FQ-611-E”.

**13 DC CHARACTERISTICS**

$V_{DDD} = V_{DDA} = 2.0$  V;  $T_{amb} = 25$  °C;  $R_L = 5$  k $\Omega$ . All voltages with respect to ground (pins  $V_{SSA}$  and  $V_{SSD}$ ); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_{DDA}$	DAC analog supply voltage	note 1	1.8	2.0	3.6	V
$V_{DDD}$	digital supply voltage	note 1	1.8	2.0	3.6	V
$I_{DDA}$	DAC analog supply current	normal operating mode; at 2.0 V supply voltage	–	2.1	–	mA
		normal operating mode; at 3.0 V supply voltage	–	3.3	–	mA
		Sleep mode	–	150	–	$\mu$ A
$I_{DDD}$	digital supply current	normal operating mode; at 2.0 V supply voltage	–	1.2	–	mA
		normal operating mode; at 3.0 V supply voltage	–	2.1	–	mA
		Sleep mode	–	50	–	$\mu$ A

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Digital input pins; note 2</b>						
V <sub>IH</sub>	HIGH-level input voltage	at 2.0 V supply voltage	1.3	–	3.3	V
		at 3.0 V supply voltage	2.0	–	5.0	V
V <sub>IL</sub>	LOW-level input voltage	at 2.0 V supply voltage	–0.5	–	+0.5	V
		at 3.0 V supply voltage	–0.5	–	+0.8	V
I <sub>LI</sub>	input leakage current		–	–	1	μA
C <sub>i</sub>	input capacitance		–	–	10	pF
<b>3-level input: pin PCS</b>						
V <sub>IH</sub>	HIGH-level input voltage		0.9V <sub>DDD</sub>	–	V <sub>DDD</sub>	V
V <sub>IM</sub>	MID-level input voltage		0.4V <sub>DDD</sub>	–	0.6V <sub>DDD</sub>	V
V <sub>IL</sub>	LOW-level input voltage		0	–	0.5	V
<b>DAC</b>						
V <sub>ref(DAC)</sub>	reference voltage	with respect to V <sub>SSA</sub>	0.45V <sub>DD</sub>	0.5V <sub>DD</sub>	0.55V <sub>DD</sub>	V
R <sub>O(ref)</sub>	V <sub>ref(DAC)</sub> reference output resistance		–	12.5	–	kΩ
I <sub>o(max)</sub>	maximum output current	(THD + N)/S < 0.1%; R <sub>L</sub> = 800 Ω	–	tbf	–	mA
R <sub>L</sub>	load resistance		3	–	–	kΩ
C <sub>L</sub>	load capacitance	note 3	–	–	50	pF

**Notes**

- All supply connections must be made to the same external power supply unit.
- At 3 V supply voltage, the input pads are TTL compatible. However, at 2.0 V supply voltage no TTL levels can be accepted, but levels from 3.3 V domain can be applied to the pins.
- When the DAC drives a capacitive load above 50 pF, a series resistance of 100 Ω must be used to prevent oscillations in the output operational amplifier.

**14 AC CHARACTERISTICS****14.1 2.0 V supply voltage**

V<sub>DDD</sub> = V<sub>DDA</sub> = 2.0 V; f<sub>i</sub> = 1 kHz; T<sub>amb</sub> = 25 °C; R<sub>L</sub> = 5 kΩ. All voltages with respect to ground (pins V<sub>SSA</sub> and V<sub>SSD</sub>); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>DAC</b>						
V <sub>o(rms)</sub>	output voltage (RMS value)	at 0 dB (FS) digital input	–	0.5	–	V
ΔV <sub>o</sub>	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f <sub>s</sub> = 44.1 kHz; at 0 dB	–	–80	–	dB
		f <sub>s</sub> = 44.1 kHz; at –60 dB; A-weighted	–	–37	–	dB
		f <sub>s</sub> = 96 kHz; at 0 dB	–	–75	–	dB
		f <sub>s</sub> = 96 kHz; at –60 dB; A-weighted	–	–35	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio	$f_s = 44.1$ kHz; code = 0; A-weighted	–	97	–	dB
		$f_s = 96$ kHz; code = 0; A-weighted	–	95	–	dB
		MUTE = HIGH; A-weighted	–	110	–	dB
$\alpha_{cs}$	channel separation		–	100	–	dB
PSRR	power supply rejection ratio	$f_{ripple} = 1$ kHz; $V_{ripple} = 30$ mV (p-p)	–	60	–	dB

**14.2 3.0 V supply voltage**

$V_{DD} = V_{DDA} = 3.0$  V;  $f_i = 1$  kHz;  $T_{amb} = 25$  °C;  $R_L = 5$  k $\Omega$ . All voltages with respect to ground (pins  $V_{SSA}$  and  $V_{SSD}$ ); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>DAC</b>						
$V_{o(rms)}$	output voltage (RMS value)	at 0 dB (FS) digital input	–	0.75	–	V
$\Delta V_o$	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	$f_s = 44.1$ kHz; at 0 dB	–	–90	–	dB
		$f_s = 44.1$ kHz; at –60 dB; A-weighted	–	–40	–	dB
		$f_s = 96$ kHz; at 0 dB	–	–85	–	dB
		$f_s = 96$ kHz; at –60 dB; A-weighted	–	–37	–	dB
S/N	signal-to-noise ratio	$f_s = 44.1$ kHz; code = 0; A-weighted	–	100	–	dB
		$f_s = 96$ kHz; code = 0; A-weighted	–	98	–	dB
		MUTE = HIGH; A-weighted	–	110	–	dB
$\alpha_{cs}$	channel separation		–	100	–	dB
PSRR	power supply rejection ratio	$f_{ripple} = 1$ kHz; $V_{ripple} = 30$ mV (p-p)	–	60	–	dB

**14.3 Timing**

$V_{DD} = V_{DDA} = 1.8$  to  $3.6$  V;  $T_{amb} = -20$  to  $+85$  °C;  $R_L = 5$  k $\Omega$ . The typical timing is specified at  $f_s = 44.1$  kHz (sampling frequency). All voltages with respect to ground (pins  $V_{SSA}$  and  $V_{SSD}$ ); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>System clock timing (see Fig.4)</b>						
$T_{sys}$	system clock cycle time	$f_{sys} = 256f_s$	35	88	780	ns
		$f_{sys} = 384f_s$	23	59	520	ns
		$f_{sys} = 512f_s$	17	44	390	ns
$t_{CWH}$	system clock HIGH time	$f_{sys} < 19.2$ MHz	$0.3T_{sys}$	–	$0.7T_{sys}$	ns
		$f_{sys} \geq 19.2$ MHz	$0.4T_{sys}$	–	$0.6T_{sys}$	ns
$t_{CWL}$	system clock LOW time	$f_{sys} < 19.2$ MHz	$0.3T_{sys}$	–	$0.7T_{sys}$	ns
		$f_{sys} \geq 19.2$ MHz	$0.4T_{sys}$	–	$0.6T_{sys}$	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Serial interface timing (see Fig.5)</b>						
$f_{BCK}$	bit clock frequency		–	–	$64f_s$	Hz
$t_{BCKH}$	bit clock HIGH time		50	–	–	ns
$t_{BCKL}$	bit clock LOW time		50	–	–	ns
$t_r$	rise time		–	–	20	ns
$t_f$	fall time		–	–	20	ns
$t_{su}(DATAI)$	set-up time data input		20	–	–	ns
$t_h(DATAI)$	hold time data input		0	–	–	ns
$t_{su}(WS)$	set-up time word select		20	–	–	ns
$t_h(WS)$	hold time word select		10	–	–	ns

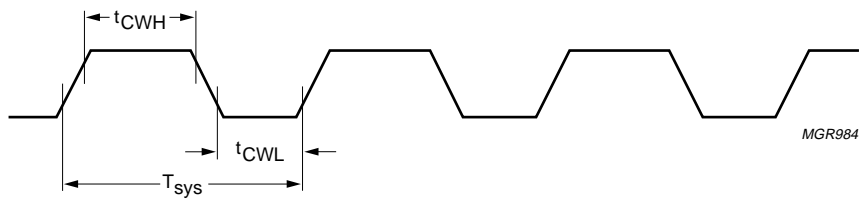


Fig.4 System clock timing.

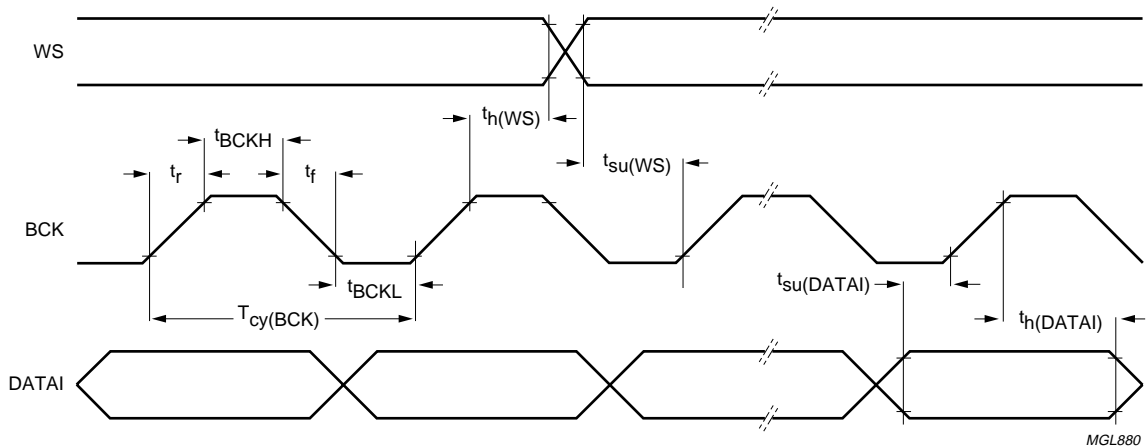


Fig.5 Serial interface timing.

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15 APPLICATION INFORMATION

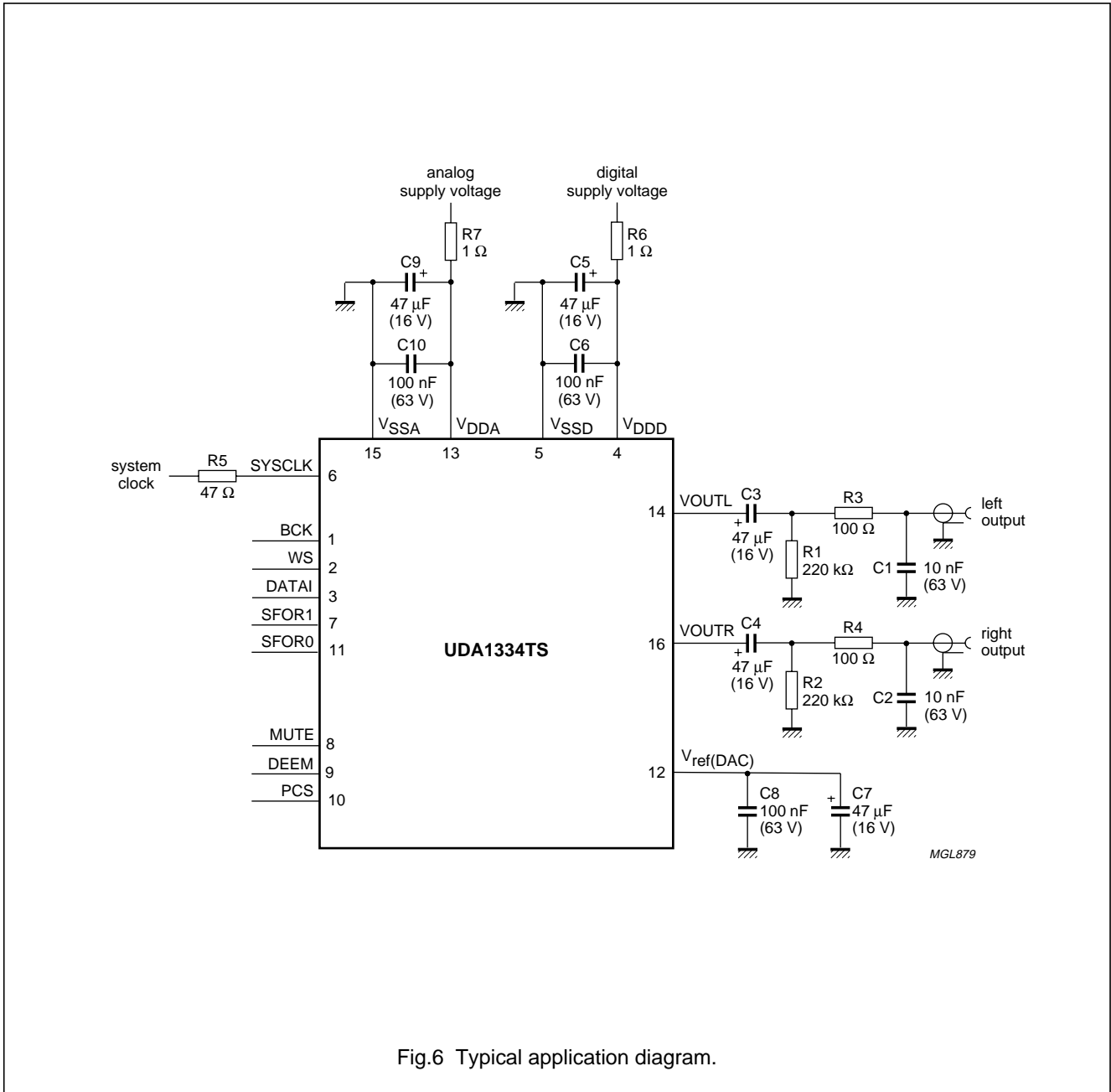


Fig.6 Typical application diagram.

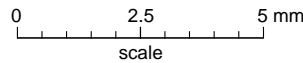
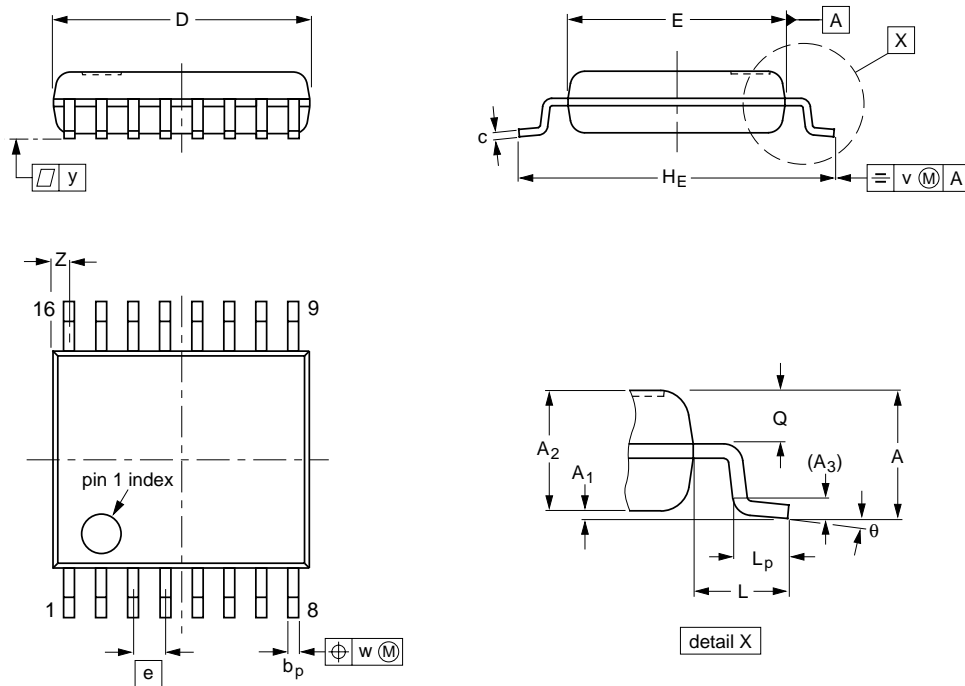
Low power audio DAC

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16 PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm

SOT369-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT369-1					94-04-20 95-02-04

## Low power audio DAC

## UDA1334TS

### 17 SOLDERING

#### 17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

#### 17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

#### 17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### 17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.



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## 17.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

## Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## 18 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

## 19 LIFE SUPPORT APPLICATIONS

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**NOTES**

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# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 3 Figtree Drive, HOMEBUSH, NSW 2140,  
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

**Belgium:** see The Netherlands

**Brazil:** see South America

**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 68 9211, Fax. +359 2 68 9102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
Tel. +45 33 29 3333, Fax. +45 33 29 3905

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615 800, Fax. +358 9 6158 0920

**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,  
Tel. +91 22 493 8541, Fax. +91 22 493 0966

**Indonesia:** PT Philips Development Corporation, Semiconductors Division,  
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,  
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),  
Tel. +39 039 203 6838, Fax +39 039 203 6800

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,  
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Pakistan:** see Singapore

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Al.Jerozolimskie 195 B, 02-222 WARSAW,  
Tel. +48 22 5710 000, Fax. +48 22 5710 001

**Portugal:** see Spain

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**Russia:** Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,  
Tel. +7 095 755 6918, Fax. +7 095 755 6919

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Tel. +65 350 2538, Fax. +65 251 6500

**Slovakia:** see Austria

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**South Africa:** S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,  
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,  
Tel. +27 11 471 5401, Fax. +27 11 471 5398

**South America:** Al. Vicente Pinzon, 173, 6th floor,  
04547-130 SÃO PAULO, SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 821 2382

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 93 301 6312, Fax. +34 93 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2741 Fax. +41 1 488 3263

**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,  
Tel. +66 2 745 4090, Fax. +66 2 398 0793

**Turkey:** Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,  
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**Uruguay:** see South America

**Vietnam:** see Singapore

**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 62 5344, Fax. +381 11 63 5777

**For all other countries apply to:** Philips Semiconductors,  
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,  
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**Internet:** <http://www.semiconductors.philips.com>

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