

BUK7222-55A

TrenchMOS™ standard level FET

Rev. 01 — 17 April 2001

Product specification

1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™¹ technology, featuring very low on-state resistance.

Product availability:

BUK7222-55A in SOT428 (D-PAK).

2. Features

- TrenchMOS™ technology
- Q101 compliant
- 175 °C rated
- Standard level compatible.

3. Applications

- Automotive and general purpose power switching:
 - ◆ 12 V and 24 V loads
 - ◆ Motors, lamps and solenoids.

4. Pinning information

Table 1: Pinning - SOT428 (D-PAK), simplified outline and symbol

| Pin | Description | Simplified outline | Symbol |
|-----|-------------|------------------------|---------------|
| 1 | gate (g) | <p>Top view MBK091</p> | <p>MBB076</p> |
| 2 | drain (d) | | |
| 3 | source (s) | | |
| mb | drain (d) | | |

SOT428 (D-PAK)

1. TrenchMOS is a trademark of Royal Philips Electronics.



5. Quick reference data

Table 2: Quick reference data

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|------------|----------------------------------|---|-----|-----|------|
| V_{DS} | drain-source voltage (DC) | | – | 55 | V |
| I_D | drain current (DC) | $T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V}$ | – | 48 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$ | – | 103 | W |
| T_j | junction temperature | | – | 175 | °C |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 25\text{ A}$ | | | |
| | | $T_j = 25\text{ °C}$ | 19 | 22 | mΩ |
| | | $T_j = 175\text{ °C}$ | – | 44 | mΩ |

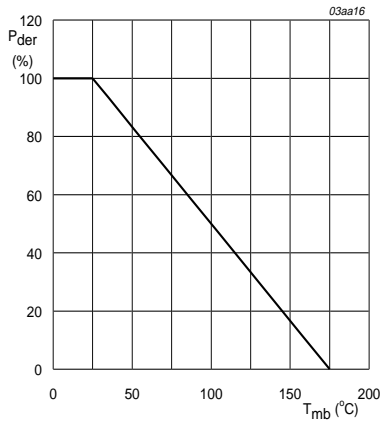
6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

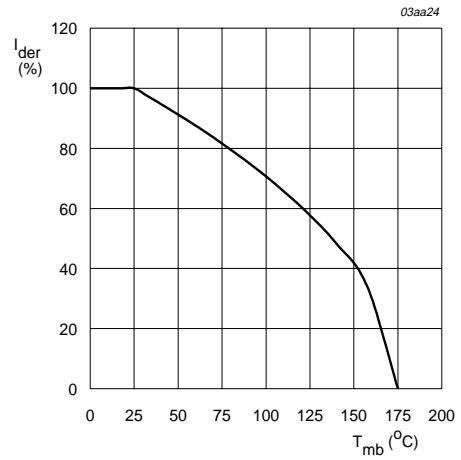
| Symbol | Parameter | Conditions | Min | Max | Unit | |
|-----------------------------|---------------------------------|--|-----|----------|------|---|
| V_{DS} | drain-source voltage (DC) | | – | 55 | V | |
| V_{DGR} | drain-gate voltage (DC) | $R_{GS} = 20\text{ k}\Omega$ | – | 55 | V | |
| V_{GS} | gate-source voltage (DC) | | – | ± 20 | V | |
| I_D | drain current (DC) | $T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2 and 3 | – | 48 | A | |
| | | $T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2 | – | 34 | A | |
| I_{DM} | peak drain current | $T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3 | [1] | – | 193 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C};$ Figure 1 | – | 103 | W | |
| T_{stg} | storage temperature | | –55 | +175 | °C | |
| T_j | operating junction temperature | | –55 | +175 | °C | |
| Source-drain diode | | | | | | |
| I_{DR} | reverse drain current (DC) | $T_{mb} = 25\text{ °C}$ | – | 48 | A | |
| I_{DRM} | pulsed reverse drain current | $T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$ | – | 193 | A | |
| Avalanche ruggedness | | | | | | |
| W_{DSS} | non-repetitive avalanche energy | unclamped inductive load; $I_D = 48\text{ A};$ $V_{DS} \leq 55\text{ V}; V_{GS} = 10\text{ V}; R_{GS} = 50\text{ }\Omega;$ starting $T_j = 25\text{ °C}$ | – | 160 | mJ | |

[1] I_{DM} is limited by chip, not package.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

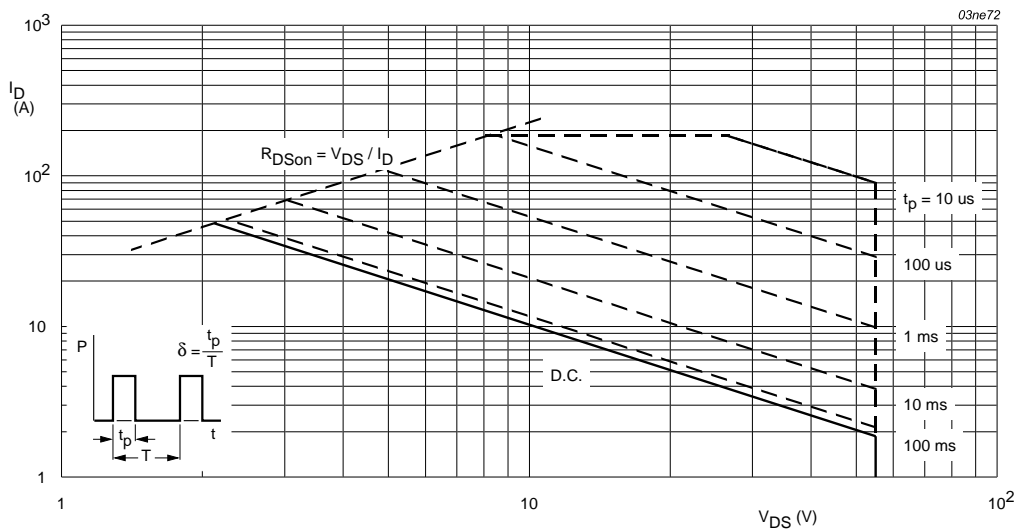
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



V_{GS} ≥ 4.5 V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

| Symbol | Parameter | Conditions | Value | Unit |
|----------------|---|------------------------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | minimum footprint, FR4 board | 71.4 | K/W |
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Figure 4 | 1.5 | K/W |

7.1 Transient thermal impedance

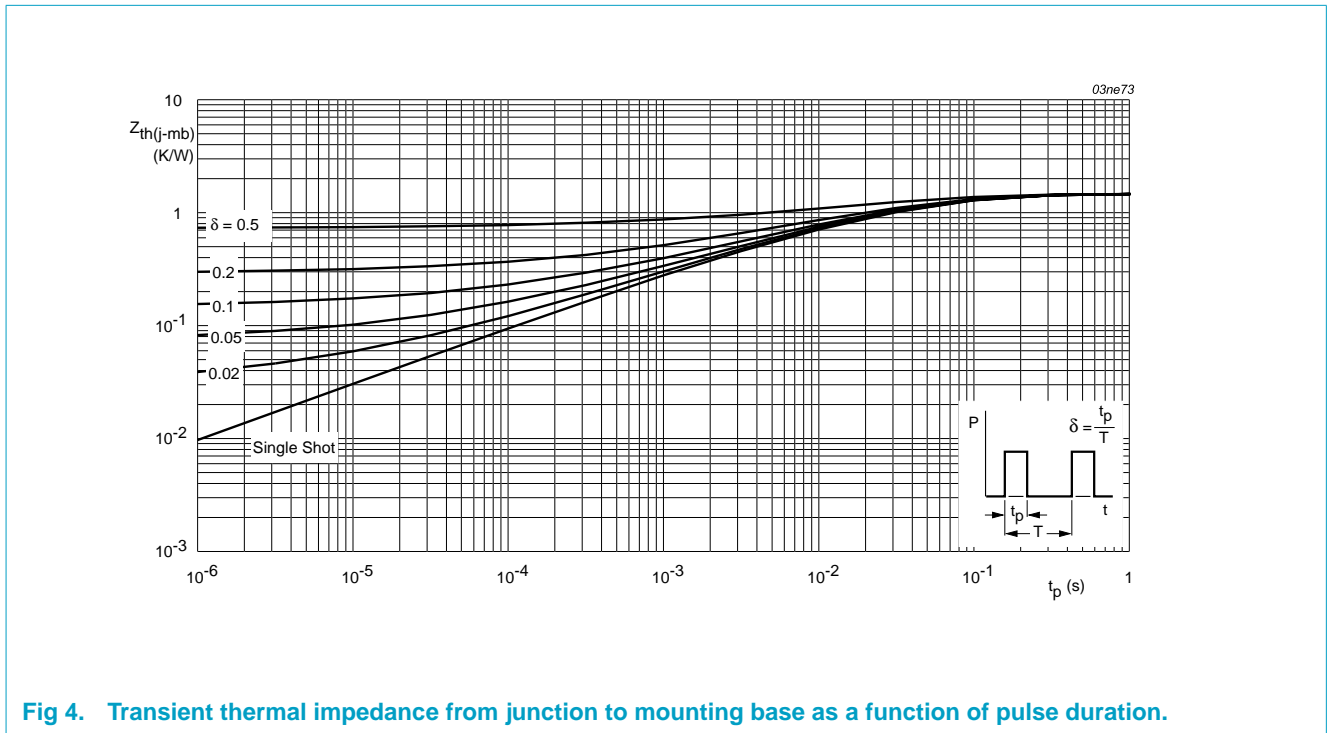


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

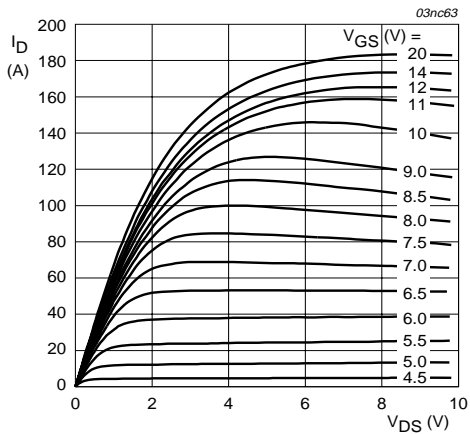
Table 5: Characteristics

$T_j = 25\text{ °C}$ unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|--|-----|------|------|---------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 0.25\text{ mA}$; $V_{GS} = 0\text{ V}$ | | | | |
| | | $T_j = 25\text{ °C}$ | 55 | – | – | V |
| | | $T_j = -55\text{ °C}$ | 50 | – | – | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9 | | | | |
| | | $T_j = 25\text{ °C}$ | 2 | 3 | 4 | V |
| | | $T_j = 175\text{ °C}$ | 1 | – | – | V |
| | | $T_j = -55\text{ °C}$ | – | – | 4.4 | V |
| I_{DSS} | drain-source leakage current | $V_{DS} = 55\text{ V}$; $V_{GS} = 0\text{ V}$ | | | | |
| | | $T_j = 25\text{ °C}$ | – | 0.05 | 10 | μA |
| | | $T_j = 175\text{ °C}$ | – | – | 500 | μA |
| I_{GSS} | gate-source leakage current | $V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0\text{ V}$ | – | 2 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; Figure 7 and 8 | | | | |
| | | $T_j = 25\text{ °C}$ | – | 19 | 22 | m Ω |
| | | $T_j = 175\text{ °C}$ | – | – | 44 | m Ω |
| Dynamic characteristics | | | | | | |
| C_{iss} | input capacitance | $V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; Figure 12 | – | 1200 | 1597 | pF |
| C_{oss} | output capacitance | | – | 290 | 349 | pF |
| C_{rss} | reverse transfer capacitance | | – | 180 | 245 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DD} = 30\text{ V}$; $R_L = 1.2\text{ }\Omega$; | – | 15 | – | ns |
| t_r | rise time | $V_{GS} = 10\text{ V}$; $R_G = 10\text{ }\Omega$; | – | 74 | – | ns |
| $t_{d(off)}$ | turn-off delay time | | – | 70 | – | ns |
| t_f | fall time | | – | 40 | – | ns |
| L_d | internal drain inductance | measured from drain to centre of die | – | 2.5 | – | nH |
| L_s | internal source inductance | measured from source lead to source bond pad | – | 7.5 | – | nH |

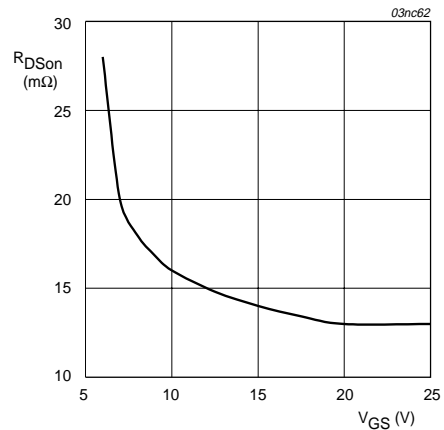
Table 5: Characteristics...continued
T_j = 25 °C unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|--------------------------------------|--|-----|------|-----|------|
| Source-drain diode | | | | | | |
| V _{SD} | source-drain (diode forward) voltage | I _S = 20 A; V _{GS} = 0 V; Figure 15 | – | 0.85 | 1.2 | V |
| t _{rr} | reverse recovery time | I _S = 20 A; dI _S /dt = –100 A/μs | – | 45 | – | ns |
| Q _r | recovered charge | V _{GS} = –10 V; V _{DS} = 30 V | – | 110 | – | nC |



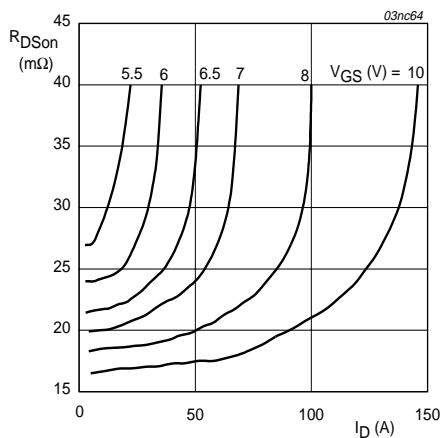
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



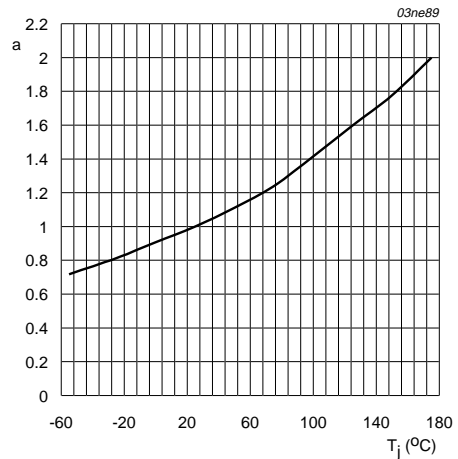
T_j = 25 °C; I_D = 25 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



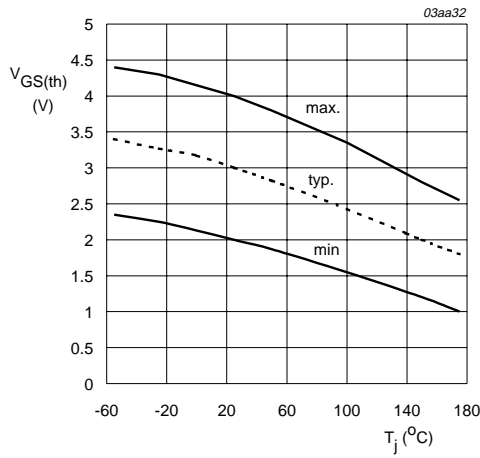
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



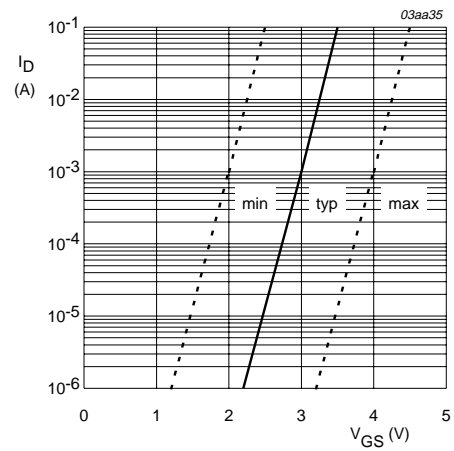
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



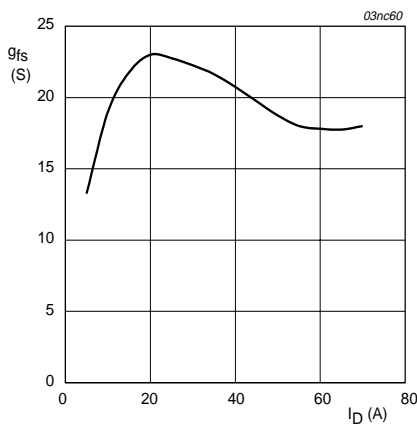
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



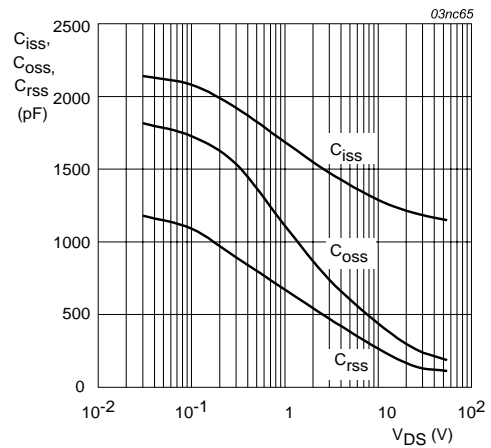
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



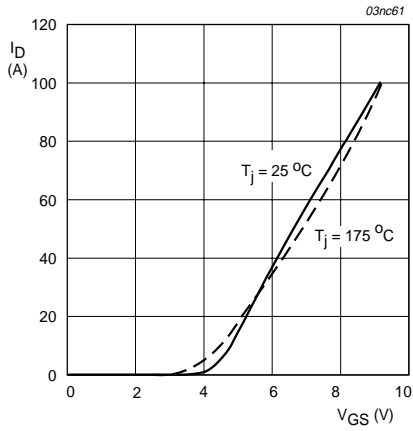
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



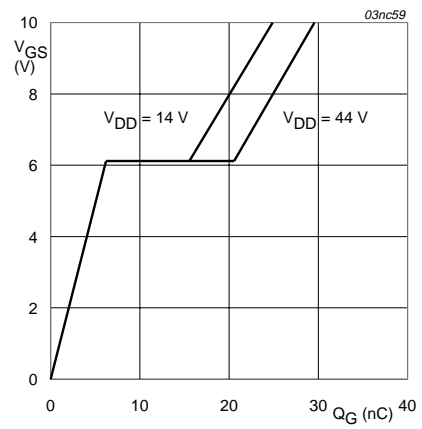
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



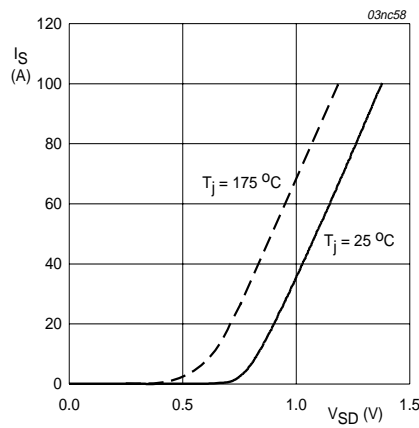
$V_{DS} = 25\text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.



$V_{GS} = 0\text{ V}$

Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.

9. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)

SOT428

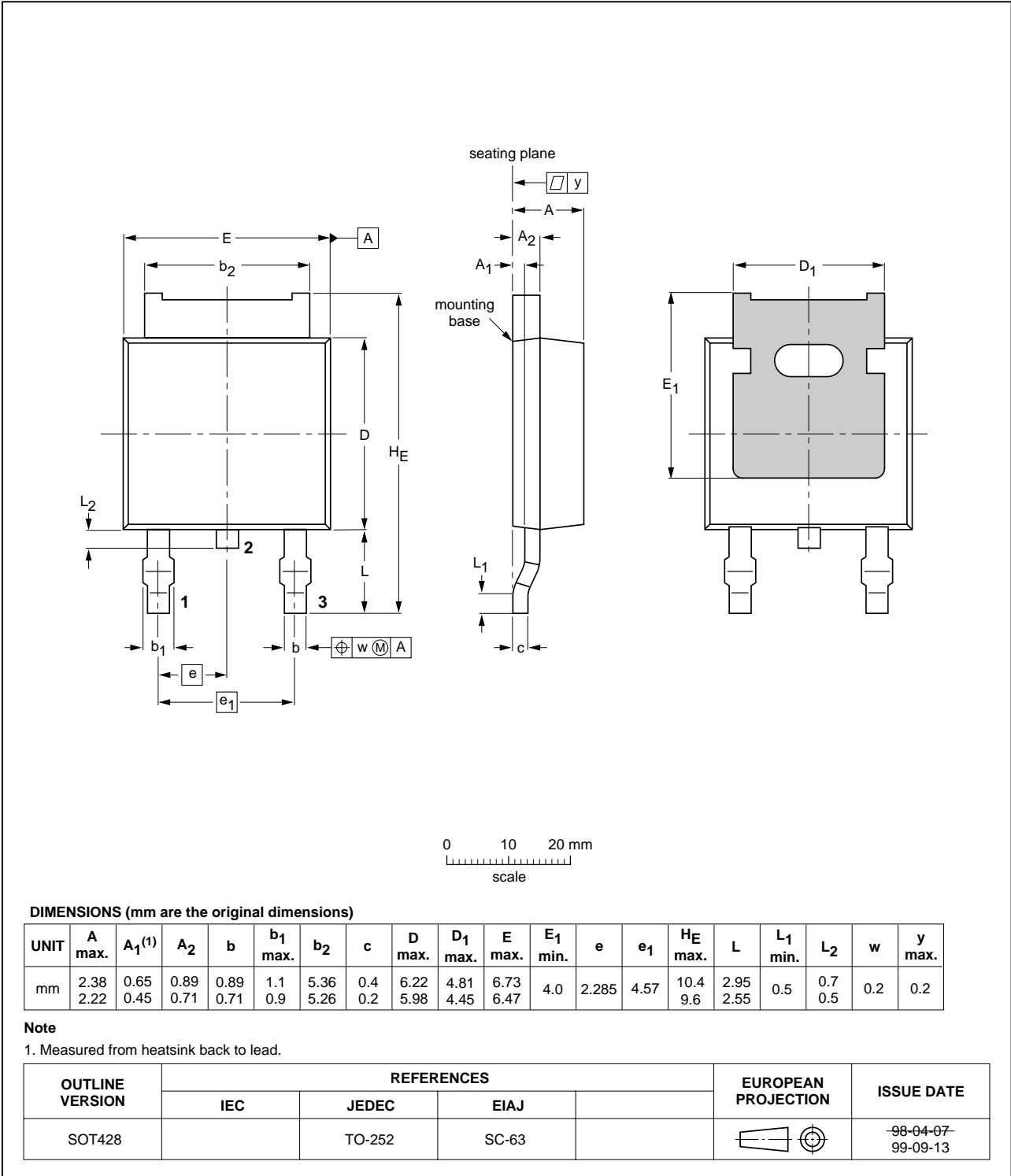


Fig 16. SOT428 (D-PAK).

10. Revision history

Table 6: Revision history

| Rev | Date | CPCN | Description |
|-----|----------|------|---|
| 01 | 20010417 | - | Product specification; initial version. |

11. Data sheet status

| Data sheet status ^[1] | Product status ^[2] | Definition |
|----------------------------------|-------------------------------|--|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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