

# BUK75/7610-55AL

N-channel TrenchMOS™ standard level FET

Rev. 01 — 31 March 2005

Product data sheet

## 1. Product profile

### 1.1 General description

N-channel enhancement mode field-effect power transistor in a plastic package using Philips General-Purpose Automotive (GPA) TrenchMOS™ technology specifically optimized for linear operation.

### 1.2 Features

- TrenchMOS™ technology
- 175 °C rated
- Q101 compliant
- Stable operation in linear mode.

### 1.3 Applications

- Automotive systems
- DC linear motor control
- Repetitive clamped inductive switching
- 12 V and 24 V loads.

### 1.4 Quick reference data

- $E_{DS(AL)S} \leq 1.1 \text{ J}$
- $I_D \leq 75 \text{ A}$
- $R_{DSon} = 8.5 \text{ m}\Omega$  (typ)
- $P_{tot} \leq 300 \text{ W}$ .

## 2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)		
2	drain (D)		
3	source (S)		
mb	mounting base; connected to drain (D)		
		SOT78 (TO-220AB)	SOT404 (D2PAK)

### 3. Ordering information

**Table 2: Ordering information**

Type number	Package		Version
	Name	Description	
BUK7510-55AL	TO-220AB	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78
BUK7610-55AL	D2PAK	Plastic single-ended surface mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

### 4. Limiting values

**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage (DC)		-	55	V	
$V_{DGR}$	drain-gate voltage (DC)	$R_{GS} = 20 \text{ k}\Omega$	-	55	V	
$V_{GS}$	gate-source voltage (DC)		-	$\pm 20$	V	
$I_D$	drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; $V_{GS} = 10 \text{ V}$ ; <a href="#">Figure 2</a> and <a href="#">3</a>	<a href="#">[1]</a> <a href="#">[3]</a>	-	122	A
			<a href="#">[2]</a>	-	75	A
		$T_{mb} = 100 \text{ }^\circ\text{C}$ ; $V_{GS} = 10 \text{ V}$ ; <a href="#">Figure 2</a>	<a href="#">[2]</a>	-	75	A
$I_{DM}$	peak drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$ ; <a href="#">Figure 3</a>	-	490	A	
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Figure 1</a>	-	300	W	
$T_{stg}$	storage temperature		-55	+175	$^\circ\text{C}$	
$T_j$	junction temperature		-55	+175	$^\circ\text{C}$	
<b>Source-drain diode</b>						
$I_{DR}$	reverse drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$	<a href="#">[1]</a> <a href="#">[3]</a>	-	122	A
			<a href="#">[2]</a>	-	75	A
$I_{DRM}$	peak reverse drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; pulsed; $t_p \leq 10 \text{ }\mu\text{s}$	-	490	A	
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 75 \text{ A}$ ; $V_{DS} \leq 55 \text{ V}$ ; $R_{GS} = 50 \text{ }\Omega$ ; $V_{GS} = 10 \text{ V}$ ; starting at $T_j = 25 \text{ }^\circ\text{C}$	-	1.1	J	
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		-	<a href="#">[4]</a>	-	

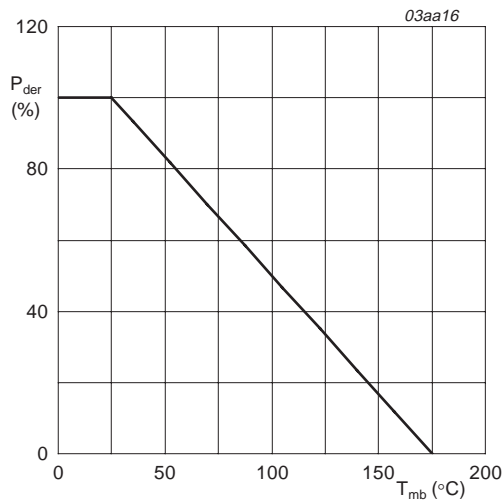
[1] Current is limited by power dissipation chip rating.

[2] Continuous current is limited by package.

[3] Refer to document *9397 750 12572* for further information.

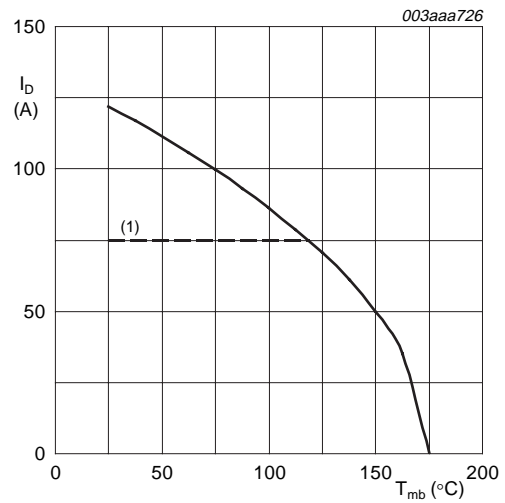
[4]

- Max value not quoted. Repetitive rating defined in [Figure 16](#).
- Single-shot avalanche rating limited by  $T_{j(max)}$  of  $175 \text{ }^\circ\text{C}$ .
- Repetitive avalanche rating limited by  $T_{j(avg)}$  of  $170 \text{ }^\circ\text{C}$ .
- Refer to application note *AN10273* for further information.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

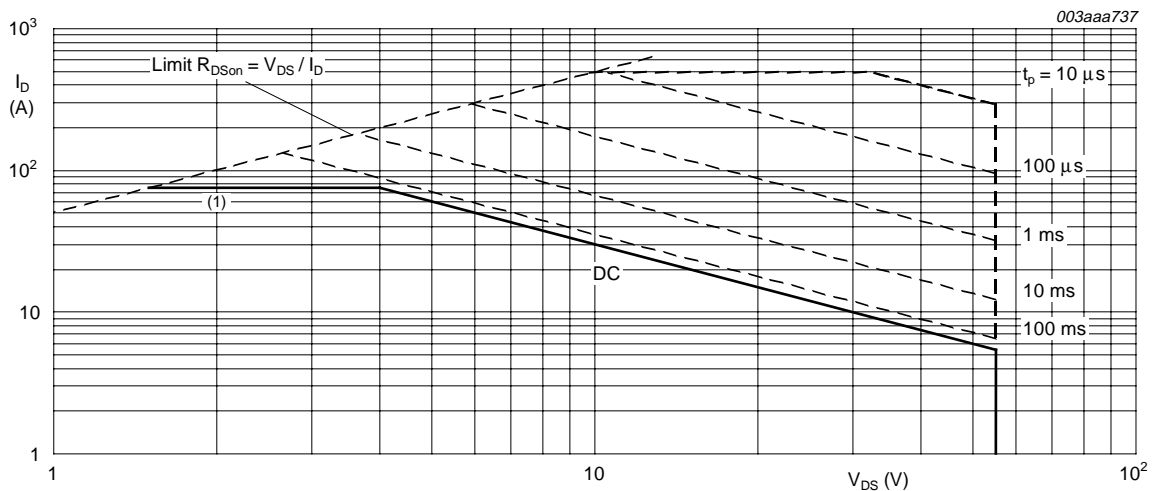
**Fig 1. Normalized total power dissipation as a function of mounting base temperature.**



$V_{GS} \geq 5\text{ V}$

(1) Capped at 75 A due to package.

**Fig 2. Continuous drain current as a function of mounting base temperature.**



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse.

(1) Capped at 75 A due to package.

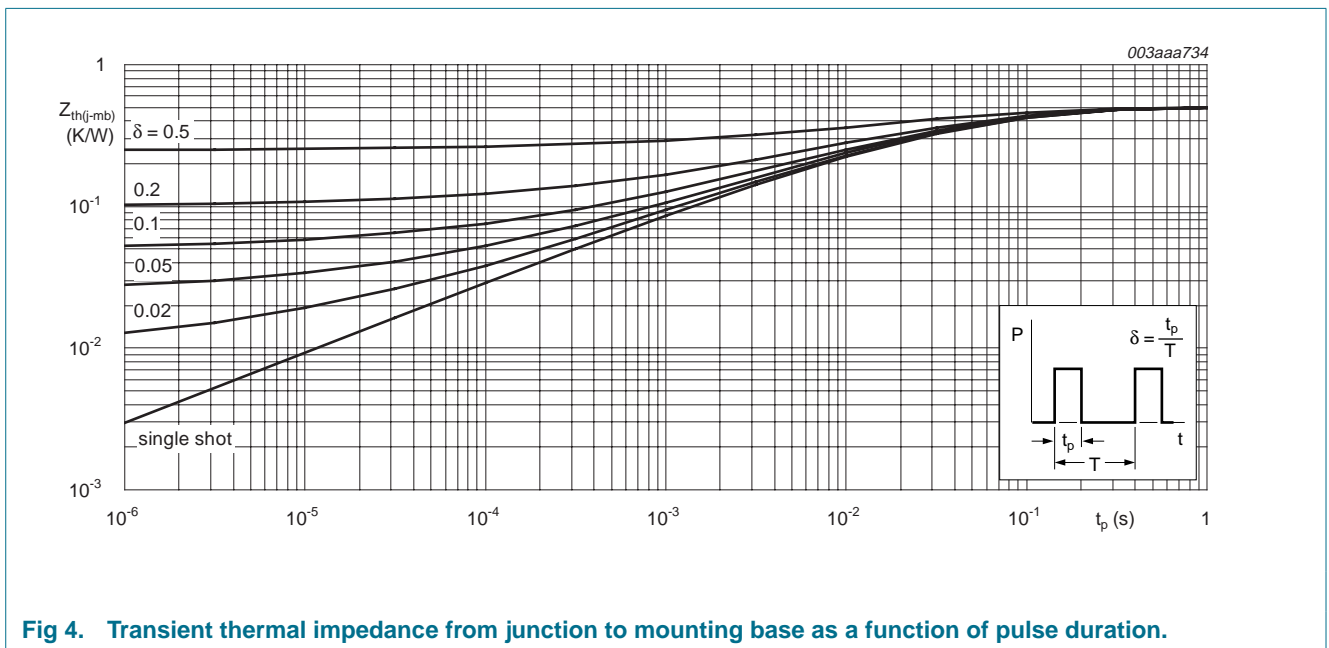
**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**

## 5. Thermal characteristics

**Table 4: Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78 (TO-220AB)	vertical in free air	-	60	-	K/W
	SOT404 (D <sup>2</sup> -PAK)	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	50	-	K/W

### 5.1 Transient thermal impedance

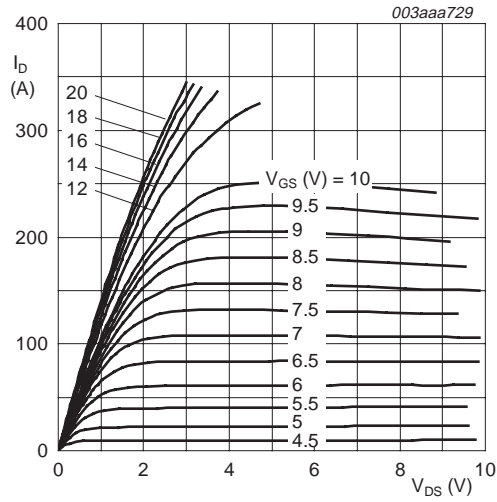


**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.**

## 6. Characteristics

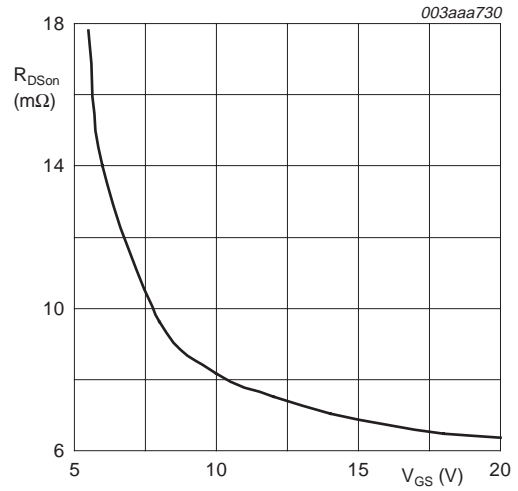
**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	55	-	-	V
		T <sub>j</sub> = -55 °C	50	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; <a href="#">Figure 9</a> and <a href="#">10</a>				
		T <sub>j</sub> = 25 °C	2	3	4	V
		T <sub>j</sub> = 175 °C	1	-	-	V
		T <sub>j</sub> = -55 °C	-	-	4.4	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 55 V; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	-	0.05	10	μA
		T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ±20 V; V <sub>DS</sub> = 0 V	-	2	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; <a href="#">Figure 6</a> and <a href="#">8</a>				
		T <sub>j</sub> = 25 °C	-	8.5	10	mΩ
		T <sub>j</sub> = 175 °C	-	-	20	mΩ
<b>Dynamic characteristics</b>						
Q <sub>g(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DD</sub> = 44 V; V <sub>GS</sub> = 10 V; <a href="#">Figure 14</a>	-	124	-	nC
Q <sub>gs</sub>	gate-source charge		-	22	-	nC
Q <sub>gd</sub>	gate-drain (Miller) charge		-	50	-	nC
V <sub>plat</sub>	plateau voltage		-	5	-	V
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; <a href="#">Figure 12</a>	-	4710	6280	pF
C <sub>oss</sub>	output capacitance		-	980	1180	pF
C <sub>rss</sub>	reverse transfer capacitance		-	560	770	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; R <sub>L</sub> = 1.2 Ω;	-	33	-	ns
t <sub>r</sub>	rise time	V <sub>GS</sub> = 10 V; R <sub>G</sub> = 10 Ω	-	117	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	132	-	ns
t <sub>f</sub>	fall time		-	95	-	ns
L <sub>d</sub>	internal drain inductance	from drain lead 6 mm from package to center of die	-	4.5	-	nH
		from contact screw on mounting base to center of die	-	3.5	-	nH
		from upper edge of drain mounting base to center of die SOT404	-	2.5	-	nH
L <sub>s</sub>	internal source inductance	from source lead to source bond pad	-	7.5	-	nH
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain (diode forward) voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; <a href="#">Figure 15</a>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs;	-	73	-	ns
Q <sub>r</sub>	recovered charge	V <sub>GS</sub> = 0 V; V <sub>R</sub> = 30 V	-	430	-	nC



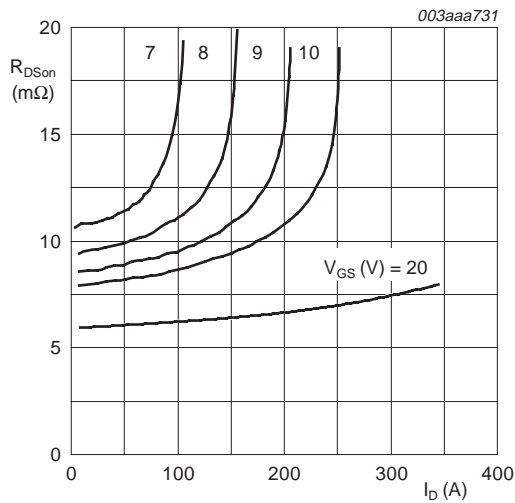
$T_j = 25\text{ }^\circ\text{C}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



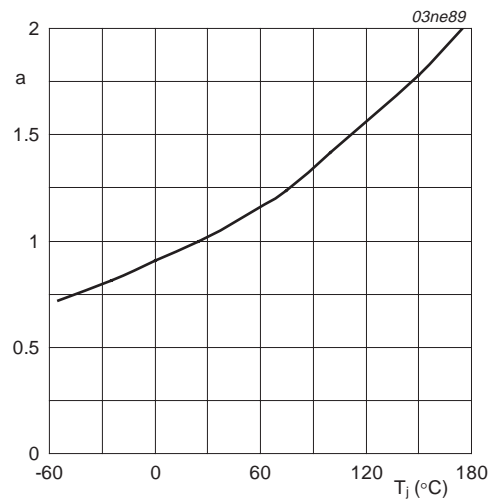
$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.**



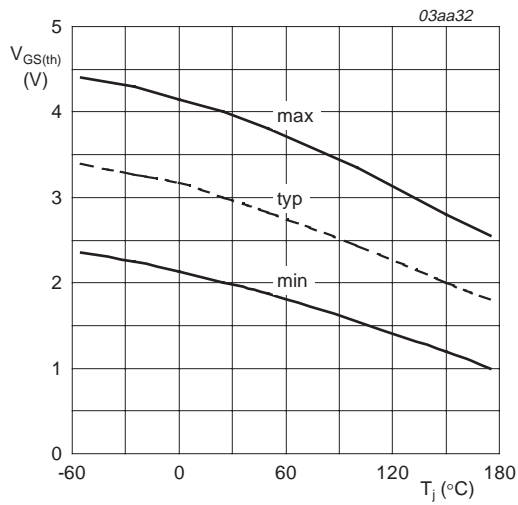
$T_j = 25\text{ }^\circ\text{C}$

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



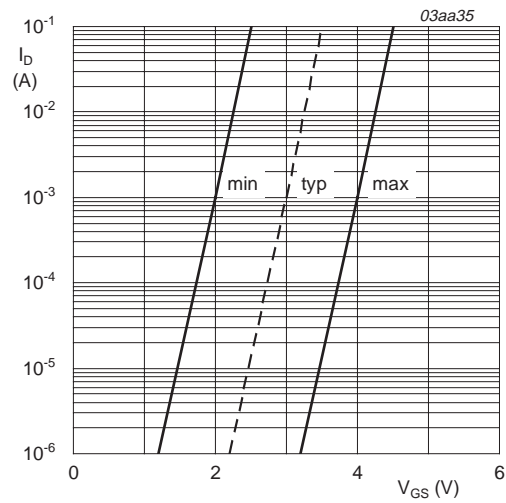
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



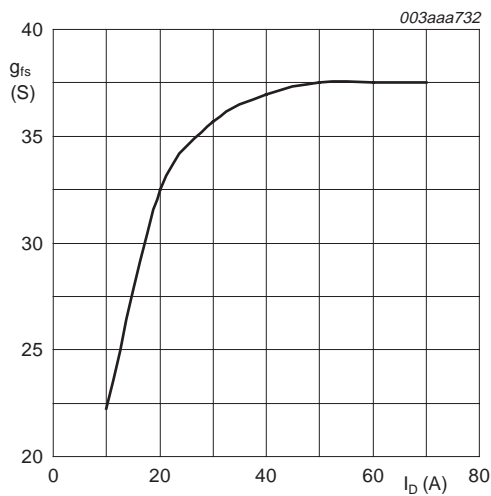
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



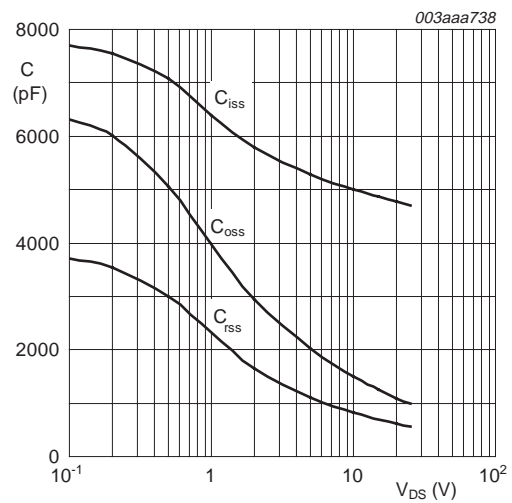
$T_j = 25 \text{ °C}; V_{DS} = V_{GS}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



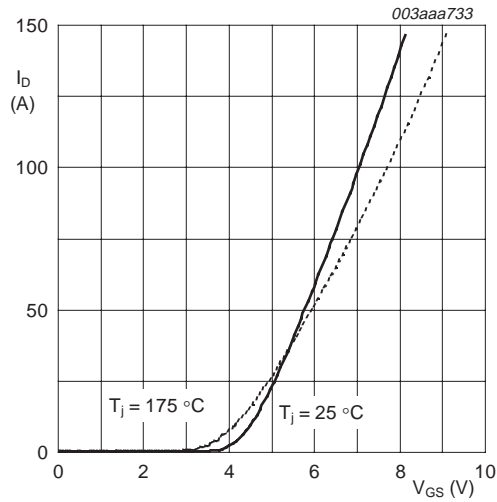
$T_j = 25 \text{ °C}; V_{DS} = 25 \text{ V}$

**Fig 11. Forward transconductance as a function of drain current; typical values.**



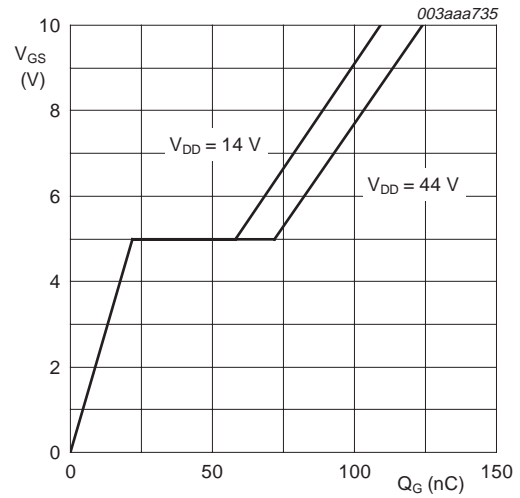
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



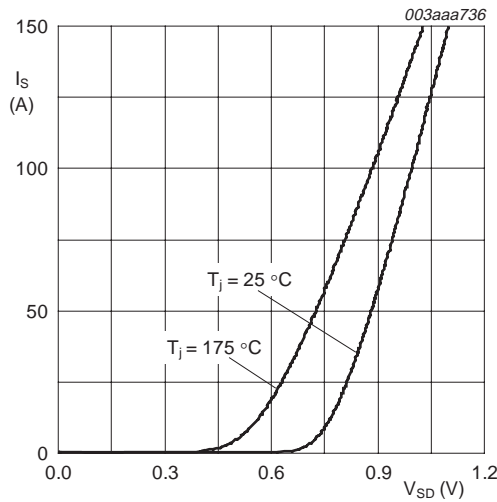
$V_{DS} = 25 \text{ V}$

**Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



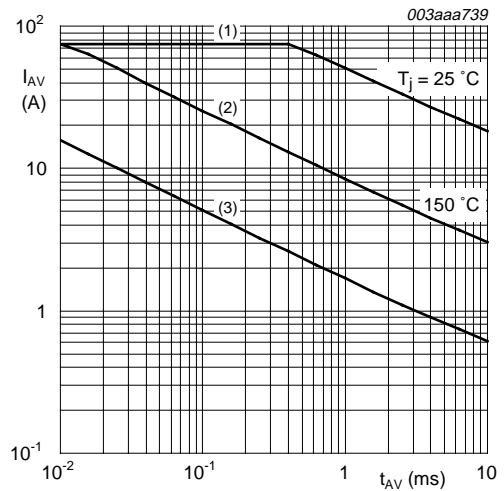
$T_j = 25 \text{ °C}; I_D = 25 \text{ A}$

**Fig 14. Gate-source voltage as a function of gate charge; typical values.**



$V_{GS} = 0 \text{ V}$

**Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



See [Table note 4](#) of [Table 3](#) Limiting values.

- (1) Single-shot.
- (2) Single-shot.
- (3) Repetitive.

**Fig 16. Single-shot and repetitive avalanche rating; avalanche current as a function of avalanche period.**



**7. Package outline**

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

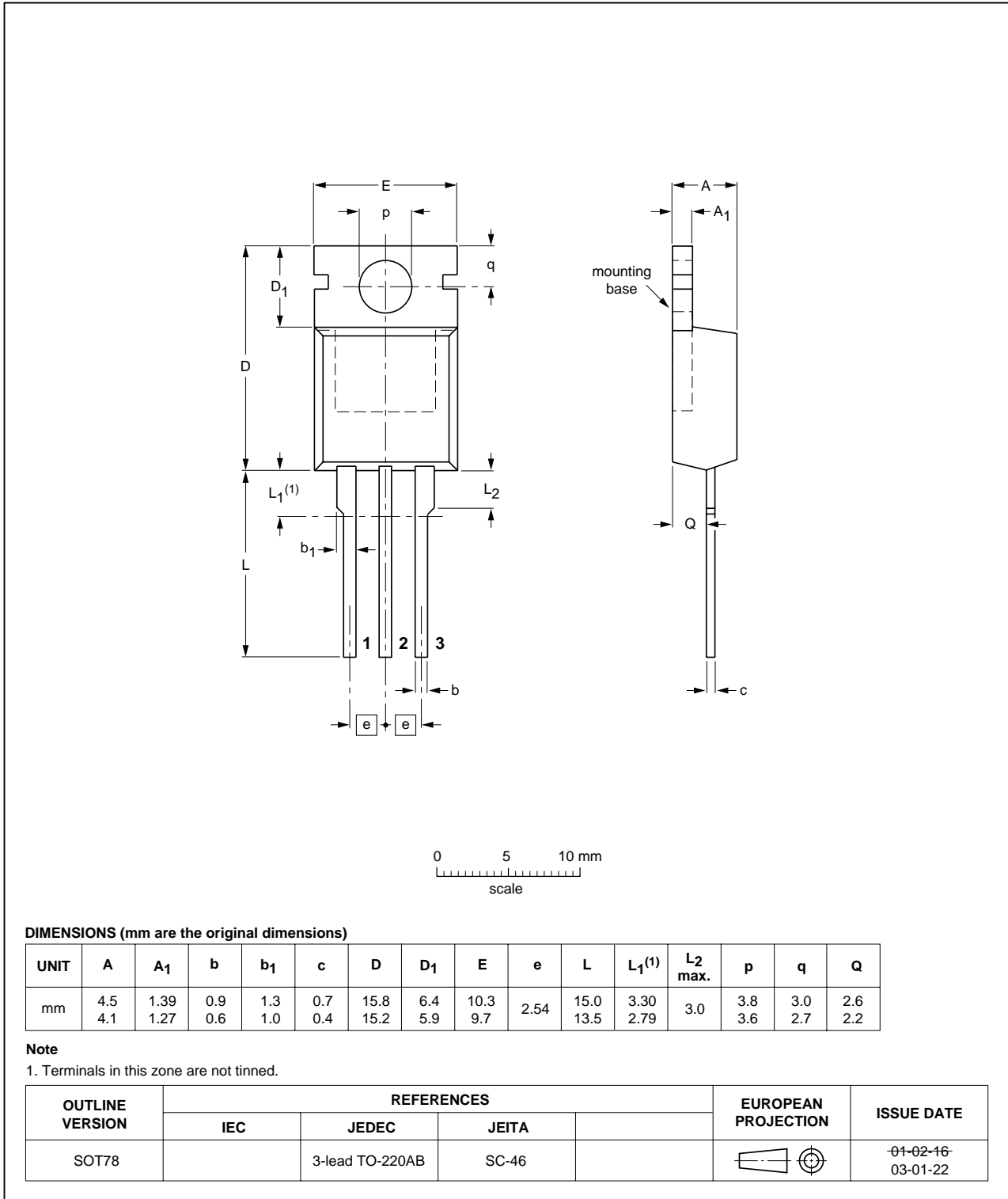
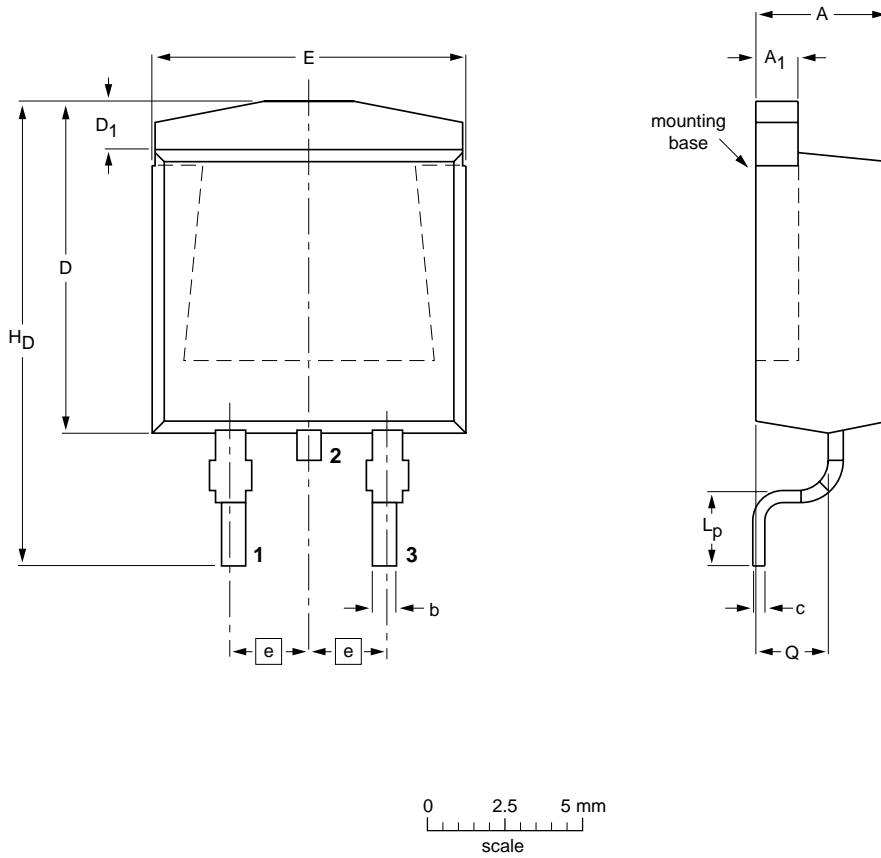


Fig 17. Package outline SOT78 (TO-220AB).

Plastic single-ended surface mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



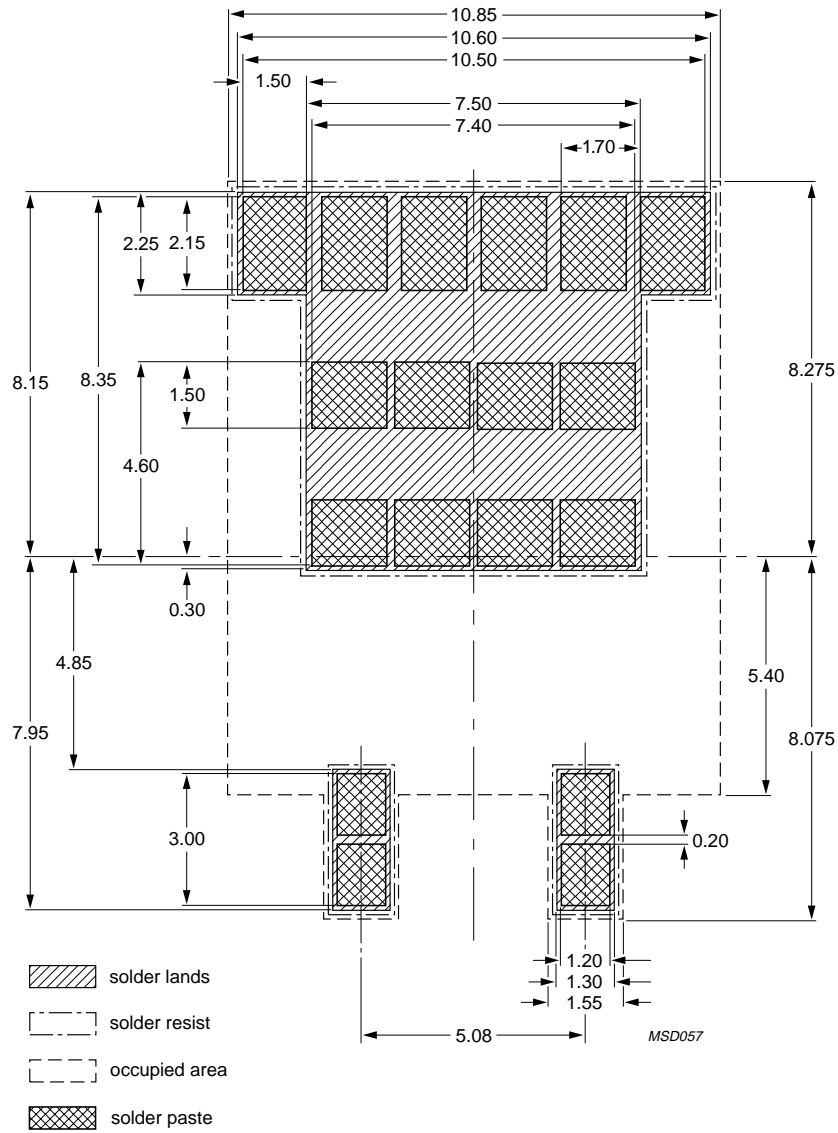
DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D max.	D <sub>1</sub>	E	e	L <sub>p</sub>	H <sub>D</sub>	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						04-10-13 05-02-11

Fig 18. Package outline SOT404 (D<sup>2</sup>-PAK).

**8. Mounting**



Dimensions in mm.

**Fig 19. Reflow soldering footprint for SOT404.**

## 9. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
BUK75_7610_55AL_1	20050331	Product data sheet	-	9397 750 14362	-

## 10. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 11. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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